Project Title: Digital to Analog Converters Analysis and Comparisons

Teammates: Jessica Diller

*Brief Description of Project:*

I’ve had exposure to different kinds of Digital to Analog Converters over years here at Olin including resistor ladders, transistor ladders, and microprocessors. Given the knowledge I have now about digital systems, I would like to deepen my knowledge in this area as well as develop my analysis skills. I plan to analyze the performance characteristics like timing, space, temperature, and operations of various DACs with a goal of final comparison between them. I have linked to a few different data sheets below that I plan to use to research the different DACs.

To show my learning, I plan to implement the DACs using behavioral Verilog (including appropriate timing delays) and create numerous test benches to easily compare results across different DACs. I would also like to include resistor and transistor ladders as comparison objects. I might choose to use a circuit simulation tool for that instead, but in a way that there is still easy result comparison options. As a stretch goal, I want to implement either one of the digital DACs or design my own new DAC based on the knowledge I’ve gained with comparisons in structural Verilog. Then, I could include that model in more comparisons.

*References:*

On DACs in general: <https://en.wikipedia.org/wiki/Digital-to-analog_converter>

Different DAC Datasheets:

<http://www.analog.com/media/en/technical-documentation/data-sheets/AD7302.pdf>

<http://www.analog.com/media/en/technical-documentation/data-sheets/AD7224.pdf>

<https://datasheets.maximintegrated.com/en/ds/MAX5480.pdf>

Resistor Ladder: <https://en.wikipedia.org/wiki/Resistor_ladder>

Transistor Ladder: <http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=705353>

*Minimum deliverables:*

* Behavioral Verilog simulations for three DACs
* Include test benches
* Characteristic comparison (i.e. how many inputs and outputs possible simultaneously)
* Timing analysis comparisons
* Physical area analysis comparisons (inside chips and just black boxing)
* Situation conditions comparisons (i.e. temperature)

*Planned deliverables:*

* Include the resistor and transistor ladders simulations as comparisons

*Stretch deliverables:*

* Design my own DAC in structural Verilog with design constraints
* Or write up the “best” one in structural Verilog
* Include test benches