Project Title: Analog to Digital Converters Analysis and Comparisons

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*Brief Description of Project:*

Given the knowledge I have now about digital systems, I would like to deepen my knowledge in the analog to digital area as well as develop my analysis skills. I plan to analyze the performance characteristics like timing, space, temperature, and operations of differing conversion techniques in ADCs with a goal of final comparison between them. I have linked to a few different data sheets below that I plan to use to research the different ADCs.

I plan to first research and understand the black boxes within the chips and the differing type of conversion techniques. To show my learning, I want to then implement the DACs using behavioral Verilog (including appropriate timing delays) with each subsystem a black box. Then, I would run test benches to easily compare results across different ADCs. As a minimum, I will understand and compare at least two different types of conversion techniques and implement one type in Verilog. Planned deliverables include two comparisons and two implementations in Verilog. Stretch goals would be three comparisons and three implementations in Verilog.

*References:*

On ADCs in general: <https://en.wikipedia.org/wiki/Analog-to-digital_converter>

Datasheets:

1. <http://ww1.microchip.com/downloads/en/DeviceDoc/21294C.pdf>
2. <http://www.analog.com/media/en/technical-documentation/data-sheets/AD9254.pdf>
3. <http://www.analog.com/media/en/technical-documentation/data-sheets/AD7701.pdf>

Info on conversion types:

1. Successive Approximation ADC: <https://en.wikipedia.org/wiki/Successive_approximation_ADC>
2. Delta-Sigma ADC: <http://www.ti.com/lit/an/slyt423/slyt423.pdf>
3. Pipelined ADC: <https://www.maximintegrated.com/en/app-notes/index.mvp/id/1023>

*Minimum deliverables:*

* Behavioral Verilog simulations including test benches – one ADC
* Characteristic comparisons (i.e. how many inputs and outputs possible simultaneously) – two ADCs
* Timing analysis comparisons – two ADCs
* Physical area analysis comparisons (inside chips and just black boxing) – two ADCs
* Situation conditions comparisons (i.e. temperature) – two ADCs

*Planned deliverables:*

* Increase behavioral Verilog simulations to two ADCs
* Increase comparisons to three ADCs

*Stretch deliverables:*

* Increase behavioral Verilog simulation to three ADCs