SYSC 4507 Assignment 4

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1. The program takes 50 cycles to fully execute. See execution tables on the pages after this one. (Assumptions made: If a branch's IP change is in the range of instructions that are loaded into dispatch, then the next instruction is pushed to the front of the dispatch queue; branches are not evaluated until the writeback stage)

2. (a) 0 execution units are busy for 26 cycles out of 50.
   (b) 1 MEM units are busy for 4 cycles out of 50.
   (c) 1 ALU units are busy for 17 cycles out of 50.
   (d) 2 ALU units are busy for 3 cycles out of 50.
   (e) As concluded in the previous assignment, this binary search program does not lend itself easily to parallelization. Since this program's branches are not predicted intelligently, and about half of the instructions depend on the results from previous instructions, the processor must frequently stall to execute instructions in single file. I would expect most searching and sorting algorithms, which rely heavily on branches, would have roughly the same performance (i.e. 50% of clock cycles have no busy execution units). Programs that lend themselves better to parallelization, such as an encryption cracker, should perform better.

3. Q3

Cycle	FI	DEC	DIS	EX	WB	Notes
1	MOV R8,#-1					0 exec units busy
	CMP R5,0					
	BLT all_done					
2	MOV 6,#0	MOV R8,#-1				0 exec units busy
	SUB R5,R5,#1	CMP R5,0				
	CMP R5,R6	BLT all_done				
3	BLT all_done	MOV 6,#0	MOV R8,#-1			0 exec units busy
	ADD R7,R6,R5	SUB R5,R5,#1	CMP R5,0			
	LSR R7,R7,#1	CMP R5,R6	BLT all_done			
4	LDR R9,[R4,R7]	BLT all_done	BLT all_done			2 ALU units busy
	CMP R9,R3	ADD R7,R6,R5	MOV R6,#0			
	BLT adjust_min	LSR R7,R7,#1	SUB R5,R5,#1	MOV R8,#-1		
			CMP R5,R6	CMP R5,0		
5	BLT adjust_min	LSR R7,R7,#1	BLT all_done	x	MOV R8,#-1	0 exec units busy
	BGT adjust_max	LDR R9,[R4,R7]	MOV R6,#0		CMP R5,0	
	MOV R8,R7	CMP R9,R3	SUB R5,R5,#1			
			CMP R5,R6			
			BLT all_done			
			ADD R7,R6,R5			
6	BGT adjust_max	LDR R9,[R4,R7]	MOV R6,#0			1 ALU unit busy
	MOV R8,R7	CMP R9,R3	SUB R5,R5,#1			
	B all_done	BLT adjust_min	CMP R5,R6	BLT all_done		
			BLT all_done			
			ADD R7,R6,R5			
			LSR R7,R7,#1			

Cycle	FI	DEC	DIS	EX	WB	Notes
7	BGT adjust_max	LDR R9,[R4,R7]	MOV R6,#0	x	BLT all_done	Branch not taken
	MOV R8,R7	CMP R9,R3	SUB R5,R5,#1			0 exec units busy
	B all_done	BLT adjust_min	CMP R5,R6			
			BLT all_done			
			ADD R7,R6,R5			
			LSR R7,R7,#1			
8	B all_done	BLT adjust_min	CMP R5,R6			2 ALU units busy
	ADD R6,R7,#1	BGT adjust_max	BLT all_done			
	B test_while	MOV R8,R7	ADD R7,R6,R5	MOV R6,#0		
			LSR R7,R7,#1	SUB R5,R5,#1		
			LDR R9,[R4,R7]			
			CMP R9,R3			
9	ADD R6,R7,#1	BGT adjust_max	BLT all_done		MOV R6,#0	1 ALU unit busy
	B test_while	MOV R8,R7	ADD R7,R6,R5		SUB R5,R5,#1	
	SUB R5,R7,#1	B all_done	LSR R7,R7,#1	CMP R5,R6		
			LDR R9,[R4,R7]			
			CMP R9,R3			
			BLT adjust_min			
10	ADD R6,R7,#1	BGT adjust_max	BLT all_done	x	CMP R5,R6	0 exec units busy
	B test_while	MOV R8,R7	ADD R7,R6,R5			
	SUB R5,R7,#1	B all_done	LSR R7,R7,#1			
			LDR R9,[R4,R7]			
			CMP R9,R3			
			BLT adjust_min			
11	B test_while	MOV R8,R7	ADD R7,R6,R5			1 ALU unit busy
	SUB R5,R7,#1	B all_done	LSR R7,R7,#1			
	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]	BLT all_done		
			CMP R9,R3			
			BLT adjust_min			
			BGT adjust_max			
12	B test_while	MOV R8,R7	ADD R7,R6,R5		BLT all_done	Branch not taken
	SUB R5,R7,#1	B all_done	LSR R7,R7,#1			0 exec units busy
	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]			
			CMP R9,R3			
			BLT adjust_min			
			BGT adjust_max			

Cycle	FI	DEC	DIS	EX		WB	Notes
13	SUB R5,R7,#1	B all_done	LSR R7,R7,#1				1 ALU unit busy
	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]				
	all_done	B test_while	CMP R9,R3	ADD R7,R6,R5			
			BLT adjust_min				
			BGT adjust_max				
			MOV R8,R7				
14	SUB R5,R7,#1	B all_done	LSR R7,R7,#1			ADD R7,R6,R5	0 exec units busy
	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]				
	all_done	B test_while	CMP R9,R3				
			BLT adjust_min				
			BGT adjust_max				
			MOV R8,R7				
15	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]				1 ALU unit busy
		B test_while	CMP R9,R3				
		SUB R5,R7,#1	BLT adjust_min	LSR R7,R7,#1			
			BGT adjust_max				
			MOV R8,R7				
			B all_done				
16	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]			LSR R7,R7,#1	0 exec units busy
		B test_while	CMP R9,R3				
		SUB R5,R7,#1	BLT adjust_min				
			BGT adjust_max				
			MOV R8,R7				
			B all_done				
17		B test_while	CMP R9,R3	LDR R9,[R4,R7]			1 MEM unit busy
		SUB R5,R7,#1	BLT adjust_min				
		B test_while	BGT adjust_max				
			MOV R8,R7				
			B all_done				
			ADD R6,R7,#1				
18		B test_while	CMP R9,R3		LDR R9,[R4,R7]		1 MEM unit busy
		SUB R5,R7,#1	BLT adjust_min				
		B test_while	BGT adjust_max				
			MOV R8,R7				
			B all_done				
			ADD R6,R7,#1				

Cycle	FI	DEC	DIS	EX	WB	Notes
19		B test_while	CMP R9,R3		LDR R9,[R4,R7]	0 exec units busy
		SUB R5,R7,#1	BLT adjust_min			
		B test_while	BGT adjust_max			
			MOV R8,R7			
			B all_done			
			ADD R6,R7,#1			
20		SUB R5,R7,#1	BLT adjust_min			1 ALU units busy
		B test_while	BGT adjust_max			
			MOV R8,R7	CMP R9,R3		
			B all_done			
			ADD R6,R7#1			
			B test_while			
21		SUB R5,R7,#1	BLT adjust_min		CMP R9,R3	0 exec units busy
		B test_while	BGT adjust_max			
			MOV R8,R7			
			B all_done			
			ADD R6,R7#1			
			B test_while			
22		B test_while	BGT adjust_max			1 ALU units busy
			MOV R8,R7			
			B all_done	BLT adjust_min		
			ADD R6,R7,#1			
			B test_while			
			SUB R5,R7,#1			
23		B test_while	BGT adjust_max		BLT adjust_min	Branch not taken
			MOV R8,R7			0 exec units busy
			B all_done			
			ADD R6,R7,#1			
			B test_while			
			SUB R5,R7,#1			
24			MOV R8,R7			1 ALU unit busy
			B all_done			
			ADD R6,R7,#1	BGT adjust_max		
			B test_while			
			SUB R5,R7,#1			
			B test_while			

Cycle	FI	DEC	DIS	EX	WB	Notes
25			MOV R8,R7		BGT adjust_max	Branch taken
			B all_done			0 exec units busy
			ADD R6,R7,#1			Branch is in dispatch range
			B test_while			
			SUB R5,R7,#1			
			B test_while			
26			B test_while			1 ALU units busy
				SUB R5,R7,#1		
27					SUB R5,R7,#1	1 ALU units busy
				B test_while		
28					B test_while	0 exec units busy
						IP rewritten here
						New instructions fetched
29	CMP R5,R6					0 exec units busy
	BLT all_done					
	ADD R7,R6,R5					
30	LSR R7,R7,#1	CMP R5,R6				0 exec units busy
	LDR R9,[R4,R7]	BLT all_done				
	CMP R9,R3	ADD R7,R6,R5				

Cycle	FI	DEC	DIS	EX	WB	Notes
31	BLT adjust_min	LSR R7,R7,#1	CMP R5,R6			0 exec units busy
	BGT adjust_max	LDR R9,[R4,R7]	BLT all_done			
	MOV R8,R7	CMP R9,R3	ADD R7,R6,R5			
32	B all_done	BLT adjust_min	BLT all_done			1 ALU units busy
	ADD R6,R7,#1	BGT adjust_max	ADD R7,R6,R5			
	B test_while	MOV R8,R7	LSR R7,R7,#1	CMP R5,R6		
			LDR R9,[R4,R7]			
			CMP R9,R3			
33	ADD R6,R7,#1	BGT adjust_max	BLT all_done		CMP R5,R6	0 exec units busy
	B test_while	MOV R8,R7	ADD R7,R6,R5			
	SUB R5,R7,#1	B all_done	LSR R7,R7,#1			
			LDR R9,[R4,R7]			
			CMP R9,R3			
			BLT adjust_min			
34	B test_while	MOV R8,R7	ADD R7,R6,R5			1 ALU unit busy
	SUB R5,R7,#1	B all_done	LSR R7,R7,#1			
	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]	BLT all_done		
			CMP R9,R3			
			BLT adjust_min			
			BGT adjust_max			
35	B test_while	MOV R8,R7	ADD R7,R6,R5		BLT all_done	Branch not taken
	SUB R5,R7,#1	B all_done	LSR R7,R7,#1			0 exec units busy
	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]			
			CMP R9,R3			
			BLT adjust_min			
			BGT adjust_max			
36	SUB R5,R7,#1	B all_done	LSR R7,R7,#1			1 ALU unit busy
	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]			
		B test_while	CMP R9,R3	ADD R7,R6,R5		
			BLT adjust_min			
			BGT adjust_max			
			MOV R8,R7			

Cycle	FI	DEC	DIS	EX		WB	Notes
37	SUB R5,R7,#1	B all_done	LSR R7,R7,#1			ADD R7,R6,R5	0 exec units busy
	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]				
		B test_while	CMP R9,R3				
			BLT adjust_min				
			BGT adjust_max				
			MOV R8,R7				
38	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]				1 ALU unit busy
		B test_while	CMP R9,R3				
		SUB R5,R7,#1	BLT adjust_min	LSR R7,R7,#1			
			BGT adjust_max				
			MOV R8,R7				
			B all_done				
39	B test_while	ADD R6,R7,#1	LDR R9,[R4,R7]			LSR R7,R7,#1	0 exec units busy
		B test_while	CMP R9,R3				
		SUB R5,R7,#1	BLT adjust_min				
			BGT adjust_max				
			MOV R8,R7				
			B all_done				
40		B test_while	CMP R9,R3	LDR R9,[R4,R7]			1 MEM unit busy
		SUB R5,R7,#1	BLT adjust_min				
		B test_while	BGT adjust_max				
			MOV R8,R7				
			B all_done				
			ADD R6,R7,#1				
41		B test_while	CMP R9,R3		LDR R9,[R4,R7]		1 MEM unit busy
		SUB R5,R7,#1	BLT adjust_min				
		B test_while	BGT adjust_max				
			MOV R8,R7				
			B all_done				
			ADD R6,R7,#1				
42		B test_while	CMP R9,R3			LDR R9,[R4,R7]	0 exec units busy
		SUB R5,R7,#1	BLT adjust_min				
		B test_while	BGT adjust_max				
			MOV R8,R7				
			B all_done				
			ADD R6,R7,#1				

Cycle	FI	DEC	DIS	EX	WB	Notes
43		SUB R5,R7,#1	BLT adjust_min			1 ALU unit busy
		B test_while	BGT adjust_max			
			MOV R8,R7	CMP R9,R3		
			B all_done			
			ADD R6,R7,#1			
			B test_while			
44		SUB R5,R7,#1	BLT adjust_min		CMP R9,R3	0 exec units busy
		B test_while	BGT adjust_max			
			MOV R8,R7			
			B all_done			
			ADD R6,R7,#1			
			B test_while			
45		B test_while	BGT adjust_max			1 ALU unit busy
			MOV R8,R7			
			B all_done	BLT adjust_min		
			ADD R6,R7,#1			
			B test_while			
			SUB R5,R7,#1			
46		B test_while	BGT adjust_max		BLT adjust_min	Branch not taken
			MOV R8,R7			0 exec units busy
			B all_done			
			ADD R6,R7,#1			
			B test_while			
			SUB R5,R7,#1			
47			MOV R8,R7			1 ALU unit busy
			B all_done			
			ADD R6,R7,#1	BGT adjust_max		
			B test_while			
			SUB R5,R7,#1			
			B test_while			
48			MOV R8,R7		BGT adjust_max	Branch not taken
			B all_done			0 exec units busy
			ADD R6,R7,#1			
			B test_while			
			SUB R5,R7,#1			
			B test_while			

Cycle	FI	DEC	DIS	EX	WB	Notes
49			ADD R6,R7,#1			2 ALU units busy
			B test_while			
			SUB R5,R7,#1	MOV R8,R7		
			B test_while	B all_done		
50			ADD R6,R7,#1		MOV R8,R7	Branch taken
			B test_while		B all_done	0 exec units busy
			SUB R5,R7,#1			Program done
			B test_while			