Jiaying Song

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TECHNICAL SKILLS

- Programming Languages: Verilog, System Verilog, VHDL, Perl, TCL, C, Java, C#
- Tools: Altim Designer,HSPICE, Spectre, Cadence Virtuoso and Encounter,FPGA Synopsys Design Compiler and Primetime, Xilinx Vivado, AutoCAD,Matlab Mentor Calibre and ModelSIM, NI Multisim, NI LabVIEW ,

EDUCATION

- **Diploma Program, Software Engineering Technology** **05/2021 -- Current**
  Centennial College, Toronto Canada.
  Courses: Java Programming, Advanced Database Concepts,Software Systems Design, Mobile Apps Development, Linear Algebra and Statistics, C# Programming.
- **M.S., Electrical and Computer Engineering** **01/2016 -- 06/2017**
  Portland State University, Portland Oregon.
  Courses: Digital IC Design I & II, ASIC: Modeling & Synthesis, SOC Design with FPGA's Formal Verification HW/SW System, Low Power Digital IC Design, HIGH Performance Digital System, IC Technologies, Linux Workshop.
- **B.S., Electronics Information Science and Technology** **08/2011 -- 07/2015**
  Harbin Institute of Technology, Harbin China.
  Courses: CMOS Analog Integrated Circuit, Semiconductor Manufacturing Technology, Microelectronic Fabrication, Verilog HDL, Microprocessor Technology.

WORKING EXPERIENCE

ELECTRICAL ENGINEER -- AcuVu Inc (Redwood City, USA) 07/2017-- 05/2021

- Designed camera cable and PCB board connection and used Altim Designer for the PCB layout. Worked with cross functional team and studied function flow and connected central unit, camera, control pad and power unit.
- Developed verification environment and tested bench components in System Verilog using UVM methodology. Participated in the EMC testing and analyzed testing result.
- Used Oscilloscope testing different signal forms, acquired data and found the camera non-working issue. Debugged the camera wire issue and fixed the system nonfunctional image missing problem.
- Verified software operation system and tested different function modes, analyzed electronics signal results and validated central unit system high speed I/O signal.

PROJECTS -- Master's Program (Portland, USA) 01/2016 -- 06/2017

- **Design and Layout of Digital CMOS Circuits**: Designed standard logic cells, And Or Inverter and static inverter with different NMOS and PMOS sizing in Cadence Virtuoso. Designed layouts of full custom and sea of gates standard cells for AOI21 and inverter and performed DRC and LVS. Implemented circuit simulation in Spectre.
- **Motion Tracking Dance Machine using FPGA**: Implemented Verilog code to provide different mono audio outputs with Xilinx Nexys 4 DDR Artix-7 FPGA board and a video camera to track and detect human (upper-body) movements. Made the VGA monitor displayed a real-time 2D dancing figure.
- **Line following rojobot using Nexys FPGA**: Developed firmware to implement the line following algorithm on Xilinx PicoBlaze softcore 8-bit microprocessor. Implemented VGA controller interface logic on Nexys 4 board to display bot icon and world map on the screen.

PROJECTS -- Bachelor's Program (Harbin, China) 08/2011 -- 07/2015

- **Design and Realization of MIPS Micro-controller:** Designed and realized of load/store instructions, arithmetic logic, and flow control instructions. Designed and realized of UART with basic functions.
- **Image Processing with Matlab**: Realized function of RGB to Gray, rotate the image, binary conversion, noise removal and image clarity in Matlab.
- **Semiconductor Manufacturing Lab working**: Produced a waffle using photolithography, diffusion and ion implantation, deposition, etching, planarization and packing.

HONORS AND AWARDS

- **Design and Application of Solar-Aeromodel:** This project winning second prize in the 2014Undergraduate Training Programs for Creativity & Entrepreneurship and the best prize at final at the seventh national college students innovation annual meeting.