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Analog Front-end for EMG Acquisition System

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***Abstract*—This paper presents a four-channel analog front-end (AFE) for electromyogram (EMG) acquisition systems. Each input channel consists of a chopper-stabilized instrumentation amplifier (IA) and a low-pass filter (LPF). A 16-bit analog-to-digital converter (ADC) is shared between four-input channels through a 4-to-1 multiplexer and a buffer amplifier. To achieve a 16-bit resolution, a second-order feed-forward incremental ADC (IADC) with a 1.5-bit quantizer is employed. The prototype AFE is fabricated in a 0.18 µm CMOS process with an active die area of 1.4 mm^2. It achieves a 1.12 µV$_{RMS}$ input referred noise with an input channel gain of 44 dB and an LPF cutoff frequency of 500 Hz, while consuming 615 µW/channel from a 1.8 V supply.**

***Index Terms*—Analog front-end (AFE), electro-myogram (EMG), instrumentation amplifier (IA), chopper stabilization, incremental analog-to-digital converter (IADC)**

I. INTRODUCTION

The acquisition of bio signals such as electrocardiograms (ECGs), electroencephalograms (EEGs), and electro-myograms (EMGs) has become an important feature of the mobile devices for human interfaces and health care applications. As shown in Fig. 1, these bio signals have various amplitudes in the range of few microvolts to millivolts and frequencies span from DC to several kHz. Therefore, an analog front-end (AFE) with a low input referred noise, programmable gain and bandwidth is required considering the target signal characteristics [1-5].

Among these bio signals, surface EMG signal is often used for motion detection by analyzing the electrical signal produced by the activity of skeletal muscles. To measure surface EMG signal under the conditions of common-mode interference and electrode offset, high common-mode rejection ratio (CMRR) and high-pass filter (HPF) characteristics are required [6-8].

This paper presents an AFE for the EMG acquisition system with four-input channels and a 16-bit analog-to-digital converter (ADC). Section II describes the architecture of the proposed AFE for the EMG acquisition system. The detailed circuit designs of the input channel and the ADC are discussed in section III and section IV, respectively. Section V reports the experimental results and the conclusions of this paper are presented in section VI.

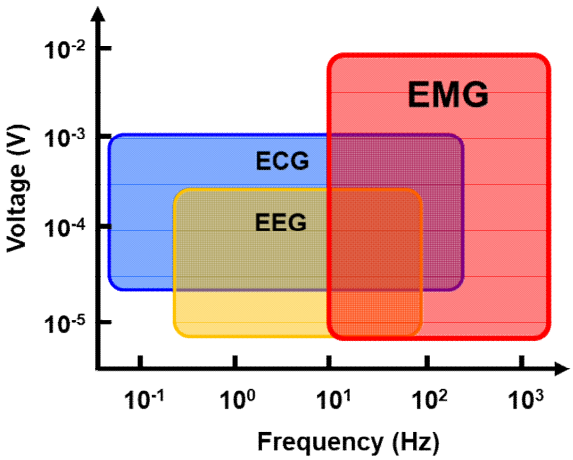

Fig. 1. Frequency and amplitude characteristics of biopotential signals.

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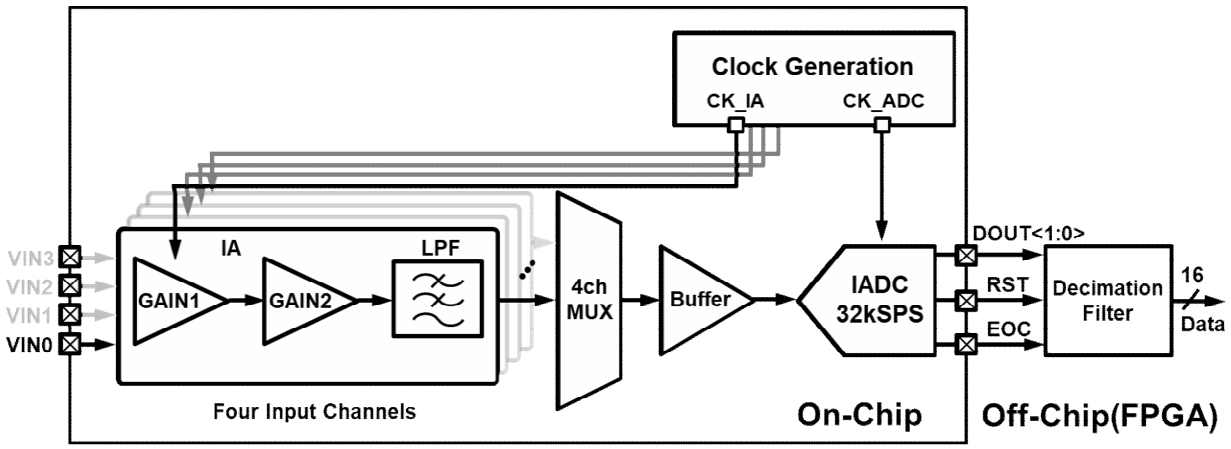


Fig. 1 Block diagram of the proposed AFE for EMG acquisition system.

II. ARCHITECTURE

Fig. 2 shows a block diagram of the proposed AFE for the EMG acquisition system. It consists of four-input channels, a multiplexer, a buffer amplifier, an ADC, a clock generator, and an off-chip decimation filter.

Each input channel consists of an instrumentation amplifier (IA) with programmable gain and a low-pass filter (LPF). A conventional three operational amplifier (op-amp) IA that consists of two cascaded gain stages is employed to achieve high gain and high input impedance with high CMRR [1, 9]. As the frequency of the EMG signal spans from a few Hz to a few kHz, the in-band noise of the AFE is dominated by the flicker noise. To attenuate flicker noise efficiently, a chopper stabilization technique is used in the IA [10-12]. A passive RC LPF is employed to reject the out-of-band noise and attenuate the glitches resulting from the chopper operation. To drive the sampling capacitor of the ADC, a buffer amplifier is used. The buffer and the ADC are shared with four-input channels using a multiplexer to reduce power consumption and area. To measure the EMG signal with the specified gain of the input channel, an ADC resolution higher than 15 bits is required. To achieve the target resolution with four-channel multiplexing, a 32-kS/s incremental ADC (IADC) is used since it can readily be multiplexed between multiple channels [13, 14]. The digital decimation filter is designed off-chip using an FPGA.

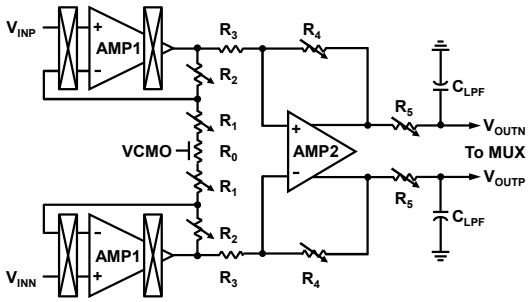


Fig. 3. Circuit diagram of the input channel.

III. INPUT CHANNEL

Fig. 3 shows the circuit diagram of the input channel. It consists of three op-amps IA and a passive LPF. The IA gain is determined by the product of the first stage gain and the second stage gain:

$$Gain = \frac{R_1 + 2R_2}{R_1} \times \frac{R_4}{R_3}. \quad (1)$$

The gain values of the first stage are 20 dB and 40dB. The gain range of the second stage is from 6 dB to 24 dB with a 6 dB step. Therefore, the total gain range of the proposed AFE is from 26 dB to 64 dB. A passive LPF is implemented using a resistor, R_5 and a capacitor, C_{LPF}. The cutoff frequency is adjusted by changing the resistance of R_5.

Fig. 4 shows the schematic of the AMP1 in the input channel. A Miller-compensated two-stage op-amp topology that consists of a folded-cascode first stage and a common-source second stage is employed to

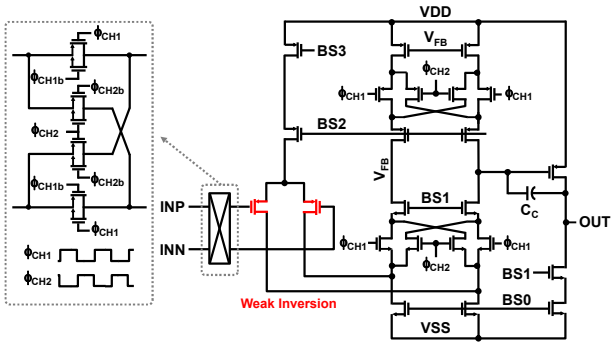


Fig. 4. Schematic of the AMP1 in the input channel.

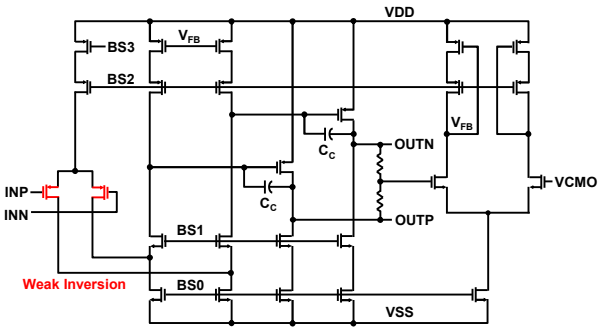


Fig. 5. Schematic of the AMP2 in the input channel.

compensate the gain reduction resulting from the weak-inversion input devices and to drive the resistive load. To reduce the effect of input offset and low-frequency noise, the chopper stabilization technique is adopted. The chopper switches are located at the input and output branches of the first stage of the AMP1. The input offset and low-frequency flicker noise of the amplifier are modulated to the chopping frequency [11]. The modulated low-frequency noise is attenuated by the following LPF. The PMOS transistors used for the input differential pair are biased in weak inversion for a low-noise design [15, 16].

Fig. 5 shows the schematic of the fully differential op-amp of the second gain stage (AMP2) with continuous-time common-mode feedback. Its input differential pair is also biased in weak inversion for a low-noise design. A two-stage topology is employed to achieve a high gain and drive the resistive loads as AMP1.

A four-input multiplexer is employed to share the following 16-bit ADC. A unity gain buffer is employed to drive the switched capacitor sampling network of the ADC with the required settling accuracy. Fig. 6 shows the circuit diagram of the fully-differential unity gain buffer. A two-stage topology with continuous-time

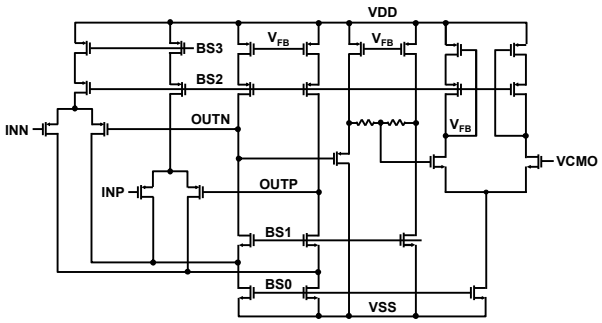


Fig. 6. Schematic of the fully-differential unity gain buffer.

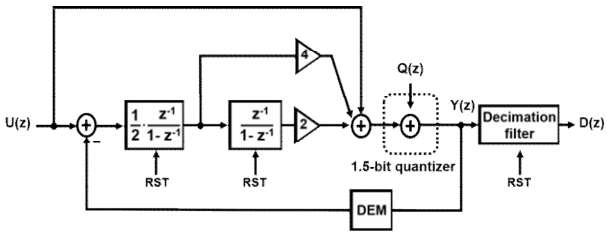


Fig. 7. Block diagram of 16-bit incremental ADC.

common-mode feedback is used.

IV. INCREMENTAL ADC

1. Modulator Topology

To achieve a resolution higher than a 16-bit, an IADC is employed. The maximum signal-to-quantization noise ratio (SQNR) of an IADC is determined by

$$SQNR \cong L \cdot 20log\left(OSR\right) + 20log\left(N-1\right) - 20\log\left(L!\right) \quad (2)$$

where L is the order of IADC, OSR is the oversampling ratio, and N is the number of levels of the quantizer [17]. Typically, the actual peak signal-to-noise ratio (SNR) of the modulator is lower than the theoretical maximum $SQNR$ because the assumptions during the analysis are not applicable in a real operation. Moreover, if flicker and thermal noises are included, the difference becomes larger. To satisfy a target performance, a second-order 1.5-bit IADC with 512 OSR is used. From (2), the maximum theoretical $SQNR$ is 108.4 dB.

Fig. 7 shows the z-domain block diagram of the proposed second-order 1.5-bit feedforward IADC. The signal transfer function (STF) and noise transfer function (NTF) of the proposed modulator is given by

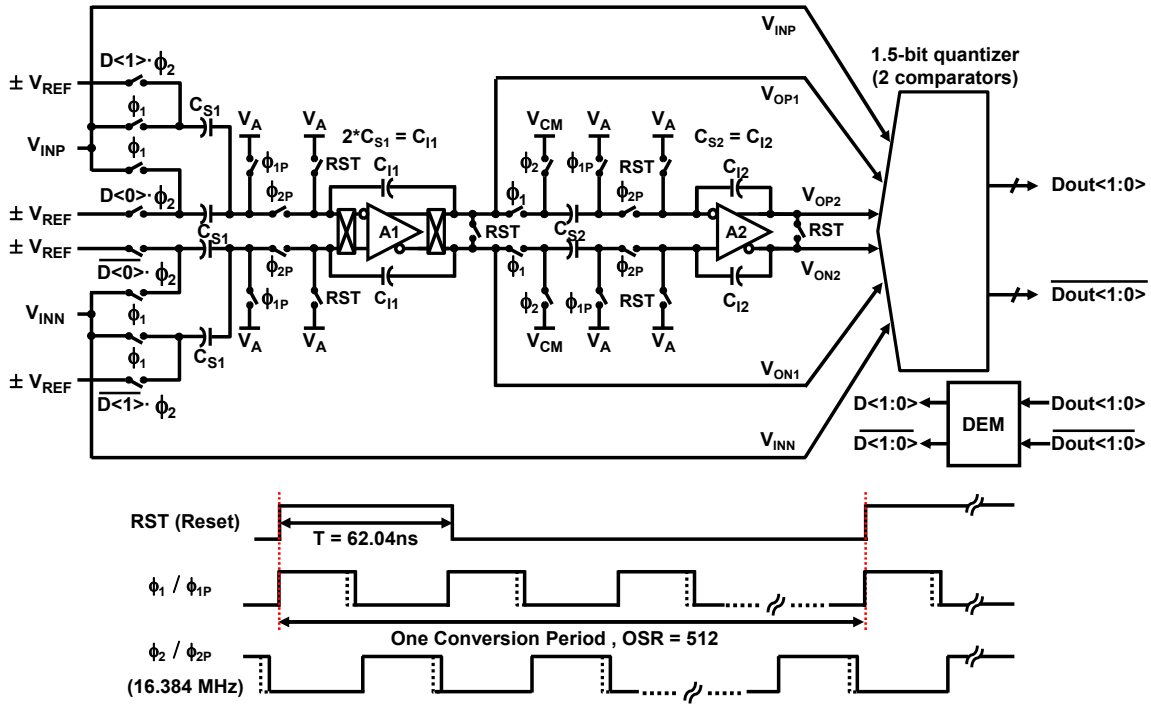


Fig. 8. Circuit schematic and timing diagram of the IADC.

$$STF = \frac{Y(z)}{U(z)} = 1, \qquad NTF = \frac{Y(z)}{Q(z)} = \left(1 - z^{-1}\right)^2. \tag{3}$$

In the feed-forward topology, the integrators process only the quantization noise. Therefore, the linearity requirement of the integrators is relaxed. Another advantage is that only one digital-to-analog converter (DAC) is required in the feedback loop [18]. Therefore, the circuit complexity and chip area can be reduced when a multibit quantizer is used.

The operation of the proposed IADC is as follows. At the beginning of each conversion cycle, the reset signal, RST, initializes the integrators and the decimation filter. After the initial reset, the analog input voltage, U(z), is modulated by the loop filter and the digital decimation filter concurrently processes the modulator output bit stream Y(z). After one conversion cycle, a valid output data D(z) is generated and the next reset pulse initializes all integrators and the decimation filter. The proposed IADC operates at a clock frequency of 16.384 MHz with an OSR of 512. The output data rate after the decimation filter is 32 kHz. The ADC can support up to a 4 kHz signal bandwidth for each channel of the proposed AFE.

2. Circuit Implementation

Fig. 8 shows the circuit and timing diagram of the modulator in the proposed 16-bit IADC. The integrator is designed with a discrete-time switched-capacitor circuit. The IADC operates with non-overlapping clocks, ϕ_1 and ϕ_2. The operation of the first integrator is as follows: During the ϕ_1 phase, C_{S1} and C_{D1} of the first integrator samples the input signal while the feedback capacitor C_{I1} holds a previous output. During the following ϕ_2 phase, C_{S1} and C_{D1} are connected to a reference voltage, $+V_{REF}$ or $-V_{REF}$, according to the 1.5-bit quantizer output. During this phase, the signal difference between the sampled input and feedback DAC is integrated in the feedback capacitor C_{I1}. The operation of the second integrator is similar to that of the first integrator except for the no-feedback path from the quantizer output. To reduce the offset and low-frequency noise of the amplifier, the chopper stabilization technique is used in the first integrator with the half frequency of the IADC operating clock. To increase the settling accuracy, bootstrap switches are used in the first integrator [19]. A single-stage folded-cascade op-amp is used for the first integrator. The PMOS input transistors are biased in weak

inversion to reduce the noise, as in the op-amp of the IA. A dynamic common-mode feedback (CMFB) with a switched-capacitor network is used. The same op-amp topology as that of the first stage is used for the second integrator. However, the input transistors are not biased in weak inversion because the noise requirement of the second integrator is much lower than that of the first integrator.

The 1.5-bit quantizer of the IADC is composed of two comparators. In the feed-forward structure, an analog adder is required to sum the signals from input and outputs of the first and second integrators. A passive summing adder composed of a switched-capacitor network is used. The input signal of the comparators in Fig. 9 is

$$V_+ - V_- = \frac{1}{7}[(V_{INP} - V_{INN}) + 4(V_{OP1} - V_{ON1}) + 2(V_{OP2} - V_{ON2}) \pm \frac{1}{3}(V_{REFP} - V_{REFN})]. \quad (4)$$

The use of a multibit quantizer results in distortion the use of a multibit DAC in the feedback path to the first integrator. In the switched-capacitor DAC of the first integrator, two equal-sized capacitors are used to obtain $-V_{REF}$, 0, and $+V_{REF}$ for a three-level quantizer output. If a single-bit quantizer is used, the linearity of the DAC is always guaranteed because it has only two levels. However, if a multibit quantizer is used, the unit capacitor mismatch of the DAC results in nonlinearity, which causes signal distortion.

A tree-structured dynamic element matching (DEM) technique shown in Fig. 10 is employed to reduce the distortion resulting from the mismatch of the unit capacitors in the feedback DAC [20-22]. It shuffles the thermometer code outputs from the 1.5-bit quantizer.

Fig. 11 shows a block diagram of the second-order decimation filter to convert a 1.5-bit output stream to 16-bit data. A second order decimation filter is employed for a second order IADC [23]. The proposed decimation filter is composed of two cascaded digital accumulators, a divider with a gain of G, and a down sampler that samples a signal at every 512 clocks.

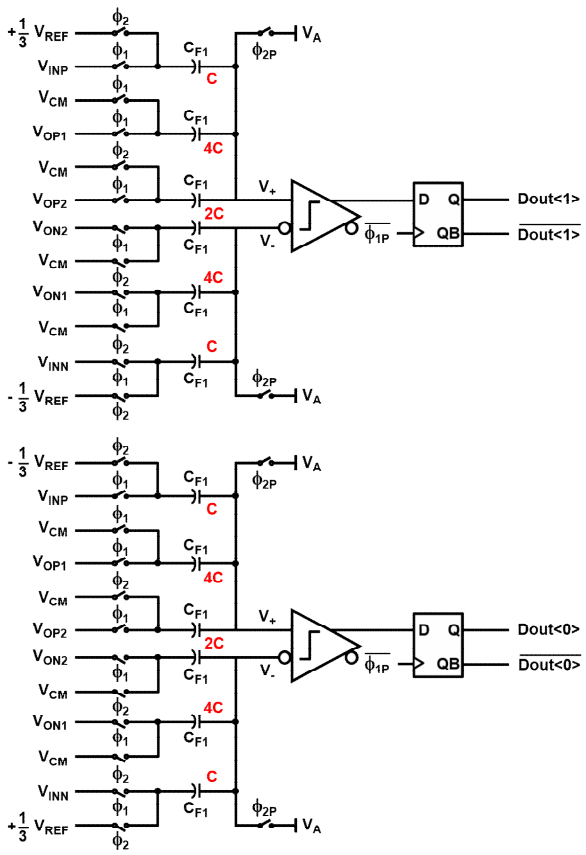


Fig. 9. Schematic of the 1.5-bit quantizer.

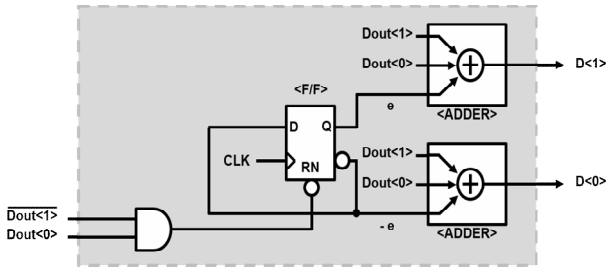


Fig. 10. Block diagram of the tree-structured dynamic element matching circuit.

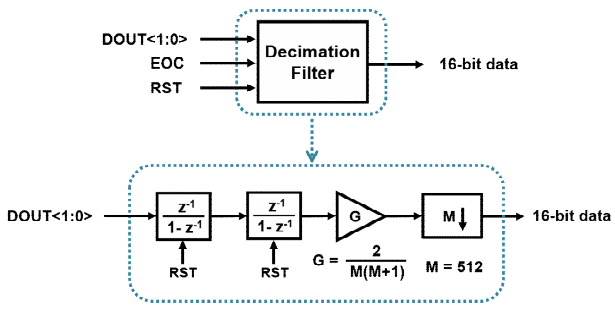


Fig. 11. Block diagram of the decimation filter.

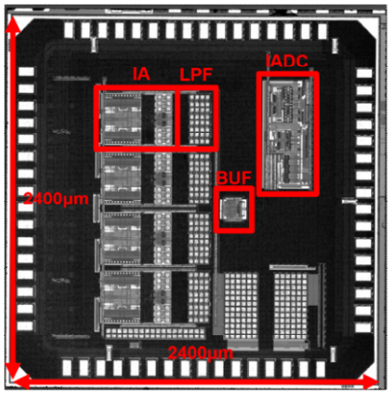


Fig. 12. Chip die photograph of the proposed AFE.

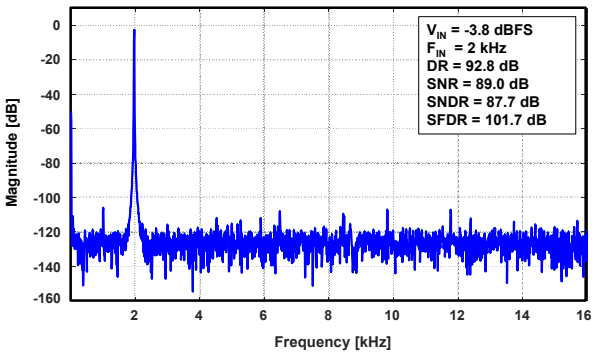


Fig. 13. Output spectrum of the IADC.

V. Measurement Results

The proposed four-channel AFE for EMG acquisition system is implemented in a 0.18 μm CMOS process. The active area of the core circuit that consists of four-input channels, a unity gain buffer and a 16-bit IADC occupies 1.4 mm^2. A chip die photograph of the prototype AFE is shown in Fig. 12.

The output spectrum of the IADC using 4096 points output data at 32 kHz sampling rate with a 2 kHz input sine wave is plotted in Fig. 13. The proposed IADC achieves 92.8 dB of dynamic range (DR), 89.0 dB of signal-to-noise ratio (SNR) and 87.7 dB of signal-to-noise and distortion ratio (SNDR), respectively. The power consumption of the proposed IADC is 1.12 mW (analog: 588 μW, digital: 535 μW) from a 1.8 V supply voltage at 16.384 MHz operating clock frequency.

Fig. 14 is an FFT output spectrum of the proposed AFE for EMG acquisition system when the IA gain is 44 dB, and the 3-dB corner frequency of the LPF is 500 Hz. The measured CMRR is 80 dB and the input referred

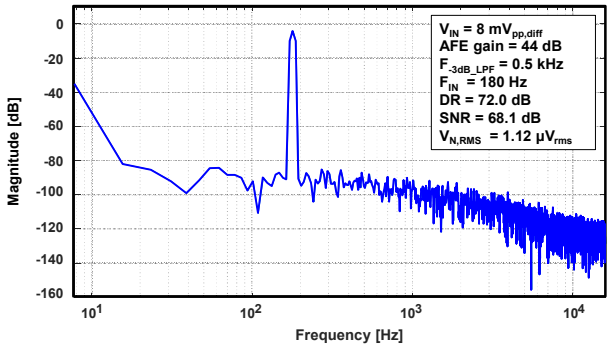


Fig. 14. Output spectrum of the proposed AFE.

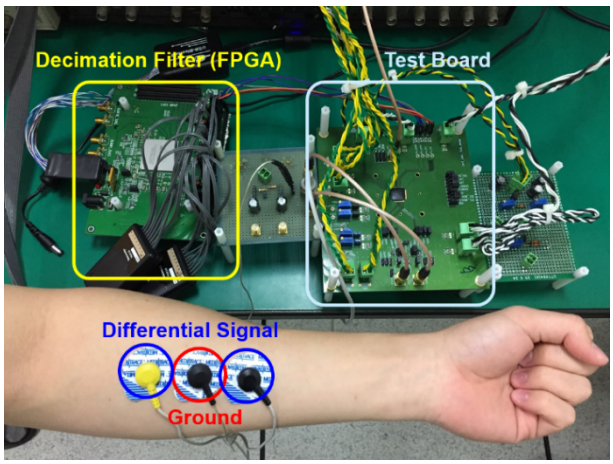
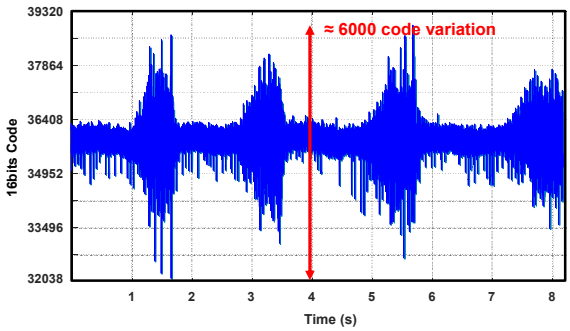


Fig. 15. Test environment of the EMG signal acquisition.

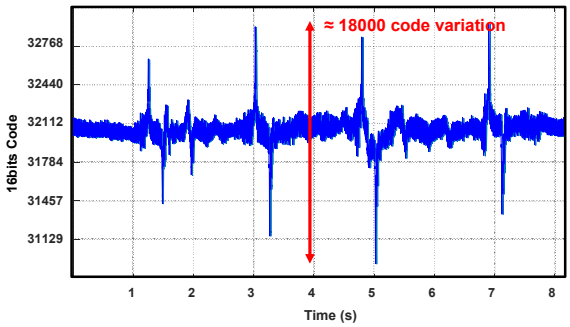
noise is 1.12 μV_{RMS} which is inversely calculated from the 44 dB of input channel gain and the 72 dB of measured DR in Fig. 14. The measured power consumption of the four- input channels is 1.13 mW with a chopping frequency of 32 kHz at a 1.8 V supply voltage. The total power consumption of the prototype AFE is 2.46 mW for four-input channels and an IADC (615 μW/channel).

Fig. 15 shows the test environment for the EMG signal acquisition with wet electrodes attached inside the forearm. Fig. 16 shows the measured waveform of the EMG signal. Here, the input channel gain of 44 dB and the LPF corner frequency of 500 Hz are used. Three different types of actions i.e. fist clenching (pads on the forearm), squat (pads on the thigh), and calf raising (pads on the calf) are repeatedly performed and the measured output waveforms are illustrated in Fig. 16(a)-(c) respectively.

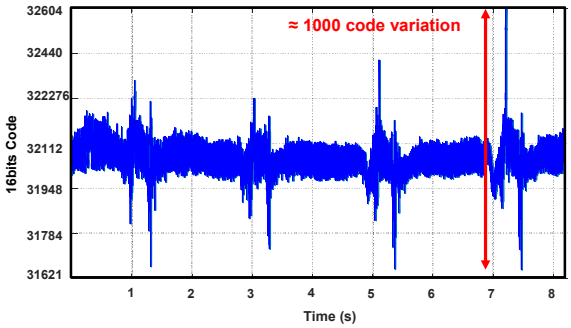
Performance summary of the prototype chip is listed in



(a) Pads on the forearm



(b) Pads on the thigh



(c) Pads on the calf

Fig. 16. A waveform of the measured EMG signal.

Table 1. Performance summary

Process	0.18 μm CMOS
Supply Voltage [V]	1.8
ADC full-scale [$V_{pp,diff}$]	2.0
Sampling Frequency [MHz]	16.384
OSR	512
Input referred noise [μV_{RMS}]	1.12
CMRR [dB]	80.1
DR [dB]	72.0
SNR [dB]	68.1 @ -4.0 dBFS input
SNDR [dB]	66.9 @ -4.0 dBFS input
Power Consumption [μW / channel]	615
Size [mm^2]	1.4

Table 2. Comparison to recently published AFEs for biopotential signal acquisition system

	This work	[24]	[25]	[26]	[27]
Process	0.18 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	65 nm CMOS	0.13 μm CMOS
Supply Voltage [V]	1.8	1.0	1.2	0.3	1.2
Gain [dB]	40 ~ 64	45.6 ~ 60	58	40	45.2 ~ 71
Bandwidth [Hz]	500 ~ 4k	31 ~ 292	0.5 ~ 500	20 ~ 425	70 ~ 400 1.2k ~ 7k
Input referred noise [μV_{RMS}]	1.12 (7.8 Hz ~16 kHz)	2.5 (0.05 Hz ~460 Hz)	1.3 (0.5 Hz ~785 Hz)	26	2.93 (1Hz ~7kHz)
NEF*	6.52	3.26	6.15	-	3.00
CMRR [dB]	72.0	> 71.2	> 100	> 70	> 95
Total current [μA]	230	0.337	7.7	0.003	4.92

$$*\text{NEF} = V_{IN,RMS} \cdot \sqrt{\frac{2 \cdot I_{TOTAL}}{\pi \cdot U_T \cdot 4kT \cdot BW}}$$

Table 1 while Table 2 compares the proposed AFE with recently published works on the AFEs for biopotential signal acquisition system. This work achieves the lowest input referred noise by employing chopper stabilized IA with LPF and shared high-resolution incremental ADC.

VI. Conclusion

A four-input channel AFE for EMG acquisition system is presented in this paper. The AFE is designed in a 0.18 μm CMOS process. The three op-amps IA with passive LPF is used for four-input channels and the second-order feed-forward IADC with 1.5-bit quantizer is employed to achieve 16-bit resolution. The chopper stabilization is used to reduce the low frequency noise and the tree structure DEM is employed to attenuate the distortion resulting from the feedback DAC capacitor mismatch in the IADC. The measured results of the prototype chip demonstrate the input referred noise of 1.12 μV_{RMS} over 16 kHz signal bandwidth with a 44 dB gain of the IA, and a 500 Hz cutoff frequency of the LPF. The total power consumption of the proposed AFE is 2.25 mW.

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REFERENCES

[1] Yixiang Qi, Lin Wei and Haiying Wang, "A Comparison of Instrumentation Amplifiers in Bioelectric Acquisition System," *2010 3rd International Conference on Biomedical Engineering and Informatics*, Oct. 2010.

[2] R. F. Yazicioglu, P. Merken, R. Puers and C. Van Hoof, "A 60 μW 60 nV/√Hz Readout Front-End for Portable Biopotential Acquisition Systems," *IEEE J. Solid-State Circuits*, Vol. 42, No. 5, pp. 1100-1110, May 2007.

[3] X. D. Zou, X. Y. Xu, L. B. Yao and Y. Lian, "A 1-V 450-nW Fully Integrated Programmable Biomedical Sensor Interface Chip," *IEEE J. Solid-State Circuits*, Vol. 44, No. 4, pp. 1067-1077, Apr. 2009.

[4] S. L. Teng, R. Rieger, Y. B. Lin, "Programmable ExG Biopotential Front-End IC for Wearable Applications," *IEEE Trans. Biomed. Circuits Syst.*, Vol. 8, No. 4, pp. 543–551, Aug. 2014.

[5] Y. W. Tseng, Y. C. Ho, S. T. Kao and C. C. Su "A 0.09 μW Low Power Front-End Biopotential Amplifier for Biosignal Recording," *IEEE Trans. Biomed. Circuits Syst.*, Vol. 6, No. 5, pp. 508–516, Oct. 2012.

[6] A. C. Metting van Rijn, A. Peper, and C. A. Grimbergen, "High-quality recording of bioelectric events. Part I: Interference reduction, theory and practice," Med. Bio. Eng. Comput., vol. 28, pp. 389–397, Sep. 1990.

[7] J. G. Webster, Medical Instrumentation: Application and Design, 2nd ed. Boston, MA: Houghton Mifflin, 1992.

[8] N. Van Helleputte, M. Konijnenburg, J. Pettine, D.-W. Jee, H. Kim, A. Morgado, R. Van Wegberg, T. Torfs, R. Mohan, A. Breeschoten, H. de Groot, C. Van Hoof and R. F. Yazicioglu "A 345 μW Multi-Sensor Biomedical SoC With Bio-Impedance, 3-Channel ECG, Motion Artifact Reduction, and Integrated DSP," *IEEE J. Solid-State Circuits*, Vol. 50, No. 1, pp. 230–244, Jan. 2015.

[9] M. A. Smither, D.R. Pugh and L. M. Woolard, "C.M.R.R. analysis of the 3-op-amp instrumentation amplifier," *Electronics Letters*, Vol. 13, No. 20, pp. 594, Sep. 1977.

[10] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of The IEEE*, Vol. 84, No. 11, pp. 1584-1614, Nov. 1996.

[11] M. A. T. Sanduleanu, A. J. M. Van Tuijl, R. F. Wassenaar, M. C. Lammers and H. Wallinga, "A low noise, low residual offset, chopped amplifier for mixed level applications," *IEEE International Conference on Electronics, Circuits and Systems.*, 1998, pp. 333-336.

[12] P. R. Gray, D. Senderowicz and D. G. Messerschmitt, "A Low-Noise Chopper-Stabilized Differential Switched-Capacitor Filtering Technique," *IEEE J. Solid-State Circuits*, Vol. 16, No. 6, pp. 708-715, Dec. 1981.

[13] V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Markus, J. Silva and G. C. Temes, "A Low-Power 22-bit Incremental ADC," *IEEE J. Solid-State Circuits*, Vol. 41, No. 7, pp. 1562-1571, Mar. 2006.

[14] J. Markus, J. Silva and G. C. Temes, "Theory and applications of incremental delta sigma converters," *IEEE Trans. Circuits Syst.I*, Vol. 51, No. 4, pp. 678-690, Apr. 2004.

[15] Masahiko Maruyama, Shigenari Taguchi, Masafumi Yamanoue and Kunihiko Iizuka, "An Analog Front-End for a Multifunction Sensor Employing a Weak-Inversion Biasing Technique With 26 nVrms, 25 aCrms, and 19 fArms Input-Referred Noise," *IEEE J. Solid-State Circuits*, Vol. 51, No. 10, pp. 2252-2261, Oct. 2016.

[16] D. J .Comer and D. T. Comer, "Using the weak inversion region to optimize input stage design of CMOS op amps," *IEEE Trans. Circuits Syst.II*, Vol. 51, No. 1, pp. 8-14, Jan. 2004.

[17] Chia-Hung Chen, Yi Zhang, Tao He, Patrick Y. Chiang and G. C. Temes, "A Micro-Power Two-Step Incremental Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, Vol. 50, No. 8, pp. 1796-1808, Aug. 2015.

[18] J. Silva, U. Moon, J. Steensgaard and G. C. Temes,

"Wideband low-distortion delta-sigma ADC topology," *Electronics Letters*, Vol. 37, No. 12, pp. 737-738, Jun. 2001.

[19] M. Dessouky and A. Kaiser, "Very Low-Voltage Digital-Audio delta-sigma Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping," *IEEE J. Solid-State Circuits*, Vol. 36, No. 3, pp. 349-355, Mar. 2001.

[20] Ian Galton, "Why Dynamic-Element-Matching DACs Work," *IEEE Trans. Circuits Syst.II*, Vol. 57, No. 2, pp. 69-74, Feb. 2010.

[21] Pieter Rombouts and Ludo Weyten, "A Study of Dynamic Element-Matching Techniques for 3-Level Unit Elements," *IEEE Trans. Circuits Syst.II*, Vol. 47, No. 11, pp. 1177-1187, Nov. 2000.

[22] Min Gyu Kim, Gil-Cho Ahn, Pavan Kumar Hanumolu, Sang-Hyeon Lee, Sang-Ho Kim, Seung-Bin You, Jae-Whui Kim, Gabor C. Temes and Un-Ku Moon, "A 0.9 V 92 dB Double-Sampled Switched-RC Delta-Sigma Audio ADC," *IEEE J. Solid-State Circuits*, Vol. 43, No. 5, pp. 1195-1206, May. 2008.

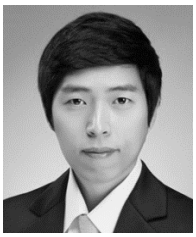
[23] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters.* Piscataway, NJ, USA: IEEE Press/Wiley, 2005.

[24] X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067–1077, 2009.

[25] J. Zheng, S. Member, W. Ki, C. Tsui, and S. Member, "A Fully Integrated Analog Front End for Biopotential Signal Sensing," *IEEE Trans. Circuits Syst. I*, vol. PP, pp. 1–10, 2018.

[26] S. Orguc, H. S. Khurana, H. Lee, and A. P. Chandrakasan, "0.3 V ultra-low power sensor interface for EMG," *in ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, 2017, pp. 219–222.

[27] T. Yang, J. Lu, M. S. Jahan, K. Griffin, J. Langford, and J. Holleman, "A configurable 5.9 μW analog front-end for biosignal acquisition," *Proc. Cust. Integr. Circuits Conf.*, vol. 2015–November, pp. 7–10, 2015.



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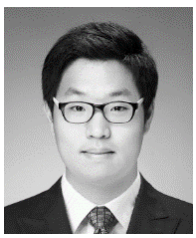

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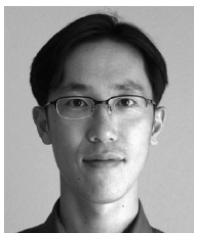

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