Marco Bacis

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Work Experience

e-Novia SpA **Milan**
Sep 2019 - Ongoing *Italy*
Software Engineer

Politecnico di Milano **Milan**
Mar 2019 - Jun 2019 *Italy*
Tutor for the IEIM course (Computer Science for Biomedical Eng. students, C language) and "Prova Finale" course (Software Engineering final project course, Java/OOP concepts etc..) at Politecnico di Milano during the second semester A.Y. 2018/2019.

Maxeler Technologies **London**
Mar 2017 - Aug 2017 *United Kingdom*
Internship in the Machine Learning team, performing design and analysis of ML algorithms for DFE (Java / FPGA-based) acceleration [1] and their integration in face detection pipelines.

Education

Politecnico di Milano **Milan (Italy)**
M.Sc. Computer Science and Engineering, 110 cum laude *Oct 2016 – Oct 2019*

Politecnico di Milano **Milan (Italy)**
B.Sc. Computer Science and Engineering, 106/110 *Oct 2013 - Jul 2016*

Languages: **Italian (native)**, English, French (basic)

Projects

BlastFunction - Accelerated serverless computing *Dec 2018 - Oct 2019*
Master thesis project aimed at integrating FPGAs and serverless computing in an efficient and transparent way. To appear at DATE 2020 conference ([2]).

CONDOR - CNN dataflow optimization using reconfigurable hardware *Nov 2016 - Jun 2018*
Research project at Politecnico di Milano focusing on machine learning acceleration using FPGAs [3, 4, 5].

BEye - Retinal segmentation algorithm on FPGA *Jan 2016 - Jul 2016*
Team manager and hardware developer). The project was presented in a top biomedical conference [6] and reached the finals at the Xilinx Open Hardware Contest.

Skills

Languages: C/C++, Python, Java, Golang, PHP, VB.NET
OS / Platforms: Linux, Mac OS, Docker, Kubernetes
HW architectures: x86, Maxeler DFE, Xilinx/Intel FPGAs (using HLS tools)
Various: LaTeX, Bash

Publications

[1] Nils Voss, Marco Bacis, Oskar Mencer, Georgi Gaydadjiev, and Wayne Luk. "Convolutional Neural Networks on Dataflow Engines". In: *IEEE International Conference on Computer Design*. 2017.

[2] Marco Bacis, Rolando Brondolin, and Marco Domenico Santambrogio. "BlastFunction: an FPGA-as-a-Service system for Accelerated Serverless Computing". In: *Design, Test, Automation and Test in Europe (DATE) Conference*. 2020.

[3] Marco Bacis, Giuseppe Natale, Emanuele Del Sozzo, and Marco Domenico Santambrogio. "A Pipelined and Scalable Dataflow Implementation of Convolutional Neural Networks on FPGA". In: *2017 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. May 2017, pp. 90–97. DOI: 10.1109/IPDPSW.2017.44.

[4] Giuseppe Natale, Marco Bacis, and Marco Domenico Santambrogio. "On how to design dataflow FPGA-based accelerators for Convolutional Neural Networks". In: *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. July 2017.

[5] Niccolò Raspa, Giuseppe Natale, Marco Bacis, and Marco Domenico Santambrogio. "A Framework with Cloud Integration for CNN Acceleration on FPGA Devices". In: *2018 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. May 2018.

[6] Lara Cavinato, Irene Fidone, Marco Bacis, Emanuele Del Sozzo, Gianluca C. Durelli, and Marco D. Santambrogio. "Software Implementation and Hardware Acceleration of Retinal Vessel Segmentation for Diabetic Retinopathy Screening Tests". In: *Engineering in Medicine and Biology Society, International Conference of the IEEE*. 2017.