Marco Bacis

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Work Experience

Mar 2017 - Aug 2017 **Maxeler Technologies**, *London*, United Kingdom.
Internship in the Machine Learning team (newly formed, second member)
- Design and analysis of ML algorithms for DFE (Java / FPGA-based) acceleration
- Accelerator integration in a pipelined architecture for facial recognition
- Tuning of the accelerator to reach high performances [1]

Education

Oct 2016 - present **M.Sc. Computer Science and Engineering**, *Politecnico di Milano*, Milan (Italy).
Attended artificial intelligence, hardware design and distributed system courses. Currently working on a thesis related to cloud architectures and FPGAs.

Oct 2013 - Jul 2016 **B.Sc. Computer Science and Engineering**, *106/110*, Politecnico di Milano, Milan (Italy).
Final project (thesis not required): design and implementation of a client-server board game named *Council of Four* using Java.

Languages **Italian (native)**, English, French (basic)

Contribution to Research Projects

Nov 2016 - Jun 2018 **CONDOR - CNN dataflow optimization using reconfigurable hardware**.
Started as a course project, evolved into a full-fledged research project :
- Responsible for hardware methodology/design
- Co-authored 3 publications on the project [2, 3, 4]

Jan 2016 - Jul 2016 **BEye - Retinal segmentation algorithm on FPGA**.
Developed during the last year of bachelor:
- Team manager (3 people) and hardware developer
- Coatuhored a paper in a top biomedical conference [5]
- Finalist at Xilinx Open Hardware Contest 2016

Skills

Languages C/C++, Java, Python, PHP, VB.NET

OSes Mac OSX, Linux (Ubuntu, Centos), Microsoft Windows

HW architectures x86, Maxeler DFE, Xilinx FPGAs (Vivado/HLS)

Various Latex, Bash scripting

Publications

[1] Nils Voss, Marco Bacis, Oskar Mencer, Georgi Gaydadjiev, and Wayne Luk. "Convolutional Neural Networks on Dataflow Engines". In: *IEEE International Conference on Computer Design*. 2017.

[2] M. Bacis, G. Natale, E. Del Sozzo, and M. D. Santambrogio. "A Pipelined and Scalable Dataflow Implementation of Convolutional Neural Networks on FPGA". In: *2017 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. May 2017, pp. 90–97. DOI: 10.1109/IPDPSW.2017.44.

[3] Giuseppe Natale, Marco Bacis, and Marco Domenico Santambrogio. "On how to design dataflow FPGA-based accelerators for Convolutional Neural Networks". In: *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. July 2017.

[4] N. Raspa, G. Natale, M. Bacis, and M. D. Santambrogio. "A Framework with Cloud Integration for CNN Acceleration on FPGA Devices". In: *2018 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. May 2018.

[5] Lara Cavinato, Irene Fidone, Marco Bacis, Emanuele Del Sozzo, Gianluca C. Durelli, and Marco D. Santambrogio. "Software Implementation and Hardware Acceleration of Retinal Vessel Segmentation for Diabetic Retinopathy Screening Tests". In: *Engineering in Medicine and Biology Society, International Conference of the IEEE*. 2017.