Marco Bacis

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Work Experience

Milan **Italy**
Politecnico di Milano *Mar 2019 - Jun 2019*
Tutor for the IEIM course (Computer Science for Biomedical Eng. students, C language) and "Prova Finale" course (Software Engineering final project course, Java/OOP concepts etc..) at Politecnico di Milano during the second semester A.Y. 2018/2019.

London **United Kingdom**
Maxeler Technologies *Mar 2017 - Aug 2017*
Internship in the Machine Learning team (newly formed, second member)
- Design and analysis of ML algorithms for DFE (Java / FPGA-based) acceleration [1]
- Accelerator integration in a pipelined architecture for facial recognition

Education

Politecnico di Milano **Milan (Italy)**
M.Sc. Computer Science and Engineering *Oct 2016 – Ongoing*
Attended artificial intelligence, hardware design and distributed system courses. Currently working on a thesis related to cloud architectures and FPGAs.

Politecnico di Milano **Milan (Italy)**
B.Sc. Computer Science and Engineering, 106/110 *Oct 2013 - Jul 2016*
Final project (thesis not required): design and implementation of a client-server board game named *Council of Four* using Java.

Languages: **Italian (native)**, English, French (basic)

Projects

Blastfunction - Accelerated serverless computing *Dec 2018 - Ongoing*
Master thesis project aimed at integrating FPGAs and serverless computing in an efficient and transparent way. Technologies used: Xilinx and Intel FPGAs, Docker, Kubernetes, C++, Golang, gRPC.

CONDOR - CNN dataflow optimization using reconfigurable hardware *Nov 2016 - Jun 2018*
Started as a course project, evolved into a full-fledged research project :
- Responsible for hardware methodology/design
- Co-authored 3 publications on the project [2, 3, 4]

BEye - Retinal segmentation algorithm on FPGA *Jan 2016 - Jul 2016*
Developed during the last year of bachelor (as team manager and hardware developer):
- Coatuhored a paper in a top biomedical conference [5]
- Finalist at Xilinx Open Hardware Contest 2016

Skills

Languages: C/C++, Java, Golang, Python, PHP, VB.NET

OS / Platforms: Linux, Mac OS, Docker, Kubernetes

HW architectures: x86, Maxeler DFE, Xilinx/Intel FPGAs (using HLS tools)

Various: LaTeX, Bash

Publications

[1] Nils Voss, Marco Bacis, Oskar Mencer, Georgi Gaydadjiev, and Wayne Luk. "Convolutional Neural Networks on Dataflow Engines". In: *IEEE International Conference on Computer Design*. 2017.

[2] M. Bacis, G. Natale, E. Del Sozzo, and M. D. Santambrogio. "A Pipelined and Scalable Dataflow Implementation of Convolutional Neural Networks on FPGA". In: *2017 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. May 2017, pp. 90–97. DOI: 10.1109/IPDPSW.2017.44.

[3] Giuseppe Natale, Marco Bacis, and Marco Domenico Santambrogio. "On how to design dataflow FPGA-based accelerators for Convolutional Neural Networks". In: *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. July 2017.

[4] N. Raspa, G. Natale, M. Bacis, and M. D. Santambrogio. "A Framework with Cloud Integration for CNN Acceleration on FPGA Devices". In: *2018 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. May 2018.

[5] Lara Cavinato, Irene Fidone, Marco Bacis, Emanuele Del Sozzo, Gianluca C. Durelli, and Marco D. Santambrogio. "Software Implementation and Hardware Acceleration of Retinal Vessel Segmentation for Diabetic Retinopathy Screening Tests". In: *Engineering in Medicine and Biology Society, International Conference of the IEEE*. 2017.