SPECIFICATIONS
NI sbRIO-9651

System on Module OEM Device

Figure 1. sbRIO-9651 SOM
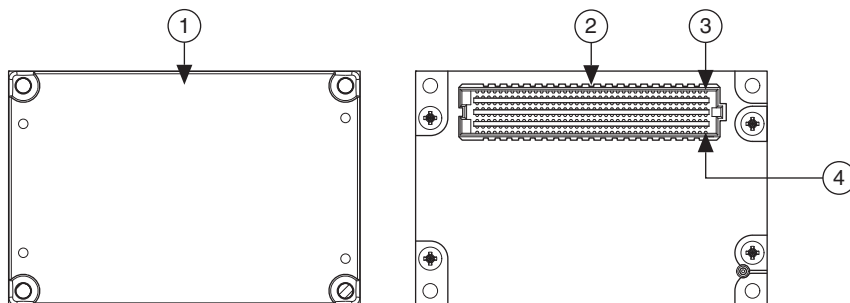
1	Heat Spreader	3	Pin 8
2	J1 8 × 40 320-pin Connector	4	Pin 1

The NI sbRIO-9651 System on Module (SOM) provides an embedded real-time processor and reconfigurable FPGA. The sbRIO-9651 SOM requires a user-designed carrier board to provide power and I/O interfaces. You can optimize the carrier board to implement the exact functions your application requires. You can design the carrier board size and connector locations to fit the packaging or enclosure of your specific system.

This document provides dimensions, pinout information, functional specifications, and electrical specifications for the sbRIO-9651 SOM. The specifications listed in this document are typical for the -40 °C to 85 °C local ambient operating temperature range unless otherwise noted.

📝 **Note** Refer to the documents listed in the *Additional Documentation Resources* section of this document for more information as you design, prototype, and implement your sbRIO-9651 SOM application. In particular, refer to the *NI sbRIO-9651 System on Module Carrier Board Design Guide* for detailed information about carrier board design techniques, guidelines, and requirements.

NATIONAL INSTRUMENTS™

Contents

Part Numbers and Accessories

Table 1 lists purchasable sbRIO-9651 SOM kits and important accessories.

Table 1. sbRIO-9651 SOM Part Numbers and Accessories

Component	Manufacturer, Part Number
Kits	
sbRIO-9651 SOM Development Kit	NI, 783525-01
sbRIO-9651 OEM Kit	NI, 783525-02
Accessories	
M3 × 7.15 mm (0.281 in.) stainless standoffs, male-female, nylon threadlock	NI, 157543-020 (20 pieces) NI, 157543-500 (500 pieces)
Heat sink*	AlphaNovatech, S01LZZ0E-A
* The sbRIO-9651 SOM development kit includes a heat sink.	

Selecting an Appropriate Mating Connector

The J1 connector on the sbRIO-9651 SOM is a Molex 45971-4185 320-pin, 8 × 40 position, SEARAY open-pin-field-array connector. To interface with the J1 connector, your carrier board design must implement a mating connector that is compatible with the Molex 45971 series or Samtec SEAF series. Table 2 lists compatible mating connectors, such as the Molex 45970 series or Samtec SEAM series.

Note Refer to the *NI sbRIO-9651 System on Module Carrier Board Design Guide* for more information about implementing a mating connector.

Table 2. sbRIO-9651 SOM Connector and Compatible Mating Connectors

Connector	Manufacturer, Part Number
sbRIO-9651 SOM J1 connector	Molex, 45971-4185 (equivalent to Samtec SEAF-40-05.0-S-08-2-A-K-TR)
Recommended mating connector*	Molex, 45970-4130
Alternative 7-mm stack height mating connectors	Molex, 45970-4185 Samtec, SEAM-40-02.0-S-08-2-A-K-TR

* Compatible connectors are available in multiple stack height and termination options. NI has secured a special Molex connector part number, 45970-4130, with a 7-mm mated pair stack height. The recommended connector is distributed through TTI, Inc. at NI-negotiated pricing and with shortened lead times. Contact TTI, Inc. directly to obtain the negotiated pricing. Online pricing might not reflect negotiated pricing. Consult Molex or Samtec for alternative stack heights and terminations.

Selecting Appropriate Standoffs

The Molex 45970 series and Samtec SEAM series connectors are available in multiple heights. The height of the mating connector you select determines the height of the standoffs you need.

To prevent over-insertion, the SEARAY connector design requires that standoffs never be less than the stack height. Because standard nominal tolerances might result in a standoff being shorter than the stack height, NI requires that you use standoffs that are 0.15 mm (0.006 in.) taller than the combined height of the J1 connector on the sbRIO-9651 SOM and the mating SEARAY connector. Therefore, to determine the required standoff height, you must add the heights of the mated connectors plus an additional 0.15 mm (0.006 in.). Refer to Samtec documentation for more information about SEARAY standoff requirements.

Table 3 provides an example standoff height calculation using a Molex 45970-4130 mating connector.

Table 3. Example Connector Configuration and Calculated Standoff Height

Component	Manufacturer, Part Number	Height
J1 connector on the sbRIO-9651 SOM	Molex, 45971-4185	5.00 mm (0.197 in.)
Mating connector	Molex, 45970-4130	2.00 mm (0.079 in.)
Required additional standoff height	—	0.15 mm (0.006 in.)
Total calculated standoff height	—	**7.15 mm (0.281 in.)**

Standoffs of 7.15 mm (0.281 in.) height are available from NI and listed in Table 1. Consult Molex or Samtec for alternative heights and options. You must observe keepouts and maximum heights with all connector combinations.

Dimensions

Figures 2 through 4 show the physical dimensions of the sbRIO-9651 SOM.

Note For two-dimensional drawings and three-dimensional models, visit `ni.com/dimensions` and search for `9651`.

Figure 2. sbRIO-9651 SOM Top View with Dimensions
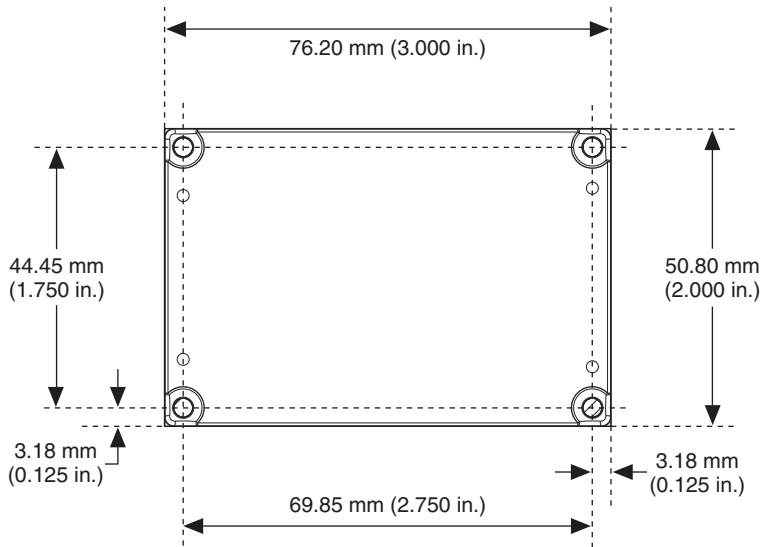
Figure 3. sbRIO-9651 SOM Bottom View with Dimensions
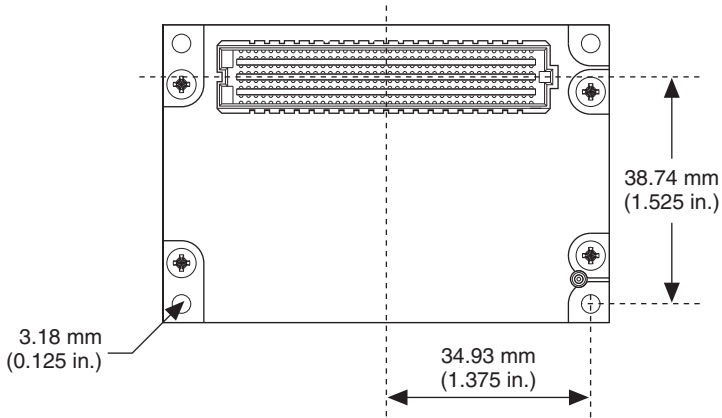
Figure 4. sbRIO-9651 SOM Side View with Dimensions
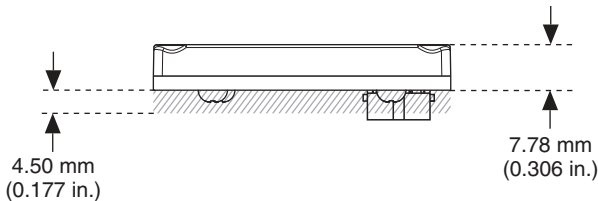
✎ **Note** Do not place components other than the SEARAY connector and mounting standoffs within 4.5 mm (0.177 in.) of the secondary-side printed circuit board surface. This keepout allows components on the sbRIO-9651 SOM to be up to 2.5 mm (0.098 in.) tall and provides a 2 mm (0.079 in.) air gap to prevent electrical shorting. The maximum component height for your carrier board in the area below the sbRIO-9651 SOM is the total SEARAY stack height less 4.5 mm (0.177 in.).

Software Requirements

Install or verify that you have installed the following software:

- LabVIEW 2014 or later
- LabVIEW Real-Time Module 2014 or later
- LabVIEW FPGA Module 2014 or later
- NI-RIO Device Drivers August 2014 or later

Functional Specifications

Processor

Type...Xilinx Zynq-7000,
XC7Z020 All Programmable SoC

Architecture ....ARM Cortex-A9

Speed...667 MHz

Cores 2

Operating system ....NI Linux Real-Time (32-bit)

Nonvolatile memory ....512 MB[1], SLC NAND Flash

Volatile memory (DRAM) ....512 MB, DDR3

Real-time clock
    Accuracy ....5 ppm

Flash reboot endurance ....100,000 cycles[2]

For information about the life span of the nonvolatile memory and about best practices for using nonvolatile memory, visit `ni.com/info` and enter the Info Code `SSDBP`.

Reconfigurable FPGA

Type...Xilinx Zynq-7000,
XC7Z020 All Programmable SoC

Number of logic cells..85,000

Number of flip-flops 106,400

Number of 6-input LUTs 53,200

Number of DSP slices (18×25 multipliers).....220

Available block RAM ....560 KB

Number of DMA channels................................16

Number of logical interrupts.............................32

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[1] Formatted capacity of nonvolatile memory may be slightly less than this value.

[2] You can increase the flash reboot endurance value by performing field maintenance on the device. If you expect that your application may exceed the maximum cycle count listed in this document, contact National Instruments support for information about how to increase the reboot endurance value.

Fixed Behavior Signals

The J1 connector dedicates pins for the following fixed I/O signals:

- Primary Ethernet (GBE0) support
- UART/Console Out (Serial1) support
- USB (USB0 and USB1) support
- SDIO support

Primary Ethernet (GBE0) Support

📝 **Note** You must connect this interface to voltage-mode-PHY-compatible Ethernet magnetics. The *NI sbRIO-9651 System on Module Carrier Board Design Guide* provides design guidelines, requirements for routing signals, and recommendations for appropriate magnetics and connectors. The following specifications depend on a suitable carrier board design that follows these guidelines and requirements.

Network interface .... 10Base-T, 100Base-TX, 1000Base-T Ethernet

Compatibility .... IEEE 802.3

Communication rates .... 10 Mbps, 100 Mbps, 1,000 Mbps
auto-negotiated, half-/full-duplex

Primary Ethernet LED Behavior

The J1 connector provides signals for implementing Ethernet LEDs on a carrier board.

The GBE0_ACT_LEDg signal indicates the link status and activity of the Ethernet connection, as described in Table 4

Table 4. Ethernet Link Activity LED Behavior

Link State	GBE0_ACT_LEDg Behavior
No link	Low
Link, but no activity	High
Link with activity	Toggling

The GBE0_SPEED_LEDg and GBE0_SPEED_LEDy signals indicate the link speed of the Ethernet connection, as described in Table 5.

Table 5. Ethernet Speed LED Behavior

Link Speed	GBE0_SPEED_LEDg*	GBE0_SPEED_LEDy*
No link	Low	Low
10Base-T	Low	Low

Table 5. Ethernet Speed LED Behavior (Continued)

Link Speed	GBE0_SPEED_LEDg*	GBE0_SPEED_LEDy*
100Base-TX	High	Low
1000Base-T	Low	High
* When enabled, GBE1 speed LEDs behave the same as GBE0 speed LEDs.		

UART/Console Out (Serial1) Support

Note You must connect this interface to an appropriate RS-232 serial transceiver on your carrier board design. The *NI sbRIO-9651 System on Module Carrier Board Design Guide* provides design guidelines, requirements for routing signals, and recommendations for a serial transceiver. The following specifications depend on a suitable carrier board design that follows these guidelines and requirements and utilizes the recommended or an equivalent transceiver.

Maximum baud rate ....230,400 bps

Data bits 5, 6, 7, 8

Stop bits 1, 2

Parity..Odd, Even, Mark, Space

Flow control ....RTS/CTS, XON/XOFF, DTR/DSR, None[1]

Console Out

When Console Out is enabled, the Serial1 interface functions as a console for the operating system. You can use a serial-port terminal program to read the IP address, read the firmware version, and access the console. Ensure that the serial-port terminal program is configured with the following settings:

- 115,200 bps
- Eight data bits
- No parity
- One stop bit
- No flow control

You can use Measurement & Automation Explorer (MAX) software or the SYS_RST# signal to enable Console Out. Refer to the *SYS_RST#* section of this document for more information about how to enable Console Out.

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[1] To enable hardware flow control and modem lines for the Serial1 interface, you must use the sbRIO CLIP Generator application. Refer to the *NI Single-Board RIO CLIP Generator Help*, described in the *Additional Documentation Resources* section of this document, for more information about using the sbRIO CLIP Generator application.

USB (USB0 and USB1) Support

📝 **Note** The *NI sbRIO-9651 System on Module Carrier Board Design Guide* provides design guidelines, requirements for routing signals, and recommendations for an appropriate connector. The following specifications depend on a suitable carrier board design that follows these guidelines and requirements.

Number of interfaces
    USB Host/Device 1 (USB0)
    USB Host-only 1 (USB1)

USB interface .... USB 2.0, Hi-Speed

Maximum data rate... 480 Mb/s per interface

Configuring the USB0 Mode

You can configure the USB0 interface to be a USB Host port or a USB Device port, as shown in Table 6. This mode is set when the system boots and does not change dynamically.

📝 **Note** USB On-The-Go (OTG) is not supported.

Table 6. Configuring the USB0 Mode

Mode	How to Enable
USB Host	Connect the USB0_MODE signal to digital ground on your carrier board
USB Device	Connect the USB0_MODE signal to the VCC_3V3 rail on your carrier board

SDIO Support

📝 **Note** The *NI sbRIO-9651 System on Module Carrier Board Design Guide* provides design guidelines, requirements for routing signals, and recommendations for an appropriate connector. The following specifications depend on a suitable carrier board design that follows these guidelines and requirements.

Supported standards.. SD, SDHC[1]

Throughput[2]
    Read .... 12.0 MB/s max
    Write .... 9.0 MB/s max

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[1] Both standard SD and microSD interfaces are supported.

[2] Throughput was benchmarked using the NI 780246-01 2 GB SD card and the 783658-01 16 GB SDHC card. Similar performance is expected on other high-performance SD/SDHC cards. Throughput depends on the removable storage used. Refer to the manufacturer specifications for the removable storage you use for more information about the expected performance of your application.

Support Signals

The J1 connector dedicates pins for the following fixed support signals:

- SYS_RST#
- CARRIER_RST#
- STATUS_LED
- TEMP_ALERT
- FPGA_CFG
- DIO_35_PUDC

> **Note** The # character at the end of a signal name indicates that the signal asserts low.

SYS_RST#

The SYS_RST# signal is a system reset signal for resetting the sbRIO-9651 SOM processor and FPGA. Asserting this signal causes the CARRIER_RST# signal to also assert. The SYS_RST# signal asserts low.

The amount of time for which this signal asserts determines the specific reset behavior, as shown in Figure 5.

Figure 5. SYS_RST# Behavior
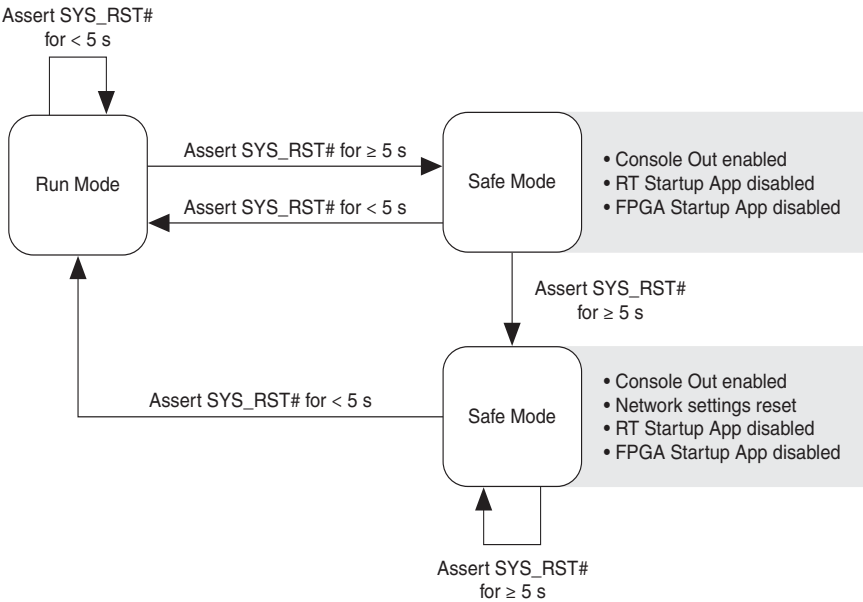
The STATUS_LED signal deasserts when the SYS_RST# signal asserts and remains deasserted until either five seconds have elapsed or the SYS_RST# signal deasserts. The STATUS_LED signal remains asserted until the operating system on the sbRIO-9651 SOM processor has loaded. When the operating system has loaded, the STATUS_LED signal follows one of the patterns described in Table 7.

You can assert the SYS_RST# signal before you apply power to the sbRIO-9651 SOM. The sbRIO-9651 SOM remains in reset until the SYS_RST# signal deasserts. If you assert the SYS_RST# signal before power is applied, then you must deassert the SYS_RST# signal within five seconds.

Configuring Device Startup Options

You can configure device startup options in MAX by completing the following steps:

1. In the MAX configuration tree, select your device under **Remote Systems**.
2. Select the **System Settings** tab.
3. Configure the following options under **Startup Settings**:
   - Safe Mode
   - Console Out
   - Disable RT Startup App
   - Enable Secure Shell (SSH) Logins
   - Disable FPGA Startup App

Refer to the *Measurement & Automation Explorer Help* for more information about these settings.

CARRIER_RST#

The CARRIER_RST# signal indicates that main power is inadequate or that the sbRIO-9651 SOM is in reset. Asserting the SYS_RST# signal causes this signal to also assert. The CARRIER_RST# signal asserts low.

You can use this signal to reset interfaces that must be initialized on the carrier board. Refer to the *NI sbRIO-9651 System on Module Carrier Board Design Guide* for more information.

STATUS_LED

The STATUS_LED signal indicates the status of the sbRIO-9651 SOM boot process and Safe Mode state, as Table 7 describes. This signal asserts high.

Table 7. STATUS_LED Patterns and Indications

LED Pattern	Indication
Off	The device is in Run Mode because software is installed and the operating system is running.
2	The device is in Safe Mode because software is not installed, which is the factory default state, or software has been improperly installed on the device. An error can occur when an attempt to upgrade the software is interrupted. Reinstall software on the device. Refer to the *Measurement & Automation Explorer Help* for information about installing software on the device.
3	The device is in user-directed Safe Mode, or the device is in Install Mode to indicate that software is currently being installed. The device enters user-directed Safe Mode when the SYS_RST# signal asserts for longer than five seconds or when you enable Safe Mode in MAX. Refer to the *Measurement & Automation Explorer Help* for information about Safe Mode.
4	The device is in Safe Mode because it has crashed twice without rebooting or cycling power between crashes. This usually indicates that the device has run out of memory or that your LabVIEW Real-Time application has crashed. Review your LabVIEW Real-Time application to resolve any memory leaks.
Continuously flashing	The device has detected an unrecoverable error. If possible, format the device. If the problem persists, contact National Instruments for support.
Solid	The device is currently booting. This pattern also indicates when the SYS_RST# signal has been asserted for longer than five seconds.

TEMP_ALERT

The TEMP_ALERT signal indicates that the onboard CPU/FPGA or Primary System temperature has exceeded the minimum or maximum temperature specifications of the sbRIO-9651 SOM. This signal is asserted high. Refer to the *Environmental* section of this document for the minimum and maximum temperature specifications.

📝 **Note** This signal is functional only when polling the TempReadings Property Node in LabVIEW Real-Time. This Property Node is part of the NI System Configuration API. The TEMP_ALERT state updates only when you access the TempReadings Property Node. If your LabVIEW Real-Time application does not implement this functionality, the TEMP_ALERT signal does not assert when an over- or under-temperature event occurs. Visit ni.com/info and enter the Info Code sbriosensors for example code and more information about how to use the TEMP_ALERT signal.

FPGA_CFG

The FPGA_CFG signal indicates when the FPGA is configured. For the fixed behavior interfaces on the sbRIO-9651 SOM to function correctly, the FPGA must be configured with a bitfile. If you do not provide a user bitfile, the sbRIO-9651 SOM loads a default bitfile. The FPGA_CFG signal asserts when a user bitfile or the default bitfile loads. This signal asserts high.

This signal is actively driven only when asserted. The sbRIO-9651 provides a pull-down to keep the signal low when deasserted.

DIO_35_PUDC

The DIO_35_PUDC signal is an FPGA Digital I/O (DIO) that also sets the Pull-up During Configuration (PUDC) state on the FPGA. To ensure that the sbRIO-9651 SOM operates correctly, this signal must be high when the FPGA is not configured. The sbRIO-9651 SOM provides a pull-up on DIO_35_PUDC. This pin may be left disconnected on your carrier board.

NI recommends that you use this signal as an output without external pull-down resistors. If you use this signal as an input, you must ensure that the signal is high when the FPGA is not configured, including initial power on.

User-Defined FPGA Signals

The J1 connector provides several banks of FPGA Digital I/O (DIO) pins that you configure for purposes specific to your application. You can use these signals to implement the following interfaces:

- Secondary Ethernet (GBE1) support
- Additional UART (Serial2 through Serial6) support
- CAN (CAN0 and CAN1) support
- FPGA DIO

Secondary Ethernet (GBE1) Support

Note This interface is a GMII interface that. When you enable this interface, you must connect it to the NI-recommended Ethernet PHY. The *NI sbRIO-9651 System on Module Carrier Board Design Guide* provides design guidelines, requirements for routing signals, and recommendations for an appropriate Ethernet PHY, appropriate magnetics, and an appropriate connector. The following specifications depend on a suitable carrier board design that follows these guidelines and requirements.

Network interface ....10Base-T, 100Base-TX, 1000Base-T Ethernet

Compatibility ....IEEE 802.3

Communication rates ....10 Mbps, 100 Mbps, 1,000 Mbps
auto-negotiated, half-/full-duplex

Secondary Ethernet LED Behavior

You can configure FPGA pins on the J1 connector to provide Ethernet speed LED signals for secondary Ethernet.

These signals have the same behavior as the Primary Ethernet speed LED signals. Refer to Table 5, *Ethernet Speed LED Behavior*, in the *Primary Ethernet LED Behavior* section of the *Primary Ethernet (GBE0) Support* section of this document for more information.

To implement an activity LED for secondary Ethernet, refer to the *NI sbRIO-9651 System on Module Carrier Board Design Guide*.

Additional UART (Serial2 through Serial6) Support

📝 **Note** You must connect each of these interfaces to an appropriate RS-232 or RS-485 serial transceiver on your carrier board design. The *NI sbRIO-9651 System on Module Carrier Board Design Guide* provides design guidelines, requirements for routing signals, and recommendations for a serial transceiver. The following specifications depend on a suitable carrier board design that follows these guidelines, requirements, and recommended or equivalent transceivers.

Maximum number of interfaces

    RS-232 .... 3 (Serial2, Serial3, Serial4)[1]

    RS-485 .... 2 (Serial5, Serial6)

Maximum baud rate .... 230,400 bps

Data bits 5, 6, 7, 8

Stop bits 1, 2

Parity .... Odd, Even, Mark, Space

RS-232 flow control .... RTS/CTS, XON/XOFF, DTR/DSR, None

RS-485 flow control .... XON/XOFF

RS-485 transmission modes .... 2-wire, 2-wire auto, 4-wire

CAN (CAN0 and CAN1) Support

📝 **Note** You must connect this interface to an appropriate CAN transceiver on your carrier board design. The *NI sbRIO-9651 System on Module Carrier Board Design Guide* provides design guidelines, requirements for routing signals, and recommendations for a CAN transceiver. The following specifications depend on a suitable carrier board design that follows these guidelines and requirements and utilizes the recommended or an equivalent transceiver.

Maximum number of CAN interfaces 2 (CAN0, CAN1)

Baud rate

    Maximum .... 1 Mbps

    Minimum .... 10 kbps

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[1] The maximum number of RS-232 interfaces does not include the Serial1 fixed behavior UART interface.

FPGA DIO

📝 **Note** Refer to the *NI sbRIO-9651 System on Module Carrier Board Design Guide* for information about FPGA DIO best practices.

Total number of DIO channels..........................160

Number of DIO channels per bank

    Bank 0 ....16 single-ended lines

    Bank 1 ....48 single-ended lines or 24 differential pairs

    Bank 2 ....48 single-ended lines or 24 differential pairs

    Bank 3 ....48 single-ended lines or 24 differential pairs

Characteristic impedance of DIO lines

    Bank 0 ....50 Ω

    Bank 1, 2, and 3

        As single-ended lines ....50 Ω

        As differential pairs...........................100 Ω

📝 **Note** Banks 1, 2, and 3 feature user-defined I/O voltage signaling levels. Your carrier board design must provide power for these lines on a per-bank basis at 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V signaling levels.

The DIO lines in Bank 0 are routed as single-ended traces. Figure 6 shows the circuitry of one 3.3 V DIO channel in Bank 0. The lines in Bank 0 include an onboard series termination resistor located at the Xilinx Zynq SoC.

Figure 6. 3.3 V DIO Channel in Bank 0
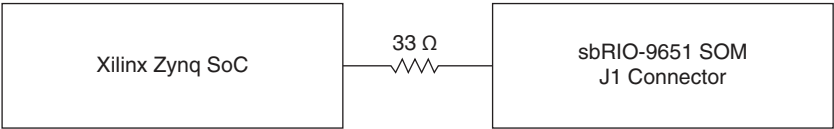
The DIO lines in Banks 1, 2, and 3 are routed as loosely coupled differential pairs from the Xilinx Zynq SoC to the J1 connector. Each DIO_*xx* line has a corresponding negative pair, DIO_*xx*_N. You can configure each pair in the sbRIO CLIP Generator application to operate as differential pairs or single-ended signals. Figure 7 shows the circuitry of one DIO channel pair in Bank 1, 2, or 3.

Figure 7. DIO Channel Pair in Bank 1, 2, or 3
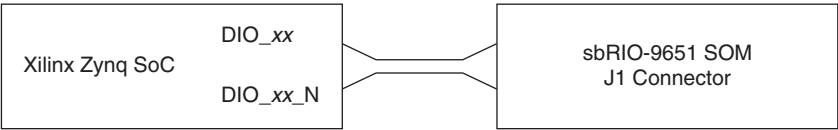
Table 8 lists the DIO pins on the J1 connector and the corresponding FPGA I/O banks, power rails, and the trace lengths on the sbRIO-9651 SOM for each group of pins.

Table 8. FPGA DIO Pins and Trace Lengths

Pins			FPGA I/O Bank	Power Rail	Shortest Trace Length on sbRIO-9651 SOM	Longest Trace Length on sbRIO-9651 SOM	Length Matching within Differential Pairs
DIO_0	...	DIO_15	Bank 0	VCC_3V3	31.24 mm (1.23 in.)	42.16 mm (1.66 in.)	—
DIO_16 DIO_16_N	... ...	DIO_39_SRCC DIO_39_N	Bank 1	VIO_BANK1	33.78 mm (1.33 in.)	37.34 mm (1.47 in.)	0.25 mm (0.01 in.)
DIO_40 DIO_40_N	... ...	DIO_63_SRCC DIO_63_N	Bank 2	VIO_BANK2	24.13 mm (0.95 in.)	26.42 mm (1.04 in.)	0.25 mm (0.01 in.)
DIO_64 DIO_64_N	... ...	DIO_87_SRCC DIO_87_N	Bank 3	VIO_BANK3	28.70 mm (1.13 in.)	30.99 mm (1.22 in.)	0.25 mm (0.01 in.)

FPGA DIO Clock Capabilities

Some FPGA DIO pins have the following FPGA clocking capabilities:

- **Single-region clock capable (SRCC)**—These pins provide a direct connection to the global clock distribution buffers in the FPGA. The pins also connect to the regional buffers on a specific bank of pins. Each SRCC pin has an _SRCC suffix in the pin name.

- **Multi-region clock capable (MRCC)**—These pins provide a direct connection to the global clock distribution buffers in the FPGA. The pins also connect to the regional and multi-regional buffers on a specific bank of pins. Each MRCC pin has an _MRCC suffix in the pin name.

> **Note** When you import a clock into LabVIEW FPGA, NI recommends that you use SRCC or MRCC pins.

Refer to the Xilinx *7 Series FPGAs Clocking Resources User Guide*, UG472, for more information about clock-capable I/O.

Ground Connections

The sbRIO-9651 SOM provides the following ground connections:

- The mounting holes and heat spreader are connected to chassis ground.
- All grounds on the J1 connector are connected to digital ground.
- Chassis ground is capacitively coupled to digital ground near each mounting hole.

Refer to the *NI sbRIO-9651 System on Module Carrier Board Design Guide* for more information about grounding best practices.

Electrical Specifications

Input Power Requirements

The sbRIO-9651 SOM requires multiple power supply rails, which are provided by the carrier board. Table 9 lists the power pin assignments on the J1 connector.

Table 9. Input Power Requirements

Input Rail	Minimum Voltage	Maximum Voltage	Nominal Voltage	Maximum Power	Bulk Capacitance*
VCC_3V3	3.201 V	3.465 V	3.3 V	7 W	370 μF
VIO_BANK1	Refer to footnote † of this table for information about these values.		1.2 V to 3.3 V†	900 mW	110 μF
VIO_BANK2			1.2 V to 3.3 V†	900 mW	110 μF
VIO_BANK3			1.2 V to 3.3 V†	900 mW	110 μF

* The bulk capacitance specified is the onboard capacitance on each input power supply rail of the sbRIO-9651 SOM. This value is specified for consideration when designing power supplies on a carrier board.

† The nominal input voltage for each VIO_BANK input rail can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V. The voltage you implement for a bank must match the requirements for the Xilinx I/O standard that have been assigned to the bank in the sbRIO CLIP Generator. Refer to the *Nominal Input Voltage Requirements* section of this document for minimum and maximum supply voltages for each Xilinx I/O standard.

📝 **Note** These specifications approximate the maximum power requirement for each input rail on an sbRIO-9651 SOM with worst-case silicon manufacturing process and maximum junction temperatures. For a more accurate estimate of the power consumption for a specific application, NI recommends that you directly measure the power the sbRIO-9651 SOM consumes when running your application in an environment that is representative of the intended use case. You can use the Xilinx Power Estimator to calculate the VIO_BANK input rail power for a given configuration.

Nominal Input Voltage Requirements

Table 10 describes the tolerances for each nominal input voltage value for a VIO_BANK input power supply rail.

📝 **Note** Tolerances are based on -3% and +5% of the nominal input voltage.

Table 10. Nominal Input Voltage Tolerances

Nominal Input Voltage	Minimum Input Voltage	Maximum Input Voltage
3.3 V	3.201 V	3.465 V
2.5 V	2.425 V	2.625 V
1.8 V	1.746 V	1.890 V
1.5 V	1.455 V	1.575 V
1.2 V	1.164 V	1.260 V

Power Sequencing Requirements

The recommended power-on sequence is to bring up the VIO_BANK1 input rail before or at the same time as the VCC_3V3 input rail. You can power the VIO_BANK2 and VIO_BANK3 input rails before or after the VCC 3V3 input rail. The power-off sequence is the opposite of the power-on sequence.

If any combination of the VCC_3V3, VIO_BANK1, VIO_BANK2, or VIO_BANK3 input rails have the same nominal voltage level, you can power them from the same supply and ramp them simultaneously.

Following the recommended power sequencing minimizes the current draw and eliminates glitches in I/O by ensuring that I/O pins are tri-stated during power-on.

📝 **Note** For any VIO_BANK input rail voltages of 3.3 V, NI recommends that you use the same power supply for the VIO_BANK and VCC_3V3 input rails. If you must use a separate 3.3 V power supply, then the voltage difference between the VIO_BANK input rail and the VCC_3V3 input rail must not exceed 2.625 V for more than 500 ms per power cycle. You can allocate the time in any percentage between the power-on and power-off ramps.

Power Supply Ramp Times

Table 11 specifies the ramp times for each input power supply rail.

Table 11. Power Supply Ramp Times

Power Supply	Minimum Time	Maximum Time
VCC_3V3 ramp time from GND to 90% of VCC_3V3	0.2 ms	50.0 ms
VIO_BANK ramp time from GND to 90% of VIO_BANK	0.2 ms	50.0 ms

Xilinx I/O Standards Nominal Voltage Requirements

Table 12 specifies the nominal voltage for each Xilinx I/O standard you can select for a VIO_BANK input power supply rail in the sbRIO CLIP Generator.

Table 12. Xilinx I/O Standards Voltage Requirements

Xilinx I/O Standard	Nominal Voltage
LVTTL	3.3 V
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18	1.8 V
LVCMOS15	1.5 V
LVCMOS12	1.2 V
LVDS_25	2.5 V
MINI_LVDS_25	2.5 V

VBAT Requirements

The J1 connector provides a pin for VBAT power, which can be connected to a battery to power the real-time clock while the sbRIO-9651 SOM is unpowered.

Table 13 lists the VBAT power specifications.

Table 13. VBAT Power Specifications

Specification	Minimum	Typical	Maximum
VBAT input voltage	2.875 V	3.0 V	5.5 V
sbRIO-9651 SOM powered VBAT current	—	25 nA	100 nA
sbRIO-9651 SOM unpowered VBAT current	—	2.6 µA average	4.2 µA average

FPGA Voltage Levels

FPGA DIO Voltage Levels

Tables 14 and 15 describe the FPGA input and output voltage levels for each Xilinx I/O standard you can select for a DIO pin in the sbRIO CLIP Generator.

Note Refer to the *Xilinx Zynq-7000 All Programmable SoC (Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics* product specification, DS187, for information about additional standards supported by the Zynq FPGA I/O.

Table 14. FPGA I/O Levels (1 of 2)

I/O Standard	Input Voltage Low, V_{IL} (V)		Input Voltage High, V_{IH} (V)		Output Voltage Low, V_{OL} Max (V)	Output Voltage High, V_{OH} Min (V)	Drive Strength (mA)
	Min	Max	Min	Max			
LVTTL	-0.30	0.80	2.00	3.45	0.40	2.40	4, 8, 12, 16, 24
LVCMOS33	-0.30	0.80	2.00	3.45	0.40	VIO - 0.40	4, 8, 12, 16
LVCMOS25	-0.30	0.70	1.70	VIO + 0.30	0.40	VIO - 0.40	4, 8, 12, 16
LVCMOS18	-0.30	35% of VIO	65% of VIO	VIO + 0.30	0.45	VIO - 0.45	4, 8, 12, 16, 24
LVCMOS15	-0.30	35% of VIO	65% of VIO	VIO + 0.30	25% of VIO	75% of VIO	4, 8, 12, 16
LVCMOS12	-0.30	35% of VIO	65% of VIO	VIO + 0.30	0.40	VIO - 0.40	4, 8, 12

Table 15. FPGA I/O Levels (2 of 2)

I/O Standard	Input Common Mode Voltage, V_{ICM} (V)			Input Differential Voltage, V_{ID} (V)			Output Common Mode Voltage, V_{OCM} (V)			Output Differential Voltage, V_{OD} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
LVDS_25	0.30	1.20	1.425	0.10	—	—	—	1.25	—	Varies with topology and loading		
MINI_LVDS_25	0.30	1.20	1.710	0.20	0.40	0.60	1.00	1.20	1.40	0.30	0.45	0.60*
* Internal V_{CCAUX} = 1.8 V ±5%												

Fixed Behavior Signal I/O Levels

Tables 16 and 17 describe the FPGA input and output voltage levels, respectively, for fixed behavior signals.

Table 16. Fixed Behavior Signal Input Voltages

Signal	V_{IL} (V)		V_{IH} (V)	
	Min	Max	Min	Max
USB0_MODE	-0.30	0.40	2.50	3.60
USB0_VBUS	-0.30	0.20	4.75	5.50
SD_CMD SD_D0 ... SD_D3 SD_CD# SD_WP SYS_RST# SERIAL1_RX	-0.30	0.80	2.00	3.45

Table 17. Fixed Behavior Signal Output Voltages

Signal	V_{OL} Max (V)	V_{OH} Min (V)	Max Sink Current (mA)	Max Source Current (mA)
GBE0_SPEED_LEDg GBE0_SPEED_LEDy USB0_CPEN SD_D0 ... SD_D3 SD_CMD SD_CLK SD_PWR_EN CARRIER_RST# STATUS_LED TEMP_ALERT SERIAL1_RX	0.400	2.735	8	-8
FPGA_CFG	Not actively driven low. Pull-down on signal.	2.735	—	-8

Table 18 lists the signals that provide pull resistors.

Table 18. Signals with Pull Resistors

Signal	Pull Value Typ (Ω)	Pull Resistor Rail
CARRIER_RST#	1.0 k	GND
SD_PWR_EN FPGA_CFG	4.7 k	GND
SYS_RST# SD_CD# SD_WP	4.7 k	VCC_3V3
USB0_MODE	100.0 k	VCC_3V3
DIO_35_PUDC	4.7 k	VIO_BANK1

Physical Characteristics

Board dimensions .... 50.8 mm (2.0 in.) × 76.2 mm (3.0 in.)

Weight .... 77 g (2.72 oz)

Mounting

Fastener torque .... 0.76 N · m (6.70 lb · in.)

Environmental

The sbRIO-9651 SOM includes three onboard temperature monitoring sensors to simplify validation of a thermal solution. The sensors measure the internal system temperature under the heat spreader, the junction temperature of the CPU/FPGA, and a secondary-side printed circuit board temperature. The sensors provide an indication of thermal performance and are used to validate the system along with the local ambient operating temperature.

Local ambient operating temperature near device
(IEC 60068-2-1, IEC 60068-2-2) .... -40 °C to 85 °C

The primary option for measuring the local ambient operating temperature is to place a thermocouple in the location shown in Figure 8.

Figure 8. Measuring the Local Ambient Operating Temperature

5.00 mm
(0.2 in.)
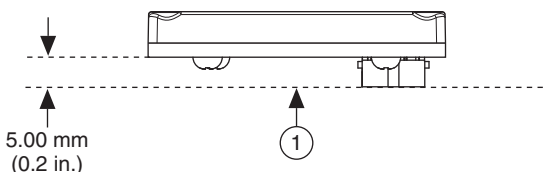
1   Measure local ambient operating temperature here.

> 📝 **Note**   Measure the local ambient temperature by placing a thermocouple near the center of the printed circuit board 5.0 mm (0.2 in.) from the board surface. This temperature must not exceed 85 °C. Alternatively, you can rely on the reported Secondary System temperature to provide a conservative estimate of the local ambient temperature.

Maximum reported onboard sensor temperature

 CPU/FPGA temperature .... 98 °C

 Primary System temperature .... 85 °C

> 📝 **Note**   Ensure that the local ambient, reported CPU/FPGA, and reported Primary System temperatures do not exceed any of the maximum temperatures listed in this document. For more information about how to access the onboard sensors, visit `ni.com/info` and enter the Info Code `sbriosensors`.

> 📝 **Note**   NI sbRIO device thermal performance is greatly influenced by several factors, including resource utilization, mounting, and adjacent power dissipation. Together, these factors can substantially affect the achievable external ambient temperature at which the maximum local and reported temperatures are reached. Additional thermal design will likely be required to remain within the maximum allowed temperature ranges. For information and examples regarding the effect of these design factors, visit `ni.com/info` and enter the Info Code `sbriocooling`. For device-specific guidelines about enabling proper thermal design, refer to the *NI sbRIO-9651 System on Module Carrier Board Design Guide*.

Storage temperature
(IEC 60068-2-1, IEC 60068-2-2) .... -40 °C to 85 °C

Operating humidity (IEC 60068-2-56) .... 10% RH to 90% RH, noncondensing

Storage humidity (IEC 60068-2-56) .... 5% RH to 95% RH, noncondensing

Pollution Degree (IEC 60664) 2

Maximum altitude .... 5,000 m

Indoor use only.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

电子信息产品污染控制管理办法 （中国 **RoHS**）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

Safety Guidelines

Operate the sbRIO-9651 SOM only as described in the user documentation.

⚠ **Caution** The sbRIO-9651 SOM must be installed in a suitable enclosure prior to use.

⚠ **Caution** National Instruments makes no product safety, electromagnetic compatibility (EMC), or CE marking compliance claims for the sbRIO-9651 SOM. The end-product supplier is responsible for conformity to any and all compliance requirements.

⚠ **Caution** Exercise caution when designing an enclosure for the sbRIO-9651 SOM. Auxiliary cooling may be necessary to keep the sbRIO-9651 SOM within the specified operating temperature range. Refer to the *Environmental* section of this document for more information about the maximum operating temperature rating. For information and examples regarding factors that can affect thermal performance, visit `ni.com/info` and enter the Info Code `sbriocooling`.

⚠ **Caution** Do not operate the sbRIO-9651 SOM in a manner not specified in the user documentation. Product misuse can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

J1 Connector Signal Groups

Table 19 lists the pins and signals on the J1 connector, grouped by interface type.

📝 **Note**   Refer to the *NI sbRIO-9651 System on Module Carrier Board Design Guide* for more information about each signal group and how to implement a particular signal in a carrier board design.

Table 19. J1 Connector Pins and Signal Groups

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
Primary Ethernet (GBE0)					
GBE0_MDI0_P	1	GBE0_MDI2_P	3	GBE0_SPEED_LEDg	5
GBE0_MDI0_N	9	GBE0_MDI2_N	11	GBE0_SPEED_LEDy	13
GBE0_MDI1_P	18	GBE0_MDI3_P	20	GBE0_ACT_LEDg	6
GBE0_MDI1_N	26	GBE0_MDI3_N	28		
USB0 Host/Device					
USB0_DP	33	USB0_MODE	65	USB0_VBUS	81
USB0_DN	41	USB0_CPEN	73		
USB1 Host					
USB1_DP	35	USB1_CPEN	50	USB1_VBUS	58
USB1_DN	43				
Serial1 UART (Console Out)					
Serial1_TX	52	Serial1_RX	60		
SDIO					
SD_CLK	15	SD_WP	40	SD_D1	22
SD_CMD	31	SD_PWR_EN	38	SD_D2	24
SD_CD#	32	SD_D0	8	SD_D3	30
Support					
STATUS_LED	14	CARRIER_RST#	37	FPGA_CFG	53
SYS_RST#	47	TEMP_ALERT	46		

Table 19. J1 Connector Pins and Signal Groups (Continued)

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
Power Input					
VCC_3V3	80	VIO_BANK1	120	VIO_BANK3	240
VCC_3V3	88	VIO_BANK1	128	VIO_BANK3	248
VCC_3V3	96	VIO_BANK2	168	VBAT	64
VCC_3V3	104	VIO_BANK2	176		
DIO Bank 0					
DIO_0	66	DIO_6	76	DIO_12	78
DIO_1	74	DIO_7	69	DIO_13	63
DIO_2	59	DIO_8	85	DIO_14	79
DIO_3	75	DIO_9	54	DIO_15_MRCC	87
DIO_4	83	DIO_10	62		
DIO_5	68	DIO_11	70		
DIO Bank 1					
DIO_16	105	DIO_24	155	DIO_32	102
DIO_16_N	113	DIO_24_N	163	DIO_32_N	94
DIO_17	129	DIO_25	100	DIO_33	126
DIO_17_N	137	DIO_25_N	92	DIO_33_N	118
DIO_18	153	DIO_26	124	DIO_34	150
DIO_18_N	161	DIO_26_N	116	DIO_34_N	142
DIO_19	98	DIO_27	148	DIO_35_PUDC	174
DIO_19_N	90	DIO_27_N	140	DIO_35_N	166
DIO_20	122	DIO_28	172	DIO_36_SRCC	111
DIO_20_N	114	DIO_28_N	164	DIO_36_N	119
DIO_21	146	DIO_29	109	DIO_37_MRCC	135
DIO_21_N	138	DIO_29_N	117	DIO_37_N	143
DIO_22	107	DIO_30	133	DIO_38_MRCC	159
DIO_22_N	115	DIO_30_N	141	DIO_38_N	167

Table 19. J1 Connector Pins and Signal Groups (Continued)

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
DIO_23	131	DIO_31	157	DIO_39_SRCC	152
DIO_23_N	139	DIO_31_N	165	DIO_39_N	144
DIO Bank 2					
DIO_40	177	DIO_48	203	DIO_56	198
DIO_40_N	185	DIO_48_N	211	DIO_56_N	190
DIO_41	201	DIO_49	227	DIO_57	222
DIO_41_N	209	DIO_49_N	235	DIO_57_N	214
DIO_42	225	DIO_50	196	DIO_58	246
DIO_42_N	233	DIO_50_N	188	DIO_58_N	238
DIO_43	170	DIO_51	220	DIO_59	183
DIO_43_N	162	DIO_51_N	212	DIO_59_N	191
DIO_44	194	DIO_52	244	DIO_60_SRCC	207
DIO_44_N	186	DIO_52_N	236	DIO_60_N	215
DIO_45	218	DIO_53	181	DIO_61_MRCC	231
DIO_45_N	210	DIO_53_N	189	DIO_61_N	239
DIO_46	242	DIO_54	205	DIO_62_MRCC	200
DIO_46_N	234	DIO_54_N	213	DIO_62_N	192
DIO_47	179	DIO_55	229	DIO_63_SRCC	224
DIO_47_N	187	DIO_55_N	237	DIO_63_N	216
DIO Bank 3					
DIO_64	249	DIO_72	299	DIO_80	294
DIO_64_N	257	DIO_72_N	307	DIO_80_N	286
DIO_65	273	DIO_73	268	DIO_81	318
DIO_65_N	281	DIO_73_N	260	DIO_81_N	310
DIO_66	297	DIO_74	292	DIO_82	255
DIO_66_N	305	DIO_74_N	284	DIO_82_N	263
DIO_67	266	DIO_75	316	DIO_83	279
DIO_67_N	258	DIO_75_N	308	DIO_83_N	287

Table 19. J1 Connector Pins and Signal Groups (Continued)

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
DIO_68	290	DIO_76	253	DIO_84_SRCC	303
DIO_68_N	282	DIO_76_N	261	DIO_84_N	311
DIO_69	314	DIO_77	277	DIO_85_MRCC	272
DIO_69_N	306	DIO_77_N	285	DIO_85_N	264
DIO_70	251	DIO_78	301	DIO_86_MRCC	296
DIO_70_N	259	DIO_78_N	309	DIO_86_N	288
DIO_71	275	DIO_79	270	DIO_87_SRCC	320
DIO_71_N	283	DIO_79_N	262	DIO_87_N	312

Table 20 lists the pins that are connected to GND and pins that are reserved and should be left disconnected.

Table 20. J1 Connector GND and Reserved Pins

Pin #	Pin #	Pin #	Pin #	Pin #	Pin #	Pin #	Pin #
GND							
2	36	77	110	154	197	241	278
4	39	82	112	156	199	243	280
7	42	84	121	158	202	245	289
10	44	86	123	160	204	247	291
12	45	89	125	169	206	250	293
16	48	91	127	171	208	252	295
17	49	93	130	173	217	254	298
19	51	95	132	175	219	256	300

Table 20. J1 Connector GND and Reserved Pins (Continued)

Pin #	Pin #	Pin #	Pin #	Pin #	Pin #	Pin #	Pin #
21	55	97	134	178	221	265	302
23	57	99	136	180	223	267	304
25	61	101	145	182	226	269	313
27	67	103	147	184	228	271	315
29	71	106	149	193	230	274	317
34	72	108	151	195	232	276	319
RESERVED-NC							
56							

J1 Connector Pinout

Figures 10 through 12 show the individual pins on the J1 connector.

Figure 9. sbRIO-9651 SOM J1 Connector Pinout (1 of 4)

Pin 153: DIO_18
Pin 154: GND
Pin 145: GND
Pin 146: DIO_21
Pin 137: DIO_17_N
Pin 138: DIO_21_N
Pin 129: DIO_17
Pin 130: GND
Pin 121: GND
Pin 122: DIO_20
Pin 113: DIO_16_N
Pin 114: DIO_20_N
Pin 105: DIO_16
Pin 106: GND
Pin 97: GND
Pin 98: DIO_19
Pin 89: GND
Pin 90: DIO_19_N
Pin 81: USB0_VBUS
Pin 82: GND
Pin 73: USB0_CPEN
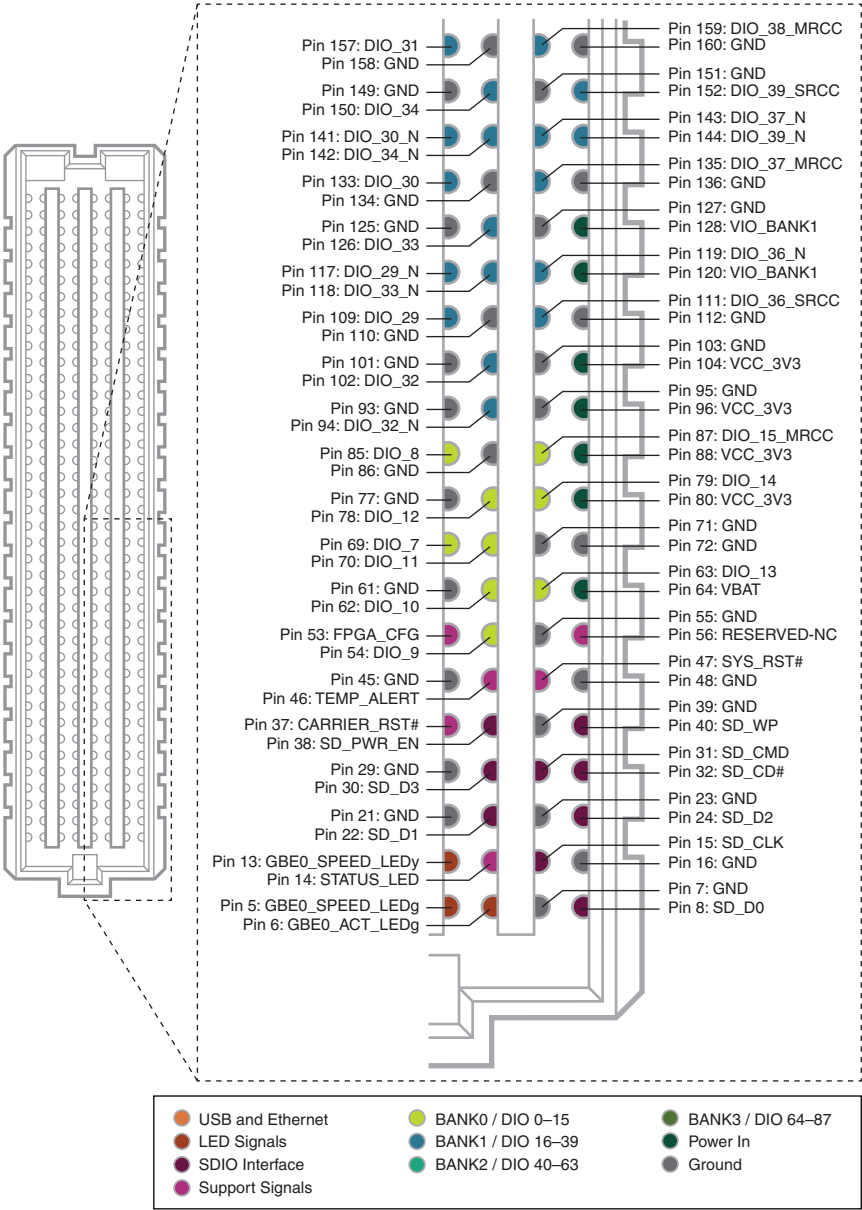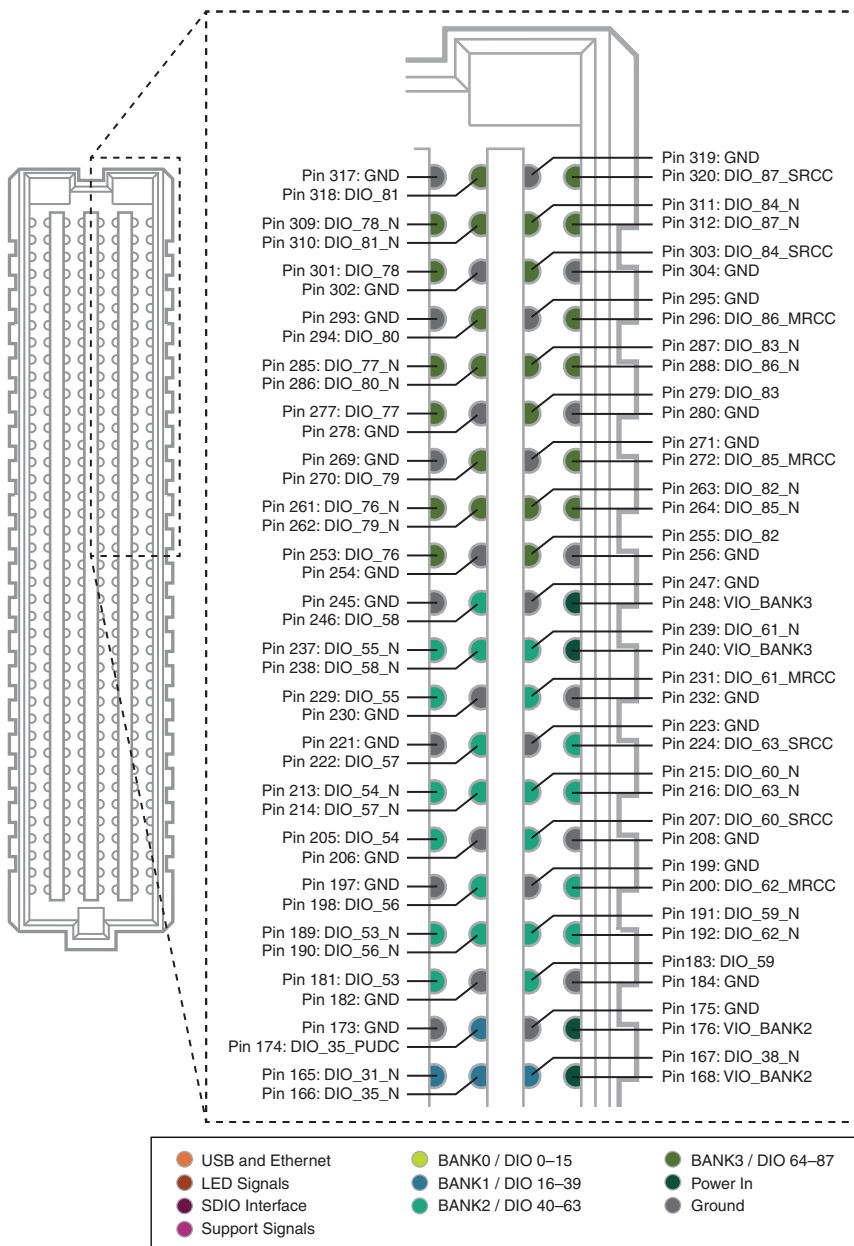Pin 74: DIO_1
Pin 65: USB0_MODE
Pin 66: DIO_0
Pin 57: GND
Pin 58: USB1_VBUS
Pin 49: GND
Pin 50: USB1_CPEN
Pin 41: USB0_DN
Pin 42: GND
Pin 33: USB0_DP
Pin 34: GND
Pin 25: GND
Pin 26: GBE0_MDI1_N
Pin 17: GND
Pin 18: GBE0_MDI1_P
Pin 9: GBE0_MDI0_N
Pin 10: GND
Pin 1: GBE0_MDI0_P
Pin 2: GND

Pin 155: DIO_24
Pin 156: GND
Pin 147: GND
Pin 148: DIO_27
Pin 139: DIO_23_N
Pin 140: DIO_27_N
Pin 131: DIO_23
Pin 132: GND
Pin 123: GND
Pin 124: DIO_26
Pin 115: DIO_22_N
Pin 116: DIO_26_N
Pin 107: DIO_22
Pin 108: GND
Pin 99: GND
Pin 100: DIO_25
Pin 91: GND
Pin 92: DIO_25_N
Pin 83 DIO_4
Pin 84: GND
Pin 75: DIO_3
Pin 76: DIO_6
Pin 67: GND
Pin 68: DIO_5
Pin 59: DIO_2
Pin 60: Serial1_RX
Pin 51: GND
Pin 52: Serial1_TX
Pin 43: USB1_DN
Pin 44: GND
Pin 35: USB1_DP
Pin 36: GND
Pin 27: GND
Pin 28: GBE0_MDI3_N
Pin 19: GND
Pin 20: GBE0_MDI3_P
Pin 11: GBE0_MDI2_N
Pin 12: GND
Pin 3: GBE0_MDI2_P
Pin 4: GND

USB and Ethernet
LED Signals
SDIO Interface
Support Signals
BANK0 / DIO 0–15
BANK1 / DIO 16–39
BANK2 / DIO 40–63
BANK3 / DIO 64–87
Power In
Ground

Figure 10. sbRIO-9651 SOM J1 Connector Pinout (2 of 4)

Pin 157: DIO_31
Pin 158: GND
Pin 149: GND
Pin 150: DIO_34
Pin 141: DIO_30_N
Pin 142: DIO_34_N
Pin 133: DIO_30
Pin 134: GND
Pin 125: GND
Pin 126: DIO_33
Pin 117: DIO_29_N
Pin 118: DIO_33_N
Pin 109: DIO_29
Pin 110: GND
Pin 101: GND
Pin 102: DIO_32
Pin 93: GND
Pin 94: DIO_32_N
Pin 85: DIO_8
Pin 86: GND
Pin 77: GND
Pin 78: DIO_12
Pin 69: DIO_7
Pin 70: DIO_11
Pin 61: GND
Pin 62: DIO_10
Pin 53: FPGA_CFG
Pin 54: DIO_9
Pin 45: GND
Pin 46: TEMP_ALERT
Pin 37: CARRIER_RST#
Pin 38: SD_PWR_EN
Pin 29: GND
Pin 30: SD_D3
Pin 21: GND
Pin 22: SD_D1
Pin 13: GBE0_SPEED_LEDy
Pin 14: STATUS_LED
Pin 5: GBE0_SPEED_LEDg
Pin 6: GBE0_ACT_LEDg

Pin 159: DIO_38_MRCC
Pin 160: GND
Pin 151: GND
Pin 152: DIO_39_SRCC
Pin 143: DIO_37_N
Pin 144: DIO_39_N
Pin 135: DIO_37_MRCC
Pin 136: GND
Pin 127: GND
Pin 128: VIO_BANK1
Pin 119: DIO_36_N
Pin 120: VIO_BANK1
Pin 111: DIO_36_SRCC
Pin 112: GND
Pin 103: GND
Pin 104: VCC_3V3
Pin 95: GND
Pin 96: VCC_3V3
Pin 87: DIO_15_MRCC
Pin 88: VCC_3V3
Pin 79: DIO_14
Pin 80: VCC_3V3
Pin 71: GND
Pin 72: GND
Pin 63: DIO_13
Pin 64: VBAT
Pin 55: GND
Pin 56: RESERVED-NC
Pin 47: SYS_RST#
Pin 48: GND
Pin 39: GND
Pin 40: SD_WP
Pin 31: SD_CMD
Pin 32: SD_CD#
Pin 23: GND
Pin 24: SD_D2
Pin 15: SD_CLK
Pin 16: GND
Pin 7: GND
Pin 8: SD_D0

● USB and Ethernet
● LED Signals
● SDIO Interface
● Support Signals

● BANK0 / DIO 0–15
● BANK1 / DIO 16–39
● BANK2 / DIO 40–63

● BANK3 / DIO 64–87
● Power In
● Ground

Figure 11. sbRIO-9651 SOM J1 Connector Pinout (3 of 4)

Pin 313: GND
Pin 314: DIO_69
Pin 305: DIO_66_N
Pin 306: DIO_69_N
Pin 297: DIO_66
Pin 298: GND
Pin 289: GND
Pin 290: DIO_68
Pin 281: DIO_65_N
Pin 282: DIO_68_N
Pin 273: DIO_65
Pin 274: GND
Pin 265: GND
Pin 266: DIO_67
Pin 257: DIO_64_N
Pin 258: DIO_67_N
Pin 249: DIO_64
Pin 250: GND
Pin 241: GND
Pin 242: DIO_46
Pin 233: DIO_42_N
Pin 234: DIO_46_N
Pin 225: DIO_42
Pin 226: GND
Pin 217: GND
Pin 218: DIO_45
Pin 209: DIO_41_N
Pin 210: DIO_45_N
Pin 201: DIO_41
Pin 202: GND
Pin 193: GND
Pin 194: DIO_44
Pin 185: DIO_40_N
Pin 186: DIO_44_N
Pin 177: DIO_40
Pin 178: GND
Pin 169: GND
Pin 170: DIO_43
Pin 161: DIO_18_N
Pin 162: DIO_43_N

Pin 315: GND
Pin 316: DIO_75
Pin 307: DIO_72_N
Pin 308: DIO_75_N
Pin 299: DIO_72
Pin 300: GND
Pin 291: GND
Pin 292: DIO_74
Pin 283: DIO_71_N
Pin 284: DIO_74_N
Pin 275: DIO_71
Pin 276: GND
Pin 267: GND
Pin 268: DIO_73
Pin 259: DIO_70_N
Pin 260: DIO_73_N
Pin 251: DIO_70
Pin 252: GND
Pin 243 GND
Pin 244: DIO_52
Pin 235: DIO_49_N
Pin 236: DIO_52_N
Pin 227: DIO_49
Pin 228: GND
Pin 219: GND
Pin 220: DIO_51
Pin 211: DIO_48_N
Pin 212: DIO_51_N
Pin 203: DIO_48
Pin 204: GND
Pin 195: GND
Pin 196: DIO_50
Pin 187 DIO_47_N
Pin 188: DIO_50_N
Pin179: DIO_47
Pin 180: GND
Pin 171: GND
Pin 172: DIO_28
Pin 163 DIO_24_N
Pin 164: DIO_28_N

- USB and Ethernet
- LED Signals
- SDIO Interface
- Support Signals
- BANK0 / DIO 0–15
- BANK1 / DIO 16–39
- BANK2 / DIO 40–63
- BANK3 / DIO 64–87
- Power In
- Ground

Figure 12. sbRIO-9651 SOM J1 Connector Pinout (4 of 4)

Pin 317: GND
Pin 318: DIO_81
Pin 309: DIO_78_N
Pin 310: DIO_81_N
Pin 301: DIO_78
Pin 302: GND
Pin 293: GND
Pin 294: DIO_80
Pin 285: DIO_77_N
Pin 286: DIO_80_N
Pin 277: DIO_77
Pin 278: GND
Pin 269: GND
Pin 270: DIO_79
Pin 261: DIO_76_N
Pin 262: DIO_79_N
Pin 253: DIO_76
Pin 254: GND
Pin 245: GND
Pin 246: DIO_58
Pin 237: DIO_55_N
Pin 238: DIO_58_N
Pin 229: DIO_55
Pin 230: GND
Pin 221: GND
Pin 222: DIO_57
Pin 213: DIO_54_N
Pin 214: DIO_57_N
Pin 205: DIO_54
Pin 206: GND
Pin 197: GND
Pin 198: DIO_56
Pin 189: DIO_53_N
Pin 190: DIO_56_N
Pin 181: DIO_53
Pin 182: GND
Pin 173: GND
Pin 174: DIO_35_PUDC
Pin 165: DIO_31_N
Pin 166: DIO_35_N

Pin 319: GND
Pin 320: DIO_87_SRCC
Pin 311: DIO_84_N
Pin 312: DIO_87_N
Pin 303: DIO_84_SRCC
Pin 304: GND
Pin 295: GND
Pin 296: DIO_86_MRCC
Pin 287: DIO_83_N
Pin 288: DIO_86_N
Pin 279: DIO_83
Pin 280: GND
Pin 271: GND
Pin 272: DIO_85_MRCC
Pin 263: DIO_82_N
Pin 264: DIO_85_N
Pin 255: DIO_82
Pin 256: GND
Pin 247: GND
Pin 248: VIO_BANK3
Pin 239: DIO_61_N
Pin 240: VIO_BANK3
Pin 231: DIO_61_MRCC
Pin 232: GND
Pin 223: GND
Pin 224: DIO_63_SRCC
Pin 215: DIO_60_N
Pin 216: DIO_63_N
Pin 207: DIO_60_SRCC
Pin 208: GND
Pin 199: GND
Pin 200: DIO_62_MRCC
Pin 191: DIO_59_N
Pin 192: DIO_62_N
Pin183: DIO_59
Pin 184: GND
Pin 175: GND
Pin 176: VIO_BANK2
Pin 167: DIO_38_N
Pin 168: VIO_BANK2

USB and Ethernet
LED Signals
SDIO Interface
Support Signals
BANK0 / DIO 0–15
BANK1 / DIO 16–39
BANK2 / DIO 40–63
BANK3 / DIO 64–87
Power In
Ground

Additional Documentation Resources

Refer to Figure 13 for additional resources as you design, prototype, and implement your sbRIO-9651 SOM application.

Figure 13. sbRIO-9651 SOM Documentation Resources

What Would You Like to Learn More About?	Resources	Availability
NI sbRIO-9651 System on Module OEM Device	*NI sbRIO-9651 System on Module OEM Device Specifications*	PDF
NI sbRIO-9651 System on Module Development Kit	*NI sbRIO-9651 System on Module Development Kit Quick Start Guide*	PDF, Included in shipping kit
Designing a carrier board for your application	*NI sbRIO-9651 System on Module Carrier Board Design Guide*	PDF
Adding an sbRIO-9651 System on Module target in LabVIEW	*LabVIEW Help (NI-RIO)*	Help file
Creating a socketed CLIP that defines the I/O configuration to use in your application	*NI Single-Board RIO CLIP Generator Help*	Help file
NI Training and Support	ni.com/singleboard/setup ni.com/training ni.com/support	Available online at ni.com

PDF available online at ni.com/manuals Help file available locally Included in the shipping kit Available online at ni.com

Revision History

Table 21 lists changes to this document since its first iteration.

Table 21. Revision History

Revision	Edition Date	Changes
B	December 2014	• Corrected the Samtec connector part numbers listed in Table 2. • Corrected Table 20 to list pin 280 as a GND pin. The previous version of this document incorrectly listed pin 288 as a GND pin. Pin 288 is DIO_86_N, as listed correctly in Table 19.
A	October 2014	—

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