VLSI PROJECT

4-BIT CARRY LOOKAHEAD ADDER

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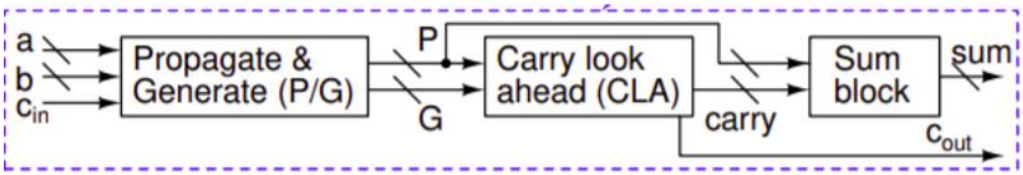
Question 1

Proposed Structure

The 4-bit carry lookahead adder is a special adder that minimizes the computing time required to calculate the sum of two 4-bit numbers and an input carry. It does this by pre-computing the carries at each step unlike a normal ripple adder and can greatly reduce the number of clock cycles required to compute the sum, although at the cost of increased circuit complexity and number of transistors.

The carry lookahead adder has primarily three blocks, namely

- Propagate and generate calculation block
- Carry lookahead calculation block
- Sum block



Consider that the numbers to be added are $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$ and input carry c_{in}.

Let the propagates be given by p_3, p_2, p_1 and p_0, and the generates be given by g_3, g_2, g_1 and g_0. Then, the propagates and generates are given by,

$$p_i = a_i \oplus b_i$$

$$g_i = a_i . b_i$$

The carry out c_{i+1} of the i^{th} bit can be calculated as,

$$c_{i+1} = p_i . c_i + g_i$$

So, for the carry lookahead block, the carries for each bit can be computed simultaneously as,

$$c_1 = p_0 . c_{in} + g_0$$

$$c_2 = p_1 . p_0 . c_{in} + p_1 . g_0 + g_1$$

$$c_3 = p_2 . p_1 . p_0 . c_{in} + p_2 . p_1 . g_0 + p_2 . g_1 + g_2$$

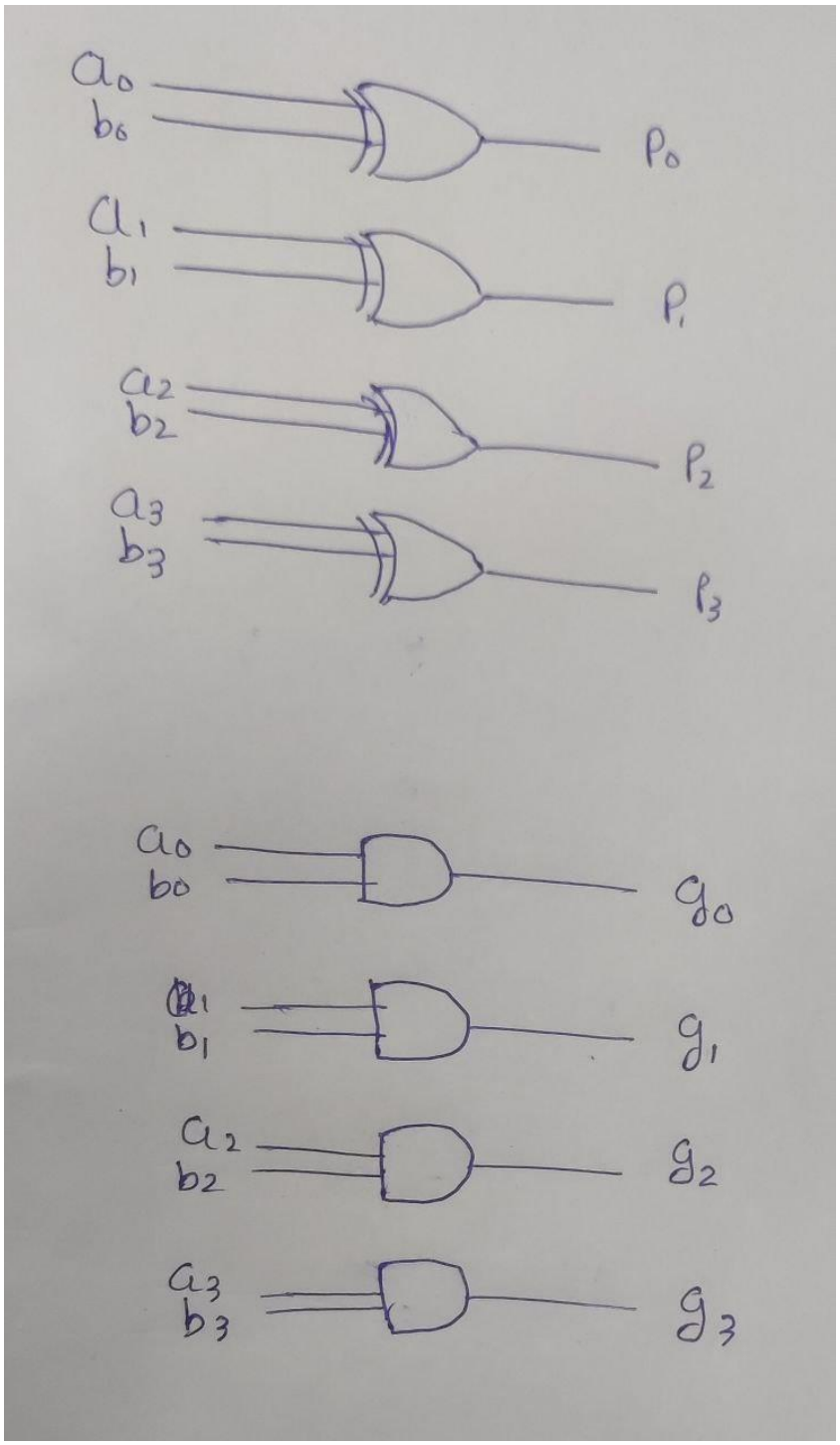
$$c_4 = p_3 . p_2 . p_1 . p_0 . c_{in} + p_3 . p_2 . p_1 . g_0 + p_3 . p_2 . g_1 + p_3 . g_2 + g_3$$

The sum bits s_0, s_1, s_2 and s_3 can be computed as,

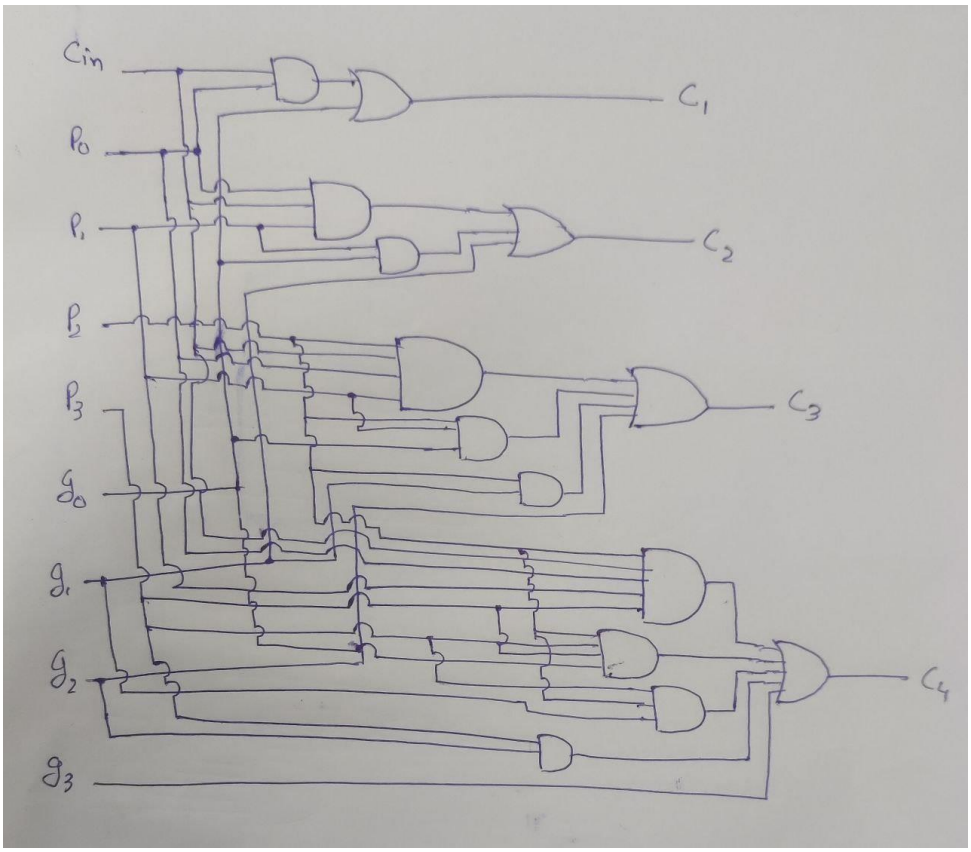
$$s_i = p_i \oplus c_i, \text{ where } c_0 = c_{in}$$

From the Boolean logic above, the circuit diagram could be summarized as,

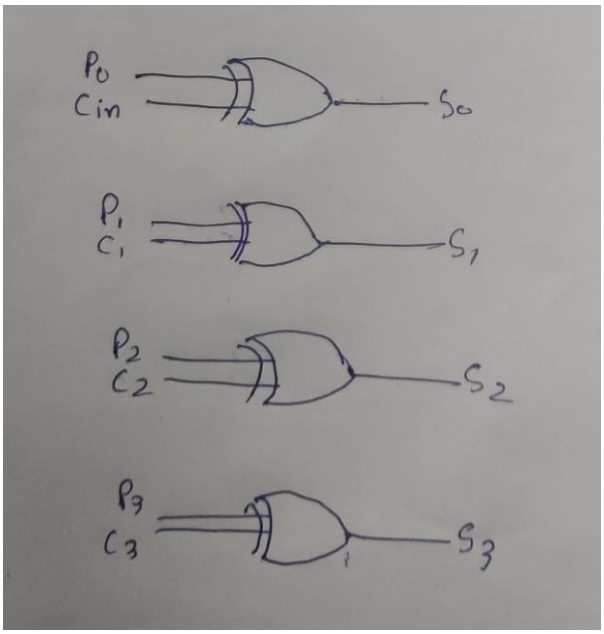
1. Propagate and generate block



2. Carry lookahead block



3. Sum block



The final result of the carry lookahead adder is a five-bit binary number $c_4 s_3 s_2 s_1 s_0$.

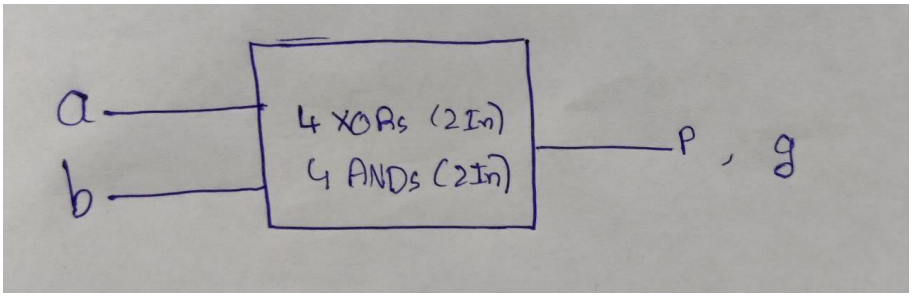
Question 2

Design Details and Topology

The entirety of the circuit is done using complementary CMOS logic, where PMOSFETs drive the pull-up network and NMOSFETs drive the pull-down network.

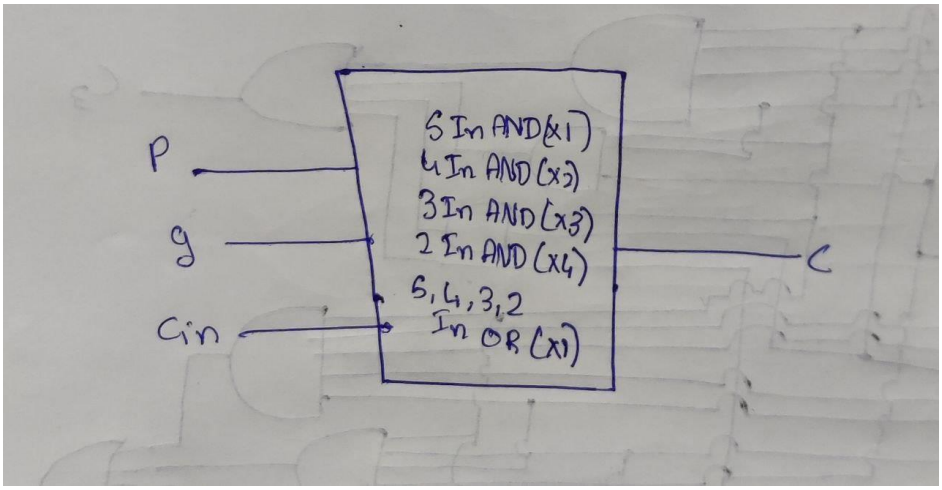
The topologies and basic structure of each block is given below,

1. Propagate and generate block



The block uses a total of four 2-input XOR gates to calculate the propagates and four 2-input AND gates to calculate the generates.

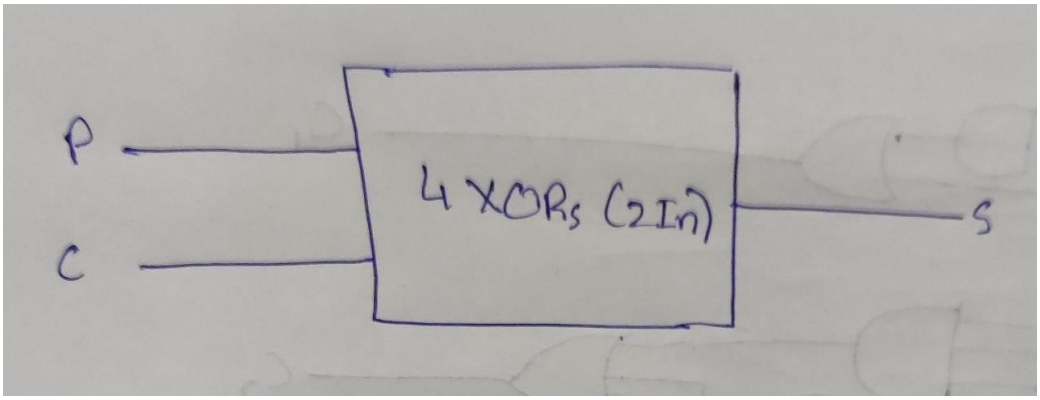
2. Carry lookahead block



The block requires a total of 14 unique gates namely,

- 1x 5-input AND gate
- 2x 4-input AND gates
- 3x 3-input AND gates
- 4x 2-input AND gates
- 1x 5-input OR gate
- 1x 4-input OR gate
- 1x 3-input OR gate
- 1x 2-input OR gate

3. Sum block



The block requires a total of four 2-input XOR gates.

For the CMOS layout, we use a λ value of 0.09 µm. and $V_{DD} = 1.8V$, with $\frac{W_P}{W_N} = \frac{20\lambda}{10\lambda}$.

Question 3

The netlist for all individual gates is given below.

1. 2-Input AND gate

```
* 2 Input AND gate
.subckt and2 OUT A B

* PUN
M1 nand A VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
```

```
9.
10.M2 VDD B nand VDD CMOSP W={width_P} L={LAMBDA} +
11.AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
12.AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
13.
14.* PDN
15.M3 node1 A GND Gnd CMOSN W={width_N} L={LAMBDA} +
16.AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
17.AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
18.
19.M4 nand B node1 Gnd CMOSN W={width_N} L={LAMBDA} +
20.AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
21.AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
22.
23.*Inverter
24.M5 OUT nand VDD VDD CMOSP W={width_P} L={LAMBDA} +
25.AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
26.AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
27.
28.M6 OUT nand GND Gnd CMOSN W={width_N} L={LAMBDA} +
29.AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
30.AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
31.
32..ends
```

2. 3-Input AND gate

```
* 3 Input AND gate
.subckt and3 OUT A B C

*PUN
M0 3nand A vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M1 3nand B vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M2 3nand C vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

*PDN
M3 3nand A node1 gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
```

```
M4 node1 B node2 gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M5 node2 C gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

*Inverter
M6 OUT 3nand VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M7 OUT 3nand GND Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.ends
```

3. 4-Input AND gate

```
* 4 Input AND gate
.subckt and4 OUT A B C D
*PUN
M0 4nand A vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M1 4nand B vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M2 4nand C vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3 4nand D vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

*PDN
M4 4nand A node1 gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M5 node1 B node2 gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
```

```
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M6 node2 C node3 gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M7 node3 D gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

*Inverter
M8 OUT 4nand VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M9 OUT 4nand GND Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.ends

```

4. 5-Input AND gate

```
* 5 Input AND gate
.subckt and5 OUT A B C D E

*PUN
M0 5nand A vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M1 5nand B vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M2 5nand C vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3 5nand D vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M4 5nand E vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

```

```
*PDN
M5 5nand A node1 gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M6 node1 B node2 gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M7 node2 C node3 gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M8 node3 D gnd node4 CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M9 node4 A gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

*Inverter
M10 OUT 5nand VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M11 OUT 5nand GND Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.ends

```

5. 2-Input OR gate

```
* 2 Input OR gate
.subckt or2 OUT A B

* PUN
M1 node1 A VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M2 NOR B node1 VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

* PDN
M3 NOR A GND Gnd CMOSN W={width_N} L={LAMBDA} +
```

```
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4 GND B NOR Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

* Inverter
M5 OUT NOR VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M6 OUT NOR GND GND CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.ends
```

6. 3-Input OR gate

```
* 3 Input OR gate
.subckt or3 OUT A B C

*PUN
M0 3nor A node1 vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M1 node1 B node2 vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M2 node2 C vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

*PDN
M3 3nor A gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4 3nor B gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
```

```
M5 3nor C gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

*Inverter
M6 OUT 3nor VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M7 OUT 3nor GND Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.ends
```

7. 4-Input OR gate

```
* 4 Input OR gate
.subckt or4 OUT A B C D

*PUN
M0 4nor A node1 vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M1 node1 B node2 vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M2 node2 C node3 vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3 node3 D vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

*PDN
M4 4nor A gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M5 4nor B gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M6 4nor C gnd gnd CMOSN W={width_N} L={LAMBDA} +
```

```
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M7 4nor D gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

*Inverter
M8 OUT 4nor VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M9 OUT 4nor GND Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.ends
```

8. 5-Input OR gate

```
* 5 Input OR gate
.subckt or5 OUT A B C D E

*PUN
M0 5nor A node1 vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M1 node1 B node2 vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M2 node2 C node3 vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3 node3 D node4 vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M4 node4 E vdd vdd CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

*PDN
M5 5nor A gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
```

```
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M6 5nor B gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M7 5nor C gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M8 5nor D gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M9 5nor E gnd gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}


*Inverter
M10 OUT 5nor VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M11 OUT 5nor GND Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.ends
```

9. 2-Input XOR gate

```
* 2 Input XOR gate
.subckt xor2 OUT A B


M1 Anot A VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M2 Anot A GND GND CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M3 Bnot B VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
```

```
M4 Bnot B GND GND CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M5 node1 A VDD VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M6 OUT Bnot node1 VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M7 VDD Anot node2 VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M8 node2 B OUT VDD CMOSP W={width_P} L={LAMBDA} +
AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M9 GND Anot node3 Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M10 node3 Bnot OUT Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M11 OUT B node4 Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M12 node4 A GND Gnd CMOSN W={width_N} L={LAMBDA} +
AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.ends
```

The netlists for the blocks are given below,

- Propagate and generate block

```
1. xxPROP0 p0 a0 b0 xor2
2. xxPROP1 p1 a1 b1 xor2
3. xxPROP2 p2 a2 b2 xor2
4. xxPROP3 p3 a3 b3 xor2
5.
```

```
xxGEN0 g0 a0 b0 and2
xxGEN1 g1 a1 b1 and2
xxGEN2 g2 a2 b2 and2
xxGEN3 g3 a3 b3 and2
```

- CLA block

```
xxANDcalc0 temp0 Cin p0 and2
xxORcalc0 c0 temp0 g0 or2

xxANDcalc11 temp11 Cin p0 p1 and3
xxANDcalc12 temp12 g0 p1 and2
xxORcalc1 c1 temp12 temp11 g1 or3

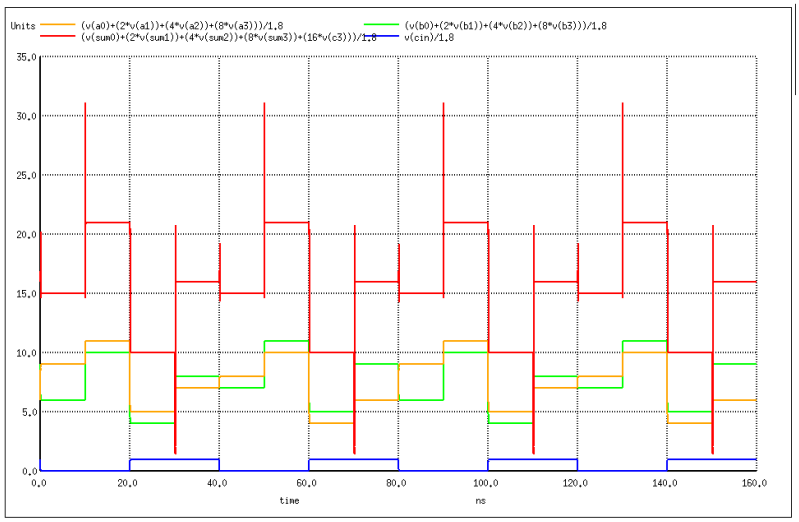
xxANDcalc21 temp21 Cin p0 p1 p2 and4
xxANDcalc22 temp22 g0 p1 p2 and3
xxANDcalc23 temp23 g1 p2 and2
xxORcalc2 c2 temp23 temp22 temp21 g2 or4

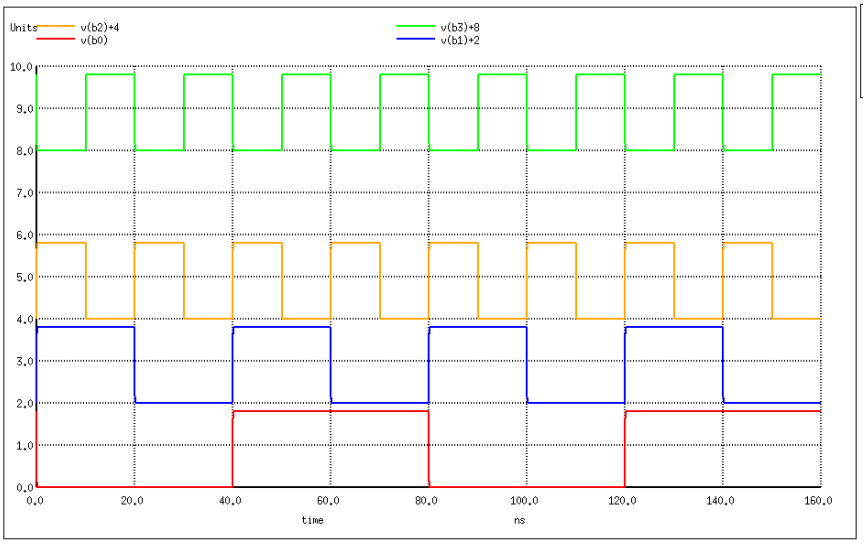
xxANDcalc31 temp31 Cin p0 p1 p2 p3 and5
xxANDcalc32 temp32 g0 p1 p2 p3 and4
xxANDcalc33 temp33 g1 p2 p3 and3
xxANDcalc34 temp34 g2 p3 and2
xxOR3 c3 temp34 temp33 temp32 temp31 g3 or5
```

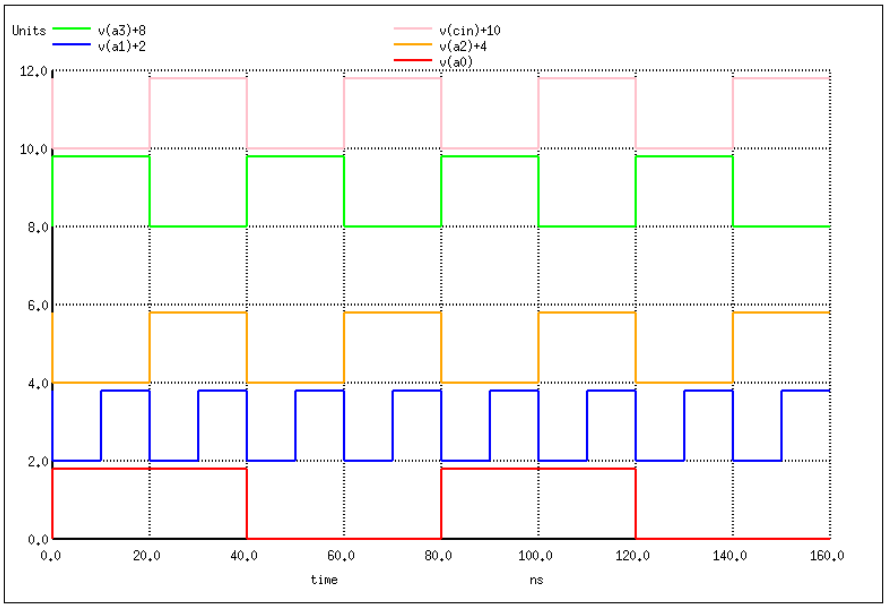
- Sum block

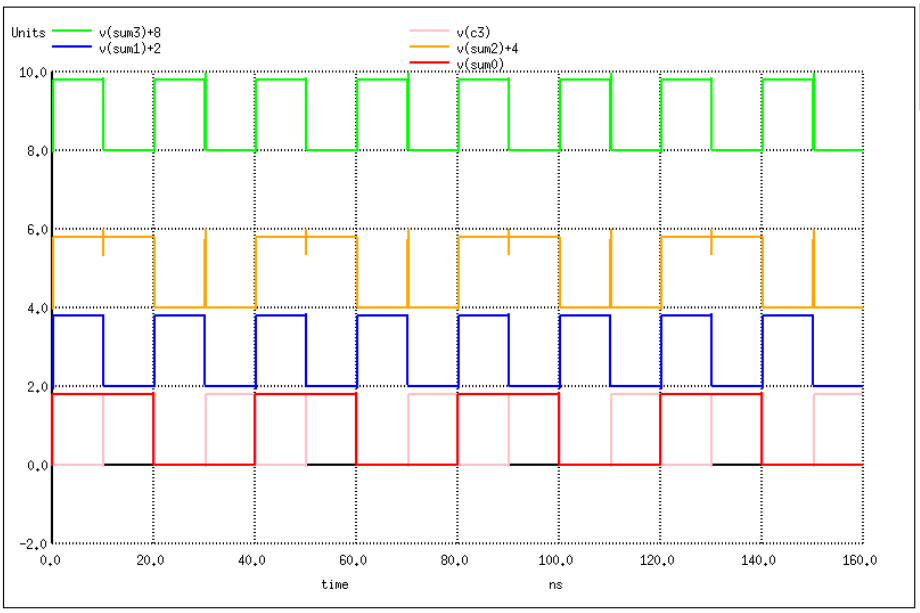
```
xxSUM0 sum0 p0 Cin xor2
xxSUM1 sum1 p1 c0 xor2
xxSUM2 sum2 p2 c1 xor2
xxSUM3 sum3 p3 c2 xor2
```

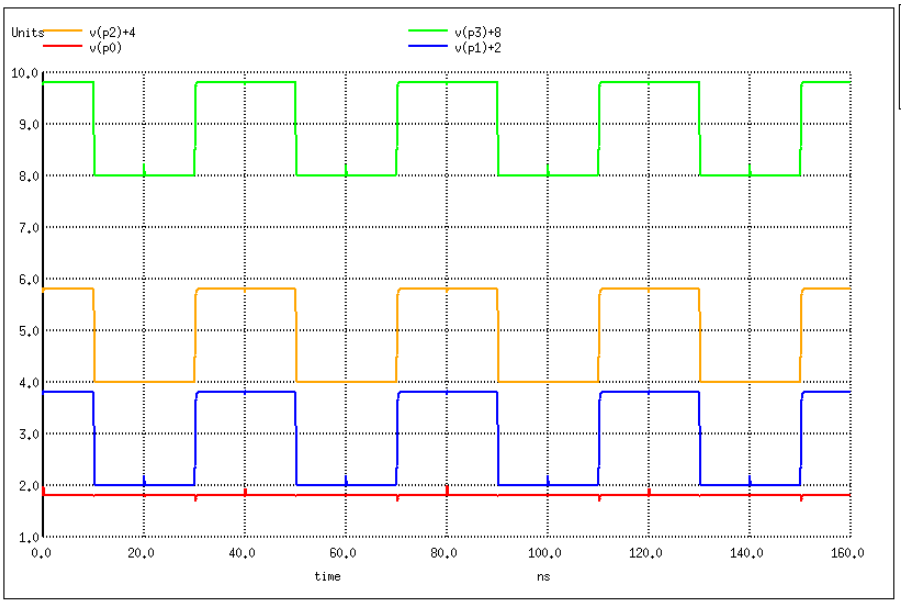
The outputs are given below,

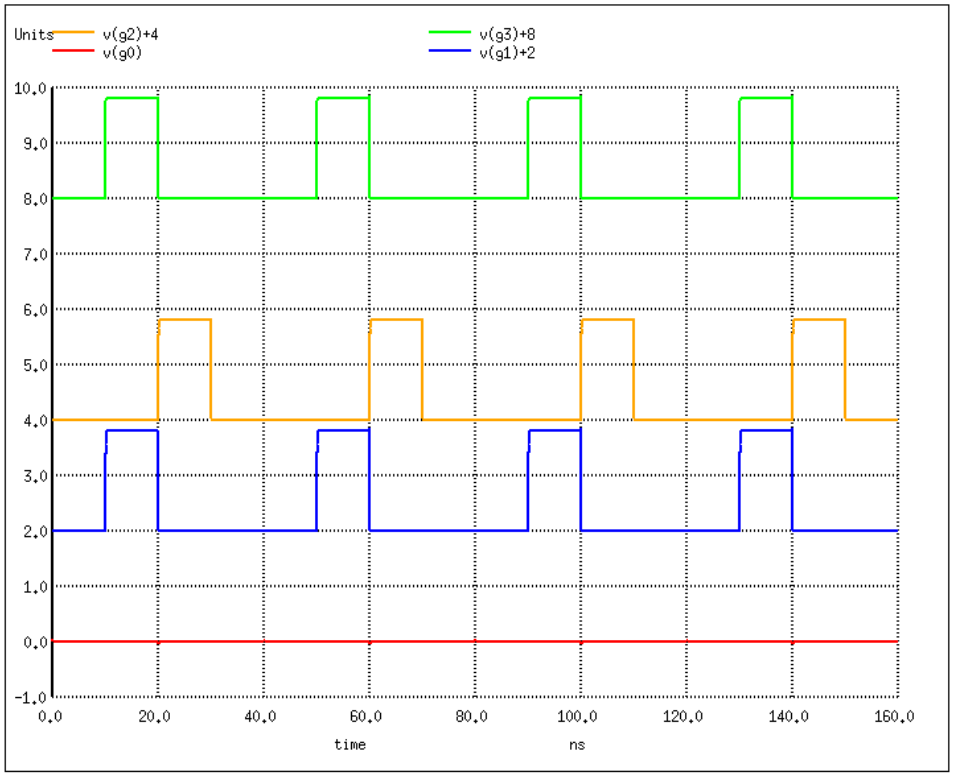


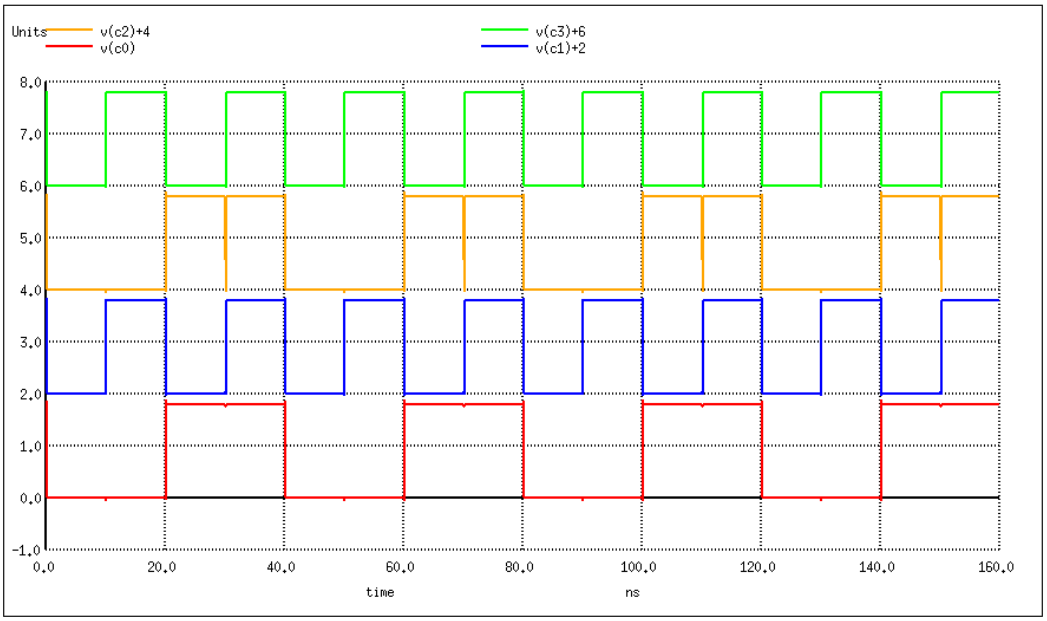

Units
v(b2)+4
v(b0)
v(b3)+8
v(b1)+2
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
ns


Units
v(a3)+8
v(a1)+2
v(cin)+10
v(a2)+4
v(a0)
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
ns


Units
v(sum3)+8
v(sum1)+2
v(c3)
v(sum2)+4
v(sum0)
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
ns

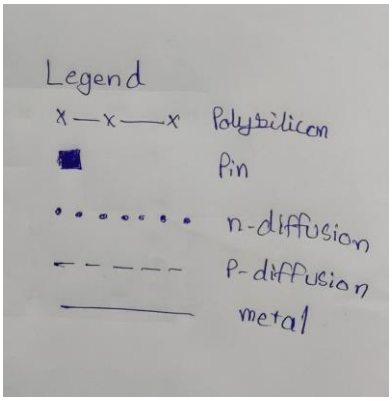

Units
v(p2)+4
v(p0)
v(p3)+8
v(p1)+2
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
ns


Units
v(g2)+4
v(g0)
v(g3)+8
v(g1)+2
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
ns

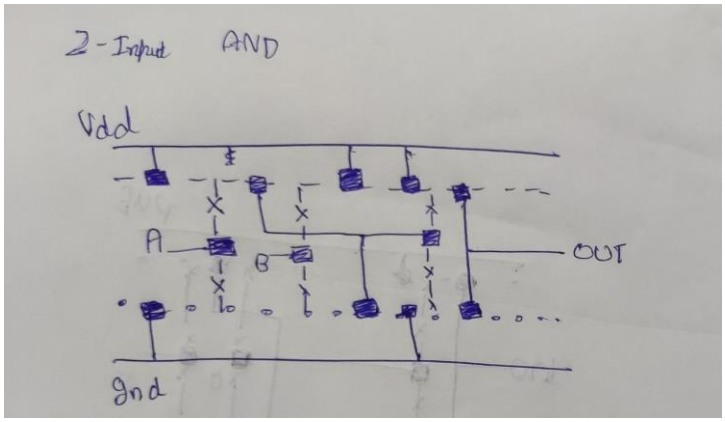

Units
v(c2)+4
v(c0)
v(c3)+6
v(c1)+2
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
ns

Question 4

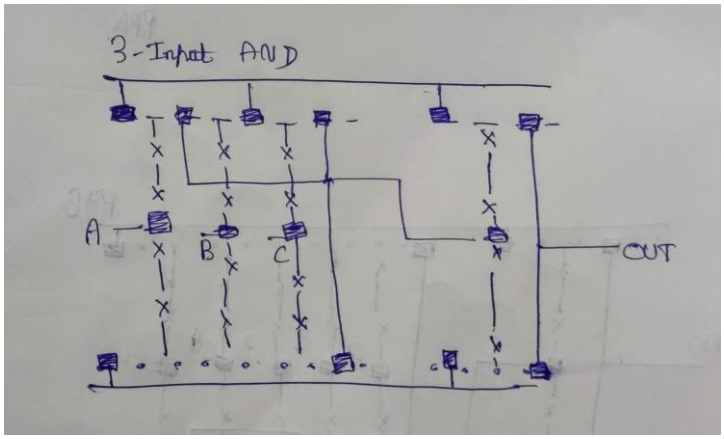
The magic layout of all unique gates used are given below along with the stick diagram legend,



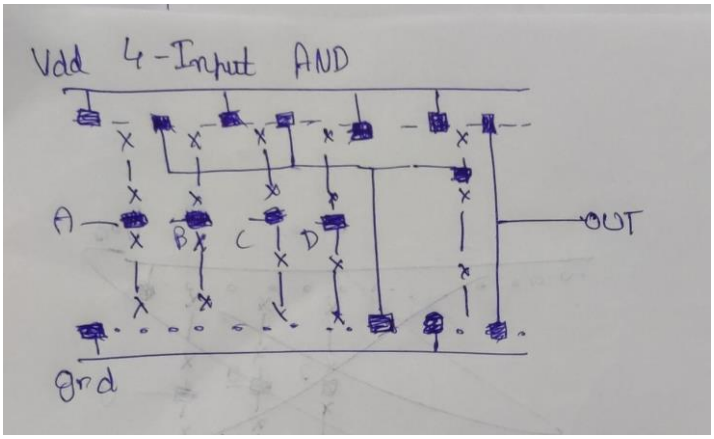
1. 2-Input AND gate



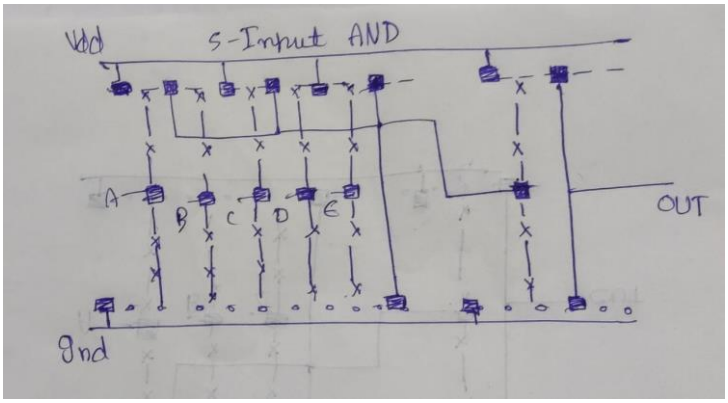
2. 3-Input AND gate



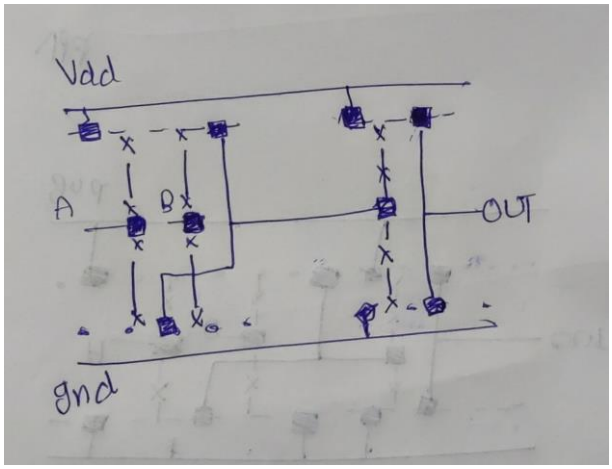
3. 4-Input AND gate



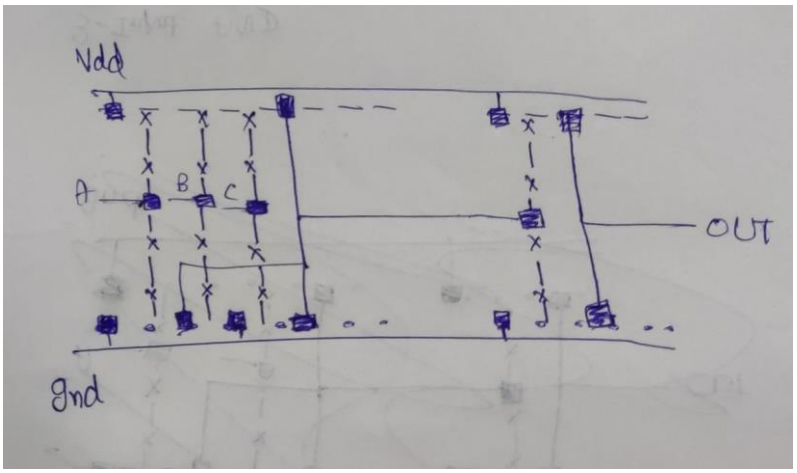
4. 5-Input AND gate



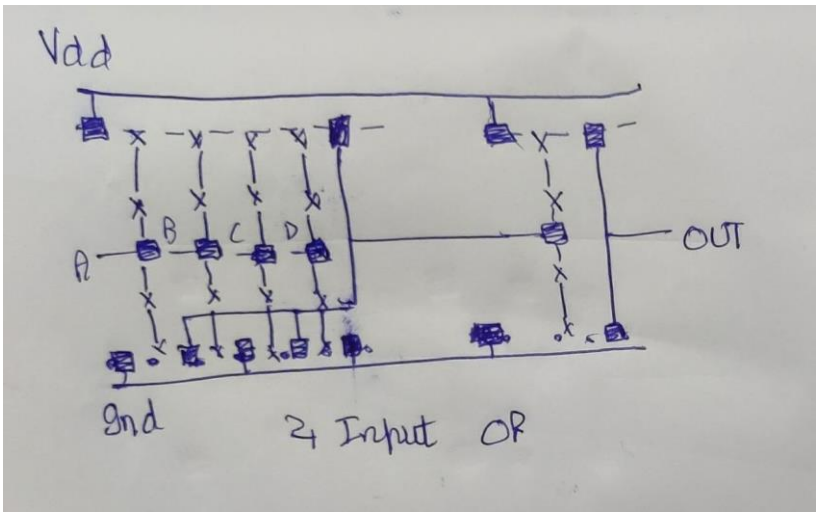
5. 2-Input OR gate



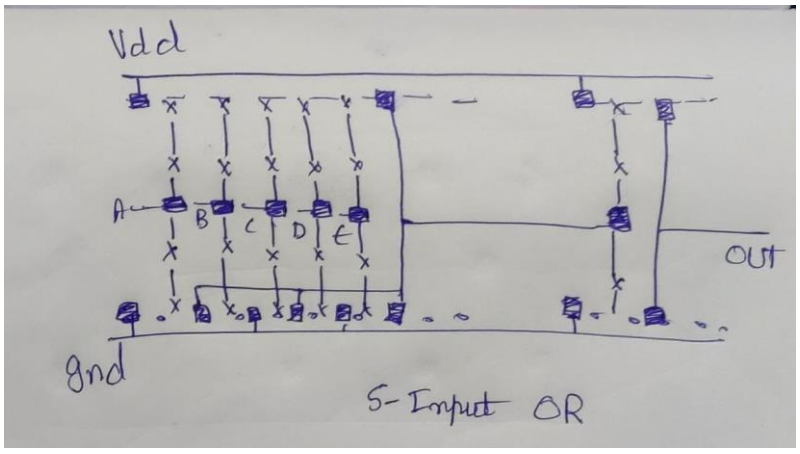
6. 3-Input OR gate



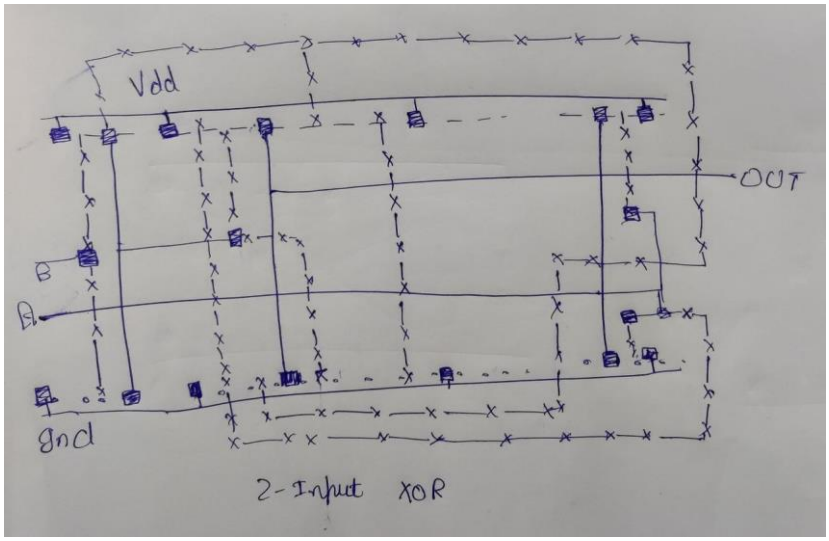
7. 4-Input OR gate



8. 5-Input OR gate

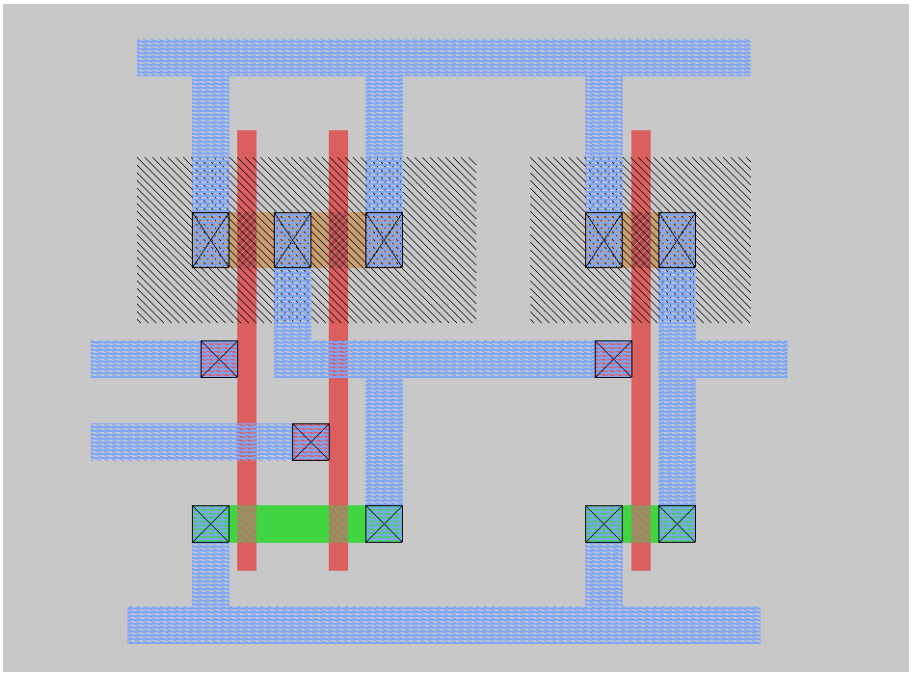


9. 2-Input XOR gate

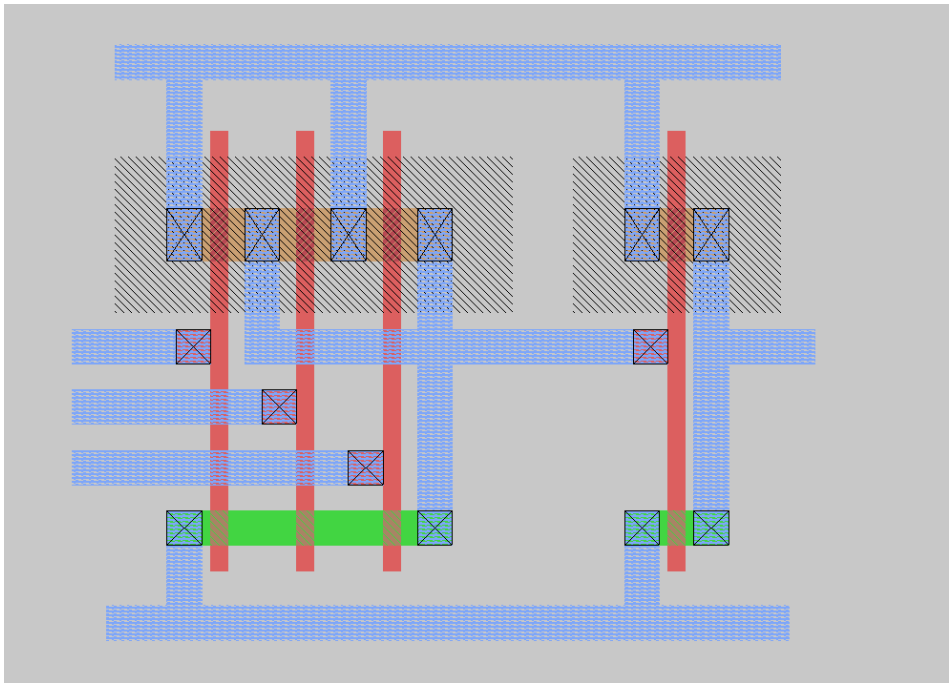


Question 5

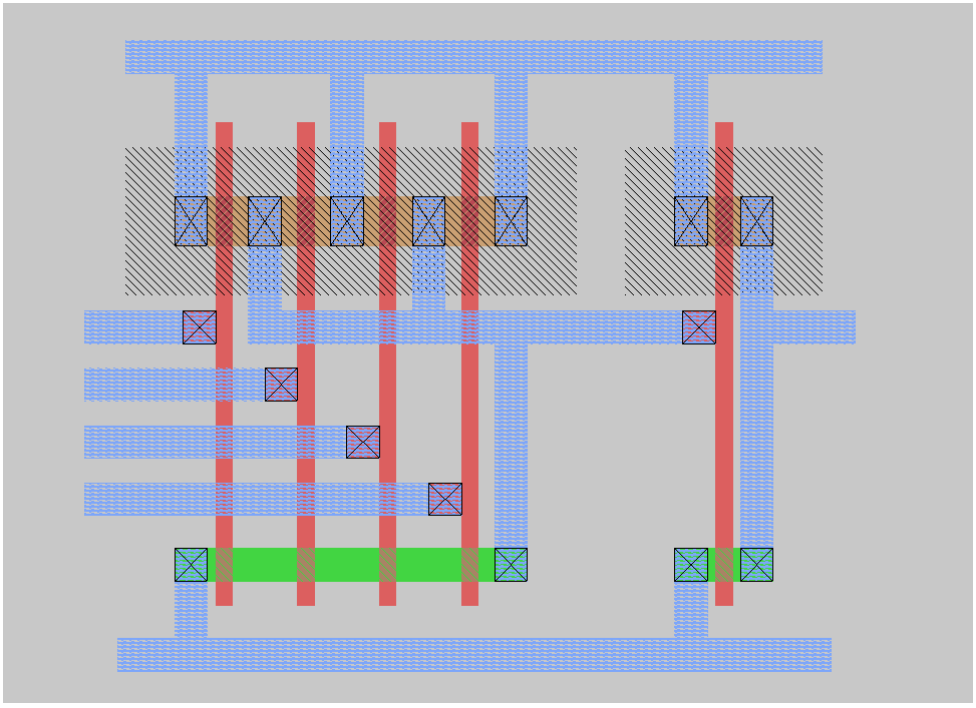
1. 2-Input AND gate



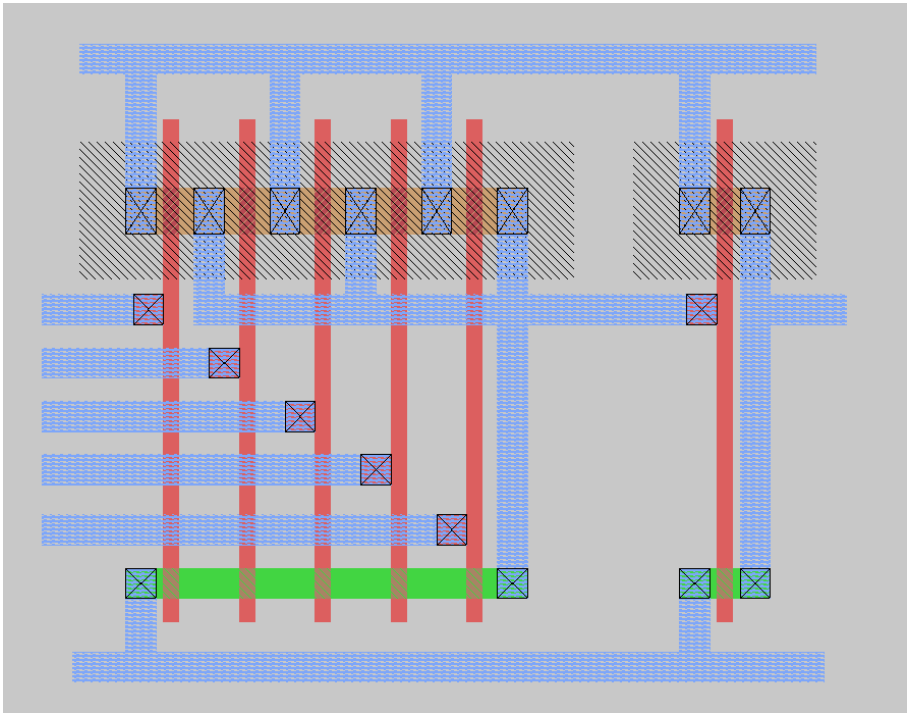
10. 3-Input AND gate



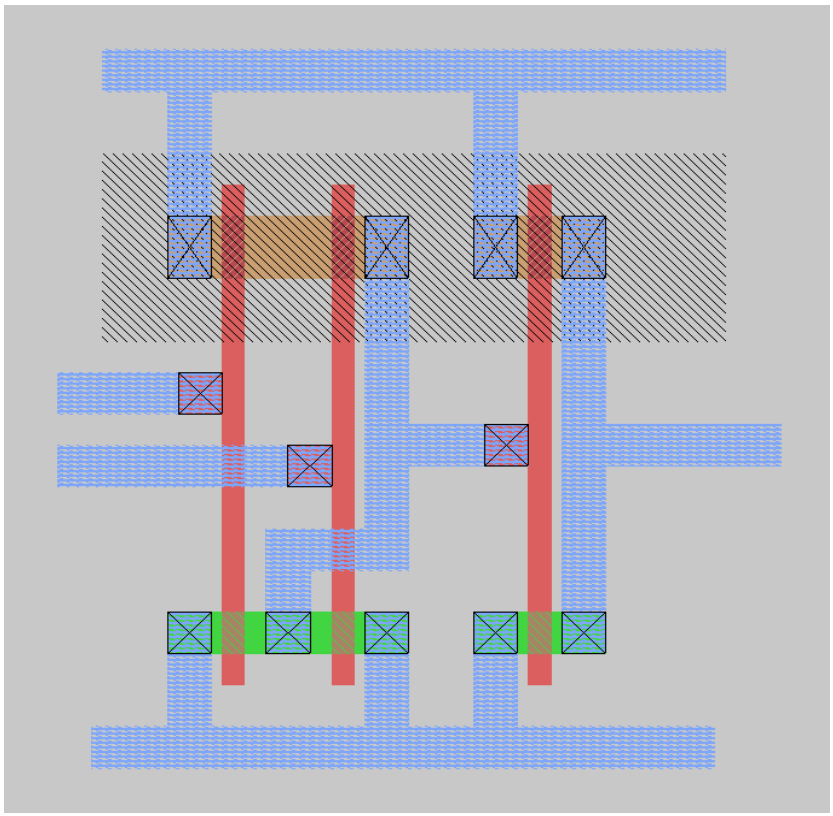
11. 4-Input AND gate



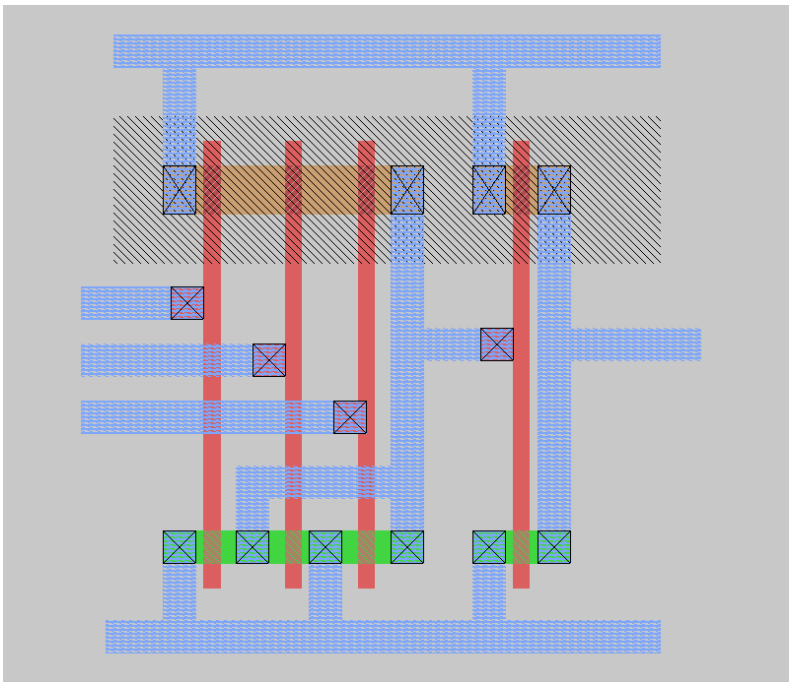
12. 5-Input AND gate



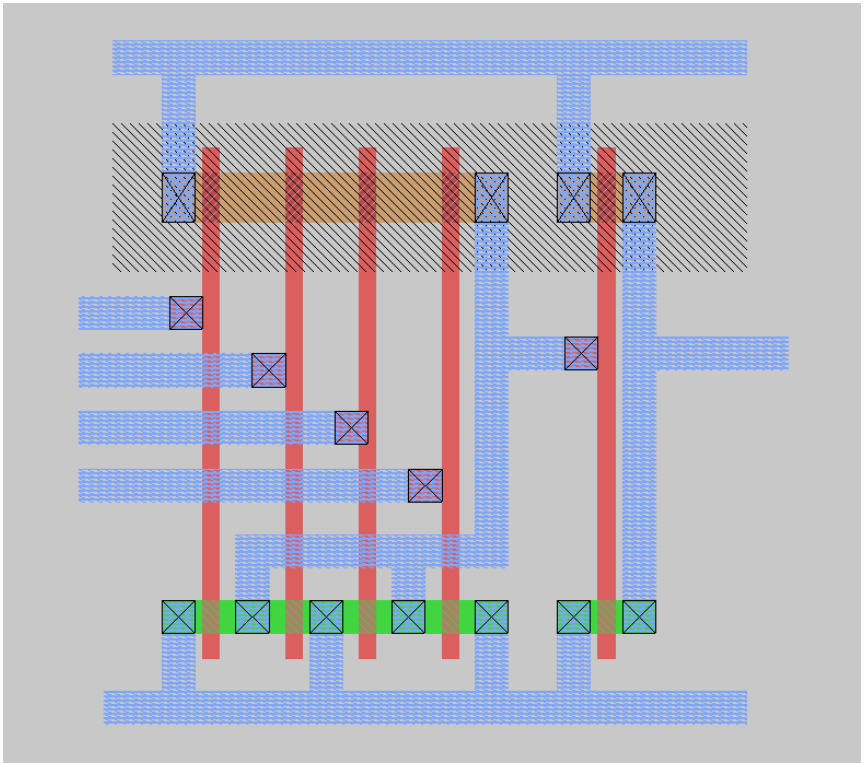
13. 2-Input OR gate



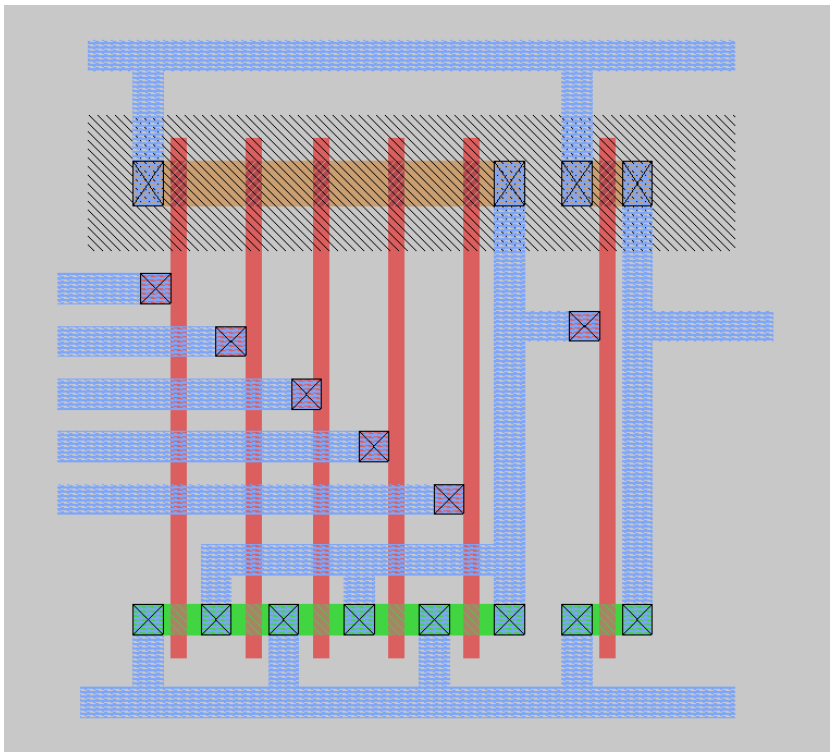
14. 3-Input OR gate



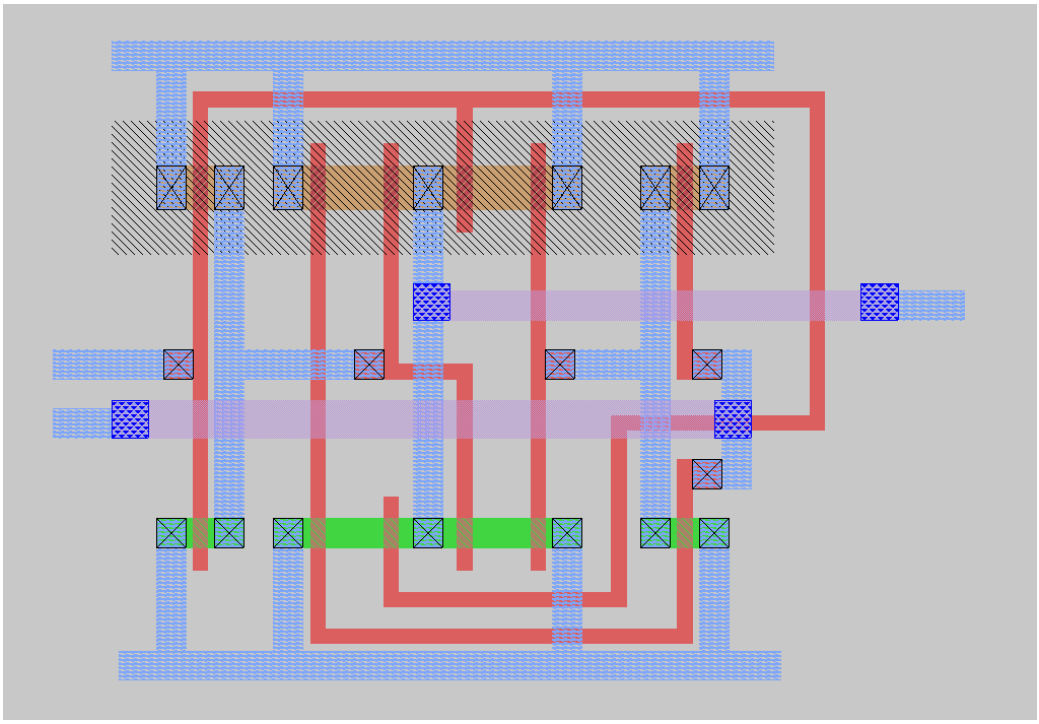
15. 4-Input OR gate



16. 5-Input OR gate

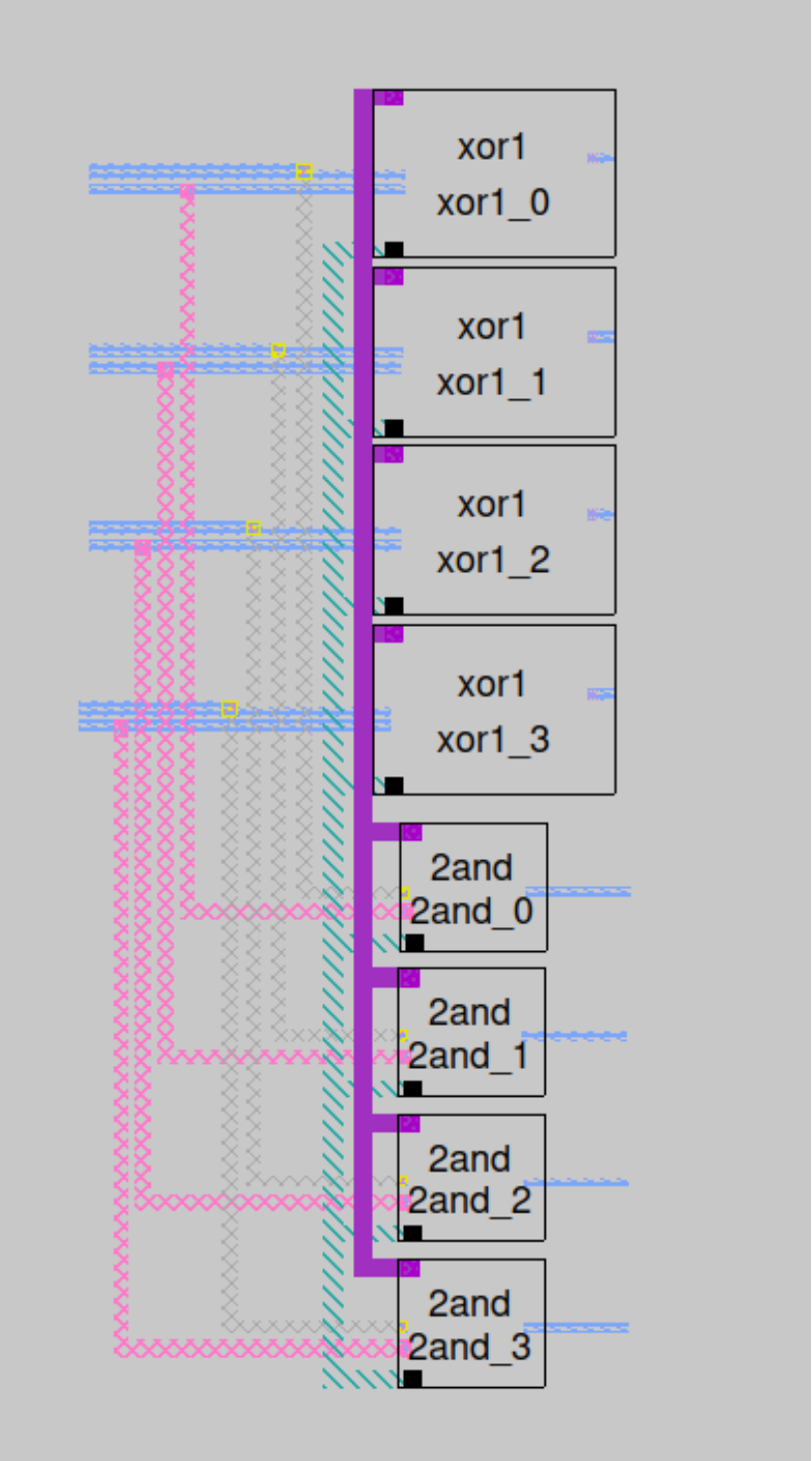


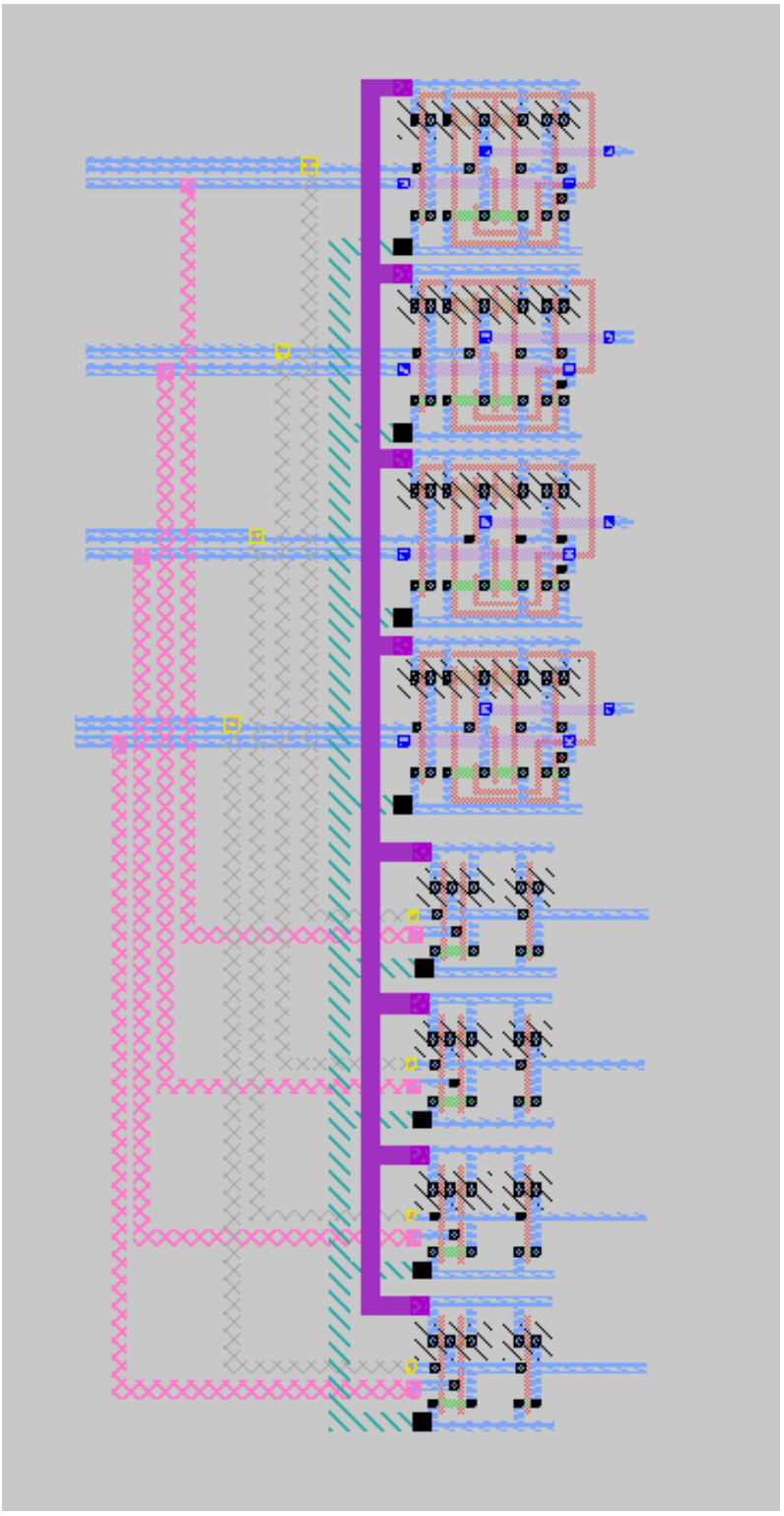
17. 2-Input XOR gate



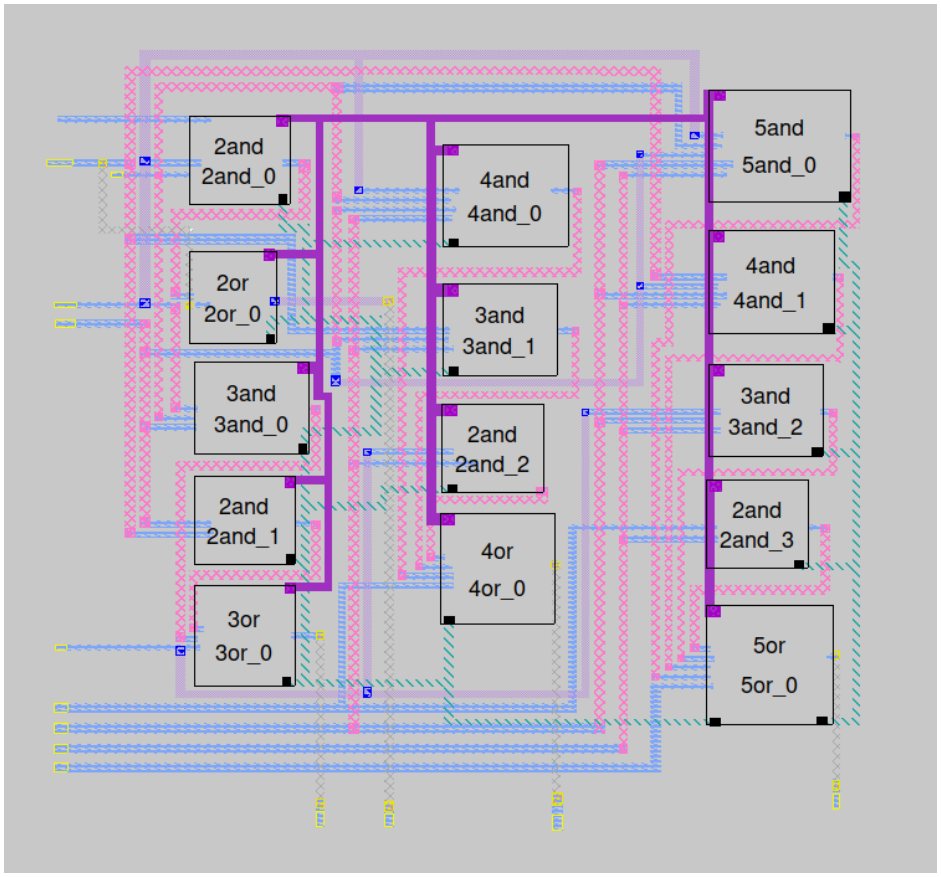
The magic layouts for the blocks are given below,

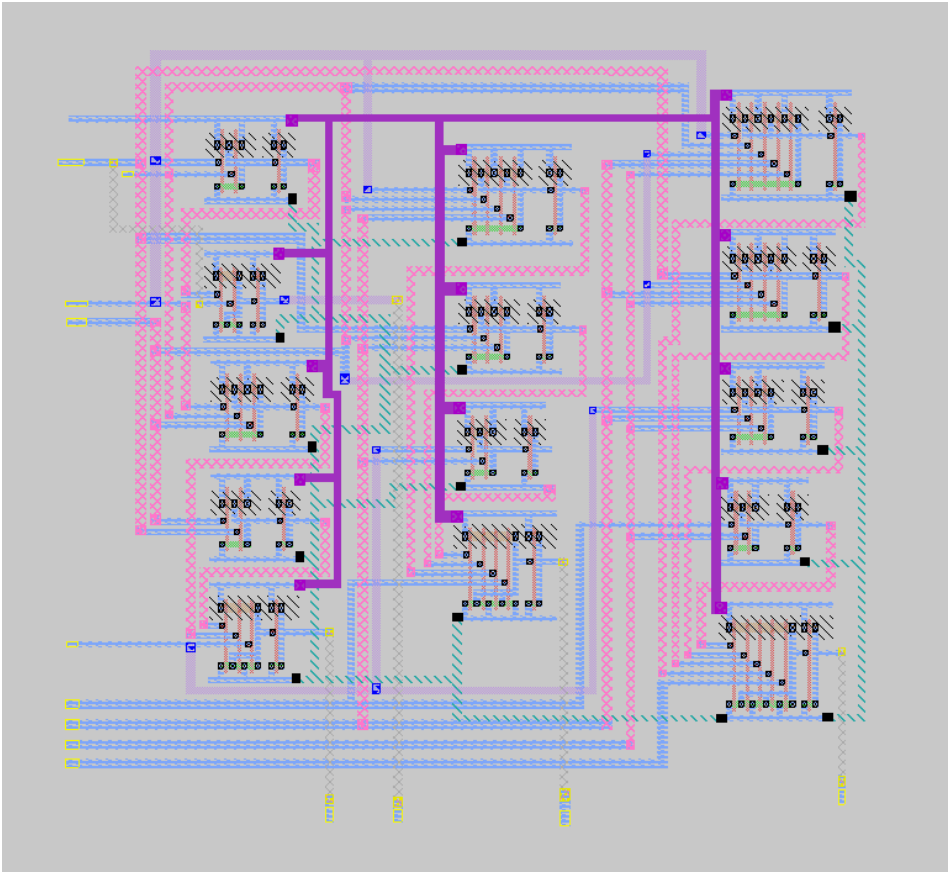
1. Propagate and generate block



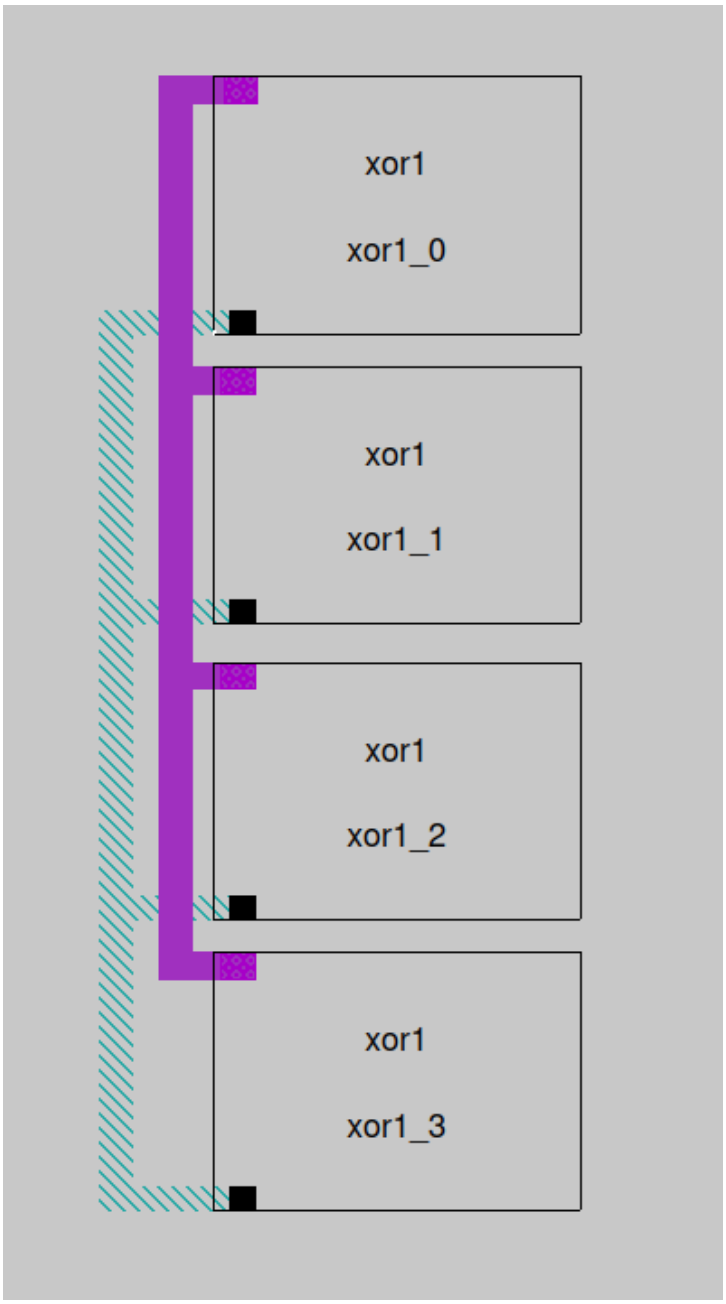


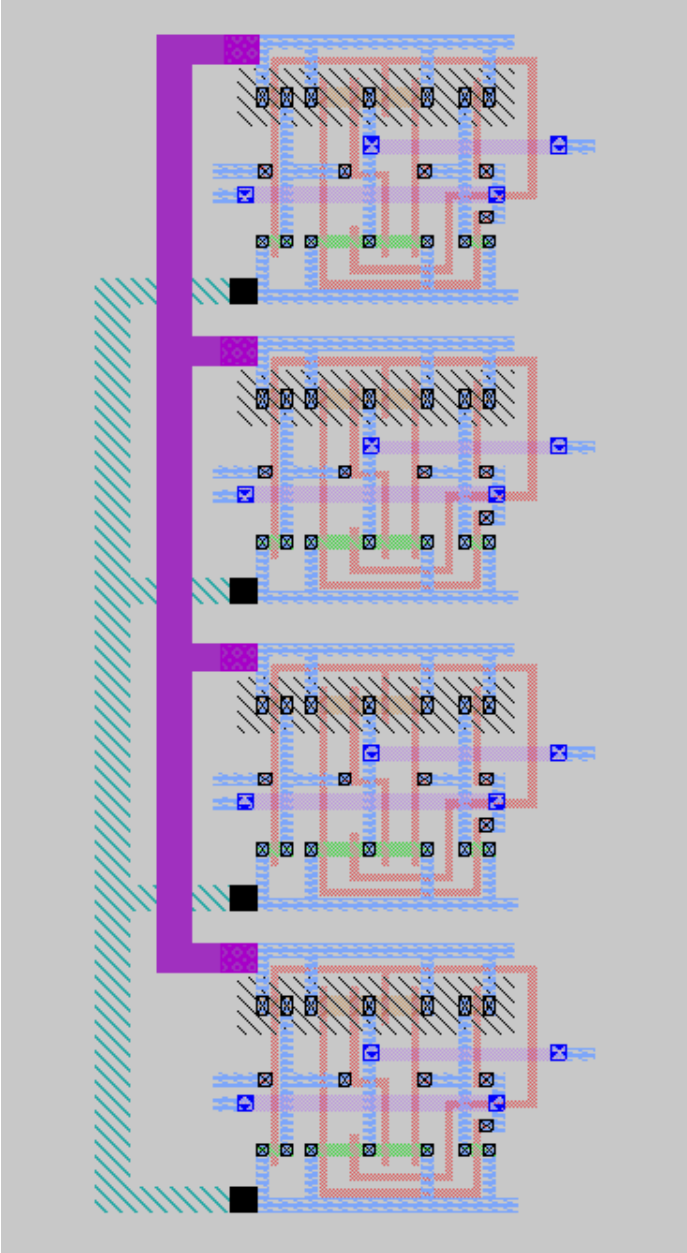
2. CLA block


2and
2and_0
2or
2or_0
3and
3and_0
2and
2and_1
3or
3or_0
4and
4and_0
3and
3and_1
2and
2and_2
4or
4or_0
5and
5and_0
4and
4and_1
3and
3and_2
2and
2and_3
5or
5or_0



3. Sum block





The magic layout extracted netlist for all three blocks are given below,

1. Propagate and generate block

```
* SPICE3 file created from test.ext - technology: scmos

.include TSMC_180nm.txt
.param SUPPLY = 1.8
.option scale=0.09u
.global gnd vdd

VDS vdd gnd 'SUPPLY'
```

```
vin1 a3 gnd 1.8
vin2 a2 gnd 0
vin3 a1 gnd 1.8
vin4 a0 gnd 1.8
vin5 b3 gnd 1.8
vin6 b2 gnd 0
vin7 b1 gnd 1.8
vin8 b0 gnd 0

M1000 Vdd b3 2and_0/a_13_5# Vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1001 g3 2and_0/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1002 2and_0/a_13_5# a3 Vdd Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1003 g3 2and_0/a_13_5# Vdd Vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1004 2and_0/a_13_5# b3 2and_0/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1005 2and_0/a_13_n25# a3 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0

M1006 Vdd b2 2and_1/a_13_5# Vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1007 g2 2and_1/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1008 2and_1/a_13_5# a2 Vdd Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1009 g2 2and_1/a_13_5# Vdd Vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1010 2and_1/a_13_5# b2 2and_1/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1011 2and_1/a_13_n25# a2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1012 Vdd b1 2and_2/a_13_5# Vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1013 g1 2and_2/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1014 2and_2/a_13_5# a1 Vdd Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1015 g1 2and_2/a_13_5# Vdd Vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1016 2and_2/a_13_5# b1 2and_2/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1017 2and_2/a_13_n25# a1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
```

```
M1018 Vdd b0 2and_3/a_13_5# Vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1019 g0 2and_3/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1020 2and_3/a_13_5# a0 Vdd Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1021 g0 2and_3/a_13_5# Vdd Vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1022 2and_3/a_13_5# b0 2and_3/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1023 2and_3/a_13_n25# a0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1024 xor1_0/a_24_2# a3 p3 Vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1025 vdd b3 xor1_0/a_32_n47# Vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1026 gnd b3 xor1_0/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1027 p3 xor1_0/a_n12_n44# xor1_0/a_4_2# Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
M1028 xor1_0/a_n12_n44# a3 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1029 gnd xor1_0/a_32_n47# xor1_0/a_24_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1030 xor1_0/a_4_2# b3 vdd Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1031 xor1_0/a_24_n44# xor1_0/a_n12_n44# p3 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1032 vdd xor1_0/a_32_n47# xor1_0/a_24_2# Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1033 p3 a3 xor1_0/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1034 xor1_0/a_4_n44# b3 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1035 xor1_0/a_n12_n44# a3 vdd Vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0

M1036 xor1_1/a_24_2# a2 p2 Vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1037 vdd b2 xor1_1/a_32_n47# Vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1038 gnd b2 xor1_1/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1039 p2 xor1_1/a_n12_n44# xor1_1/a_4_2# Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
M1040 xor1_1/a_n12_n44# a2 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
```

```
M1041 gnd xor1_1/a_32_n47# xor1_1/a_24_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1042 xor1_1/a_4_2# b2 vdd Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1043 xor1_1/a_24_n44# xor1_1/a_n12_n44# p2 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1044 vdd xor1_1/a_32_n47# xor1_1/a_24_2# Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1045 p2 a2 xor1_1/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1046 xor1_1/a_4_n44# b2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1047 xor1_1/a_n12_n44# a2 vdd Vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1048 xor1_2/a_24_2# a1 p1 Vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1049 vdd b1 xor1_2/a_32_n47# Vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1050 gnd b1 xor1_2/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1051 p1 xor1_2/a_n12_n44# xor1_2/a_4_2# Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
M1052 xor1_2/a_n12_n44# a1 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1053 gnd xor1_2/a_32_n47# xor1_2/a_24_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1054 xor1_2/a_4_2# b1 vdd Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1055 xor1_2/a_24_n44# xor1_2/a_n12_n44# p1 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1056 vdd xor1_2/a_32_n47# xor1_2/a_24_2# Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1057 p1 a1 xor1_2/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1058 xor1_2/a_4_n44# b1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1059 xor1_2/a_n12_n44# a1 vdd Vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1060 xor1_3/a_24_2# a0 p0 Vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1061 vdd b0 xor1_3/a_32_n47# Vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1062 gnd b0 xor1_3/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1063 p0 xor1_3/a_n12_n44# xor1_3/a_4_2# Vdd CMOSP w=6 l=2
```

```
+  ad=0 pd=0 as=48 ps=28
M1064 xor1_3/a_n12_n44# a0 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1065 gnd xor1_3/a_32_n47# xor1_3/a_24_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1066 xor1_3/a_4_2# b0 vdd Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1067 xor1_3/a_24_n44# xor1_3/a_n12_n44# p0 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1068 vdd xor1_3/a_32_n47# xor1_3/a_24_2# Vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1069 p0 a0 xor1_3/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1070 xor1_3/a_4_n44# b0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1071 xor1_3/a_n12_n44# a0 vdd Vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


C0 b2 b0 0.08fF
C1 b3 xor1_0/a_32_n47# 0.28fF
C2 b3 gnd 0.15fF
C3 gnd a1 0.08fF
C4 a2 vdd 0.04fF
C5 b2 vdd 0.15fF
C6 xor1_0/a_32_n47# gnd 0.04fF
C7 gnd g3 0.06fF
C8 gnd xor1_2/a_n12_n44# 0.08fF
C9 Vdd vdd 0.05fF
C10 b0 2and_3/a_13_5# 0.17fF
C11 Vdd a2 0.14fF
C12 g0 Vdd 0.06fF
C13 gnd 2and_3/a_13_5# 0.02fF
C14 2and_0/a_13_5# Vdd 0.09fF
C15 a0 gnd 0.01fF
C16 b0 xor1_3/a_32_n47# 0.28fF
C17 g1 gnd 0.06fF
C18 Vdd vdd 0.12fF
C19 Vdd vdd 0.05fF
C20 xor1_2/a_n12_n44# a1 0.08fF
C21 a2 2and_1/a_13_5# 0.04fF
C22 b3 b0 0.08fF
C23 b0 vdd 0.01fF
C24 gnd gnd 0.04fF
C25 Vdd a3 0.08fF
C26 a3 vdd 0.02fF
C27 b3 vdd 0.15fF
C28 gnd gnd 0.33fF
C29 b2 gnd 0.17fF
```

```
C30 vdd Vdd 0.12fF
C31 xor1_3/a_n12_n44# gnd 0.08fF
C32 gnd gnd 0.04fF
C33 a0 gnd 0.01fF
C34 Vdd a0 0.08fF
C35 vdd xor1_2/a_32_n47# 0.06fF
C36 a2 p2 0.01fF
C37 Vdd p0 0.02fF
C38 Vdd Vdd 0.06fF
C39 g2 2and_1/a_13_5# 0.05fF
C40 b2 b1 0.60fF
C41 b0 gnd 0.01fF
C42 a3 vdd 0.23fF
C43 vdd vdd 0.05fF
C44 b3 gnd 0.11fF
C45 a3 vdd 0.04fF
C46 vdd gnd 0.15fF
C47 b2 vdd 0.13fF
C48 b0 a0 2.76fF
C49 gnd gnd 0.04fF
C50 2and_3/a_13_5# Vdd 0.09fF
C51 gnd vdd 0.76fF
C52 Vdd b2 0.13fF
C53 a0 vdd 0.05fF
C54 Vdd b0 0.08fF
C55 b3 2and_1/a_13_5# 0.17fF
C56 g0 Vdd 0.03fF
C57 b3 b1 0.08fF
C58 xor1_3/a_32_n47# vdd 0.06fF
C59 gnd 2and_1/a_13_5# 0.02fF
C60 b0 b0 0.12fF
C61 b1 vdd 0.01fF
C62 gnd gnd 0.05fF
C63 gnd gnd 0.05fF
C64 b0 gnd 0.01fF
C65 vdd b0 0.01fF
C66 b3 vdd 0.13fF
C67 gnd gnd 0.15fF
C68 vdd vdd 0.09fF
C69 gnd vdd 0.37fF
C70 a2 Vdd 0.08fF
C71 xor1_1/a_n12_n44# vdd 0.12fF
C72 vdd a1 0.23fF
C73 b2 a1 0.10fF
C74 Vdd Vdd 0.03fF
C75 vdd xor1_2/a_n12_n44# 0.12fF
C76 a0 gnd 0.05fF
C77 Vdd 2and_3/a_13_5# 0.02fF
```

```
C78 b2 p2 0.10fF
C79 b1 gnd 0.01fF
C80 Vdd 2and_0/a_13_5# 0.02fF
C81 a0 xor1_3/a_n12_n44# 0.08fF
C82 b0 vdd 0.01fF
C83 gnd b0 0.12fF
C84 xor1_0/a_n12_n44# vdd 0.12fF
C85 b1 a0 0.10fF
C86 gnd gnd 0.15fF
C87 gnd vdd 0.09fF
C88 b3 b3 0.07fF
C89 g3 Vdd 0.03fF
C90 b3 Vdd 0.08fF
C91 xor1_1/a_32_n47# vdd 0.06fF
C92 b3 a1 0.10fF
C93 a1 vdd 0.01fF
C94 Vdd xor1_1/a_n12_n44# 0.09fF
C95 a2 b2 2.69fF
C96 xor1_3/a_32_n47# Vdd 0.09fF
C97 a0 vdd 0.23fF
C98 a0 vdd 0.04fF
C99 Vdd Vdd 0.06fF
C100 Vdd 2and_3/a_13_5# 0.08fF
C101 a2 gnd 0.08fF
C102 b1 b0 0.60fF
C103 gnd 2and_0/a_13_5# 0.02fF
C104 b1 2and_2/a_13_5# 0.17fF
C105 Vdd p3 0.02fF
C106 xor1_3/a_32_n47# p0 0.10fF
C107 b1 gnd 0.02fF
C108 Vdd a3 0.14fF
C109 Vdd Vdd 0.06fF
C110 b0 gnd 0.06fF
C111 b3 Vdd 0.08fF
C112 xor1_0/a_32_n47# vdd 0.06fF
C113 p1 Vdd 0.02fF
C114 gnd b3 0.03fF
C115 vdd gnd 0.15fF
C116 gnd vdd 0.09fF
C117 Vdd b1 0.08fF
C118 g2 Vdd 0.06fF
C119 b3 a2 0.10fF
C120 b0 xor1_3/a_n12_n44# 0.20fF
C121 g3 2and_0/a_13_5# 0.05fF
C122 p1 xor1_2/a_32_n47# 0.10fF
C123 a2 vdd 0.01fF
C124 a1 gnd 0.01fF
C125 Vdd xor1_1/a_32_n47# 0.09fF
```

```
C126 b1 p1 0.10fF
C127 b1 b1 0.07fF
C128 b0 b1 0.08fF
C129 Vdd Vdd 0.03fF
C130 xor1_1/a_n12_n44# p2 0.12fF
C131 b0 b0 0.08fF
C132 b1 vdd 0.15fF
C133 Vdd b3 0.13fF
C134 a0 vdd 0.02fF
C135 g2 Vdd 0.03fF
C136 b0 vdd 0.05fF
C137 a3 p3 0.01fF
C138 Vdd a0 0.14fF
C139 Vdd 2and_2/a_13_5# 0.02fF
C140 a2 gnd 0.05fF
C141 a1 gnd 0.05fF
C142 g3 Vdd 0.06fF
C143 a2 xor1_1/a_n12_n44# 0.08fF
C144 vdd gnd 0.76fF
C145 a0 p0 0.01fF
C146 a1 gnd 0.02fF
C147 b2 gnd 0.12fF
C148 xor1_1/a_32_n47# p2 0.10fF
C149 2and_2/a_13_5# Vdd 0.09fF
C150 xor1_3/a_32_n47# gnd 0.04fF
C151 b1 gnd 0.17fF
C152 2and_0/a_13_5# a3 0.04fF
C153 Vdd xor1_0/a_n12_n44# 0.09fF
C154 xor1_2/a_32_n47# Vdd 0.09fF
C155 b1 Vdd 0.13fF
C156 b3 p3 0.10fF
C157 p1 a1 0.01fF
C158 a3 b3 2.71fF
C159 gnd vdd 1.29fF
C160 vdd vdd 0.05fF
C161 b3 a3 0.24fF
C162 a3 vdd 0.05fF
C163 Vdd Vdd 0.06fF
C164 Vdd 2and_2/a_13_5# 0.08fF
C165 a1 b1 0.23fF
C166 b3 b2 0.77fF
C167 b1 xor1_2/a_32_n47# 0.28fF
C168 xor1_2/a_n12_n44# p1 0.12fF
C169 b2 vdd 0.01fF
C170 Vdd vdd 0.12fF
C171 a2 xor1_1/a_32_n47# 0.10fF
C172 a3 gnd 0.08fF
C173 xor1_3/a_n12_n44# vdd 0.12fF
```

```
C174 b0 Vdd 0.13fF
C175 b3 a2 0.23fF
C176 2and_2/a_13_5# g1 0.05fF
C177 b1 gnd 0.03fF
C178 b1 vdd 0.13fF
C179 Vdd xor1_0/a_32_n47# 0.09fF
C180 b0 p0 0.10fF
C181 gnd gnd 0.05fF
C182 b3 b2 0.07fF
C183 Vdd vdd 0.05fF
C184 xor1_0/a_n12_n44# p3 0.12fF
C185 gnd gnd 0.04fF
C186 vdd vdd 0.05fF
C187 vdd vdd 0.05fF
C188 a2 gnd 0.02fF
C189 a3 xor1_0/a_n12_n44# 0.08fF
C190 b3 vdd 0.03fF
C191 a1 2and_2/a_13_5# 0.04fF
C192 Vdd Vdd 0.03fF
C193 2and_1/a_13_5# Vdd 0.02fF
C194 b2 gnd 0.02fF
C195 a1 gnd 0.05fF
C196 b2 xor1_1/a_n12_n44# 0.20fF
C197 b3 gnd 0.12fF
C198 a0 gnd 0.08fF
C199 2and_0/a_13_5# Vdd 0.08fF
C200 a0 b0 0.23fF
C201 gnd xor1_2/a_32_n47# 0.04fF
C202 xor1_1/a_n12_n44# gnd 0.08fF
C203 Vdd a1 0.14fF
C204 g0 gnd 0.06fF
C205 Vdd g1 0.06fF
C206 gnd b1 0.12fF
C207 g2 gnd 0.06fF
C208 b2 a0 0.10fF
C209 2and_2/a_13_5# gnd 0.02fF
C210 xor1_2/a_n12_n44# Vdd 0.09fF
C211 Vdd a1 0.08fF
C212 xor1_2/a_32_n47# a1 0.10fF
C213 gnd gnd 0.05fF
C214 gnd vdd 0.88fF
C215 b1 a1 2.69fF
C216 xor1_0/a_32_n47# p3 0.10fF
C217 a3 xor1_0/a_32_n47# 0.10fF
C218 b3 xor1_0/a_n12_n44# 0.23fF
C219 Vdd xor1_3/a_n12_n44# 0.09fF
C220 b3 gnd 0.15fF
C221 b1 xor1_2/a_n12_n44# 0.20fF
```

```
C222 Vdd g1 0.03fF
C223 xor1_3/a_32_n47# a0 0.10fF
C224 vdd gnd 0.35fF
C225 a2 gnd 0.05fF
C226 b2 gnd 0.15fF
C227 a1 vdd 0.04fF
C228 Vdd 2and_1/a_13_5# 0.09fF
C229 b2 xor1_1/a_32_n47# 0.28fF
C230 a2 vdd 0.23fF
C231 xor1_0/a_n12_n44# gnd 0.08fF
C232 xor1_3/a_n12_n44# p0 0.12fF
C233 a0 2and_3/a_13_5# 0.04fF
C234 gnd b3 0.03fF
C235 gnd b0 0.03fF
C236 g0 2and_3/a_13_5# 0.05fF
C237 Vdd Vdd 0.03fF
C238 xor1_1/a_32_n47# gnd 0.04fF
C239 b3 a0 0.10fF
C240 a0 vdd 0.01fF
C241 Vdd p2 0.02fF
C242 Vdd vdd 0.12fF
C243 b0 gnd 0.12fF
C244 Vdd vdd 0.05fF
C245 b3 2and_0/a_13_5# 0.17fF
C246 2and_1/a_13_5# Vdd 0.08fF
C247 vdd Gnd 0.78fF
C248 vdd Gnd 0.01fF
C249 gnd Gnd 0.01fF
C250 vdd Gnd 0.03fF
C251 b0 Gnd 0.83fF
C252 gnd Gnd 0.41fF
C253 p0 Gnd 0.81fF
C254 vdd Gnd 0.41fF
C255 xor1_3/a_32_n47# Gnd 0.42fF
C256 xor1_3/a_n12_n44# Gnd 0.50fF
C257 b0 Gnd 2.07fF
C258 a0 Gnd 2.06fF
C259 Vdd Gnd 1.63fF
C260 gnd Gnd 0.52fF
C261 p1 Gnd 0.81fF
C262 vdd Gnd 0.41fF
C263 xor1_2/a_32_n47# Gnd 0.42fF
C264 xor1_2/a_n12_n44# Gnd 0.50fF
C265 b1 Gnd 2.84fF
C266 a1 Gnd 2.05fF
C267 Vdd Gnd 1.63fF
C268 gnd Gnd 0.49fF
C269 p2 Gnd 0.81fF
```

```
C270 vdd Gnd 0.41fF
C271 xor1_1/a_32_n47# Gnd 0.42fF
C272 xor1_1/a_n12_n44# Gnd 0.50fF
C273 b2 Gnd 2.83fF
C274 a2 Gnd 2.05fF
C275 Vdd Gnd 1.63fF
C276 gnd Gnd 0.54fF
C277 p3 Gnd 0.81fF
C278 vdd Gnd 0.41fF
C279 xor1_0/a_32_n47# Gnd 0.42fF
C280 xor1_0/a_n12_n44# Gnd 0.50fF
C281 b3 Gnd 2.83fF
C282 a3 Gnd 2.05fF
C283 Vdd Gnd 1.63fF
C284 gnd Gnd 0.34fF
C285 g0 Gnd 0.29fF
C286 Vdd Gnd 0.36fF
C287 2and_3/a_13_5# Gnd 0.37fF
C288 b0 Gnd 0.32fF
C289 a0 Gnd 0.28fF
C290 Vdd Gnd 0.43fF
C291 Vdd Gnd 0.67fF
C292 gnd Gnd 0.34fF
C293 g1 Gnd 0.07fF
C294 Vdd Gnd 0.36fF
C295 2and_2/a_13_5# Gnd 0.37fF
C296 b1 Gnd 0.32fF
C297 a1 Gnd 0.28fF
C298 Vdd Gnd 0.43fF
C299 Vdd Gnd 0.67fF
C300 gnd Gnd 0.34fF
C301 g2 Gnd 0.29fF
C302 Vdd Gnd 0.27fF
C303 2and_1/a_13_5# Gnd 0.37fF
C304 b3 Gnd 0.32fF
C305 a2 Gnd 0.28fF
C306 Vdd Gnd 0.43fF
C307 Vdd Gnd 0.67fF
C308 gnd Gnd 0.34fF
C309 g3 Gnd 0.29fF
C310 Vdd Gnd 0.36fF
C311 2and_0/a_13_5# Gnd 0.37fF
C312 b3 Gnd 0.32fF
C313 a3 Gnd 0.28fF
C314 Vdd Gnd 0.43fF
C315 Vdd Gnd 0.67fF

.tran 0.05n 10n
```

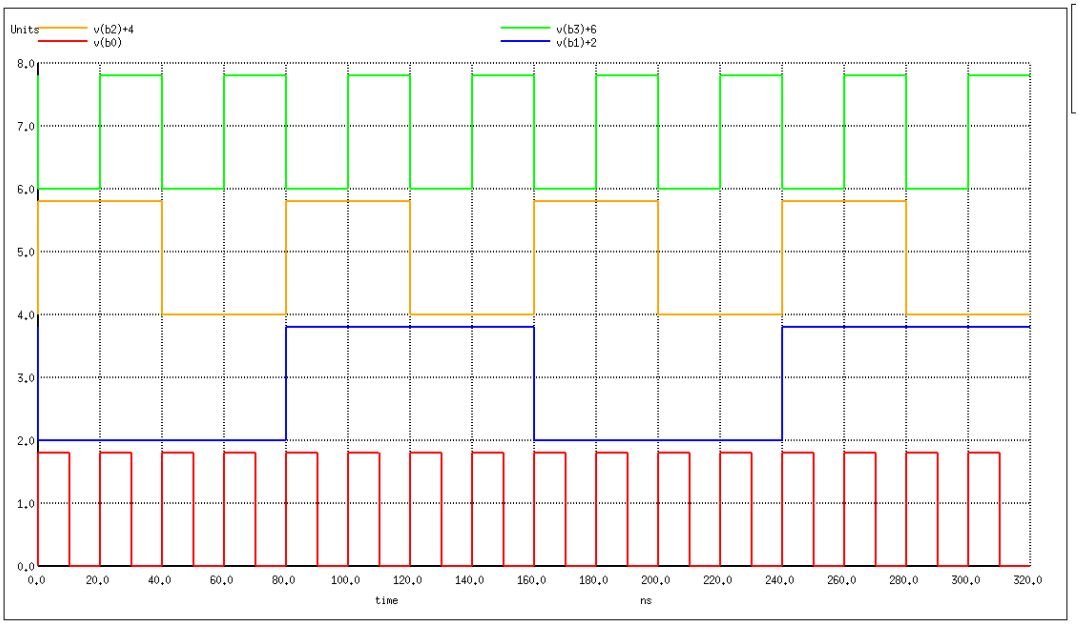
```
.control
run

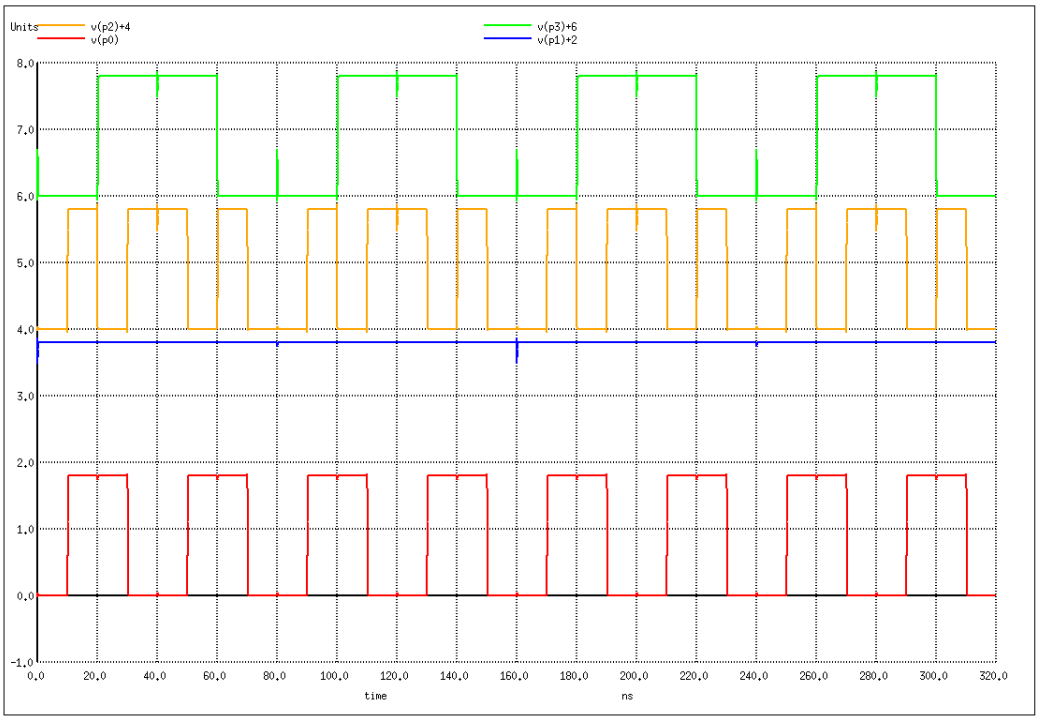
set color0 = white
set color1 = black

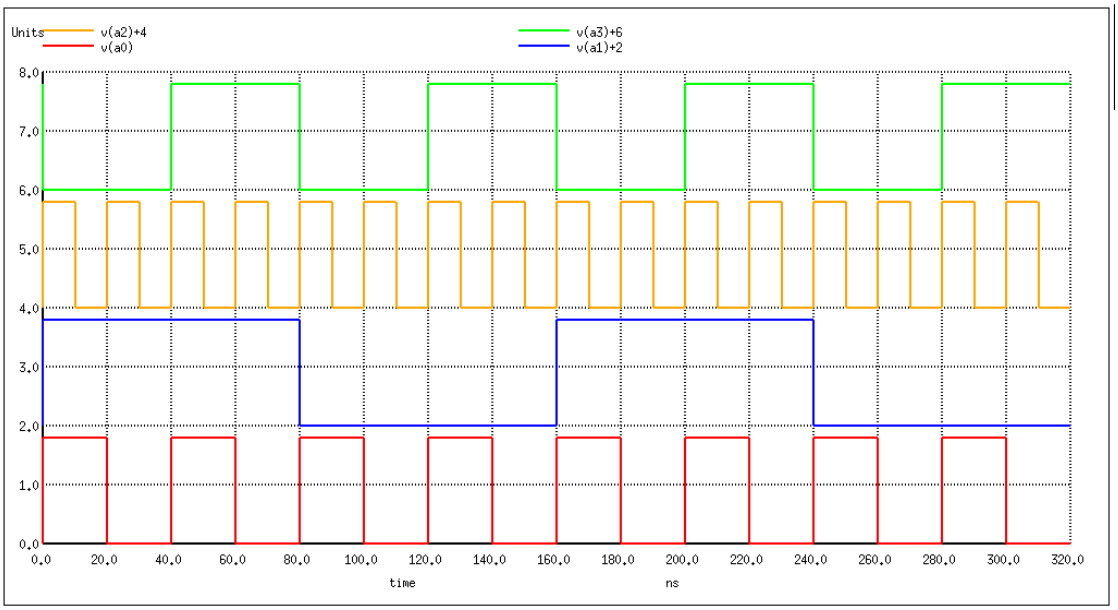
plot v(p0) v(p1)+2 v(p2)+4 v(p3)+6 v(g0)+8 v(g1)+10 v(g2)+12 v(g3)+14

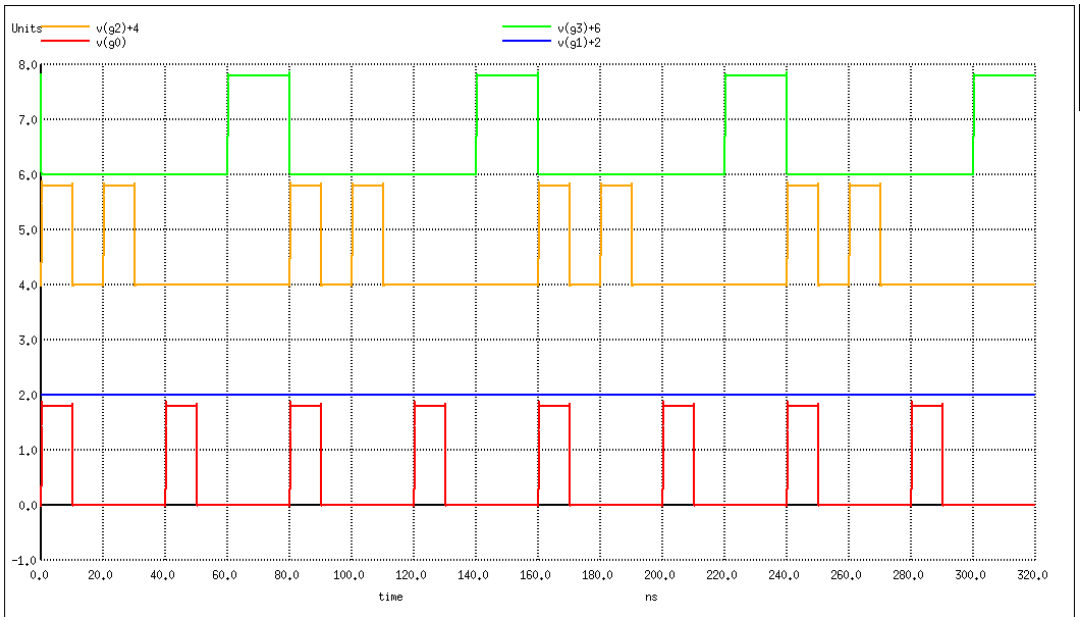

.endc
```

The outputs are given below,




Units
v(p2)+4
v(p0)
v(p3)+6
v(p1)+2
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0
320.0
time
ns


Units
v(a2)+4
v(a0)
v(a3)+6
v(a1)+2
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0
320.0
time
ns



2. CLA block

```
* SPICE3 file created from cla.ext - technology: scmos

.option scale=0.09u

M1000 3and_0/a_13_5# m1_n38_n151# m1_80_n107# 3and_0/w_0_n1# pfet w=6 l=2
+  ad=84 pd=52 as=108 ps=72
M1001 3and_0/a_13_n28# m1_n15_n136# m1_81_n168# Gnd nfet w=4 l=2
+  ad=32 pd=24 as=40 ps=36
M1002 m1_89_n136# 3and_0/a_13_5# m1_81_n168# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1003 m1_80_n107# m1_n27_n143# 3and_0/a_13_5# 3and_0/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 m1_89_n136# 3and_0/a_13_5# m1_80_n107# 3and_0/w_53_n1# pfet w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1005 3and_0/a_13_5# m1_n15_n136# m1_80_n107# 3and_0/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1006 3and_0/a_13_5# m1_n38_n151# 3and_0/a_23_n28# Gnd nfet w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1007 3and_0/a_23_n28# m1_n27_n143# 3and_0/a_13_n28# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1008 4or_0/a_0_n37# m1_156_n262# m1_191_n296# Gnd nfet w=4 l=2
+  ad=64 pd=48 as=92 ps=78
M1009 4or_0/a_0_n37# m1_178_n248# m1_191_n296# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1010 m1_271_n254# 4or_0/a_0_n37# m1_191_n296# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1011 4or_0/a_19_13# m1_156_n262# 4or_0/a_10_13# 4or_0/w_n13_7# pfet w=6 l=2
```

```
+  ad=48 pd=28 as=42 ps=26
M1012 m1_191_n296# m1_169_n255# 4or_0/a_0_n37# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1013 m1_271_n254# 4or_0/a_0_n37# m1_190_n221# 4or_0/w_n13_7# pfet w=6 l=2
+  ad=30 pd=22 as=60 ps=44
M1014 4or_0/a_0_13# m1_178_n248# m1_190_n221# 4or_0/w_n13_7# pfet w=6 l=2
+  ad=48 pd=28 as=0 ps=0
M1015 4or_0/a_0_n37# g2 4or_0/a_19_13# 4or_0/w_n13_7# pfet w=6 l=2
+  ad=36 pd=24 as=0 ps=0
M1016 4or_0/a_10_13# m1_169_n255# 4or_0/a_0_13# 4or_0/w_n13_7# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1017 m1_191_n296# g2 4or_0/a_0_n37# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1018 3and_1/a_13_5# m1_119_n93# m1_193_n48# 3and_1/w_0_n1# pfet w=6 l=2
+  ad=84 pd=52 as=108 ps=72
M1019 3and_1/a_13_n28# m1_n49_n10# m1_194_n109# Gnd nfet w=4 l=2
+  ad=32 pd=24 as=40 ps=36
M1020 m1_276_n77# 3and_1/a_13_5# m1_194_n109# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1021 m1_193_n48# m1_n38_n95# 3and_1/a_13_5# 3and_1/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1022 m1_276_n77# 3and_1/a_13_5# m1_193_n48# 3and_1/w_53_n1# pfet w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1023 3and_1/a_13_5# m1_n49_n10# m1_193_n48# 3and_1/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1024 3and_1/a_13_5# m1_119_n93# 3and_1/a_23_n28# Gnd nfet w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1025 3and_1/a_23_n28# m1_n38_n95# 3and_1/a_13_n28# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1026 3and_2/a_13_5# m1_322_n153# m1_393_n109# 3and_2/w_0_n1# pfet w=6 l=2
+  ad=84 pd=52 as=108 ps=72
M1027 3and_2/a_13_n28# g1 m1_467_n170# Gnd nfet w=4 l=2
+  ad=32 pd=24 as=40 ps=36
M1028 m1_474_n138# 3and_2/a_13_5# m1_467_n170# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1029 m1_393_n109# m1_304_n147# 3and_2/a_13_5# 3and_2/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1030 m1_474_n138# 3and_2/a_13_5# m1_393_n109# 3and_2/w_53_n1# pfet w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1031 3and_2/a_13_5# g1 m1_393_n109# 3and_2/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1032 3and_2/a_13_5# m1_322_n153# 3and_2/a_23_n28# Gnd nfet w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1033 3and_2/a_23_n28# m1_304_n147# 3and_2/a_13_n28# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1034 m1_65_79# p0 2and_0/a_13_5# 2and_0/w_0_n1# pfet w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1035 m1_69_49# 2and_0/a_13_5# 2and_0/a_6_n25# Gnd nfet w=4 l=2
```

```
+  ad=20 pd=18 as=40 ps=36
M1036 2and_0/a_13_5# c_in m1_65_79# 2and_0/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1037 m1_69_49# 2and_0/a_13_5# m1_65_79# 2and_0/w_43_n1# pfet w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1038 2and_0/a_13_5# p0 2and_0/a_13_n25# Gnd nfet w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1039 2and_0/a_13_n25# c_in 2and_0/a_6_n25# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1040 m1_71_n193# m1_n49_n231# 2and_1/a_13_5# 2and_1/w_0_n1# pfet w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1041 m1_79_n222# 2and_1/a_13_5# m1_72_n251# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1042 2and_1/a_13_5# m1_n38_n223# m1_71_n193# 2and_1/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1043 m1_79_n222# 2and_1/a_13_5# m1_71_n193# 2and_1/w_43_n1# pfet w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1044 2and_1/a_13_5# m1_n49_n231# 2and_1/a_13_n25# Gnd nfet w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1045 2and_1/a_13_n25# m1_n38_n223# m1_72_n251# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1046 m1_192_n139# m1_119_n177# 2and_2/a_13_5# 2and_2/w_0_n1# pfet w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1047 2and_2/a_56_n25# 2and_2/a_13_5# m1_260_n199# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1048 2and_2/a_13_5# g1 m1_192_n139# 2and_2/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1049 2and_2/a_56_n25# 2and_2/a_13_5# m1_192_n139# 2and_2/w_43_n1# pfet w=6
l=2
+  ad=30 pd=22 as=0 ps=0
M1050 2and_2/a_13_5# m1_119_n177# 2and_2/a_13_n25# Gnd nfet w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1051 2and_2/a_13_n25# g1 m1_260_n199# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1052 m1_391_n196# m1_322_n235# 2and_3/a_13_5# 2and_3/w_0_n1# pfet w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1053 m1_464_n225# 2and_3/a_13_5# m1_454_n254# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1054 2and_3/a_13_5# g2 m1_391_n196# 2and_3/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1055 m1_464_n225# 2and_3/a_13_5# m1_391_n196# 2and_3/w_43_n1# pfet w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1056 2and_3/a_13_5# m1_322_n235# 2and_3/a_13_n25# Gnd nfet w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1057 2and_3/a_13_n25# g2 m1_454_n254# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1058 m1_478_n322# 5or_0/a_0_n44# m1_390_n290# 5or_0/w_n13_7# pfet w=6 l=2
+  ad=30 pd=22 as=60 ps=44
```

```
M1059 m1_471_n372# m1_347_n338# 5or_0/a_0_n44# Gnd nfet w=4 l=2
+  ad=100 pd=82 as=88 ps=68
M1060 m1_478_n322# 5or_0/a_0_n44# m1_471_n372# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1061 5or_0/a_0_n44# m1_357_n331# m1_471_n372# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1062 5or_0/a_0_n44# m1_376_n317# m1_471_n372# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1063 5or_0/a_19_13# m1_357_n331# 5or_0/a_10_13# 5or_0/w_n13_7# pfet w=6 l=2
+  ad=48 pd=28 as=42 ps=26
M1064 5or_0/a_0_13# m1_376_n317# m1_390_n290# 5or_0/w_n13_7# pfet w=6 l=2
+  ad=48 pd=28 as=0 ps=0
M1065 5or_0/a_29_13# m1_347_n338# 5or_0/a_19_13# 5or_0/w_n13_7# pfet w=6 l=2
+  ad=48 pd=28 as=0 ps=0
M1066 m1_471_n372# m1_366_n324# 5or_0/a_0_n44# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1067 5or_0/a_10_13# m1_366_n324# 5or_0/a_0_13# 5or_0/w_n13_7# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1068 5or_0/a_0_n44# g3 5or_0/a_29_13# 5or_0/w_n13_7# pfet w=6 l=2
+  ad=36 pd=24 as=0 ps=0
M1069 5or_0/a_0_n44# g3 m1_471_n372# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1070 m1_60_n56# 2or_0/a_0_n30# m1_55_n22# 2or_0/w_n13_0# pfet w=6 l=2
+  ad=30 pd=22 as=60 ps=44
M1071 m1_57_n85# m1_4_n58# 2or_0/a_0_n30# Gnd nfet w=4 l=2
+  ad=60 pd=54 as=32 ps=24
M1072 2or_0/a_0_n30# m1_4_n58# 2or_0/a_0_6# 2or_0/w_n13_0# pfet w=6 l=2
+  ad=30 pd=22 as=48 ps=28
M1073 m1_60_n56# 2or_0/a_0_n30# m1_57_n85# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1074 2or_0/a_0_6# m1_n15_n51# m1_55_n22# 2or_0/w_n13_0# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1075 2or_0/a_0_n30# m1_n15_n51# m1_57_n85# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1076 m1_492_69# 5and_0/a_13_5# m1_394_98# 5and_0/w_73_n1# pfet w=6 l=2
+  ad=30 pd=22 as=156 ps=100
M1077 5and_0/a_13_5# m1_n38_n95# m1_394_98# 5and_0/w_0_n1# pfet w=6 l=2
+  ad=132 pd=80 as=0 ps=0
M1078 5and_0/a_43_n43# m1_304_46# 5and_0/a_33_n43# Gnd nfet w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1079 5and_0/a_33_n43# m1_n38_n95# 5and_0/a_23_n43# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1080 m1_394_98# m1_106_104# 5and_0/a_13_5# 5and_0/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1081 5and_0/a_23_n43# m1_106_104# 5and_0/a_13_n43# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1082 m1_492_69# 5and_0/a_13_5# m1_488_22# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=40 ps=36
```

```
M1083 5and_0/a_13_n43# c_in m1_488_22# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1084 5and_0/a_13_5# m1_322_39# m1_394_98# 5and_0/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1085 5and_0/a_13_5# c_in m1_394_98# 5and_0/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1086 m1_394_98# m1_304_46# 5and_0/a_13_5# 5and_0/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1087 5and_0/a_13_5# m1_322_39# 5and_0/a_43_n43# Gnd nfet w=4 l=2
+  ad=24 pd=20 as=0 ps=0
M1088 m1_76_n307# 3or_0/a_0_n30# m1_71_n273# 3or_0/w_n13_7# pfet w=6 l=2
+  ad=30 pd=22 as=60 ps=44
M1089 m1_69_n343# m1_n11_n309# 3or_0/a_0_n30# Gnd nfet w=4 l=2
+  ad=68 pd=58 as=56 ps=44
M1090 m1_76_n307# 3or_0/a_0_n30# m1_69_n343# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1091 3or_0/a_0_n30# g1 3or_0/a_10_13# 3or_0/w_n13_7# pfet w=6 l=2
+  ad=36 pd=24 as=42 ps=26
M1092 3or_0/a_0_13# m1_n1_n302# m1_71_n273# 3or_0/w_n13_7# pfet w=6 l=2
+  ad=48 pd=28 as=0 ps=0
M1093 3or_0/a_10_13# m1_n11_n309# 3or_0/a_0_13# 3or_0/w_n13_7# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1094 3or_0/a_0_n30# g1 m1_69_n343# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1095 3or_0/a_0_n30# m1_n1_n302# m1_69_n343# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1096 4and_0/a_33_n36# m1_107_12# 4and_0/a_23_n36# Gnd nfet w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1097 4and_0/a_13_5# m1_107_12# m1_193_57# 4and_0/w_0_n1# pfet w=6 l=2
+  ad=96 pd=56 as=144 ps=96
M1098 4and_0/a_23_n36# m1_107_21# 4and_0/a_13_n36# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1099 4and_0/a_13_n36# c_in m1_194_n12# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=40 ps=36
M1100 m1_193_57# m1_107_21# 4and_0/a_13_5# 4and_0/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1101 4and_0/a_13_5# c_in m1_193_57# 4and_0/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1102 m1_271_28# 4and_0/a_13_5# m1_193_57# 4and_0/w_61_n1# pfet w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1103 m1_271_28# 4and_0/a_13_5# m1_194_n12# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1104 m1_193_57# m1_119_6# 4and_0/a_13_5# 4and_0/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1105 4and_0/a_13_5# m1_119_6# 4and_0/a_33_n36# Gnd nfet w=4 l=2
+  ad=24 pd=20 as=0 ps=0
M1106 4and_1/a_33_n36# m1_304_n51# 4and_1/a_23_n36# Gnd nfet w=4 l=2
+  ad=32 pd=24 as=32 ps=24
```

```
M1107 4and_1/a_13_5# m1_304_n51# m1_393_n8# 4and_1/w_0_n1# pfet w=6 l=2
+  ad=96 pd=56 as=144 ps=96
M1108 4and_1/a_23_n36# m1_n38_n95# 4and_1/a_13_n36# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1109 4and_1/a_13_n36# m1_346_n37# m1_476_n77# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=40 ps=36
M1110 m1_393_n8# m1_n38_n95# 4and_1/a_13_5# 4and_1/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1111 4and_1/a_13_5# m1_346_n37# m1_393_n8# 4and_1/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1112 m1_483_n37# 4and_1/a_13_5# m1_393_n8# 4and_1/w_61_n1# pfet w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1113 m1_483_n37# 4and_1/a_13_5# m1_476_n77# Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1114 m1_393_n8# m1_322_n59# 4and_1/a_13_5# 4and_1/w_0_n1# pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1115 4and_1/a_13_5# m1_322_n59# 4and_1/a_33_n36# Gnd nfet w=4 l=2
+  ad=24 pd=20 as=0 ps=0
C0 5and_0/w_0_n1# m1_394_98# 0.08fF
C1 g1 m1_304_n147# 1.50fF
C2 m1_89_n136# m1_81_n168# 0.06fF
C3 m1_n1_n302# m2_n1_n302# 0.06fF
C4 m1_106_104# m5_55_n22# 0.07fF
C5 p1 m2_n38_n223# 0.08fF
C6 g1 m2_357_n331# 0.06fF
C7 m1_65_79# c_in 0.13fF
C8 m1_393_n8# m1_483_n37# 0.06fF
C9 g1 m1_n1_n302# 0.08fF
C10 m1_391_n196# m1_464_n225# 0.06fF
C11 2and_3/a_13_5# m1_454_n254# 0.02fF
C12 m1_n38_n95# m2_156_n262# 0.17fF
C13 5and_0/w_0_n1# c_in 0.08fF
C14 m1_357_n331# m1_347_n338# 1.01fF
C15 5or_0/w_n13_7# m1_390_n290# 0.06fF
C16 m1_366_n324# g3 0.08fF
C17 m1_n15_n136# m1_n27_n143# 0.57fF
C18 3and_0/w_0_n1# 3and_0/a_13_5# 0.05fF
C19 m1_60_n56# m5_55_n22# 0.05fF
C20 m2_107_n87# m4_57_n85# 0.15fF
C21 3and_1/a_13_5# m1_n38_n95# 0.16fF
C22 3or_0/w_n13_7# m1_n1_n302# 0.06fF
C23 m1_119_n93# m5_55_n22# 0.04fF
C24 4and_1/w_61_n1# m1_483_n37# 0.03fF
C25 m1_n38_n95# m2_n27_n143# 0.07fF
C26 m2_n15_n49# m2_n15_n136# 0.02fF
C27 m1_60_n56# m1_57_n85# 0.06fF
C28 m1_178_n248# m2_178_n248# 0.06fF
C29 4and_0/a_13_5# m1_194_n12# 0.02fF
```

```
C30 2and_2/w_0_n1# 2and_2/a_13_5# 0.02fF
C31 p0 m2_n27_n143# 0.12fF
C32 m1_190_n221# m5_55_n22# 0.01fF
C33 2or_0/a_0_n30# m1_55_n22# 0.04fF
C34 g1 g2 0.48fF
C35 carry2 m3_271_n254# 0.04fF
C36 m1_478_n322# m3_483_n421# 0.04fF
C37 m1_346_n37# m5_55_n22# 0.03fF
C38 m1_n49_n10# m2_n15_n49# 0.10fF
C39 m1_107_12# m1_119_6# 1.57fF
C40 4and_0/w_61_n1# m1_271_28# 0.03fF
C41 m1_107_21# 4and_0/a_13_5# 0.16fF
C42 g2 m2_119_n378# 0.16fF
C43 g2 m3_271_n254# 0.01fF
C44 p2 m2_119_n378# 0.15fF
C45 p2 m3_271_n254# 0.02fF
C46 g3 m4_57_n85# 0.05fF
C47 4and_0/w_0_n1# m1_107_21# 0.08fF
C48 m1_71_n193# m1_79_n222# 0.06fF
C49 2and_1/a_13_5# m1_72_n251# 0.02fF
C50 g0 m3_n69_48# 0.04fF
C51 m1_478_n322# m1_471_n372# 0.06fF
C52 g1 2and_2/w_0_n1# 0.08fF
C53 m1_474_n138# m2_366_n324# 0.06fF
C54 m1_322_n59# 4and_1/a_13_5# 0.12fF
C55 m1_454_n254# m5_55_n22# 0.02fF
C56 2and_1/w_0_n1# m1_71_n193# 0.06fF
C57 2and_1/w_43_n1# 2and_1/a_13_5# 0.08fF
C58 m1_107_12# m5_55_n22# 0.04fF
C59 3and_2/a_13_5# m1_393_n109# 0.13fF
C60 m1_71_n193# m5_55_n22# 0.03fF
C61 m1_72_n251# m4_57_n85# 0.03fF
C62 5or_0/a_0_n44# m1_471_n372# 0.33fF
C63 m1_390_n290# m1_478_n322# 0.06fF
C64 m1_178_n248# m1_156_n262# 0.08fF
C65 m2_376_n317# m5_55_n22# 0.07fF
C66 m1_178_n248# g2 0.08fF
C67 m1_71_n273# m1_76_n307# 0.06fF
C68 3or_0/a_0_n30# m1_69_n343# 0.21fF
C69 m1_n38_n95# m2_169_n255# 0.09fF
C70 5and_0/w_73_n1# 5and_0/a_13_5# 0.08fF
C71 m1_106_104# m1_304_46# 0.08fF
C72 c_in m1_322_39# 0.08fF
C73 3and_2/w_0_n1# 3and_2/a_13_5# 0.05fF
C74 5or_0/a_0_n44# m1_390_n290# 0.05fF
C75 m1_n11_n309# m2_n11_n309# 0.07fF
C76 m2_n11_n309# m4_57_n85# 0.16fF
C77 m1_n38_n95# m5_55_n22# 0.17fF
```

```
C78 4and_1/a_13_5# m1_476_n77# 0.02fF
C79 m2_156_n262# m2_169_n255# 0.18fF
C80 m1_57_n85# m1_n38_n95# 0.50fF
C81 m1_n15_n136# m1_n38_n151# 0.08fF
C82 3and_0/w_0_n1# m1_80_n107# 0.05fF
C83 3and_0/w_53_n1# 3and_0/a_13_5# 0.08fF
C84 m2_156_n262# m5_55_n22# 0.06fF
C85 5and_0/a_13_5# m1_488_22# 0.02fF
C86 m1_304_n147# m2_347_n338# 0.06fF
C87 g1 m2_304_n147# 0.09fF
C88 2and_2/a_13_5# 2and_2/a_56_n25# 0.05fF
C89 2and_0/w_43_n1# m1_69_49# 0.03fF
C90 p0 2and_0/a_13_5# 0.17fF
C91 g1 m3_145_n56# 0.09fF
C92 2and_0/w_0_n1# c_in 0.08fF
C93 m2_347_n338# m2_357_n331# 0.46fF
C94 m1_60_n56# m2_107_n87# 0.11fF
C95 m2_n49_n231# m2_n38_n223# 0.37fF
C96 m1_106_104# m2_n49_n231# 0.10fF
C97 5or_0/w_n13_7# m1_366_n324# 0.06fF
C98 m2_n15_n49# m4_57_n85# 0.09fF
C99 m2_n27_n143# m5_55_n22# 0.06fF
C100 m1_n49_n10# m2_119_n378# 0.07fF
C101 m1_193_57# m1_271_28# 0.06fF
C102 3and_1/a_13_5# m1_193_n48# 0.13fF
C103 2or_0/w_n13_0# m1_4_n58# 0.06fF
C104 m1_304_n51# m2_322_n393# 0.07fF
C105 m1_n15_n136# m2_n15_n136# 0.08fF
C106 g2 m2_347_n338# 0.06fF
C107 4or_0/a_0_n37# m1_271_n254# 0.05fF
C108 m1_346_n37# m2_n49_n231# 0.07fF
C109 g3 m3_94_n434# 0.01fF
C110 m1_119_6# m5_55_n22# 0.04fF
C111 m1_n38_n223# 2and_1/a_13_5# 0.04fF
C112 m1_169_n255# m1_156_n262# 0.86fF
C113 4or_0/w_n13_7# 4or_0/a_0_n37# 0.09fF
C114 m1_107_12# m2_107_n87# 0.06fF
C115 m1_169_n255# g2 0.08fF
C116 4and_1/w_0_n1# 4and_1/a_13_5# 0.05fF
C117 m1_346_n37# m1_304_n51# 0.08fF
C118 2and_3/w_0_n1# m1_322_n235# 0.08fF
C119 m1_393_n109# m5_55_n22# 0.05fF
C120 m1_n38_n95# m1_304_46# 1.45fF
C121 5and_0/w_73_n1# m1_394_98# 0.03fF
C122 g1 m1_322_n153# 0.08fF
C123 3and_2/w_0_n1# m1_393_n109# 0.05fF
C124 m2_169_n255# m5_55_n22# 0.06fF
C125 m2_n1_n302# m4_57_n85# 0.08fF
```

```
C126 m1_304_n147# m2_357_n331# 0.06fF
C127 3or_0/w_n13_7# m1_76_n307# 0.03fF
C128 m1_69_49# 2and_0/a_6_n25# 0.06fF
C129 g1 m4_57_n85# 0.17fF
C130 g1 m1_n11_n309# 0.77fF
C131 m1_n38_n95# m2_107_n87# 0.11fF
C132 5and_0/w_0_n1# m1_106_104# 0.08fF
C133 m1_357_n331# g3 0.08fF
C134 m1_366_n324# 5or_0/a_0_n44# 0.08fF
C135 m1_n27_n143# m1_n38_n151# 0.87fF
C136 m1_n15_n136# 3and_0/a_13_5# 0.04fF
C137 3and_0/w_53_n1# m1_80_n107# 0.03fF
C138 m2_119_n378# m4_57_n85# 0.42fF
C139 m1_119_n177# m1_260_n199# 0.03fF
C140 m3_271_n254# m4_57_n85# 0.10fF
C141 m3_178_n49# m5_55_n22# 0.14fF
C142 3or_0/w_n13_7# m1_n11_n309# 0.06fF
C143 m1_193_n48# m5_55_n22# 0.05fF
C144 m1_n38_n95# m2_n49_n231# 0.09fF
C145 c_in m3_n69_48# 0.08fF
C146 m2_n15_n136# m3_n69_48# 0.01fF
C147 2and_2/w_0_n1# m1_192_n139# 0.06fF
C148 2and_2/w_43_n1# 2and_2/a_13_5# 0.08fF
C149 m1_193_n48# m3_178_n49# 0.07fF
C150 p0 m2_n49_n231# 0.07fF
C151 m1_191_n296# m4_57_n85# 0.01fF
C152 m2_n27_n143# m2_107_n87# 0.03fF
C153 m1_n38_n95# m1_304_n51# 1.31fF
C154 c_in g0 0.04fF
C155 m1_89_n136# m2_n11_n309# 0.02fF
C156 m1_107_12# 4and_0/a_13_5# 0.08fF
C157 g2 m2_357_n331# 0.06fF
C158 m1_n49_n10# m3_n69_48# 0.01fF
C159 m2_n27_n143# m2_n49_n231# 0.22fF
C160 m1_n15_n51# m1_4_n58# 0.31fF
C161 3and_1/w_0_n1# m1_n49_n10# 0.08fF
C162 p3 m3_271_n254# 0.01fF
C163 carry0 m3_145_n56# 0.03fF
C164 carry1 m3_94_n434# 0.03fF
C165 4and_0/w_0_n1# m1_107_12# 0.08fF
C166 m1_190_n221# m1_271_n254# 0.06fF
C167 4or_0/a_0_n37# m1_191_n296# 0.25fF
C168 2and_3/a_13_5# m1_391_n196# 0.09fF
C169 2and_1/w_43_n1# m1_71_n193# 0.03fF
C170 m1_119_n177# m2_156_n262# 0.07fF
C171 5and_0/a_13_5# m1_394_98# 0.21fF
C172 m1_322_n153# m1_467_n170# 0.05fF
C173 3and_2/a_13_5# m1_474_n138# 0.05fF
```

```
C174 4or_0/w_n13_7# m1_190_n221# 0.06fF
C175 m1_156_n262# g2 1.02fF
C176 4and_1/w_0_n1# m1_393_n8# 0.08fF
C177 m1_n38_n223# m2_n38_n223# 0.08fF
C178 c_in 5and_0/a_13_5# 0.04fF
C179 m1_106_104# m1_322_39# 0.08fF
C180 3and_2/w_53_n1# 3and_2/a_13_5# 0.08fF
C181 m1_304_46# m5_55_n22# 0.02fF
C182 m1_322_39# m2_322_n393# 0.06fF
C183 5and_0/w_0_n1# m1_n38_n95# 0.08fF
C184 m1_347_n338# g3 1.27fF
C185 3and_0/w_53_n1# m1_89_n136# 0.03fF
C186 m1_n27_n143# 3and_0/a_13_5# 0.16fF
C187 m2_169_n255# m3_192_n139# 0.01fF
C188 m1_304_n147# m2_304_n147# 0.09fF
C189 g1 m2_322_n393# 0.07fF
C190 m1_322_n153# m2_347_n338# 0.06fF
C191 m1_192_n139# 2and_2/a_56_n25# 0.06fF
C192 2and_2/a_13_5# m1_260_n199# 0.02fF
C193 m3_192_n139# m5_55_n22# 0.05fF
C194 g1 m3_94_n434# 0.07fF
C195 m1_194_n109# m4_57_n85# 0.03fF
C196 2and_3/w_43_n1# m1_464_n225# 0.03fF
C197 m1_60_n56# m2_119_n378# 0.13fF
C198 5or_0/w_n13_7# m1_357_n331# 0.06fF
C199 m1_376_n317# m1_366_n324# 0.47fF
C200 m2_n49_n231# m5_55_n22# 0.06fF
C201 p1 m2_n49_n231# 0.09fF
C202 m1_119_n93# m2_119_n378# 0.09fF
C203 m1_65_79# m2_n27_n143# 0.07fF
C204 m1_391_n196# m5_55_n22# 0.02fF
C205 2or_0/a_0_n30# m1_60_n56# 0.05fF
C206 3and_1/a_13_5# m1_276_n77# 0.05fF
C207 m1_304_n51# m5_55_n22# 0.03fF
C208 m1_n49_n10# m1_55_n22# 0.44fF
C209 m1_119_6# 4and_0/a_13_5# 0.12fF
C210 m1_n15_n51# m2_n15_n49# 0.11fF
C211 m2_n27_n143# m2_n15_n49# 0.10fF
C212 2or_0/w_n13_0# 2or_0/a_0_n30# 0.09fF
C213 m1_322_n59# m2_322_n393# 0.08fF
C214 4and_0/w_0_n1# m1_119_6# 0.08fF
C215 m1_79_n222# m1_72_n251# 0.06fF
C216 m1_119_n177# m2_169_n255# 0.06fF
C217 m1_322_n235# m2_347_n338# 0.06fF
C218 g2 m2_304_n147# 0.07fF
C219 g2 m3_145_n56# 0.02fF
C220 m1_119_n177# m5_55_n22# 0.04fF
C221 p2 m2_304_n147# 0.05fF
```

```
C222 4and_1/a_13_5# m1_393_n8# 0.17fF
C223 p2 m3_145_n56# 0.02fF
C224 2and_1/w_43_n1# m1_79_n222# 0.03fF
C225 m1_n49_n231# 2and_1/a_13_5# 0.17fF
C226 m1_393_n109# m1_474_n138# 0.06fF
C227 m1_476_n77# m4_454_n254# 0.03fF
C228 m1_169_n255# 4or_0/a_0_n37# 0.08fF
C229 m1_346_n37# m1_322_n59# 0.08fF
C230 4and_1/w_61_n1# 4and_1/a_13_5# 0.08fF
C231 2and_3/w_0_n1# 2and_3/a_13_5# 0.02fF
C232 m1_467_n170# m4_454_n254# 0.03fF
C233 m2_357_n331# m2_366_n324# 0.35fF
C234 m1_n38_n95# m1_322_39# 0.17fF
C235 5and_0/w_73_n1# m1_492_69# 0.03fF
C236 m1_304_n147# m1_322_n153# 1.38fF
C237 g1 3and_2/a_13_5# 0.04fF
C238 3and_2/w_53_n1# m1_393_n109# 0.03fF
C239 m1_322_n153# m2_357_n331# 0.06fF
C240 m1_71_n273# m5_55_n22# 0.03fF
C241 3or_0/a_0_n30# m1_71_n273# 0.04fF
C242 m1_n38_n95# m2_119_n378# 0.19fF
C243 m1_492_69# m2_347_n338# 0.06fF
C244 c_in m2_n15_n136# 0.12fF
C245 m1_65_79# m5_55_n22# 0.03fF
C246 m1_357_n331# 5or_0/a_0_n44# 0.08fF
C247 m1_n38_n151# 3and_0/a_13_5# 0.12fF
C248 m1_492_69# m1_488_22# 0.06fF
C249 m1_276_n77# m2_169_n255# 0.06fF
C250 g1 m2_156_n262# 0.07fF
C251 m1_n1_n302# m1_n11_n309# 0.36fF
C252 2and_0/a_13_5# m1_65_79# 0.09fF
C253 m1_304_46# m2_n49_n231# 0.08fF
C254 5or_0/w_n13_7# m1_347_n338# 0.06fF
C255 m2_347_n338# m4_454_n254# 0.07fF
C256 m1_n49_n10# c_in 0.16fF
C257 m1_271_28# m1_194_n12# 0.06fF
C258 2and_2/w_43_n1# m1_192_n139# 0.03fF
C259 g2 m2_366_n324# 0.06fF
C260 2and_0/w_0_n1# p0 0.08fF
C261 m1_193_n48# m1_276_n77# 0.06fF
C262 m1_119_n93# m1_194_n109# 0.05fF
C263 m1_n38_n95# m1_322_n59# 0.17fF
C264 carry3 m3_483_n421# 0.04fF
C265 m1_471_n372# m4_57_n85# 0.01fF
C266 m1_322_n235# m2_357_n331# 0.06fF
C267 m1_n49_n10# m3_145_n56# 0.01fF
C268 g2 m4_57_n85# 0.09fF
C269 2and_3/w_0_n1# m5_55_n22# 0.06fF
```

```
C270 3and_1/w_0_n1# m1_119_n93# 0.08fF
C271 p2 m4_57_n85# 0.43fF
C272 m1_346_n37# m2_347_n338# 0.07fF
C273 m1_79_n222# m2_n1_n302# 0.07fF
C274 5and_0/a_13_5# m1_492_69# 0.05fF
C275 3and_2/a_13_5# m1_467_n170# 0.02fF
C276 m1_156_n262# 4or_0/a_0_n37# 0.08fF
C277 m1_119_6# m2_119_n378# 0.07fF
C278 c_in m1_107_21# 1.24fF
C279 4or_0/a_0_n37# g2 0.38fF
C280 4and_1/w_61_n1# m1_393_n8# 0.03fF
C281 g2 m1_322_n235# 0.78fF
C282 2and_1/w_0_n1# m1_n38_n223# 0.08fF
C283 m1_106_104# 5and_0/a_13_5# 0.16fF
C284 m1_322_39# m5_55_n22# 0.03fF
C285 g1 m2_169_n255# 0.06fF
C286 4and_1/w_0_n1# m1_346_n37# 0.08fF
C287 g1 m5_55_n22# 0.07fF
C288 g1 3or_0/a_0_n30# 0.30fF
C289 3and_2/w_0_n1# g1 0.08fF
C290 5and_0/w_0_n1# m1_304_46# 0.08fF
C291 2and_0/a_6_n25# m4_57_n85# 0.03fF
C292 m1_347_n338# 5or_0/a_0_n44# 0.08fF
C293 m2_357_n331# m4_454_n254# 0.07fF
C294 m1_304_n147# m2_322_n393# 0.07fF
C295 m3_483_n421# m4_454_n254# 0.11fF
C296 3or_0/w_n13_7# 3or_0/a_0_n30# 0.09fF
C297 m1_n38_n95# m2_347_n338# 0.07fF
C298 m1_376_n317# m1_357_n331# 0.08fF
C299 m2_304_n147# m4_57_n85# 0.07fF
C300 3and_1/w_0_n1# m1_n38_n95# 0.08fF
C301 m3_145_n56# m4_57_n85# 0.48fF
C302 2and_0/w_0_n1# 2and_0/a_13_5# 0.02fF
C303 m1_65_79# m2_n49_n231# 0.08fF
C304 m1_n49_n10# m4_57_n85# 0.09fF
C305 3and_1/a_13_5# m1_194_n109# 0.02fF
C306 m1_55_n22# m1_60_n56# 0.06fF
C307 2or_0/a_0_n30# m1_57_n85# 0.13fF
C308 m1_471_n372# m4_454_n254# 0.03fF
C309 m1_322_n59# m5_55_n22# 0.03fF
C310 m1_260_n199# m2_178_n248# 0.07fF
C311 3and_1/w_0_n1# 3and_1/a_13_5# 0.05fF
C312 m1_376_n317# m2_376_n317# 0.06fF
C313 m1_366_n324# m2_366_n324# 0.06fF
C314 2or_0/w_n13_0# m1_55_n22# 0.06fF
C315 m1_n38_n95# 4and_1/w_0_n1# 0.08fF
C316 m1_n15_n51# m3_n69_48# 0.01fF
C317 m2_n27_n143# m3_n69_48# 0.12fF
```

```
C318 p0 g0 0.19fF
C319 m1_n38_n151# m2_n38_n223# 0.09fF
C320 4and_0/w_0_n1# 4and_0/a_13_5# 0.05fF
C321 g2 m2_322_n393# 0.07fF
C322 m1_357_n331# m2_357_n331# 0.06fF
C323 g2 m3_94_n434# 0.01fF
C324 p3 m3_145_n56# 0.01fF
C325 p2 m3_94_n434# 0.02fF
C326 m1_194_n12# m4_57_n85# 0.03fF
C327 m1_193_57# m5_55_n22# 0.05fF
C328 m1_394_98# m1_492_69# 0.06fF
C329 m1_347_n338# m2_347_n338# 0.06fF
C330 m1_346_n37# 4and_1/a_13_5# 0.04fF
C331 2and_3/w_0_n1# m1_391_n196# 0.06fF
C332 2and_3/w_43_n1# 2and_3/a_13_5# 0.08fF
C333 m1_n27_n143# m2_n27_n143# 0.06fF
C334 3and_2/w_53_n1# m1_474_n138# 0.03fF
C335 m1_304_n147# 3and_2/a_13_5# 0.16fF
C336 m1_304_46# m1_322_39# 1.45fF
C337 m1_n38_n95# 5and_0/a_13_5# 0.08fF
C338 m1_76_n307# m4_57_n85# 0.04fF
C339 c_in m1_106_104# 0.68fF
C340 3and_0/a_13_5# m1_80_n107# 0.13fF
C341 2and_0/a_13_5# m1_69_49# 0.05fF
C342 m2_107_n87# m2_119_n378# 0.16fF
C343 m1_322_39# m2_n49_n231# 0.07fF
C344 5or_0/w_n13_7# g3 0.06fF
C345 m1_376_n317# m1_347_n338# 0.08fF
C346 m2_347_n338# m5_55_n22# 0.06fF
C347 2and_2/w_43_n1# 2and_2/a_56_n25# 0.03fF
C348 m1_119_n177# 2and_2/a_13_5# 0.17fF
C349 m1_322_n235# m2_366_n324# 0.06fF
C350 m1_n38_n95# 4and_1/a_13_5# 0.16fF
C351 m1_60_n56# m3_145_n56# 0.09fF
C352 m1_n49_n10# m1_60_n56# 0.17fF
C353 m1_169_n255# m2_169_n255# 0.06fF
C354 m1_119_n93# m3_145_n56# 0.01fF
C355 m1_4_n58# 2or_0/a_0_n30# 0.19fF
C356 m1_n49_n10# m1_119_n93# 0.08fF
C357 3and_1/w_0_n1# m1_193_n48# 0.05fF
C358 3and_1/w_53_n1# 3and_1/a_13_5# 0.08fF
C359 m1_156_n262# m2_156_n262# 0.06fF
C360 4and_0/w_61_n1# 4and_0/a_13_5# 0.08fF
C361 m1_192_n139# m5_55_n22# 0.05fF
C362 g1 m1_119_n177# 0.84fF
C363 g3 m3_271_n254# 0.01fF
C364 m1_119_n177# m2_119_n378# 0.10fF
C365 4or_0/w_n13_7# m1_271_n254# 0.03fF
```

```
C366 m1_271_28# m2_156_n262# 0.06fF
C367 c_in m1_107_12# 0.08fF
C368 m1_304_n51# m1_322_n59# 1.53fF
C369 g2 2and_3/a_13_5# 0.04fF
C370 2and_1/w_0_n1# m1_n49_n231# 0.08fF
C371 m1_n38_n223# m2_n11_n309# 0.07fF
C372 m2_n11_n309# m2_n1_n302# 0.11fF
C373 m2_169_n255# m2_178_n248# 0.11fF
C374 m2_366_n324# m4_454_n254# 0.08fF
C375 m2_178_n248# m5_55_n22# 0.09fF
C376 g1 m2_n11_n309# 0.02fF
C377 m1_304_n147# m5_55_n22# 0.02fF
C378 m1_n38_n95# m2_n15_n136# 0.08fF
C379 c_in m1_n38_n95# 0.08fF
C380 5and_0/w_0_n1# m1_322_39# 0.08fF
C381 3and_2/w_0_n1# m1_304_n147# 0.08fF
C382 g3 5or_0/a_0_n44# 0.48fF
C383 m1_n38_n151# m1_81_n168# 0.05fF
C384 3and_0/a_13_5# m1_89_n136# 0.05fF
C385 m2_357_n331# m5_55_n22# 0.05fF
C386 m1_322_n153# m2_322_n393# 0.08fF
C387 2and_2/a_56_n25# m1_260_n199# 0.06fF
C388 m1_76_n307# m3_94_n434# 0.02fF
C389 3or_0/w_n13_7# m1_71_n273# 0.06fF
C390 p0 2and_0/a_6_n25# 0.03fF
C391 p0 c_in 0.66fF
C392 m1_n38_n95# m2_304_n147# 0.11fF
C393 m1_366_n324# m1_357_n331# 0.92fF
C394 3and_0/w_0_n1# m1_n15_n136# 0.08fF
C395 m1_n38_n95# m3_145_n56# 0.09fF
C396 m1_60_n56# m4_57_n85# 0.06fF
C397 m2_322_n393# m4_57_n85# 0.07fF
C398 m1_55_n22# m5_55_n22# 0.03fF
C399 m1_n49_n10# m1_n38_n95# 1.46fF
C400 m3_94_n434# m4_57_n85# 0.12fF
C401 2and_0/w_0_n1# m1_65_79# 0.06fF
C402 2and_0/w_43_n1# 2and_0/a_13_5# 0.08fF
C403 m1_119_n93# m4_57_n85# 0.05fF
C404 m1_n15_n51# c_in 0.10fF
C405 c_in m2_n27_n143# 0.15fF
C406 m2_n27_n143# m2_n15_n136# 0.13fF
C407 m2_156_n262# m3_145_n56# 0.01fF
C408 m1_n49_n10# m2_156_n262# 0.07fF
C409 4and_0/a_13_5# m1_193_57# 0.17fF
C410 m1_271_n254# m3_271_n254# 0.02fF
C411 m2_n49_n231# m2_347_n338# 0.11fF
C412 g2 m5_55_n22# 0.04fF
C413 m1_n49_n10# 3and_1/a_13_5# 0.04fF
```

```
C414 3and_1/w_53_n1# m1_193_n48# 0.03fF
C415 m1_483_n37# m1_476_n77# 0.06fF
C416 m1_464_n225# m1_454_n254# 0.06fF
C417 m2_n49_n231# m3_n69_48# 0.13fF
C418 m1_390_n290# m5_55_n22# 0.02fF
C419 m1_4_n58# m3_n69_48# 0.04fF
C420 m1_n49_n10# m2_n27_n143# 0.09fF
C421 m1_107_21# m1_107_12# 1.60fF
C422 4and_0/w_0_n1# m1_193_57# 0.08fF
C423 m1_322_n235# m2_322_n393# 0.08fF
C424 p3 m2_322_n393# 0.08fF
C425 m1_464_n225# m2_376_n317# 0.06fF
C426 m1_260_n199# m4_57_n85# 0.03fF
C427 m1_271_n254# m1_191_n296# 0.06fF
C428 m1_304_n51# m2_347_n338# 0.07fF
C429 g1 2and_2/a_13_5# 0.04fF
C430 p3 m3_94_n434# 0.01fF
C431 g0 m2_n49_n231# 0.09fF
C432 2and_1/a_13_5# m1_71_n193# 0.09fF
C433 m2_366_n324# m2_376_n317# 0.10fF
C434 m1_474_n138# m1_467_n170# 0.06fF
C435 m1_192_n139# m3_192_n139# 0.04fF
C436 4or_0/a_0_n37# m1_190_n221# 0.04fF
C437 c_in m1_119_6# 0.08fF
C438 2and_3/w_43_n1# m1_391_n196# 0.03fF
C439 m1_76_n307# m1_69_n343# 0.06fF
C440 m1_304_46# 5and_0/a_13_5# 0.08fF
C441 m1_322_n153# 3and_2/a_13_5# 0.12fF
C442 4or_0/w_n13_7# m1_178_n248# 0.06fF
C443 m1_394_98# m5_55_n22# 0.05fF
C444 4and_1/w_0_n1# m1_304_n51# 0.08fF
C445 m1_69_n343# m4_57_n85# 0.03fF
C446 5or_0/w_n13_7# m1_478_n322# 0.03fF
C447 3and_0/a_13_5# m1_81_n168# 0.02fF
C448 m1_80_n107# m1_89_n136# 0.06fF
C449 m1_107_21# m2_n27_n143# 0.11fF
C450 m1_n38_n95# m4_57_n85# 0.11fF
C451 c_in m5_55_n22# 0.15fF
C452 g1 m2_119_n378# 0.13fF
C453 m1_65_79# m1_69_49# 0.06fF
C454 2and_0/a_13_5# 2and_0/a_6_n25# 0.02fF
C455 g1 3or_0/w_n13_7# 0.06fF
C456 m1_n49_n231# m2_n49_n231# 0.07fF
C457 g1 m3_271_n254# 0.07fF
C458 m1_322_n235# m1_454_n254# 0.03fF
C459 2and_3/a_13_5# m1_464_n225# 0.05fF
C460 2and_0/a_13_5# c_in 0.04fF
C461 m1_376_n317# g3 0.08fF
```

```
C462 m1_366_n324# m1_347_n338# 0.08fF
C463 5or_0/w_n13_7# 5or_0/a_0_n44# 0.09fF
C464 3and_0/w_0_n1# m1_n27_n143# 0.08fF
C465 m2_156_n262# m4_57_n85# 0.15fF
C466 m1_n49_n10# m5_55_n22# 0.11fF
C467 m1_69_49# m2_n15_n49# 0.09fF
C468 m1_276_n77# m1_194_n109# 0.06fF
C469 m1_393_n8# m5_55_n22# 0.05fF
C470 m1_119_6# m1_194_n12# 0.04fF
C471 2or_0/w_n13_0# m1_60_n56# 0.03fF
C472 m2_n15_n49# m3_n69_48# 0.13fF
C473 m1_80_n107# m1_n38_n95# 0.82fF
C474 m1_107_21# m1_119_6# 0.08fF
C475 4and_0/w_61_n1# m1_193_57# 0.03fF
C476 m1_81_n168# m4_57_n85# 0.04fF
C477 m1_n49_n231# m1_72_n251# 0.03fF
C478 2and_1/a_13_5# m1_79_n222# 0.05fF
C479 m1_304_n51# 4and_1/a_13_5# 0.08fF
C480 m1_322_n235# 2and_3/a_13_5# 0.17fF
C481 m1_454_n254# m4_454_n254# 0.03fF
C482 m1_107_21# m5_55_n22# 0.04fF
C483 m1_483_n37# m2_357_n331# 0.06fF
C484 2and_1/w_0_n1# 2and_1/a_13_5# 0.02fF
C485 m1_n49_n231# m2_n11_n309# 0.07fF
C486 m1_79_n222# m4_57_n85# 0.04fF
C487 5or_0/a_0_n44# m1_478_n322# 0.05fF
C488 4or_0/w_n13_7# m1_169_n255# 0.06fF
C489 m2_376_n317# m4_454_n254# 0.07fF
C490 m2_366_n324# m5_55_n22# 0.05fF
C491 3or_0/a_0_n30# m1_76_n307# 0.05fF
C492 m1_322_n153# m5_55_n22# 0.03fF
C493 m1_n38_n95# m2_n38_n223# 0.10fF
C494 5and_0/w_0_n1# 5and_0/a_13_5# 0.08fF
C495 m1_106_104# m1_n38_n95# 0.81fF
C496 c_in m1_304_46# 0.08fF
C497 3and_2/w_0_n1# m1_322_n153# 0.08fF
C498 m2_169_n255# m4_57_n85# 0.07fF
C499 m4_57_n85# m5_55_n22# 1.21fF
C500 m1_n11_n309# 3or_0/a_0_n30# 0.08fF
C501 4and_1/a_13_5# m1_483_n37# 0.05fF
C502 m1_322_n59# m1_476_n77# 0.04fF
C503 m1_n38_n95# m2_322_n393# 0.12fF
C504 m1_304_46# m2_304_n147# 0.08fF
C505 3and_0/w_0_n1# m1_n38_n151# 0.08fF
C506 m1_57_n85# m4_57_n85# 0.03fF
C507 m1_322_39# m1_488_22# 0.05fF
C508 g1 m2_347_n338# 0.06fF
C509 2and_2/a_13_5# m1_192_n139# 0.09fF
```

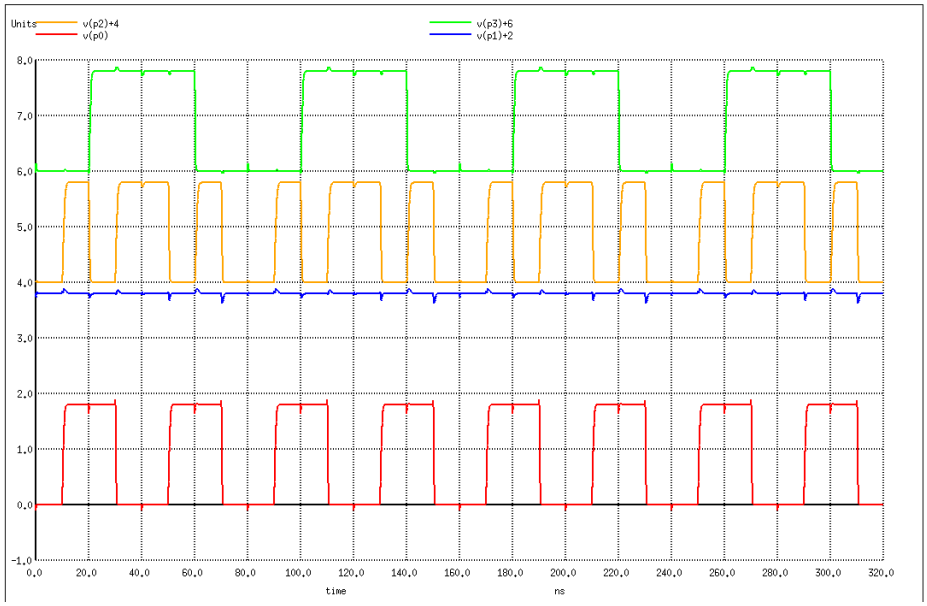
```
C510 m1_119_n93# m1_n38_n95# 1.47fF
C511 2and_0/w_43_n1# m1_65_79# 0.03fF
C512 c_in m2_n49_n231# 0.34fF
C513 m2_n27_n143# m2_n38_n223# 0.18fF
C514 m1_106_104# m2_n27_n143# 0.11fF
C515 m1_4_n58# c_in 0.02fF
C516 5or_0/w_n13_7# m1_376_n317# 0.06fF
C517 m1_119_n93# m2_156_n262# 0.07fF
C518 m1_n49_n10# m2_107_n87# 0.07fF
C519 4and_0/a_13_5# m1_271_28# 0.05fF
C520 2and_2/w_0_n1# m1_119_n177# 0.08fF
C521 m1_322_n235# m5_55_n22# 0.04fF
C522 m1_119_n93# 3and_1/a_13_5# 0.12fF
C523 3and_1/w_53_n1# m1_276_n77# 0.03fF
C524 m1_n38_n95# m1_346_n37# 0.92fF
C525 m1_n49_n10# m2_n49_n231# 0.12fF
C526 m1_80_n107# m5_55_n22# 0.03fF
C527 2or_0/w_n13_0# m1_n15_n51# 0.06fF
C528 m1_322_n59# m2_347_n338# 0.07fF
C529 m1_304_n51# m2_304_n147# 0.09fF
C530 m1_271_n254# g2 0.03fF
C531 c_in 4and_0/a_13_5# 0.04fF
C532 g3 m3_145_n56# 0.01fF
C533 m1_n38_n223# m1_n49_n231# 0.68fF
C534 m1_322_39# 5and_0/a_13_5# 0.12fF
C535 m1_119_n177# m3_145_n56# 0.01fF
C536 4or_0/w_n13_7# m1_156_n262# 0.06fF
C537 m1_178_n248# m1_169_n255# 0.44fF
C538 c_in 4and_0/w_0_n1# 0.08fF
C539 4or_0/w_n13_7# g2 0.06fF
C540 4and_1/w_0_n1# m1_322_n59# 0.08fF
C541 2and_3/w_0_n1# g2 0.08fF
C542 m5_55_n22# Gnd 0.28fF **FLOATING
C543 m4_57_n85# Gnd 0.23fF **FLOATING
C544 m3_483_n421# Gnd 0.07fF **FLOATING
C545 m3_192_n139# Gnd 0.00fF **FLOATING
C546 m3_94_n434# Gnd 0.12fF **FLOATING
C547 m2_376_n317# Gnd 0.42fF **FLOATING
C548 m2_366_n324# Gnd 0.48fF **FLOATING
C549 m2_n11_n309# Gnd 0.11fF **FLOATING
C550 m2_n38_n223# Gnd 0.64fF **FLOATING
C551 m2_n15_n136# Gnd 0.30fF **FLOATING
C552 m2_357_n331# Gnd 0.57fF **FLOATING
C553 m2_119_n378# Gnd 0.81fF **FLOATING
C554 m2_107_n87# Gnd 0.11fF **FLOATING
C555 m2_156_n262# Gnd 0.11fF **FLOATING
C556 m2_322_n393# Gnd 0.91fF **FLOATING
C557 m2_304_n147# Gnd 0.25fF **FLOATING
```

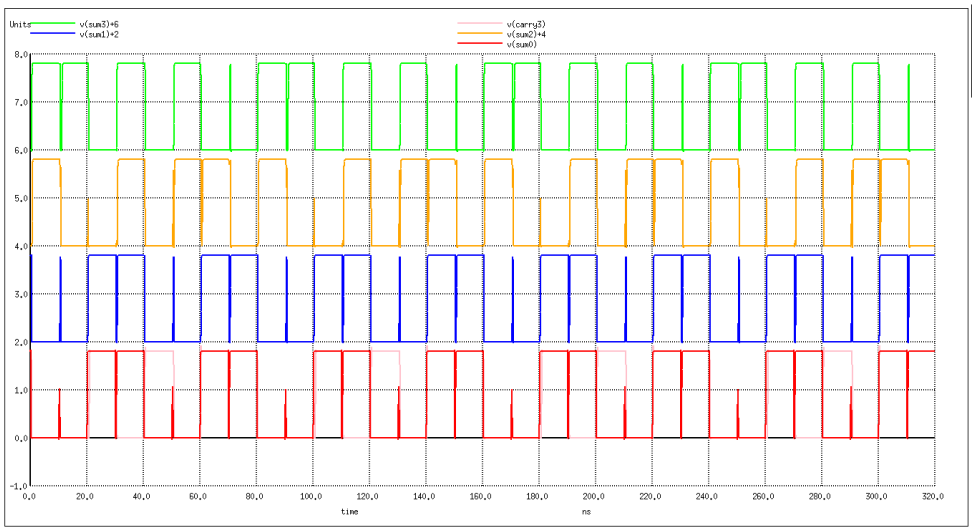
```
C558 m2_347_n338# Gnd 0.71fF **FLOATING
C559 m2_n49_n231# Gnd 1.42fF **FLOATING
C560 m2_n27_n143# Gnd 0.19fF **FLOATING
C561 carry3 Gnd 0.09fF **FLOATING
C562 carry2 Gnd 0.06fF **FLOATING
C563 carry0 Gnd 0.05fF **FLOATING
C564 carry1 Gnd 0.05fF **FLOATING
C565 p3 Gnd 0.38fF **FLOATING
C566 p2 Gnd 0.41fF **FLOATING
C567 p1 Gnd 0.29fF **FLOATING
C568 g0 Gnd 0.05fF **FLOATING
C569 m1_476_n77# Gnd 0.39fF
C570 m1_483_n37# Gnd 0.14fF
C571 m1_393_n8# Gnd 0.38fF
C572 4and_1/a_13_5# Gnd 0.52fF
C573 m1_322_n59# Gnd 0.29fF
C574 m1_304_n51# Gnd 0.40fF
C575 m1_346_n37# Gnd 0.48fF
C576 4and_1/w_61_n1# Gnd 0.43fF
C577 4and_1/w_0_n1# Gnd 0.99fF
C578 m1_194_n12# Gnd 0.34fF
C579 m1_271_28# Gnd 0.23fF
C580 m1_193_57# Gnd 0.25fF
C581 4and_0/a_13_5# Gnd 0.52fF
C582 m1_119_6# Gnd 0.64fF
C583 m1_107_12# Gnd 0.65fF
C584 m1_107_21# Gnd 0.62fF
C585 4and_0/w_61_n1# Gnd 0.43fF
C586 4and_0/w_0_n1# Gnd 0.99fF
C587 m1_69_n343# Gnd 0.13fF
C588 m1_76_n307# Gnd 0.26fF
C589 m1_71_n273# Gnd 0.31fF
C590 3or_0/a_0_n30# Gnd 0.46fF
C591 m1_n11_n309# Gnd 0.34fF
C592 m1_n1_n302# Gnd 0.29fF
C593 3or_0/w_n13_7# Gnd 1.21fF
C594 m1_488_22# Gnd 0.41fF
C595 m1_492_69# Gnd 0.14fF
C596 m1_394_98# Gnd 0.42fF
C597 5and_0/a_13_5# Gnd 0.62fF
C598 m1_322_39# Gnd 0.69fF
C599 m1_304_46# Gnd 0.37fF
C600 m1_n38_n95# Gnd 1.16fF
C601 m1_106_104# Gnd 1.75fF
C602 5and_0/w_73_n1# Gnd 0.43fF
C603 5and_0/w_0_n1# Gnd 1.18fF
C604 m1_57_n85# Gnd 0.31fF
C605 m1_55_n22# Gnd 0.28fF
```

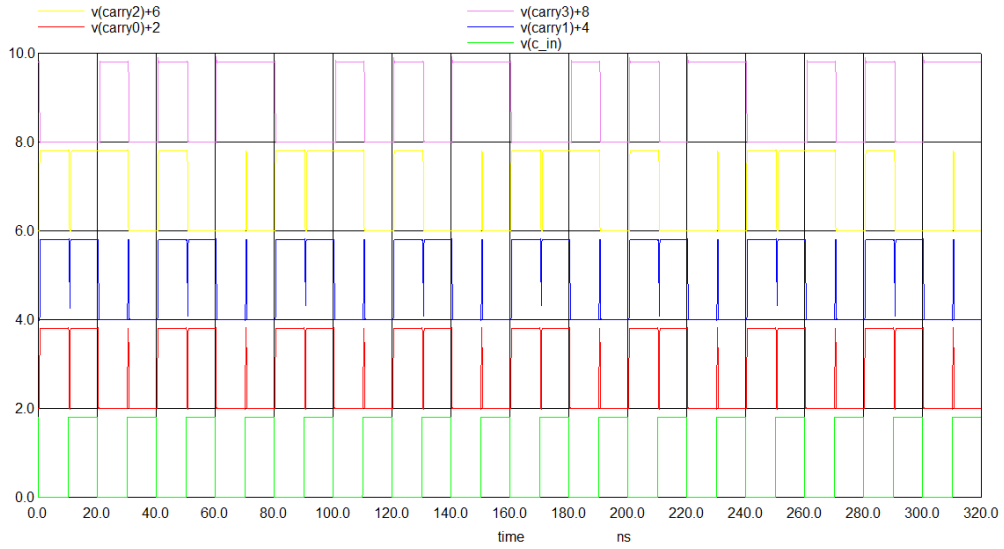
```
C606 2or_0/a_0_n30# Gnd 0.35fF
C607 m1_4_n58# Gnd 0.29fF
C608 m1_n15_n51# Gnd 0.23fF
C609 2or_0/w_n13_0# Gnd 1.03fF
C610 m1_471_n372# Gnd 0.42fF
C611 m1_478_n322# Gnd 0.25fF
C612 m1_390_n290# Gnd 0.31fF
C613 5or_0/a_0_n44# Gnd 0.65fF
C614 g3 Gnd 0.86fF
C615 m1_347_n338# Gnd 0.61fF
C616 m1_357_n331# Gnd 0.55fF
C617 m1_366_n324# Gnd 0.51fF
C618 m1_376_n317# Gnd 0.45fF
C619 5or_0/w_n13_7# Gnd 1.55fF
C620 m1_454_n254# Gnd 0.33fF
C621 m1_464_n225# Gnd 0.17fF
C622 m1_391_n196# Gnd 0.28fF
C623 2and_3/a_13_5# Gnd 0.37fF
C624 m1_322_n235# Gnd 0.53fF
C625 g2 Gnd 1.04fF
C626 2and_3/w_43_n1# Gnd 0.43fF
C627 2and_3/w_0_n1# Gnd 0.67fF
C628 m1_260_n199# Gnd 0.31fF
C629 2and_2/a_56_n25# Gnd 0.11fF
C630 m1_192_n139# Gnd 0.28fF
C631 2and_2/a_13_5# Gnd 0.37fF
C632 m1_119_n177# Gnd 0.52fF
C633 2and_2/w_43_n1# Gnd 0.43fF
C634 2and_2/w_0_n1# Gnd 0.67fF
C635 m1_72_n251# Gnd 0.33fF
C636 m1_79_n222# Gnd 0.17fF
C637 m1_71_n193# Gnd 0.36fF
C638 2and_1/a_13_5# Gnd 0.37fF
C639 m1_n49_n231# Gnd 0.51fF
C640 m1_n38_n223# Gnd 0.46fF
C641 2and_1/w_43_n1# Gnd 0.43fF
C642 2and_1/w_0_n1# Gnd 0.67fF
C643 2and_0/a_6_n25# Gnd 0.29fF
C644 m1_69_49# Gnd 0.17fF
C645 m1_65_79# Gnd 0.69fF
C646 2and_0/a_13_5# Gnd 0.37fF
C647 p0 Gnd 0.17fF
C648 2and_0/w_43_n1# Gnd 0.43fF
C649 2and_0/w_0_n1# Gnd 0.67fF
C650 m1_467_n170# Gnd 0.37fF
C651 m1_474_n138# Gnd 0.17fF
C652 m1_393_n109# Gnd 0.33fF
C653 3and_2/a_13_5# Gnd 0.43fF
```

```
C654 m1_322_n153# Gnd 0.46fF
C655 m1_304_n147# Gnd 0.59fF
C656 g1 Gnd 1.40fF
C657 3and_2/w_53_n1# Gnd 0.43fF
C658 3and_2/w_0_n1# Gnd 0.83fF
C659 m1_194_n109# Gnd 0.32fF
C660 m1_276_n77# Gnd 0.18fF
C661 m1_193_n48# Gnd 0.06fF
C662 3and_1/a_13_5# Gnd 0.43fF
C663 m1_119_n93# Gnd 0.57fF
C664 m1_n49_n10# Gnd 0.45fF
C665 3and_1/w_53_n1# Gnd 0.43fF
C666 3and_1/w_0_n1# Gnd 0.83fF
C667 m1_191_n296# Gnd 0.36fF
C668 m1_271_n254# Gnd 0.23fF
C669 m1_190_n221# Gnd 0.28fF
C670 4or_0/a_0_n37# Gnd 0.54fF
C671 m1_156_n262# Gnd 0.51fF
C672 m1_169_n255# Gnd 0.37fF
C673 m1_178_n248# Gnd 0.31fF
C674 4or_0/w_n13_7# Gnd 1.39fF
C675 m1_81_n168# Gnd 0.36fF
C676 m1_89_n136# Gnd 0.14fF
C677 m1_80_n107# Gnd 0.39fF
C678 3and_0/a_13_5# Gnd 0.43fF
C679 m1_n38_n151# Gnd 0.43fF
C680 m1_n27_n143# Gnd 0.37fF
C681 m1_n15_n136# Gnd 0.29fF
C682 3and_0/w_53_n1# Gnd 0.43fF
C683 3and_0/w_0_n1# Gnd 0.83fF
```

The outputs are given below,







3. Sum block

```
* SPICE3 file created from sumblock.ext - technology: scmos

.include TSMC_180nm.txt
.param SUPPLY = 1.8
.option scale=0.09u
.global gnd vdd

VDS vdd gnd 'SUPPLY'
vin1 p3 gnd 1.8
vin2 p2 gnd 0
vin3 p1 gnd 0
vin4 p0 gnd 0
vin5 carry2 gnd 0
vin6 carry1 gnd 1.8
vin8 carry0 gnd 0
vin7 c_in gnd 1.8

M1000 xor1_0/a_24_2# p3 sum3 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1001 vdd carry2 xor1_0/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1002 gnd carry2 xor1_0/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1003 sum3 xor1_0/a_n12_n44# xor1_0/a_4_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
M1004 xor1_0/a_n12_n44# p3 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1005 gnd xor1_0/a_32_n47# xor1_0/a_24_n44# Gnd CMOSN w=4 l=2
```

```
+  ad=0 pd=0 as=32 ps=24
M1006 xor1_0/a_4_2# carry2 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1007 xor1_0/a_24_n44# xor1_0/a_n12_n44# sum3 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1008 vdd xor1_0/a_32_n47# xor1_0/a_24_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1009 sum3 p3 xor1_0/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1010 xor1_0/a_4_n44# carry2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1011 xor1_0/a_n12_n44# p3 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1012 xor1_1/a_24_2# p2 sum2 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1013 vdd carry1 xor1_1/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1014 gnd carry1 xor1_1/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1015 sum2 xor1_1/a_n12_n44# xor1_1/a_4_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
M1016 xor1_1/a_n12_n44# p2 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1017 gnd xor1_1/a_32_n47# xor1_1/a_24_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1018 xor1_1/a_4_2# carry1 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1019 xor1_1/a_24_n44# xor1_1/a_n12_n44# sum2 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1020 vdd xor1_1/a_32_n47# xor1_1/a_24_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1021 sum2 p2 xor1_1/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1022 xor1_1/a_4_n44# carry1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1023 xor1_1/a_n12_n44# p2 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1024 xor1_2/a_24_2# p1 sum1 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1025 vdd carry0 xor1_2/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1026 gnd carry0 xor1_2/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1027 sum1 xor1_2/a_n12_n44# xor1_2/a_4_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
```

```
M1028 xor1_2/a_n12_n44# p1 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1029 gnd xor1_2/a_32_n47# xor1_2/a_24_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1030 xor1_2/a_4_2# carry0 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1031 xor1_2/a_24_n44# xor1_2/a_n12_n44# sum1 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1032 vdd xor1_2/a_32_n47# xor1_2/a_24_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1033 sum1 p1 xor1_2/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1034 xor1_2/a_4_n44# carry0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1035 xor1_2/a_n12_n44# p1 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1036 xor1_3/a_24_2# p0 sum0 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1037 vdd c_in xor1_3/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1038 gnd c_in xor1_3/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1039 sum0 xor1_3/a_n12_n44# xor1_3/a_4_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
M1040 xor1_3/a_n12_n44# p0 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1041 gnd xor1_3/a_32_n47# xor1_3/a_24_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1042 xor1_3/a_4_2# c_in vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1043 xor1_3/a_24_n44# xor1_3/a_n12_n44# sum0 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1044 vdd xor1_3/a_32_n47# xor1_3/a_24_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1045 sum0 p0 xor1_3/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1046 xor1_3/a_4_n44# c_in gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1047 xor1_3/a_n12_n44# p0 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
C0 p1 vdd 0.14fF
C1 gnd xor1_2/a_n12_n44# 0.08fF
C2 sum1 p1 0.01fF
C3 xor1_3/a_32_n47# gnd 0.04fF
C4 sum2 p2 0.01fF
C5 gnd gnd 0.04fF
C6 sum2 carry1 0.10fF
```

```
C7 xor1_1/a_n12_n44# vdd 0.09fF
C8 vdd carry2 0.13fF
C9 vdd gnd 0.05fF
C10 vdd p2 0.14fF
C11 sum3 xor1_0/a_32_n47# 0.09fF
C12 vdd vdd 0.12fF
C13 xor1_2/a_32_n47# p1 0.10fF
C14 c_in p0 0.64fF
C15 vdd carry1 0.13fF
C16 sum1 vdd 0.02fF
C17 gnd carry0 0.12fF
C18 vdd p3 0.23fF
C19 sum0 c_in 0.10fF
C20 xor1_1/a_n12_n44# p2 0.08fF
C21 xor1_1/a_n12_n44# carry1 0.20fF
C22 carry2 gnd 0.12fF
C23 carry2 xor1_0/a_32_n47# 0.28fF
C24 sum3 xor1_0/a_n12_n44# 0.12fF
C25 vdd xor1_2/a_32_n47# 0.06fF
C26 carry1 p2 0.64fF
C27 xor1_2/a_32_n47# vdd 0.09fF
C28 c_in vdd 0.13fF
C29 sum1 xor1_2/a_32_n47# 0.09fF
C30 gnd p1 0.08fF
C31 vdd vdd 0.12fF
C32 gnd gnd 0.04fF
C33 xor1_1/a_32_n47# gnd 0.04fF
C34 carry2 xor1_0/a_n12_n44# 0.20fF
C35 xor1_1/a_n12_n44# vdd 0.12fF
C36 vdd p2 0.23fF
C37 c_in xor1_3/a_n12_n44# 0.20fF
C38 sum0 p0 0.01fF
C39 vdd xor1_0/a_32_n47# 0.09fF
C40 p0 vdd 0.14fF
C41 gnd xor1_2/a_32_n47# 0.04fF
C42 xor1_3/a_32_n47# c_in 0.28fF
C43 sum0 vdd 0.02fF
C44 vdd xor1_0/a_n12_n44# 0.09fF
C45 xor1_0/a_32_n47# gnd 0.04fF
C46 sum3 p3 0.01fF
C47 p0 xor1_3/a_n12_n44# 0.08fF
C48 vdd p0 0.23fF
C49 sum0 xor1_3/a_n12_n44# 0.12fF
C50 gnd xor1_0/a_n12_n44# 0.08fF
C51 c_in gnd 0.12fF
C52 carry2 p3 0.64fF
C53 sum2 xor1_1/a_32_n47# 0.09fF
C54 vdd xor1_3/a_n12_n44# 0.09fF
```

```
C55 xor1_1/a_32_n47# vdd 0.09fF
C56 vdd vdd 0.12fF
C57 xor1_3/a_32_n47# p0 0.10fF
C58 xor1_2/a_n12_n44# carry0 0.20fF
C59 gnd gnd 0.04fF
C60 sum0 xor1_3/a_32_n47# 0.09fF
C61 vdd vdd 0.12fF
C62 vdd p3 0.14fF
C63 gnd gnd 0.04fF
C64 xor1_1/a_32_n47# p2 0.10fF
C65 xor1_1/a_n12_n44# gnd 0.08fF
C66 xor1_1/a_32_n47# carry1 0.28fF
C67 vdd xor1_3/a_n12_n44# 0.12fF
C68 xor1_3/a_32_n47# vdd 0.09fF
C69 p0 gnd 0.08fF
C70 xor1_2/a_n12_n44# p1 0.08fF
C71 gnd p2 0.08fF
C72 vdd gnd 0.05fF
C73 gnd carry1 0.12fF
C74 vdd xor1_0/a_32_n47# 0.06fF
C75 gnd p3 0.08fF
C76 xor1_0/a_32_n47# p3 0.10fF
C77 vdd xor1_2/a_n12_n44# 0.12fF
C78 xor1_1/a_32_n47# vdd 0.06fF
C79 carry0 p1 0.64fF
C80 xor1_2/a_n12_n44# vdd 0.09fF
C81 sum1 xor1_2/a_n12_n44# 0.12fF
C82 vdd xor1_3/a_32_n47# 0.06fF
C83 sum3 carry2 0.10fF
C84 vdd xor1_0/a_n12_n44# 0.12fF
C85 gnd gnd 0.66fF
C86 xor1_0/a_n12_n44# p3 0.08fF
C87 xor1_3/a_n12_n44# gnd 0.08fF
C88 carry0 vdd 0.13fF
C89 sum1 carry0 0.10fF
C90 vdd gnd 0.06fF
C91 vdd gnd 0.05fF
C92 sum2 vdd 0.02fF
C93 sum3 vdd 0.02fF
C94 vdd p1 0.23fF
C95 xor1_2/a_32_n47# carry0 0.28fF
C96 sum2 xor1_1/a_n12_n44# 0.12fF
C97 gnd Gnd 0.36fF
C98 gnd Gnd 0.12fF
C99 gnd Gnd 0.54fF
C100 sum0 Gnd 0.79fF
C101 vdd Gnd 0.43fF
C102 xor1_3/a_32_n47# Gnd 0.42fF
```

```
C103 xor1_3/a_n12_n44# Gnd 0.50fF
C104 c_in Gnd 1.71fF
C105 p0 Gnd 1.65fF
C106 vdd Gnd 1.63fF
C107 gnd Gnd 0.54fF
C108 sum1 Gnd 0.79fF
C109 vdd Gnd 0.43fF
C110 xor1_2/a_32_n47# Gnd 0.42fF
C111 xor1_2/a_n12_n44# Gnd 0.50fF
C112 carry0 Gnd 1.71fF
C113 p1 Gnd 1.65fF
C114 vdd Gnd 1.63fF
C115 gnd Gnd 0.54fF
C116 sum2 Gnd 0.79fF
C117 vdd Gnd 0.43fF
C118 xor1_1/a_32_n47# Gnd 0.42fF
C119 xor1_1/a_n12_n44# Gnd 0.50fF
C120 carry1 Gnd 1.71fF
C121 p2 Gnd 1.65fF
C122 vdd Gnd 1.63fF
C123 gnd Gnd 0.54fF
C124 sum3 Gnd 0.79fF
C125 vdd Gnd 0.43fF
C126 xor1_0/a_32_n47# Gnd 0.42fF
C127 xor1_0/a_n12_n44# Gnd 0.50fF
C128 carry2 Gnd 1.71fF
C129 p3 Gnd 1.65fF
C130 vdd Gnd 1.63fF

.tran 0.01n 40n

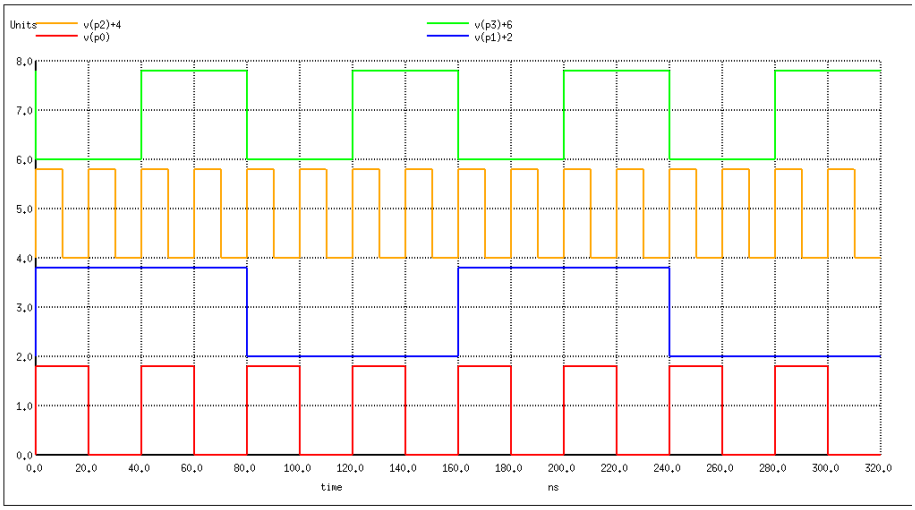
.control
run

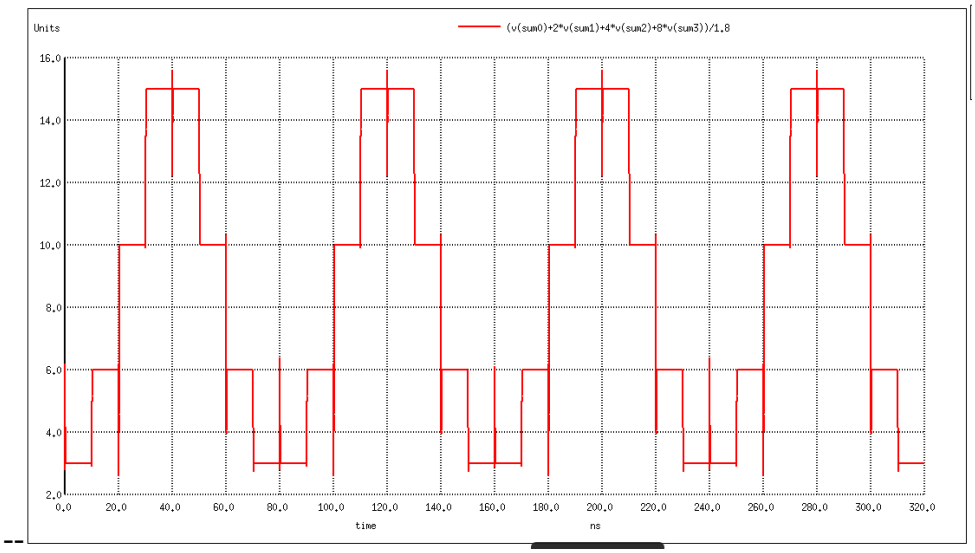
set color0 = white
set color1 = black

plot (v(sum0)+2*v(sum1)+4*v(sum2)+8*v(sum3))/1.8

.endc
```

The outputs are given below,





Question 6

The NGspice netlist for the integrated circuit is given below,

```
.include TSMC_180nm.txt
.include and2.subs
.include and3.subs
.include and4.subs
.include and5.subs
.include or2.subs
.include or3.subs
.include or4.subs
.include or5.subs
.include xor2.subs

.param Supply=1.8
```

```
.param LAMBDA=0.09u
.param width_N=10*LAMBDA
.param width_P=20*LAMBDA
.global vdd gnd

VDS vdd gnd Supply

.param logic1 = Supply
.param logic0 = 0

* A = a3a2a1a0
VA0 a0 gnd pulse logic0 logic1 0ns 100ps 100ps 39.9ns 80ns
VA1 a1 gnd pulse logic1 logic0 0ns 100ps 100ps 9.9ns 20ns
VA2 a2 gnd pulse logic1 logic0 0ns 100ps 100ps 19.9ns 40ns
VA3 a3 gnd pulse logic0 logic1 0ns 100ps 100ps 19.9ns 40ns

* B = b3b2b1b0
VB0 b0 gnd pulse logic1 logic0 0ns 100ps 100ps 39.9ns 80ns
VB1 b1 gnd pulse logic0 logic1 0ns 100ps 100ps 19.9ns 40ns
VB2 b2 gnd pulse logic0 logic1 0ns 100ps 100ps 9.9ns 20ns
VB3 b3 gnd pulse logic1 logic0 0ns 100ps 100ps 9.9ns 20ns

VC0 Cin gnd pulse logic1 logic0 0ns 100ps 100ps 19.9ns 40ns

xxPROP0 p0 a0 b0 xor2
xxPROP1 p1 a1 b1 xor2
xxPROP2 p2 a2 b2 xor2
xxPROP3 p3 a3 b3 xor2

xxGEN0 g0 a0 b0 and2
xxGEN1 g1 a1 b1 and2
xxGEN2 g2 a2 b2 and2
xxGEN3 g3 a3 b3 and2

xxANDcalc0 temp0 Cin p0 and2
xxORcalc0 c0 temp0 g0 or2

xxANDcalc11 temp11 Cin p0 p1 and3
xxANDcalc12 temp12 g0 p1 and2
xxORcalc1 c1 temp12 temp11 g1 or3

xxANDcalc21 temp21 Cin p0 p1 p2 and4
xxANDcalc22 temp22 g0 p1 p2 and3
xxANDcalc23 temp23 g1 p2 and2
xxORcalc2 c2 temp23 temp22 temp21 g2 or4

xxANDcalc31 temp31 Cin p0 p1 p2 p3 and5
xxANDcalc32 temp32 g0 p1 p2 p3 and4
```

```
xxANDcalc33 temp33 g1 p2 p3 and3
xxANDcalc34 temp34 g2 p3 and2
xxOR3 c3 temp34 temp33 temp32 temp31 g3 or5

xxSUM0 sum0 p0 Cin xor2
xxSUM1 sum1 p1 c0 xor2
xxSUM2 sum2 p2 c1 xor2
xxSUM3 sum3 p3 c2 xor2

.tran 0.05n 160n

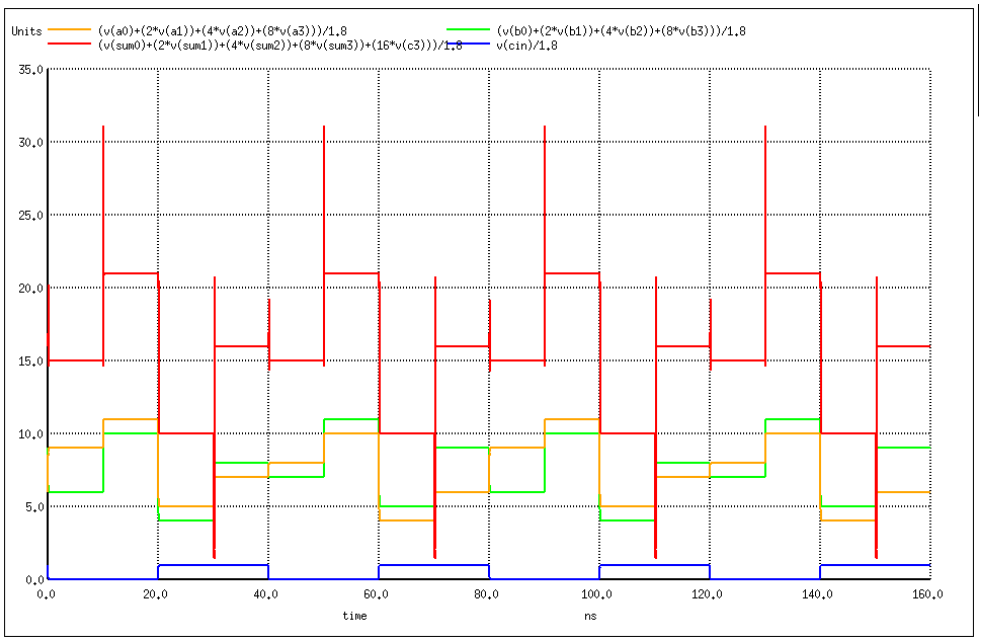
.control
run

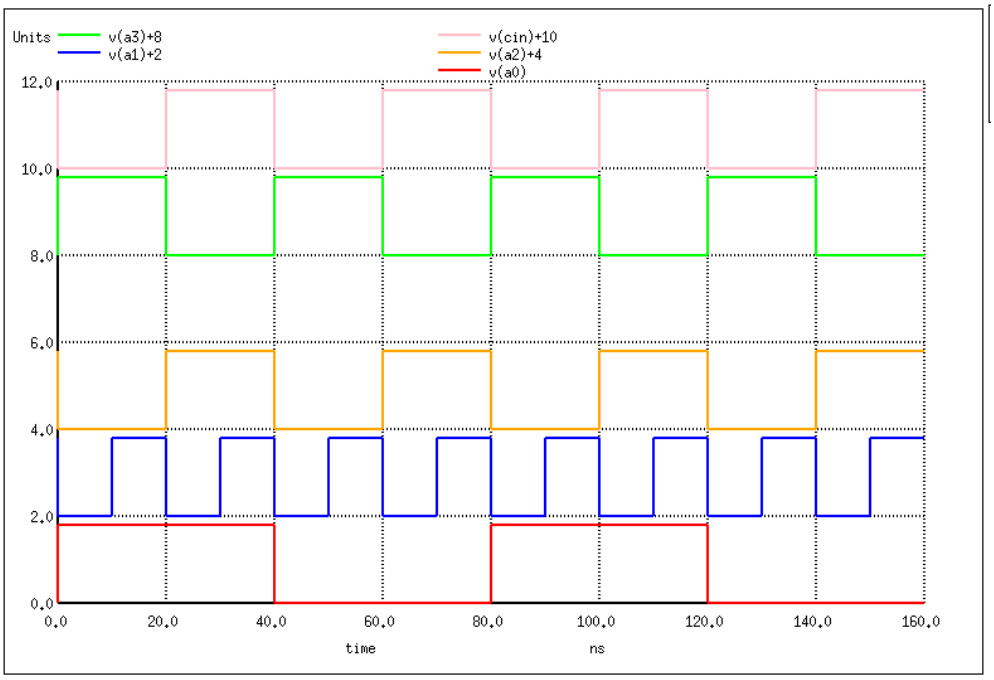
set color0 = white
set color1 = black
plot (v(sum0)+(2*v(sum1))+(4*v(sum2))+(8*v(sum3))+(16*v(c3)))/1.8 v(Cin)/1.8
(v(a0)+(2*v(a1))+(4*v(a2))+(8*v(a3)))/1.8
(v(b0)+(2*v(b1))+(4*v(b2))+(8*v(b3)))/1.8

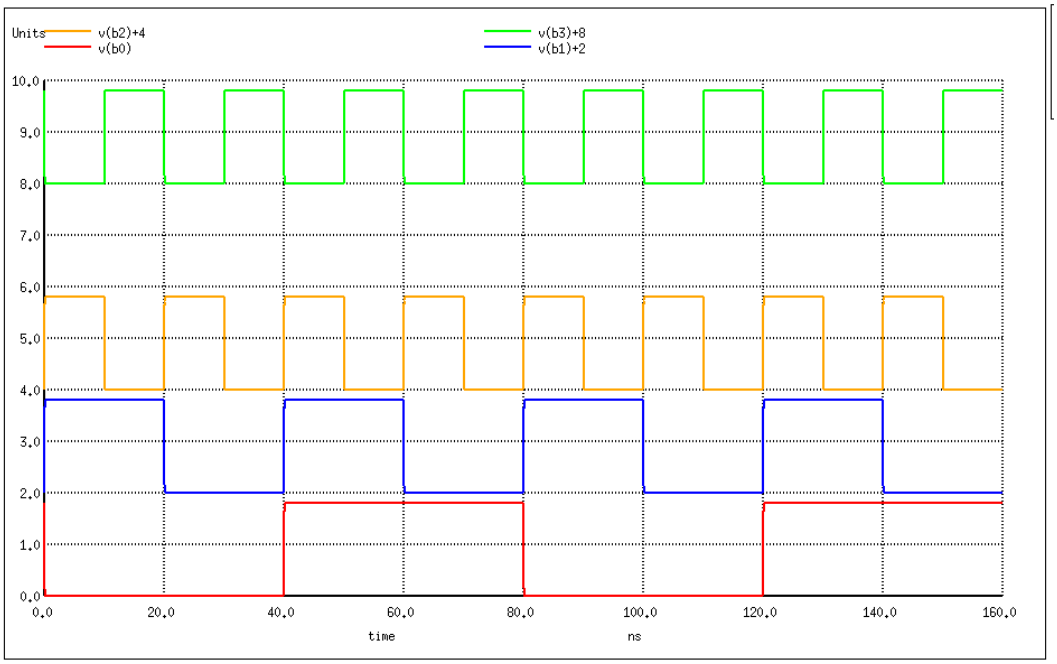
plot v(sum0) v(sum1)+2 v(sum2)+4 v(sum3)+8 v(c3)
plot v(a0) v(a1)+2 v(a2)+4 v(a3)+8 v(Cin)+10
plot v(b0) v(b1)+2 v(b2)+4 v(b3)+8

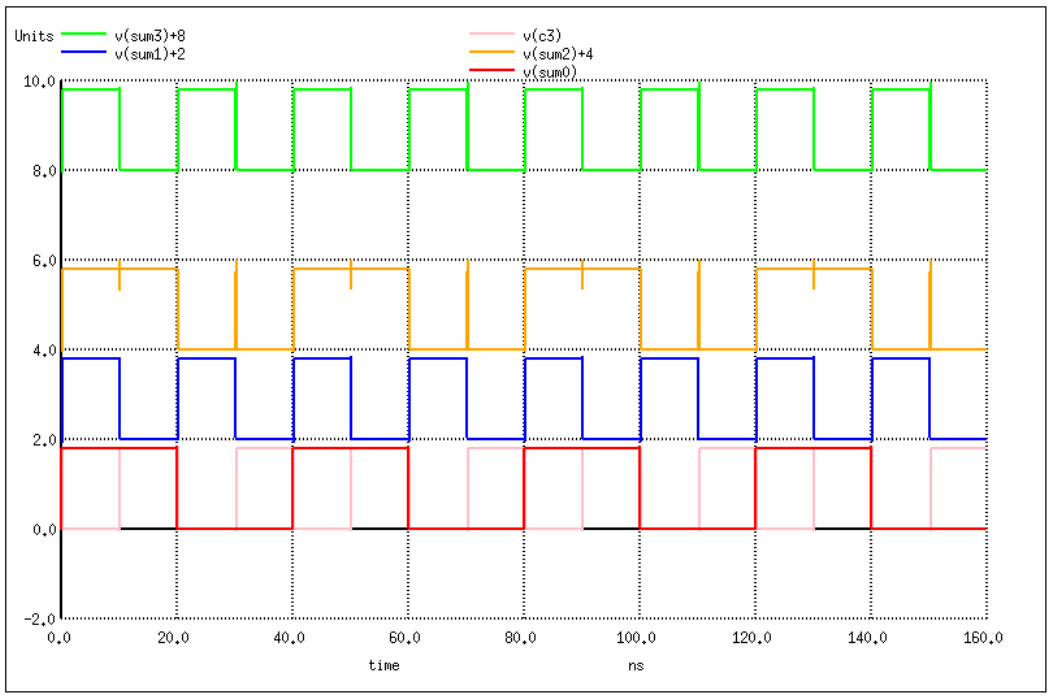
set curplottitle = "Jewel Benny, 2020102057"
.endc
.end
```

The outputs of the above netlist are given below,







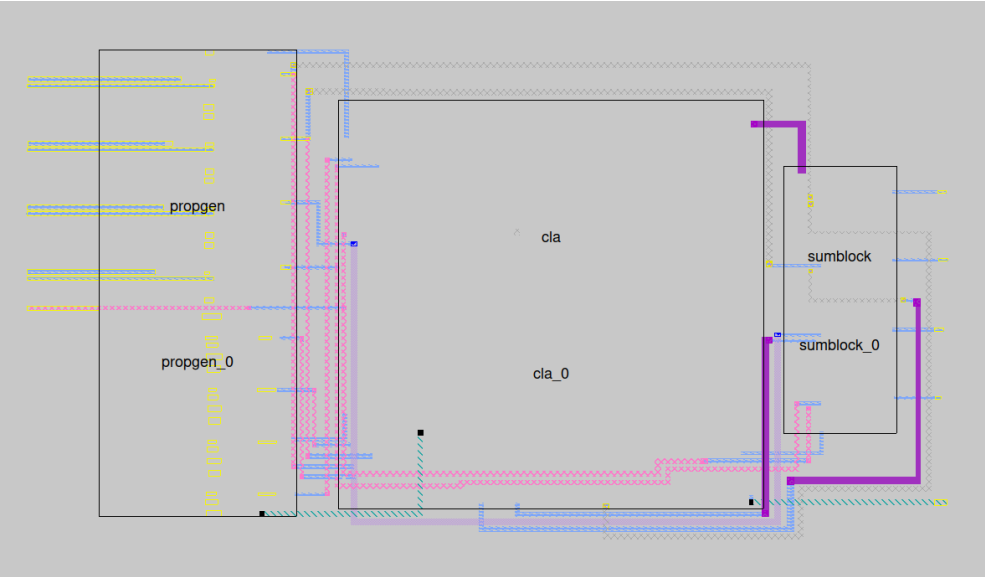


Question 7

The spacing details and floor plans of the blocks and the overall circuit are given below,

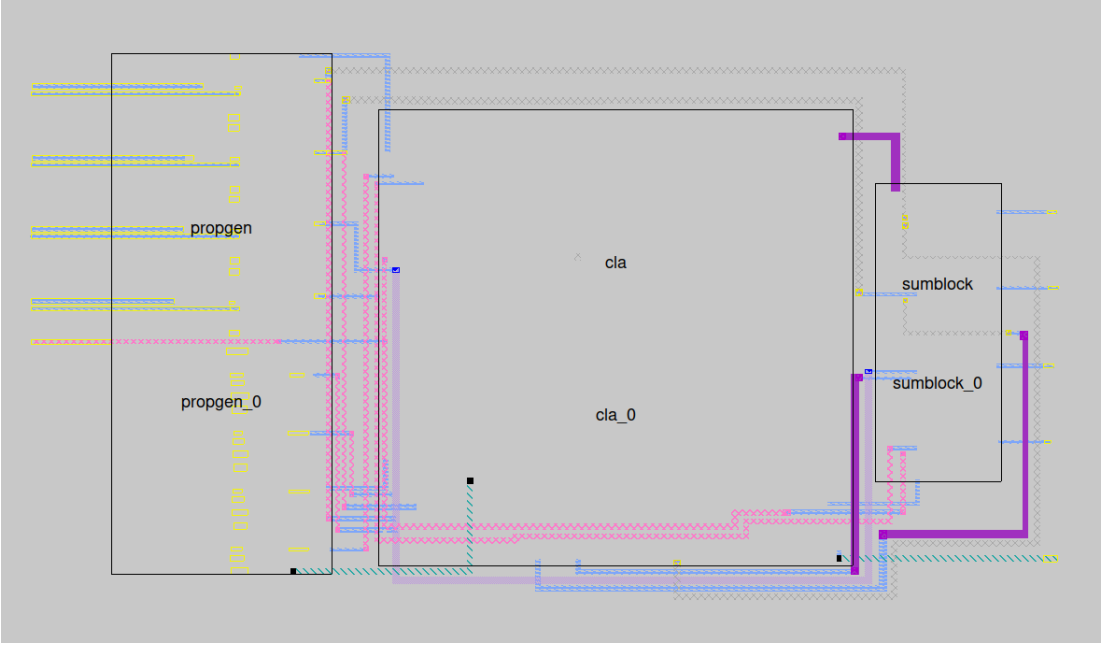
- Propagate and generate block – 284 λ $*$ 670 λ
- CLA block - 611 λ $*$ 587 λ
- Sum block - 162 λ $*$ 383 λ

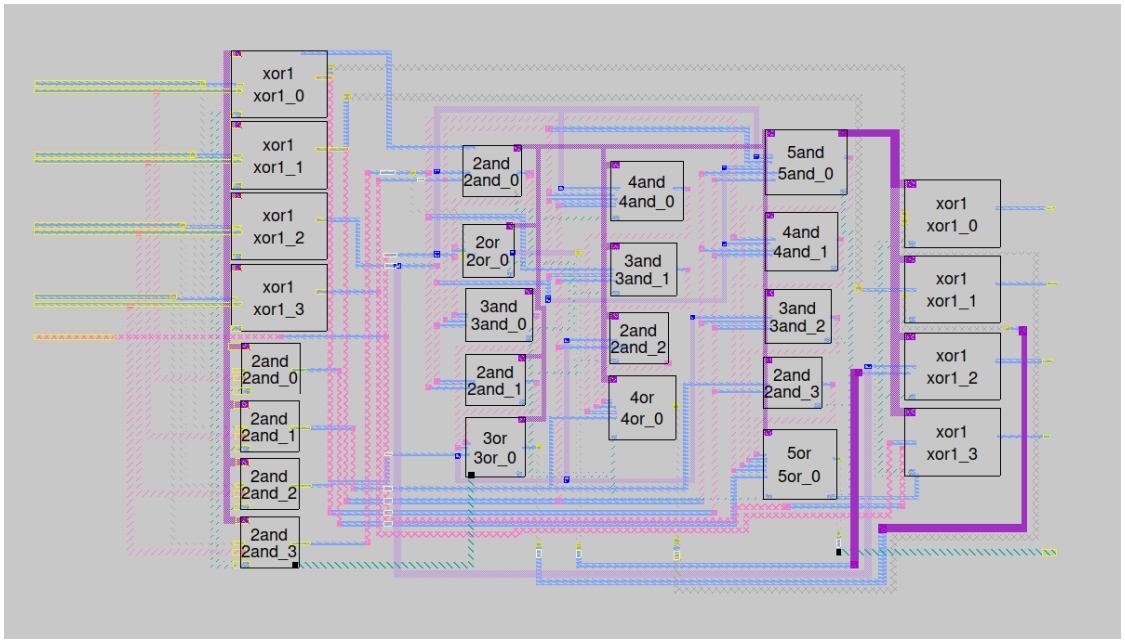
- Overall circuit - 1184 $\lambda * 688\ \lambda$

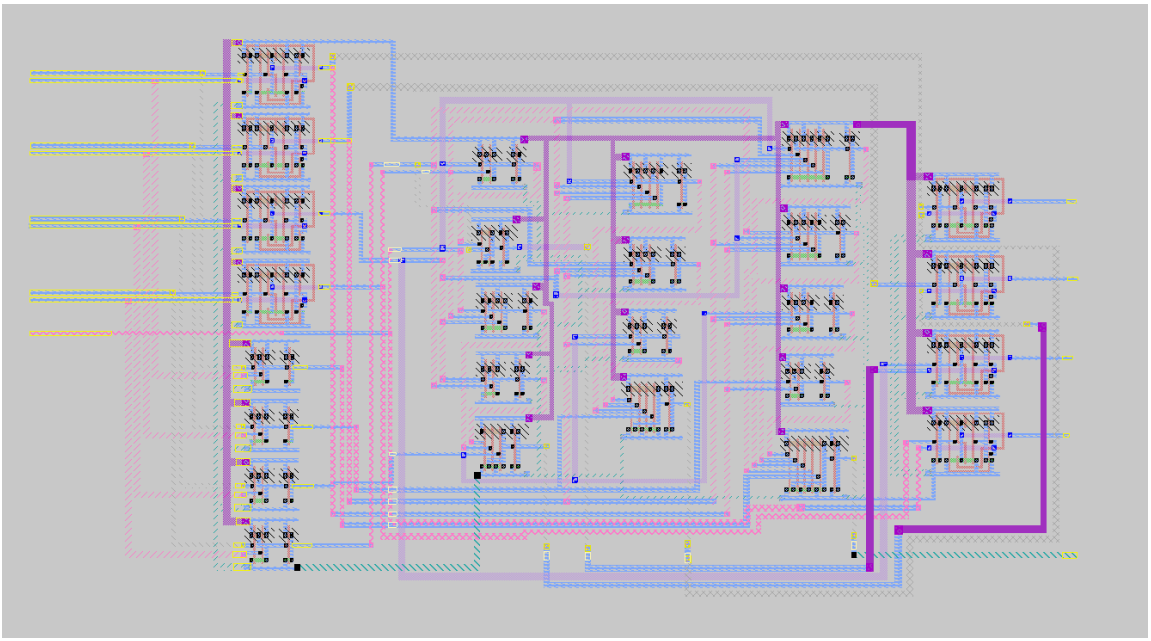


Question 8

The MAGIC layout of the complete circuit is given below,







The SPICE netlist of the above circuit is given below,

```
* SPICE3 file created from cla_adder.ext - technology: scmos

* SPICE3 file created from 5or.ext - technology: scmos

.include TSMC_180nm.txt
.param SUPPLY = 1.8
.option scale=0.09u
```

```
.global gnd vdd

VDS vdd gnd 'SUPPLY'
vin1 a3 gnd pulse 1.8 0 0ns 100ps 100ps 39.9ns 80ns
vin2 a2 gnd pulse 0 1.8 0ns 100ps 100ps 9.9ns 20ns
vin3 a1 gnd pulse 0 1.8 0ns 100ps 100ps 79.9ns 160ns
vin4 a0 gnd pulse 0 1.8 0ns 100ps 100ps 19.9ns 40ns
vin5 b3 gnd pulse 1.8 0 0ns 100ps 100ps 19.9ns 40ns
vin6 b2 gnd pulse 0 1.8 0ns 100ps 100ps 39.9ns 80ns
vin7 b1 gnd pulse 1.8 0 0ns 100ps 100ps 79.9ns 160ns
vin8 b0 gnd pulse 0 1.8 0ns 100ps 100ps 9.9ns 20ns
vin9 c_in gnd pulse 1.8 0 0ns 100ps 100ps 9.9ns 20ns

*vin1 a3 gnd 0
*vin2 a2 gnd 0
*vin3 a1 gnd 0
*vin4 a0 gnd 0
*vin5 b3 gnd 0
*vin6 b2 gnd 0
*vin7 b1 gnd 0
*vin8 b0 gnd 0
*vin9 c_in gnd 0

M1000 cla_0/3and_0/a_13_5# p1 vdd vdd CMOSP w=6 l=2
+  ad=84 pd=52 as=108 ps=72
M1001 cla_0/3and_0/a_13_n28# c_in gnd Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=40 ps=36
M1002 t2_3and cla_0/3and_0/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1003 vdd p0 cla_0/3and_0/a_13_5# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 t2_3and cla_0/3and_0/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1005 cla_0/3and_0/a_13_5# c_in vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1006 cla_0/3and_0/a_13_5# p1 cla_0/3and_0/a_23_n28# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1007 cla_0/3and_0/a_23_n28# p0 cla_0/3and_0/a_13_n28# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1008 cla_0/4or_0/a_0_n37# t3_3and gnd Gnd CMOSN w=4 l=2
+  ad=64 pd=48 as=92 ps=78
M1009 cla_0/4or_0/a_0_n37# t3_4and gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1010 carry2 cla_0/4or_0/a_0_n37# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1011 cla_0/4or_0/a_19_13# t3_3and cla_0/4or_0/a_10_13# vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=42 ps=26
```

```
M1012 gnd t3_2and cla_0/4or_0/a_0_n37# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1013 carry2 cla_0/4or_0/a_0_n37# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=60 ps=44
M1014 cla_0/4or_0/a_0_13# t3_4and vdd vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=0 ps=0
M1015 cla_0/4or_0/a_0_n37# g2 cla_0/4or_0/a_19_13# vdd CMOSP w=6 l=2
+  ad=36 pd=24 as=0 ps=0
M1016 cla_0/4or_0/a_10_13# t3_2and cla_0/4or_0/a_0_13# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1017 gnd g2 cla_0/4or_0/a_0_n37# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0

M1018 cla_0/3and_1/a_13_5# p2 vdd vdd CMOSP w=6 l=2
+  ad=84 pd=52 as=108 ps=72
M1019 cla_0/3and_1/a_13_n28# g0 gnd Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=40 ps=36
M1020 t3_3and cla_0/3and_1/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1021 vdd p1 cla_0/3and_1/a_13_5# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1022 t3_3and cla_0/3and_1/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1023 cla_0/3and_1/a_13_5# g0 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1024 cla_0/3and_1/a_13_5# p2 cla_0/3and_1/a_23_n28# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1025 cla_0/3and_1/a_23_n28# p1 cla_0/3and_1/a_13_n28# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1026 cla_0/3and_2/a_13_5# p3 vdd vdd CMOSP w=6 l=2
+  ad=84 pd=52 as=108 ps=72
M1027 cla_0/3and_2/a_13_n28# g1 gnd Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=40 ps=36
M1028 t4_3and cla_0/3and_2/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1029 vdd p2 cla_0/3and_2/a_13_5# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1030 t4_3and cla_0/3and_2/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1031 cla_0/3and_2/a_13_5# g1 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1032 cla_0/3and_2/a_13_5# p3 cla_0/3and_2/a_23_n28# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1033 cla_0/3and_2/a_23_n28# p2 cla_0/3and_2/a_13_n28# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
```

```
M1034 vdd p0 cla_0/2and_0/a_13_5# vdd CMOSP w=6 l=2
+  ad=216 pd=156 as=48 ps=28
M1035 t1_2and cla_0/2and_0/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1036 cla_0/2and_0/a_13_5# c_in vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1037 t1_2and cla_0/2and_0/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1038 cla_0/2and_0/a_13_5# p0 cla_0/2and_0/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1039 cla_0/2and_0/a_13_n25# c_in gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1040 vdd p1 cla_0/2and_1/a_13_5# vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1041 t2_2and cla_0/2and_1/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1042 cla_0/2and_1/a_13_5# g0 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1043 t2_2and cla_0/2and_1/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1044 cla_0/2and_1/a_13_5# p1 cla_0/2and_1/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1045 cla_0/2and_1/a_13_n25# g0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1046 vdd p2 cla_0/2and_2/a_13_5# vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1047 t3_2and cla_0/2and_2/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1048 cla_0/2and_2/a_13_5# g1 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1049 t3_2and cla_0/2and_2/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1050 cla_0/2and_2/a_13_5# p2 cla_0/2and_2/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1051 cla_0/2and_2/a_13_n25# g1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1052 vdd p3 cla_0/2and_3/a_13_5# vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1053 t4_2and cla_0/2and_3/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1054 cla_0/2and_3/a_13_5# g2 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1055 t4_2and cla_0/2and_3/a_13_5# vdd vdd CMOSP w=6 l=2
```

```
+  ad=30 pd=22 as=0 ps=0
M1056 cla_0/2and_3/a_13_5# p3 cla_0/2and_3/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1057 cla_0/2and_3/a_13_n25# g2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1058 carry3 cla_0/5or_0/a_0_n44# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=60 ps=44
M1059 gnd t4_2and cla_0/5or_0/a_0_n44# Gnd CMOSN w=4 l=2
+  ad=180 pd=154 as=88 ps=68
M1060 carry3 cla_0/5or_0/a_0_n44# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1061 cla_0/5or_0/a_0_n44# t4_3and gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1062 cla_0/5or_0/a_0_n44# t4_5and gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1063 cla_0/5or_0/a_19_13# t4_3and cla_0/5or_0/a_10_13# vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=42 ps=26
M1064 cla_0/5or_0/a_0_13# t4_5and vdd vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=0 ps=0
M1065 cla_0/5or_0/a_29_13# t4_2and cla_0/5or_0/a_19_13# vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=0 ps=0
M1066 gnd t4_4and cla_0/5or_0/a_0_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1067 cla_0/5or_0/a_10_13# t4_4and cla_0/5or_0/a_0_13# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1068 cla_0/5or_0/a_0_n44# g3 cla_0/5or_0/a_29_13# vdd CMOSP w=6 l=2
+  ad=36 pd=24 as=0 ps=0
M1069 cla_0/5or_0/a_0_n44# g3 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1070 carry0 cla_0/2or_0/a_0_n30# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=60 ps=44
M1071 gnd t1_2and cla_0/2or_0/a_0_n30# Gnd CMOSN w=4 l=2
+  ad=60 pd=54 as=32 ps=24
M1072 cla_0/2or_0/a_0_n30# t1_2and cla_0/2or_0/a_0_6# vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=48 ps=28
M1073 carry0 cla_0/2or_0/a_0_n30# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1074 cla_0/2or_0/a_0_6# g0 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1075 cla_0/2or_0/a_0_n30# g0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1076 t4_5and cla_0/5and_0/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=156 ps=100
```

```
M1077 cla_0/5and_0/a_13_5# p1 vdd vdd CMOSP w=6 l=2
+  ad=132 pd=80 as=0 ps=0
M1078 cla_0/5and_0/a_43_n43# p2 cla_0/5and_0/a_33_n43# Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1079 cla_0/5and_0/a_33_n43# p1 cla_0/5and_0/a_23_n43# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1080 vdd p0 cla_0/5and_0/a_13_5# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1081 cla_0/5and_0/a_23_n43# p0 cla_0/5and_0/a_13_n43# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1082 t4_5and cla_0/5and_0/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1083 cla_0/5and_0/a_13_n43# c_in gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1084 cla_0/5and_0/a_13_5# p3 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1085 cla_0/5and_0/a_13_5# c_in vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1086 vdd p2 cla_0/5and_0/a_13_5# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1087 cla_0/5and_0/a_13_5# p3 cla_0/5and_0/a_43_n43# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=0 ps=0


M1088 carry1 cla_0/3or_0/a_0_n30# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=60 ps=44
M1089 gnd t2_2and cla_0/3or_0/a_0_n30# Gnd CMOSN w=4 l=2
+  ad=68 pd=58 as=56 ps=44
M1090 carry1 cla_0/3or_0/a_0_n30# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1091 cla_0/3or_0/a_0_n30# g1 cla_0/3or_0/a_10_13# vdd CMOSP w=6 l=2
+  ad=36 pd=24 as=42 ps=26
M1092 cla_0/3or_0/a_0_13# t2_3and vdd vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=0 ps=0
M1093 cla_0/3or_0/a_10_13# t2_2and cla_0/3or_0/a_0_13# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1094 cla_0/3or_0/a_0_n30# g1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1095 cla_0/3or_0/a_0_n30# t2_3and gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1096 cla_0/4and_0/a_33_n36# p1 cla_0/4and_0/a_23_n36# Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1097 cla_0/4and_0/a_13_5# p1 vdd vdd CMOSP w=6 l=2
+  ad=96 pd=56 as=144 ps=96
M1098 cla_0/4and_0/a_23_n36# p0 cla_0/4and_0/a_13_n36# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1099 cla_0/4and_0/a_13_n36# c_in gnd Gnd CMOSN w=4 l=2
```

```
+  ad=0 pd=0 as=40 ps=36
M1100 vdd p0 cla_0/4and_0/a_13_5# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1101 cla_0/4and_0/a_13_5# c_in vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1102 t3_4and cla_0/4and_0/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1103 t3_4and cla_0/4and_0/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1104 vdd p2 cla_0/4and_0/a_13_5# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1105 cla_0/4and_0/a_13_5# p2 cla_0/4and_0/a_33_n36# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=0 ps=0


M1106 cla_0/4and_1/a_33_n36# p2 cla_0/4and_1/a_23_n36# Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1107 cla_0/4and_1/a_13_5# p2 vdd vdd CMOSP w=6 l=2
+  ad=96 pd=56 as=144 ps=96
M1108 cla_0/4and_1/a_23_n36# p1 cla_0/4and_1/a_13_n36# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1109 cla_0/4and_1/a_13_n36# g0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=40 ps=36
M1110 vdd p1 cla_0/4and_1/a_13_5# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1111 cla_0/4and_1/a_13_5# g0 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1112 t4_4and cla_0/4and_1/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1113 t4_4and cla_0/4and_1/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1114 vdd p3 cla_0/4and_1/a_13_5# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1115 cla_0/4and_1/a_13_5# p3 cla_0/4and_1/a_33_n36# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=0 ps=0


M1116 sumblock_0/xor1_0/a_24_2# p3 sum3 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1117 vdd carry2 sumblock_0/xor1_0/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1118 gnd carry2 sumblock_0/xor1_0/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1119 sum3 sumblock_0/xor1_0/a_n12_n44# sumblock_0/xor1_0/a_4_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=48 ps=28
M1120 sumblock_0/xor1_0/a_n12_n44# p3 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
```

```
M1121 gnd sumblock_0/xor1_0/a_32_n47# sumblock_0/xor1_0/a_24_n44# Gnd CMOSN
w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1122 sumblock_0/xor1_0/a_4_2# carry2 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1123 sumblock_0/xor1_0/a_24_n44# sumblock_0/xor1_0/a_n12_n44# sum3 Gnd CMOSN
w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1124 vdd sumblock_0/xor1_0/a_32_n47# sumblock_0/xor1_0/a_24_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=0 ps=0
M1125 sum3 p3 sumblock_0/xor1_0/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1126 sumblock_0/xor1_0/a_4_n44# carry2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1127 sumblock_0/xor1_0/a_n12_n44# p3 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0

M1128 sumblock_0/xor1_1/a_24_2# p2 sum2 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1129 vdd carry1 sumblock_0/xor1_1/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1130 gnd carry1 sumblock_0/xor1_1/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1131 sum2 sumblock_0/xor1_1/a_n12_n44# sumblock_0/xor1_1/a_4_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=48 ps=28
M1132 sumblock_0/xor1_1/a_n12_n44# p2 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1133 gnd sumblock_0/xor1_1/a_32_n47# sumblock_0/xor1_1/a_24_n44# Gnd CMOSN
w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1134 sumblock_0/xor1_1/a_4_2# carry1 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1135 sumblock_0/xor1_1/a_24_n44# sumblock_0/xor1_1/a_n12_n44# sum2 Gnd CMOSN
w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1136 vdd sumblock_0/xor1_1/a_32_n47# sumblock_0/xor1_1/a_24_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=0 ps=0
M1137 sum2 p2 sumblock_0/xor1_1/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1138 sumblock_0/xor1_1/a_4_n44# carry1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1139 sumblock_0/xor1_1/a_n12_n44# p2 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1140 sumblock_0/xor1_2/a_24_2# p1 sum1 vdd CMOSP w=6 l=2
```

```
+  ad=48 pd=28 as=48 ps=28
M1141 vdd carry0 sumblock_0/xor1_2/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1142 gnd carry0 sumblock_0/xor1_2/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1143 sum1 sumblock_0/xor1_2/a_n12_n44# sumblock_0/xor1_2/a_4_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=48 ps=28
M1144 sumblock_0/xor1_2/a_n12_n44# p1 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1145 gnd sumblock_0/xor1_2/a_32_n47# sumblock_0/xor1_2/a_24_n44# Gnd CMOSN
w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1146 sumblock_0/xor1_2/a_4_2# carry0 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1147 sumblock_0/xor1_2/a_24_n44# sumblock_0/xor1_2/a_n12_n44# sum1 Gnd CMOSN
w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1148 vdd sumblock_0/xor1_2/a_32_n47# sumblock_0/xor1_2/a_24_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=0 ps=0
M1149 sum1 p1 sumblock_0/xor1_2/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1150 sumblock_0/xor1_2/a_4_n44# carry0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1151 sumblock_0/xor1_2/a_n12_n44# p1 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1152 sumblock_0/xor1_3/a_24_2# p0 sum0 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1153 vdd c_in sumblock_0/xor1_3/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1154 gnd c_in sumblock_0/xor1_3/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1155 sum0 sumblock_0/xor1_3/a_n12_n44# sumblock_0/xor1_3/a_4_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=48 ps=28
M1156 sumblock_0/xor1_3/a_n12_n44# p0 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1157 gnd sumblock_0/xor1_3/a_32_n47# sumblock_0/xor1_3/a_24_n44# Gnd CMOSN
w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1158 sumblock_0/xor1_3/a_4_2# c_in vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1159 sumblock_0/xor1_3/a_24_n44# sumblock_0/xor1_3/a_n12_n44# sum0 Gnd CMOSN
w=4 l=2
+  ad=0 pd=0 as=32 ps=24
```

```
M1160 vdd sumblock_0/xor1_3/a_32_n47# sumblock_0/xor1_3/a_24_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=0 ps=0
M1161 sum0 p0 sumblock_0/xor1_3/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1162 sumblock_0/xor1_3/a_4_n44# c_in gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1163 sumblock_0/xor1_3/a_n12_n44# p0 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1164 vdd b3 propgen_0/2and_0/a_13_5# vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1165 g3 propgen_0/2and_0/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1166 propgen_0/2and_0/a_13_5# a3 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1167 g3 propgen_0/2and_0/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1168 propgen_0/2and_0/a_13_5# b3 propgen_0/2and_0/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1169 propgen_0/2and_0/a_13_n25# a3 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1170 vdd b2 propgen_0/2and_1/a_13_5# vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1171 g2 propgen_0/2and_1/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1172 propgen_0/2and_1/a_13_5# a2 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1173 g2 propgen_0/2and_1/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1174 propgen_0/2and_1/a_13_5# b2 propgen_0/2and_1/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1175 propgen_0/2and_1/a_13_n25# a2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1176 vdd b1 propgen_0/2and_2/a_13_5# vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1177 g1 propgen_0/2and_2/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1178 propgen_0/2and_2/a_13_5# a1 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1179 g1 propgen_0/2and_2/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1180 propgen_0/2and_2/a_13_5# b1 propgen_0/2and_2/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
```

```
M1181 propgen_0/2and_2/a_13_n25# a1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1182 vdd b0 propgen_0/2and_3/a_13_5# vdd CMOSP w=6 l=2
+  ad=96 pd=68 as=48 ps=28
M1183 g0 propgen_0/2and_3/a_13_5# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=40 ps=36
M1184 propgen_0/2and_3/a_13_5# a0 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1185 g0 propgen_0/2and_3/a_13_5# vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0
M1186 propgen_0/2and_3/a_13_5# b0 propgen_0/2and_3/a_13_n25# Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=32 ps=24
M1187 propgen_0/2and_3/a_13_n25# a0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0


M1188 propgen_0/xor1_0/a_24_2# a3 p3 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1189 vdd b3 propgen_0/xor1_0/a_32_n47# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=30 ps=22
M1190 gnd b3 propgen_0/xor1_0/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1191 p3 propgen_0/xor1_0/a_n12_n44# propgen_0/xor1_0/a_4_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
M1192 propgen_0/xor1_0/a_n12_n44# a3 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1193 gnd propgen_0/xor1_0/a_32_n47# propgen_0/xor1_0/a_24_n44# Gnd CMOSN w=4
l=2
+  ad=0 pd=0 as=32 ps=24
M1194 propgen_0/xor1_0/a_4_2# b3 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1195 propgen_0/xor1_0/a_24_n44# propgen_0/xor1_0/a_n12_n44# p3 Gnd CMOSN w=4
l=2
+  ad=0 pd=0 as=32 ps=24
M1196 vdd propgen_0/xor1_0/a_32_n47# propgen_0/xor1_0/a_24_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=0 ps=0
M1197 p3 a3 propgen_0/xor1_0/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1198 propgen_0/xor1_0/a_4_n44# b3 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1199 propgen_0/xor1_0/a_n12_n44# a3 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1200 propgen_0/xor1_1/a_24_2# a2 p2 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
```

```
M1201 vdd b2 propgen_0/xor1_1/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1202 gnd b2 propgen_0/xor1_1/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1203 p2 propgen_0/xor1_1/a_n12_n44# propgen_0/xor1_1/a_4_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
M1204 propgen_0/xor1_1/a_n12_n44# a2 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1205 gnd propgen_0/xor1_1/a_32_n47# propgen_0/xor1_1/a_24_n44# Gnd CMOSN w=4
l=2
+  ad=0 pd=0 as=32 ps=24
M1206 propgen_0/xor1_1/a_4_2# b2 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1207 propgen_0/xor1_1/a_24_n44# propgen_0/xor1_1/a_n12_n44# p2 Gnd CMOSN w=4
l=2
+  ad=0 pd=0 as=32 ps=24
M1208 vdd propgen_0/xor1_1/a_32_n47# propgen_0/xor1_1/a_24_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=0 ps=0
M1209 p2 a2 propgen_0/xor1_1/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1210 propgen_0/xor1_1/a_4_n44# b2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1211 propgen_0/xor1_1/a_n12_n44# a2 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1212 propgen_0/xor1_2/a_24_2# a1 p1 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1213 vdd b1 propgen_0/xor1_2/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1214 gnd b1 propgen_0/xor1_2/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1215 p1 propgen_0/xor1_2/a_n12_n44# propgen_0/xor1_2/a_4_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
M1216 propgen_0/xor1_2/a_n12_n44# a1 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1217 gnd propgen_0/xor1_2/a_32_n47# propgen_0/xor1_2/a_24_n44# Gnd CMOSN w=4
l=2
+  ad=0 pd=0 as=32 ps=24
M1218 propgen_0/xor1_2/a_4_2# b1 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1219 propgen_0/xor1_2/a_24_n44# propgen_0/xor1_2/a_n12_n44# p1 Gnd CMOSN w=4
l=2
+  ad=0 pd=0 as=32 ps=24
M1220 vdd propgen_0/xor1_2/a_32_n47# propgen_0/xor1_2/a_24_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=0 ps=0
M1221 p1 a1 propgen_0/xor1_2/a_4_n44# Gnd CMOSN w=4 l=2
```

```
+  ad=0 pd=0 as=32 ps=24
M1222 propgen_0/xor1_2/a_4_n44# b1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1223 propgen_0/xor1_2/a_n12_n44# a1 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


M1224 propgen_0/xor1_3/a_24_2# a0 p0 vdd CMOSP w=6 l=2
+  ad=48 pd=28 as=48 ps=28
M1225 vdd b0 propgen_0/xor1_3/a_32_n47# vdd CMOSP w=6 l=2
+  ad=120 pd=88 as=30 ps=22
M1226 gnd b0 propgen_0/xor1_3/a_32_n47# Gnd CMOSN w=4 l=2
+  ad=80 pd=72 as=20 ps=18
M1227 p0 propgen_0/xor1_3/a_n12_n44# propgen_0/xor1_3/a_4_2# vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=48 ps=28
M1228 propgen_0/xor1_3/a_n12_n44# a0 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1229 gnd propgen_0/xor1_3/a_32_n47# propgen_0/xor1_3/a_24_n44# Gnd CMOSN w=4
l=2
+  ad=0 pd=0 as=32 ps=24
M1230 propgen_0/xor1_3/a_4_2# b0 vdd vdd CMOSP w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1231 propgen_0/xor1_3/a_24_n44# propgen_0/xor1_3/a_n12_n44# p0 Gnd CMOSN w=4
l=2
+  ad=0 pd=0 as=32 ps=24
M1232 vdd propgen_0/xor1_3/a_32_n47# propgen_0/xor1_3/a_24_2# vdd CMOSP w=6
l=2
+  ad=0 pd=0 as=0 ps=0
M1233 p0 a0 propgen_0/xor1_3/a_4_n44# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1234 propgen_0/xor1_3/a_4_n44# b0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1235 propgen_0/xor1_3/a_n12_n44# a0 vdd vdd CMOSP w=6 l=2
+  ad=30 pd=22 as=0 ps=0


C0 g2 gnd 0.06fF
C1 g0 vdd 0.44fF
C2 vdd cla_0/3and_0/a_13_5# 0.05fF
C3 vdd p2 0.07fF
C4 vdd vdd 0.03fF
C5 g2 gnd 0.05fF
C6 gnd g0 0.12fF
C7 c_in gnd 0.06fF
C8 a1 gnd 0.01fF
C9 sumblock_0/xor1_1/a_32_n47# sum2 0.09fF
C10 vdd gnd 0.02fF
C11 vdd p3 0.08fF
C12 gnd gnd 0.20fF
```

```
C13 propgen_0/xor1_3/a_32_n47# vdd 0.06fF
C14 b0 p0 0.10fF
C15 carry0 gnd 0.12fF
C16 vdd vdd 0.03fF
C17 a3 gnd 0.08fF
C18 propgen_0/xor1_0/a_n12_n44# p3 0.12fF
C19 gnd gnd 0.16fF
C20 p0 gnd 0.07fF
C21 p1 gnd 0.07fF
C22 a2 gnd 0.05fF
C23 gnd gnd 0.59fF
C24 p0 gnd 0.01fF
C25 g1 gnd 0.06fF
C26 vdd sumblock_0/xor1_3/a_32_n47# 0.06fF
C27 g3 gnd 0.05fF
C28 gnd gnd 0.09fF
C29 vdd sum1 0.03fF
C30 c_in gnd 0.08fF
C31 gnd gnd 0.05fF
C32 vdd a3 0.14fF
C33 g2 gnd 0.06fF
C34 gnd gnd 0.93fF
C35 b0 gnd 0.09fF
C36 b1 gnd 0.07fF
C37 propgen_0/2and_3/a_13_5# b0 0.17fF
C38 propgen_0/xor1_2/a_32_n47# gnd 0.04fF
C39 gnd b3 0.03fF
C40 vdd p3 0.03fF
C41 p2 gnd 0.05fF
C42 cla_0/3and_1/a_13_5# t3_3and 0.05fF
C43 vdd gnd 0.05fF
C44 gnd gnd 0.37fF
C45 gnd gnd 0.07fF
C46 vdd gnd 0.48fF
C47 vdd vdd 0.03fF
C48 p2 p0 0.08fF
C49 p3 gnd 0.03fF
C50 vdd gnd 0.02fF
C51 p1 cla_0/2and_1/a_13_5# 0.17fF
C52 vdd t2_2and 0.03fF
C53 sumblock_0/xor1_0/a_32_n47# vdd 0.06fF
C54 sum0 gnd 0.06fF
C55 g1 cla_0/2and_2/a_13_5# 0.04fF
C56 gnd p2 0.07fF
C57 gnd gnd 0.16fF
C58 vdd gnd 0.06fF
C59 sumblock_0/xor1_0/a_n12_n44# carry2 0.20fF
C60 t4_5and vdd 0.06fF
```

```
C61 vdd vdd 0.03fF
C62 vdd gnd 0.03fF
C63 a1 b1 4.17fF
C64 vdd propgen_0/xor1_2/a_n12_n44# 0.09fF
C65 gnd vdd 0.04fF
C66 vdd t4_3and 0.06fF
C67 g0 vdd 0.01fF
C68 gnd gnd 0.01fF
C69 vdd p1 0.09fF
C70 g3 vdd 0.07fF
C71 g1 vdd 0.06fF
C72 gnd p2 0.06fF
C73 propgen_0/2and_3/a_13_5# g0 0.05fF
C74 gnd gnd 0.02fF
C75 sum0 g0 0.17fF
C76 t4_4and cla_0/5or_0/a_0_n44# 0.08fF
C77 p3 p1 0.17fF
C78 vdd gnd 0.06fF
C79 p1 p2 1.57fF
C80 gnd p0 0.07fF
C81 vdd g3 0.06fF
C82 gnd gnd 0.14fF
C83 gnd gnd 0.16fF
C84 a0 vdd 0.04fF
C85 gnd c_in 0.34fF
C86 t4_4and gnd 0.06fF
C87 cla_0/3and_2/a_13_5# vdd 0.13fF
C88 gnd gnd 0.09fF
C89 p2 gnd 0.03fF
C90 vdd gnd 0.09fF
C91 vdd p2 0.02fF
C92 vdd cla_0/4and_0/a_13_5# 0.05fF
C93 p1 p2 1.31fF
C94 gnd gnd 0.06fF
C95 gnd gnd 0.09fF
C96 vdd gnd 0.07fF
C97 vdd cla_0/3and_2/a_13_5# 0.05fF
C98 gnd sum0 0.13fF
C99 p0 gnd 0.06fF
C100 cla_0/4or_0/a_0_n37# sum2 0.05fF
C101 p3 gnd 0.05fF
C102 sum2 carry1 0.10fF
C103 p2 cla_0/2and_2/a_13_5# 0.17fF
C104 vdd vdd 0.05fF
C105 c_in p1 0.08fF
C106 gnd g0 0.10fF
C107 p1 gnd 0.11fF
C108 b1 gnd 0.01fF
```

```
C109 vdd vdd 0.05fF
C110 vdd cla_0/2and_0/a_13_5# 0.02fF
C111 vdd gnd 0.04fF
C112 vdd vdd 0.05fF
C113 a0 gnd 0.08fF
C114 propgen_0/xor1_3/a_n12_n44# p0 0.12fF
C115 vdd cla_0/4and_1/a_13_5# 0.05fF
C116 g0 p2 0.08fF
C117 carry1 gnd 0.04fF
C118 p2 gnd 0.02fF
C119 b3 gnd 0.12fF
C120 propgen_0/xor1_0/a_32_n47# p3 0.09fF
C121 vdd p2 0.23fF
C122 cla_0/4or_0/a_0_n37# vdd 0.04fF
C123 vdd sum2 0.03fF
C124 gnd gnd 0.05fF
C125 b3 gnd 0.12fF
C126 propgen_0/2and_0/a_13_5# a3 0.04fF
C127 g0 p1 1.46fF
C128 vdd gnd 0.16fF
C129 vdd vdd 0.12fF
C130 g2 gnd 0.06fF
C131 b2 gnd 0.01fF
C132 gnd gnd 0.04fF
C133 carry2 sum3 0.10fF
C134 gnd gnd 0.53fF
C135 g1 vdd 0.09fF
C136 gnd p0 0.06fF
C137 t3_2and t3_3and 0.86fF
C138 vdd vdd 0.06fF
C139 gnd gnd 0.09fF
C140 vdd b1 0.08fF
C141 vdd vdd 0.06fF
C142 t2_2and gnd 0.06fF
C143 vdd b3 0.13fF
C144 vdd propgen_0/2and_2/a_13_5# 0.08fF
C145 t4_4and t4_5and 0.47fF
C146 gnd vdd 0.13fF
C147 sumblock_0/xor1_0/a_n12_n44# vdd 0.12fF
C148 p2 gnd 0.04fF
C149 gnd gnd 0.03fF
C150 vdd p1 0.11fF
C151 gnd gnd 0.15fF
C152 gnd vdd 0.09fF
C153 gnd gnd 0.12fF
C154 p3 cla_0/2and_3/a_13_5# 0.17fF
C155 g1 propgen_0/2and_2/a_13_5# 0.05fF
C156 gnd gnd 0.05fF
```

```
C157 gnd g0 0.07fF
C158 g2 gnd 0.09fF
C159 gnd p1 0.19fF
C160 gnd t4_3and 0.06fF
C161 vdd propgen_0/xor1_2/a_32_n47# 0.09fF
C162 a1 propgen_0/xor1_2/a_n12_n44# 0.08fF
C163 vdd t3_4and 0.06fF
C164 cla_0/4and_0/a_13_5# gnd 0.02fF
C165 g0 cla_0/3and_1/a_13_5# 0.04fF
C166 vdd vdd 0.03fF
C167 a3 vdd 0.08fF
C168 c_in vdd 0.08fF
C169 cla_0/3or_0/a_0_n30# gnd 0.21fF
C170 cla_0/5and_0/a_13_5# p0 0.16fF
C171 propgen_0/2and_1/a_13_5# vdd 0.09fF
C172 sumblock_0/xor1_2/a_32_n47# p1 0.10fF
C173 vdd gnd 0.01fF
C174 sum3 gnd 0.06fF
C175 vdd g0 0.08fF
C176 sum0 sumblock_0/xor1_3/a_n12_n44# 0.12fF
C177 vdd p3 0.14fF
C178 p0 cla_0/4and_0/a_13_5# 0.16fF
C179 gnd vdd 0.66fF
C180 vdd gnd 0.01fF
C181 vdd p2 0.07fF
C182 b0 vdd 0.05fF
C183 vdd p2 0.07fF
C184 vdd t3_4and 0.06fF
C185 sum1 vdd 0.02fF
C186 p2 vdd 0.01fF
C187 sumblock_0/xor1_1/a_n12_n44# p2 0.08fF
C188 a2 p2 0.01fF
C189 propgen_0/xor1_1/a_n12_n44# vdd 0.12fF
C190 propgen_0/2and_0/a_13_5# b3 0.17fF
C191 vdd gnd 0.03fF
C192 p1 p3 0.17fF
C193 t3_2and gnd 0.06fF
C194 p1 gnd 0.05fF
C195 cla_0/3and_0/a_13_5# t2_3and 0.05fF
C196 vdd g2 0.07fF
C197 a0 gnd 0.01fF
C198 vdd gnd 0.01fF
C199 gnd gnd 0.06fF
C200 vdd gnd 0.05fF
C201 c_in p1 0.08fF
C202 sum0 vdd 0.03fF
C203 vdd vdd 0.05fF
C204 g1 p3 0.08fF
```

```
C205 gnd g2 0.16fF
C206 cla_0/4or_0/a_0_n37# gnd 0.25fF
C207 a2 gnd 0.10fF
C208 vdd t3_2and 0.03fF
C209 vdd cla_0/3and_0/a_13_5# 0.08fF
C210 gnd gnd 0.01fF
C211 a1 gnd 0.01fF
C212 gnd gnd 0.12fF
C213 vdd a0 0.08fF
C214 p3 p2 1.45fF
C215 cla_0/5or_0/a_0_n44# vdd 0.09fF
C216 sum3 vdd 0.06fF
C217 vdd cla_0/2and_3/a_13_5# 0.02fF
C218 b0 gnd 0.12fF
C219 propgen_0/xor1_3/a_32_n47# p0 0.09fF
C220 g0 p3 0.08fF
C221 sumblock_0/xor1_1/a_n12_n44# vdd 0.12fF
C222 b3 gnd 0.07fF
C223 propgen_0/xor1_0/a_n12_n44# gnd 0.08fF
C224 vdd p0 0.14fF
C225 vdd gnd 0.05fF
C226 sum0 vdd 0.04fF
C227 p0 gnd 0.07fF
C228 vdd gnd 0.15fF
C229 vdd p1 0.08fF
C230 p1 vdd 0.07fF
C231 t4_5and vdd 0.03fF
C232 vdd a0 0.14fF
C233 vdd b3 0.08fF
C234 gnd p3 0.06fF
C235 g1 gnd 0.07fF
C236 gnd gnd 0.03fF
C237 sum0 gnd 0.01fF
C238 vdd gnd 0.07fF
C239 vdd propgen_0/xor1_0/a_n12_n44# 0.09fF
C240 g1 g2 1.17fF
C241 gnd p1 0.09fF
C242 gnd gnd 0.18fF
C243 vdd vdd 0.06fF
C244 gnd vdd 0.18fF
C245 vdd t3_2and 0.06fF
C246 vdd t3_3and 0.06fF
C247 cla_0/3and_1/a_13_5# gnd 0.02fF
C248 p1 gnd 0.11fF
C249 gnd p1 0.12fF
C250 vdd t3_4and 0.06fF
C251 propgen_0/2and_2/a_13_5# vdd 0.02fF
C252 c_in p0 1.24fF
```

```
C253 vdd g0 0.03fF
C254 sum0 gnd 0.05fF
C255 gnd p3 0.08fF
C256 gnd gnd 0.22fF
C257 vdd vdd 0.12fF
C258 b1 propgen_0/xor1_2/a_n12_n44# 0.20fF
C259 a1 propgen_0/xor1_2/a_32_n47# 0.10fF
C260 carry0 sum1 0.10fF
C261 p0 gnd 0.06fF
C262 gnd gnd 0.35fF
C263 p3 gnd 0.07fF
C264 g1 gnd 0.07fF
C265 gnd p3 0.06fF
C266 gnd gnd 0.43fF
C267 b1 gnd 0.03fF
C268 g2 gnd 0.06fF
C269 g3 p1 0.16fF
C270 p1 cla_0/4and_0/a_13_5# 0.08fF
C271 vdd g0 0.08fF
C272 gnd t2_2and 0.07fF
C273 gnd gnd 0.01fF
C274 vdd g1 0.06fF
C275 vdd p3 0.07fF
C276 vdd sumblock_0/xor1_3/a_32_n47# 0.09fF
C277 vdd p1 0.08fF
C278 cla_0/3and_2/a_13_5# t4_3and 0.05fF
C279 sumblock_0/xor1_1/a_32_n47# p2 0.10fF
C280 vdd vdd 0.01fF
C281 gnd gnd 1.83fF
C282 t4_4and t4_2and 0.08fF
C283 propgen_0/xor1_1/a_32_n47# vdd 0.06fF
C284 b2 p2 0.10fF
C285 vdd vdd 0.08fF
C286 cla_0/5and_0/a_13_5# vdd 0.21fF
C287 vdd t4_5and 0.06fF
C288 vdd p2 0.08fF
C289 vdd t2_3and 0.06fF
C290 gnd g2 0.07fF
C291 b0 gnd 0.01fF
C292 vdd vdd 0.05fF
C293 vdd gnd 0.07fF
C294 vdd gnd 0.07fF
C295 p1 gnd 0.05fF
C296 vdd vdd 0.06fF
C297 gnd p0 0.08fF
C298 cla_0/4or_0/a_0_n37# g2 0.38fF
C299 vdd cla_0/3and_2/a_13_5# 0.08fF
C300 vdd gnd 0.01fF
```

```
C301 vdd gnd 0.09fF
C302 gnd g2 0.06fF
C303 p0 vdd 0.64fF
C304 vdd gnd 0.05fF
C305 sum0 vdd 0.06fF
C306 vdd sum2 0.06fF
C307 b2 gnd 0.20fF
C308 g1 t2_2and 0.77fF
C309 cla_0/3and_2/a_13_5# gnd 0.02fF
C310 p1 vdd 0.08fF
C311 c_in cla_0/3and_0/a_13_5# 0.04fF
C312 p0 p1 0.87fF
C313 vdd vdd 0.03fF
C314 p1 gnd 0.17fF
C315 b1 gnd 0.01fF
C316 gnd gnd 0.04fF
C317 c_in vdd 0.04fF
C318 gnd gnd 0.13fF
C319 gnd gnd 0.15fF
C320 g2 p3 0.78fF
C321 vdd g2 0.06fF
C322 vdd gnd 0.08fF
C323 propgen_0/xor1_3/a_n12_n44# gnd 0.08fF
C324 vdd vdd 0.08fF
C325 vdd cla_0/4and_1/a_13_5# 0.08fF
C326 sumblock_0/xor1_1/a_32_n47# vdd 0.06fF
C327 p3 gnd 0.03fF
C328 vdd gnd 0.05fF
C329 propgen_0/xor1_0/a_32_n47# gnd 0.04fF
C330 g1 cla_0/3or_0/a_0_n30# 0.30fF
C331 gnd p3 0.08fF
C332 sum2 vdd 0.02fF
C333 g0 vdd 0.06fF
C334 t2_3and t2_2and 0.36fF
C335 gnd vdd 0.31fF
C336 p3 cla_0/5and_0/a_13_5# 0.12fF
C337 gnd vdd 0.88fF
C338 vdd b0 0.13fF
C339 vdd g0 0.08fF
C340 g0 gnd 0.03fF
C341 a3 b3 4.18fF
C342 carry2 vdd 0.13fF
C343 sum3 gnd 0.04fF
C344 vdd propgen_0/xor1_0/a_32_n47# 0.09fF
C345 t1_2and g0 0.31fF
C346 propgen_0/2and_3/a_13_5# a0 0.04fF
C347 c_in vdd 0.13fF
C348 vdd gnd 0.46fF
```

```
C349 gnd vdd 0.02fF
C350 gnd vdd 0.37fF
C351 c_in p2 0.08fF
C352 gnd t3_4and 0.06fF
C353 vdd p1 0.17fF
C354 vdd vdd 0.03fF
C355 gnd gnd 0.15fF
C356 gnd vdd 0.09fF
C357 p3 vdd 0.06fF
C358 c_in p1 0.08fF
C359 sumblock_0/xor1_3/a_n12_n44# vdd 0.12fF
C360 cla_0/2and_1/a_13_5# vdd 0.09fF
C361 gnd p1 0.07fF
C362 gnd gnd 0.05fF
C363 vdd p3 0.06fF
C364 g2 gnd 0.04fF
C365 vdd p1 0.08fF
C366 gnd gnd 0.10fF
C367 a1 vdd 0.23fF
C368 b1 propgen_0/xor1_2/a_32_n47# 0.28fF
C369 vdd p1 0.50fF
C370 vdd t3_3and 0.03fF
C371 gnd sumblock_0/xor1_3/a_32_n47# 0.04fF
C372 p0 gnd 0.04fF
C373 p2 vdd 0.01fF
C374 g1 gnd 0.32fF
C375 vdd p1 0.08fF
C376 sumblock_0/xor1_2/a_n12_n44# vdd 0.09fF
C377 g1 vdd 0.08fF
C378 c_in gnd 0.05fF
C379 vdd gnd 0.05fF
C380 gnd p1 0.07fF
C381 propgen_0/2and_3/a_13_5# vdd 0.09fF
C382 propgen_0/2and_0/a_13_5# p3 0.05fF
C383 sum1 gnd 0.02fF
C384 g3 vdd 0.07fF
C385 gnd gnd 0.01fF
C386 vdd g2 0.08fF
C387 propgen_0/2and_2/a_13_5# gnd 0.02fF
C388 vdd propgen_0/2and_0/a_13_5# 0.09fF
C389 carry1 p2 0.66fF
C390 vdd t4_3and 0.06fF
C391 sumblock_0/xor1_0/a_32_n47# sum3 0.09fF
C392 g2 gnd 0.07fF
C393 a2 gnd 0.08fF
C394 propgen_0/xor1_1/a_n12_n44# p2 0.12fF
C395 sum2 gnd 0.06fF
C396 a1 gnd 0.19fF
```

```
C397 propgen_0/2and_2/a_13_5# b1 0.17fF
C398 gnd sum0 0.11fF
C399 vdd gnd 0.02fF
C400 p1 cla_0/4and_1/a_13_5# 0.16fF
C401 cla_0/3and_0/a_13_5# gnd 0.02fF
C402 vdd gnd 0.06fF
C403 a0 gnd 0.01fF
C404 t2_2and vdd 0.06fF
C405 gnd p2 0.08fF
C406 c_in g0 0.10fF
C407 vdd vdd 0.07fF
C408 g2 p1 0.16fF
C409 cla_0/4and_1/a_13_5# vdd 0.17fF
C410 g1 cla_0/3and_2/a_13_5# 0.04fF
C411 p2 p3 1.38fF
C412 vdd vdd 0.03fF
C413 p3 p0 0.08fF
C414 t4_3and g3 0.08fF
C415 gnd gnd 0.13fF
C416 a1 gnd 0.05fF
C417 cla_0/3or_0/a_0_n30# vdd 0.09fF
C418 sum0 vdd 0.06fF
C419 vdd vdd 0.06fF
C420 vdd cla_0/2and_3/a_13_5# 0.08fF
C421 gnd gnd 0.08fF
C422 propgen_0/xor1_3/a_32_n47# gnd 0.04fF
C423 gnd gnd 0.03fF
C424 g0 cla_0/4and_1/a_13_5# 0.04fF
C425 vdd p1 0.09fF
C426 gnd gnd 0.01fF
C427 vdd vdd 0.06fF
C428 vdd vdd 0.12fF
C429 p0 vdd 0.07fF
C430 c_in gnd 0.12fF
C431 c_in vdd 0.13fF
C432 vdd p2 0.08fF
C433 p2 p1 1.47fF
C434 vdd c_in 0.08fF
C435 gnd p0 0.11fF
C436 p1 gnd 0.36fF
C437 t4_5and gnd 0.06fF
C438 a0 b0 4.17fF
C439 vdd propgen_0/xor1_3/a_n12_n44# 0.09fF
C440 gnd gnd 0.03fF
C441 p2 vdd 0.08fF
C442 a3 propgen_0/xor1_0/a_n12_n44# 0.08fF
C443 vdd t4_2and 0.06fF
C444 t3_2and cla_0/4or_0/a_0_n37# 0.08fF
```

```
C445 propgen_0/2and_0/a_13_5# vdd 0.08fF
C446 p2 gnd 0.05fF
C447 g2 vdd 0.06fF
C448 vdd vdd 0.12fF
C449 gnd gnd 0.14fF
C450 propgen_0/2and_1/a_13_5# vdd 0.08fF
C451 sumblock_0/xor1_2/a_n12_n44# gnd 0.08fF
C452 sumblock_0/xor1_2/a_n12_n44# carry0 0.20fF
C453 g3 vdd 0.01fF
C454 gnd p1 0.11fF
C455 p1 vdd 0.02fF
C456 gnd gnd 0.10fF
C457 vdd g0 0.08fF
C458 gnd gnd 0.14fF
C459 vdd t3_2and 0.06fF
C460 carry0 vdd 0.04fF
C461 vdd gnd 0.04fF
C462 t4_5and gnd 0.06fF
C463 p2 gnd 0.02fF
C464 vdd g0 0.06fF
C465 vdd p1 0.10fF
C466 c_in cla_0/5and_0/a_13_5# 0.04fF
C467 t4_2and gnd 0.06fF
C468 t3_4and gnd 0.06fF
C469 cla_0/5and_0/a_13_5# vdd 0.08fF
C470 p2 cla_0/3and_1/a_13_5# 0.12fF
C471 sum2 gnd 0.01fF
C472 p1 gnd 0.04fF
C473 vdd gnd 0.02fF
C474 gnd gnd 0.03fF
C475 gnd t4_4and 0.06fF
C476 cla_0/3or_0/a_0_n30# sum1 0.05fF
C477 gnd vdd 0.05fF
C478 vdd vdd 0.06fF
C479 vdd cla_0/2and_1/a_13_5# 0.02fF
C480 sum0 vdd 0.10fF
C481 gnd gnd 0.03fF
C482 gnd p1 0.09fF
C483 p2 cla_0/4and_0/a_13_5# 0.12fF
C484 vdd vdd 0.06fF
C485 gnd gnd 0.07fF
C486 vdd p2 0.06fF
C487 sumblock_0/xor1_0/a_n12_n44# sum3 0.12fF
C488 carry2 gnd 0.12fF
C489 sumblock_0/xor1_1/a_n12_n44# carry1 0.20fF
C490 p3 gnd 0.12fF
C491 vdd vdd 0.05fF
C492 propgen_0/2and_1/a_13_5# b2 0.17fF
```

```
C493 sum2 g2 0.03fF
C494 sum3 vdd 0.03fF
C495 b2 gnd 0.12fF
C496 propgen_0/xor1_1/a_32_n47# p2 0.09fF
C497 p2 vdd 0.04fF
C498 b1 gnd 0.28fF
C499 vdd gnd 0.03fF
C500 gnd g0 0.07fF
C501 sumblock_0/xor1_1/a_n12_n44# gnd 0.08fF
C502 b0 gnd 0.01fF
C503 gnd gnd 0.04fF
C504 p0 gnd 0.03fF
C505 cla_0/2and_0/a_13_5# t1_2and 0.05fF
C506 vdd vdd 0.07fF
C507 b2 a3 0.23fF
C508 vdd t3_3and 0.06fF
C509 gnd gnd 0.02fF
C510 gnd vdd 0.04fF
C511 p1 vdd 0.14fF
C512 p3 gnd 0.04fF
C513 g2 vdd 0.07fF
C514 vdd a2 0.14fF
C515 gnd vdd 0.08fF
C516 cla_0/2and_2/a_13_5# vdd 0.09fF
C517 vdd t2_3and 0.03fF
C518 p0 cla_0/3and_0/a_13_5# 0.16fF
C519 gnd p2 0.07fF
C520 gnd p1 0.17fF
C521 b1 gnd 0.01fF
C522 t1_2and cla_0/2or_0/a_0_n30# 0.19fF
C523 g2 cla_0/2and_3/a_13_5# 0.04fF
C524 vdd g1 0.08fF
C525 vdd vdd 0.03fF
C526 gnd gnd 0.03fF
C527 vdd sum1 0.06fF
C528 gnd p3 0.03fF
C529 p1 vdd 0.09fF
C530 p1 gnd 0.21fF
C531 a2 gnd 0.05fF
C532 vdd propgen_0/xor1_3/a_32_n47# 0.09fF
C533 a0 propgen_0/xor1_3/a_n12_n44# 0.08fF
C534 vdd vdd 0.06fF
C535 g1 gnd 0.07fF
C536 b3 propgen_0/xor1_0/a_n12_n44# 0.23fF
C537 a3 propgen_0/xor1_0/a_32_n47# 0.10fF
C538 gnd vdd 0.03fF
C539 c_in p0 0.68fF
C540 sum0 vdd 0.02fF
```

```
C541 gnd gnd 0.03fF
C542 vdd gnd 0.04fF
C543 cla_0/5or_0/a_0_n44# t4_3and 0.08fF
C544 a3 vdd 0.04fF
C545 cla_0/5and_0/a_13_5# vdd 0.08fF
C546 carry2 gnd 0.02fF
C547 sumblock_0/xor1_2/a_32_n47# vdd 0.09fF
C548 g3 gnd 0.01fF
C549 vdd gnd 0.05fF
C550 p1 a1 0.01fF
C551 gnd gnd 0.05fF
C552 cla_0/2and_3/a_13_5# vdd 0.09fF
C553 p3 gnd 0.02fF
C554 c_in p2 0.08fF
C555 p0 sumblock_0/xor1_3/a_32_n47# 0.10fF
C556 cla_0/2and_1/a_13_5# t2_2and 0.05fF
C557 p1 gnd 0.16fF
C558 vdd vdd 0.03fF
C559 gnd vdd 0.11fF
C560 propgen_0/xor1_2/a_n12_n44# vdd 0.12fF
C561 vdd gnd 0.04fF
C562 cla_0/5or_0/a_0_n44# g3 0.48fF
C563 carry2 p3 0.67fF
C564 a0 gnd 0.02fF
C565 a3 gnd 0.02fF
C566 a3 b3 0.24fF
C567 gnd gnd 0.02fF
C568 vdd vdd 0.06fF
C569 g2 vdd 0.02fF
C570 vdd gnd 0.03fF
C571 vdd p2 0.08fF
C572 b0 a0 0.23fF
C573 a0 gnd 0.29fF
C574 p1 gnd 0.08fF
C575 carry0 p1 1.30fF
C576 gnd gnd 0.03fF
C577 g3 gnd 0.08fF
C578 b2 gnd 0.07fF
C579 sumblock_0/xor1_1/a_32_n47# carry1 0.28fF
C580 gnd vdd 0.09fF
C581 g1 gnd 0.06fF
C582 gnd gnd 0.09fF
C583 propgen_0/xor1_1/a_n12_n44# gnd 0.08fF
C584 a1 gnd 0.02fF
C585 sumblock_0/xor1_0/a_32_n47# vdd 0.09fF
C586 sumblock_0/xor1_1/a_32_n47# gnd 0.04fF
C587 gnd vdd 0.07fF
C588 vdd gnd 0.13fF
```

```
C589 a0 gnd 0.01fF
C590 vdd vdd 0.03fF
C591 vdd p2 0.14fF
C592 gnd p1 0.06fF
C593 cla_0/4and_1/a_13_5# t4_4and 0.05fF
C594 vdd t4_3and 0.03fF
C595 p2 cla_0/3and_2/a_13_5# 0.16fF
C596 vdd gnd 0.07fF
C597 t4_4and vdd 0.06fF
C598 t4_2and cla_0/2and_3/a_13_5# 0.05fF
C599 gnd vdd 0.76fF
C600 vdd b2 0.13fF
C601 vdd sumblock_0/xor1_3/a_n12_n44# 0.09fF
C602 vdd p0 0.08fF
C603 g1 vdd 0.06fF
C604 b2 gnd 0.03fF
C605 t4_3and gnd 0.06fF
C606 p1 g0 0.92fF
C607 p2 gnd 0.03fF
C608 vdd p1 0.16fF
C609 vdd cla_0/2and_0/a_13_5# 0.08fF
C610 vdd gnd 0.07fF
C611 b2 vdd 0.08fF
C612 c_in p0 0.72fF
C613 vdd vdd 0.03fF
C614 t3_4and g2 0.08fF
C615 gnd vdd 0.08fF
C616 t4_5and t4_3and 0.08fF
C617 cla_0/2and_0/a_13_5# vdd 0.09fF
C618 gnd p2 0.08fF
C619 vdd gnd 0.05fF
C620 propgen_0/2and_0/a_13_5# gnd 0.02fF
C621 sumblock_0/xor1_2/a_32_n47# gnd 0.04fF
C622 carry0 sumblock_0/xor1_2/a_32_n47# 0.28fF
C623 vdd p0 0.08fF
C624 p1 gnd 0.12fF
C625 p0 gnd 0.11fF
C626 vdd cla_0/2and_2/a_13_5# 0.02fF
C627 cla_0/3and_1/a_13_5# p1 0.16fF
C628 vdd p0 0.08fF
C629 gnd t2_3and 0.02fF
C630 g0 gnd 0.01fF
C631 vdd gnd 0.02fF
C632 b2 gnd 0.06fF
C633 g0 vdd 0.06fF
C634 vdd vdd 0.12fF
C635 vdd cla_0/2or_0/a_0_n30# 0.09fF
C636 gnd vdd 0.30fF
```

```
C637 vdd vdd 0.12fF
C638 b0 propgen_0/xor1_3/a_n12_n44# 0.20fF
C639 a0 propgen_0/xor1_3/a_32_n47# 0.10fF
C640 sumblock_0/xor1_2/a_n12_n44# vdd 0.12fF
C641 a3 vdd 0.23fF
C642 b3 propgen_0/xor1_0/a_32_n47# 0.28fF
C643 t3_3and cla_0/4or_0/a_0_n37# 0.08fF
C644 t4_5and g3 0.08fF
C645 vdd p3 0.02fF
C646 b3 vdd 0.05fF
C647 gnd gnd 0.29fF
C648 propgen_0/2and_1/a_13_5# a3 0.04fF
C649 gnd gnd 0.08fF
C650 t3_3and gnd 0.06fF
C651 p0 gnd 0.07fF
C652 vdd p3 0.23fF
C653 gnd vdd 1.29fF
C654 p1 b1 0.10fF
C655 gnd gnd 0.11fF
C656 vdd t3_3and 0.06fF
C657 p1 gnd 0.03fF
C658 a3 gnd 0.05fF
C659 propgen_0/xor1_2/a_32_n47# vdd 0.06fF
C660 vdd vdd 0.03fF
C661 cla_0/5and_0/a_13_5# gnd 0.02fF
C662 g0 gnd 0.09fF
C663 p2 gnd 0.04fF
C664 gnd p1 0.07fF
C665 gnd gnd 0.33fF
C666 a1 vdd 0.08fF
C667 p2 gnd 0.07fF
C668 t4_4and gnd 0.06fF
C669 t4_2and vdd 0.03fF
C670 vdd vdd 0.06fF
C671 vdd cla_0/2and_1/a_13_5# 0.08fF
C672 vdd p2 0.09fF
C673 g2 gnd 0.01fF
C674 vdd p1 0.07fF
C675 b0 gnd 0.37fF
C676 c_in sumblock_0/xor1_3/a_32_n47# 0.28fF
C677 gnd t1_2and 0.09fF
C678 g3 gnd 2.94fF
C679 vdd p3 0.06fF
C680 g1 gnd 0.07fF
C681 gnd vdd 0.02fF
C682 gnd gnd 0.04fF
C683 vdd gnd 0.06fF
C684 gnd sumblock_0/xor1_3/a_n12_n44# 0.08fF
```

```
C685 vdd g1 0.06fF
C686 vdd gnd 0.07fF
C687 sumblock_0/xor1_0/a_n12_n44# vdd 0.09fF
C688 propgen_0/xor1_1/a_32_n47# gnd 0.04fF
C689 sumblock_0/xor1_2/a_n12_n44# sum1 0.12fF
C690 gnd carry1 0.12fF
C691 t2_3and gnd 0.06fF
C692 vdd g0 0.07fF
C693 sumblock_0/xor1_1/a_n12_n44# vdd 0.09fF
C694 gnd vdd 0.08fF
C695 gnd gnd 0.42fF
C696 gnd gnd 0.13fF
C697 vdd gnd 0.14fF
C698 b0 gnd 0.01fF
C699 propgen_0/2and_3/a_13_5# vdd 0.02fF
C700 c_in p3 0.08fF
C701 cla_0/2and_0/a_13_5# gnd 0.02fF
C702 vdd gnd 0.07fF
C703 vdd t4_5and 0.06fF
C704 cla_0/4and_1/a_13_5# gnd 0.02fF
C705 gnd gnd 0.16fF
C706 g2 gnd 0.08fF
C707 a2 b2 4.16fF
C708 vdd propgen_0/xor1_1/a_n12_n44# 0.09fF
C709 vdd vdd 0.06fF
C710 vdd p1 0.08fF
C711 vdd cla_0/4and_0/a_13_5# 0.08fF
C712 gnd p0 0.11fF
C713 cla_0/2and_2/a_13_5# t3_2and 0.05fF
C714 p1 cla_0/3and_0/a_13_5# 0.12fF
C715 gnd g0 0.07fF
C716 gnd gnd 0.06fF
C717 a1 gnd 0.05fF
C718 vdd vdd 0.12fF
C719 g2 vdd 0.03fF
C720 vdd vdd 0.07fF
C721 vdd t4_4and 0.03fF
C722 p2 p3 1.53fF
C723 vdd p2 0.08fF
C724 vdd g2 0.06fF
C725 gnd cla_0/2and_3/a_13_5# 0.02fF
C726 gnd gnd 0.07fF
C727 a2 vdd 0.04fF
C728 vdd t3_3and 0.06fF
C729 a0 vdd 0.23fF
C730 b0 propgen_0/xor1_3/a_32_n47# 0.28fF
C731 p2 p1 1.45fF
C732 g1 gnd 0.17fF
```

```
C733 t4_3and gnd 0.06fF
C734 vdd cla_0/2or_0/a_0_n30# 0.13fF
C735 gnd gnd 0.08fF
C736 propgen_0/2and_3/a_13_5# gnd 0.02fF
C737 gnd gnd 0.03fF
C738 vdd p1 0.08fF
C739 vdd p2 0.06fF
C740 gnd sumblock_0/xor1_0/a_32_n47# 0.04fF
C741 vdd vdd 0.08fF
C742 gnd p3 0.06fF
C743 p1 gnd 0.08fF
C744 gnd gnd 0.03fF
C745 p1 propgen_0/xor1_2/a_n12_n44# 0.12fF
C746 t3_4and t3_2and 0.44fF
C747 propgen_0/2and_1/a_13_5# gnd 0.02fF
C748 g0 c_in 0.16fF
C749 c_in cla_0/4and_0/a_13_5# 0.04fF
C750 carry0 gnd 0.05fF
C751 vdd t2_2and 0.06fF
C752 cla_0/2and_1/a_13_5# gnd 0.02fF
C753 b3 gnd 0.01fF
C754 sum3 vdd 0.02fF
C755 propgen_0/2and_1/a_13_5# vdd 0.02fF
C756 a1 gnd 0.08fF
C757 vdd gnd 0.04fF
C758 t4_2and t4_3and 1.01fF
C759 p1 vdd 0.23fF
C760 gnd gnd 0.15fF
C761 g1 vdd 0.06fF
C762 c_in t1_2and 0.02fF
C763 g0 p1 0.68fF
C764 vdd vdd 0.08fF
C765 vdd g1 0.09fF
C766 gnd p2 0.07fF
C767 vdd gnd 0.05fF
C768 gnd gnd 0.04fF
C769 gnd g0 0.11fF
C770 vdd a3 0.08fF
C771 vdd cla_0/3and_1/a_13_5# 0.05fF
C772 sum2 gnd 0.02fF
C773 gnd g1 0.13fF
C774 t4_2and g3 1.27fF
C775 vdd vdd 0.01fF
C776 gnd gnd 0.02fF
C777 p3 vdd 0.08fF
C778 a3 gnd 0.02fF
C779 vdd vdd 0.05fF
C780 gnd g1 0.02fF
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C781 gnd gnd 0.07fF
C782 gnd gnd 0.11fF
C783 p2 gnd 0.05fF
C784 p0 p1 1.60fF
C785 gnd vdd 0.39fF
C786 sumblock_0/xor1_1/a_32_n47# vdd 0.09fF
C787 gnd gnd 0.14fF
C788 a0 gnd 0.05fF
C789 vdd gnd 0.08fF
C790 gnd vdd 0.04fF
C791 t2_2and gnd 0.04fF
C792 vdd gnd 0.03fF
C793 vdd t4_4and 0.06fF
C794 p3 cla_0/3and_2/a_13_5# 0.12fF
C795 vdd gnd 0.06fF
C796 gnd gnd 0.08fF
C797 t4_2and vdd 0.06fF
C798 vdd p1 0.16fF
C799 g2 gnd 0.07fF
C800 vdd propgen_0/xor1_1/a_32_n47# 0.09fF
C801 a2 propgen_0/xor1_1/a_n12_n44# 0.08fF
C802 sum0 p0 0.01fF
C803 gnd sum1 0.06fF
C804 a1 b1 0.23fF
C805 g1 vdd 0.03fF
C806 propgen_0/2and_0/a_13_5# vdd 0.02fF
C807 sumblock_0/xor1_2/a_32_n47# vdd 0.06fF
C808 gnd p0 0.10fF
C809 p3 gnd 0.03fF
C810 cla_0/2and_2/a_13_5# gnd 0.02fF
C811 b1 gnd 0.06fF
C812 t3_2and g2 0.08fF
C813 gnd gnd 0.09fF
C814 vdd gnd 0.05fF
C815 c_in p0 0.66fF
C816 sumblock_0/xor1_0/a_32_n47# p3 0.10fF
C817 p1 sum1 0.01fF
C818 vdd t1_2and 0.06fF
C819 vdd vdd 0.06fF
C820 vdd cla_0/2and_2/a_13_5# 0.08fF
C821 vdd p1 0.08fF
C822 b2 vdd 0.05fF
C823 cla_0/3or_0/a_0_n30# t2_2and 0.08fF
C824 sum2 p2 0.01fF
C825 gnd gnd 1.44fF
C826 gnd vdd 0.42fF
C827 vdd p0 0.02fF
C828 vdd p2 0.08fF
```

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C829 p2 gnd 0.03fF
C830 gnd p2 0.10fF
C831 a3 p3 0.01fF
C832 propgen_0/xor1_0/a_n12_n44# vdd 0.12fF
C833 sumblock_0/xor1_0/a_n12_n44# gnd 0.08fF
C834 g1 t2_3and 0.08fF
C835 vdd vdd 0.16fF
C836 vdd vdd 0.18fF
C837 p1 gnd 0.07fF
C838 a2 gnd 0.01fF
C839 gnd gnd 0.44fF
C840 vdd cla_0/2or_0/a_0_n30# 0.04fF
C841 g3 gnd 0.01fF
C842 cla_0/5and_0/a_13_5# p1 0.08fF
C843 vdd p1 0.82fF
C844 p1 propgen_0/xor1_2/a_32_n47# 0.09fF
C845 gnd gnd 1.21fF
C846 gnd gnd 0.11fF
C847 vdd gnd 0.11fF
C848 g2 gnd 0.07fF
C849 gnd gnd 0.08fF
C850 b1 gnd 0.12fF
C851 cla_0/3and_1/a_13_5# vdd 0.13fF
C852 g0 gnd 0.11fF
C853 gnd gnd 0.08fF
C854 gnd gnd 0.05fF
C855 vdd gnd 0.02fF
C856 p2 gnd 0.12fF
C857 sum0 sumblock_0/xor1_3/a_32_n47# 0.09fF
C858 sumblock_0/xor1_2/a_32_n47# sum1 0.09fF
C859 vdd vdd 0.03fF
C860 g0 cla_0/2and_1/a_13_5# 0.04fF
C861 g1 p2 0.84fF
C862 gnd p3 0.08fF
C863 gnd g1 0.07fF
C864 t4_5and cla_0/5and_0/a_13_5# 0.05fF
C865 vdd a1 0.14fF
C866 p0 sumblock_0/xor1_3/a_n12_n44# 0.08fF
C867 cla_0/4and_0/a_13_5# vdd 0.17fF
C868 sum1 gnd 0.04fF
C869 gnd g1 0.06fF
C870 g1 gnd 0.06fF
C871 vdd gnd 0.01fF
C872 carry0 gnd 0.04fF
C873 vdd gnd 0.04fF
C874 vdd gnd 0.15fF
C875 vdd vdd 0.05fF
C876 vdd carry1 0.13fF
```

```
C877 gnd gnd 0.07fF
C878 b0 gnd 0.01fF
C879 a0 gnd 0.05fF
C880 propgen_0/2and_1/a_13_5# g2 0.05fF
C881 cla_0/3or_0/a_0_n30# vdd 0.04fF
C882 p3 gnd 0.05fF
C883 g3 gnd 0.03fF
C884 vdd g0 0.07fF
C885 vdd gnd 0.03fF
C886 vdd vdd 0.12fF
C887 b2 propgen_0/xor1_1/a_n12_n44# 0.20fF
C888 a2 propgen_0/xor1_1/a_32_n47# 0.10fF
C889 vdd vdd 0.03fF
C890 vdd p2 0.08fF
C891 sum0 cla_0/2or_0/a_0_n30# 0.05fF
C892 gnd t2_3and 0.06fF
C893 g1 vdd 0.06fF
C894 cla_0/5or_0/a_0_n44# gnd 0.33fF
C895 vdd t3_2and 0.06fF
C896 a1 vdd 0.04fF
C897 gnd gnd 0.35fF
C898 vdd t1_2and 0.03fF
C899 vdd gnd 0.03fF
C900 vdd vdd 0.05fF
C901 sumblock_0/xor1_0/a_n12_n44# p3 0.08fF
C902 c_in vdd 0.08fF
C903 cla_0/5or_0/a_0_n44# t4_2and 0.08fF
C904 gnd gnd 0.08fF
C905 vdd gnd 0.08fF
C906 p2 cla_0/4and_1/a_13_5# 0.08fF
C907 t1_2and vdd 0.06fF
C908 vdd p3 0.08fF
C909 a1 propgen_0/2and_2/a_13_5# 0.04fF
C910 p3 gnd 0.06fF
C911 p1 p0 0.81fF
C912 c_in p0 0.57fF
C913 gnd g0 0.09fF
C914 gnd gnd 0.06fF
C915 sumblock_0/xor1_1/a_n12_n44# sum2 0.12fF
C916 t2_3and vdd 0.06fF
C917 vdd p0 0.08fF
C918 vdd gnd 0.02fF
C919 vdd b0 0.08fF
C920 sum0 c_in 0.10fF
C921 t4_4and t4_3and 0.92fF
C922 vdd vdd 0.05fF
C923 a0 p0 0.01fF
C924 propgen_0/xor1_3/a_n12_n44# vdd 0.12fF
```

```
C925 vdd p3 0.08fF
C926 sum1 vdd 0.04fF
C927 gnd gnd 0.03fF
C928 p3 gnd 0.03fF
C929 g1 gnd 0.07fF
C930 vdd c_in 0.08fF
C931 propgen_0/xor1_0/a_32_n47# vdd 0.06fF
C932 b3 p3 0.10fF
C933 c_in vdd 0.08fF
C934 gnd vdd 0.05fF
C935 c_in gnd 0.15fF
C936 g2 vdd 0.06fF
C937 b2 gnd 0.01fF
C938 vdd vdd 0.05fF
C939 gnd p3 0.08fF
C940 vdd t4_2and 0.06fF
C941 sum1 gnd 0.01fF
C942 p1 gnd 0.08fF
C943 t4_4and g3 0.08fF
C944 vdd cla_0/4or_0/a_0_n37# 0.09fF
C945 t3_4and t3_3and 0.08fF
C946 carry0 vdd 0.13fF
C947 gnd t2_2and 0.07fF
C948 gnd p3 0.06fF
C949 cla_0/5or_0/a_0_n44# vdd 0.05fF
C950 vdd propgen_0/2and_2/a_13_5# 0.09fF
C951 gnd gnd 0.10fF
C952 propgen_0/xor1_2/a_n12_n44# gnd 0.08fF
C953 vdd gnd 0.07fF
C954 p2 gnd 0.05fF
C955 gnd vdd 0.09fF
C956 gnd gnd 0.15fF
C957 gnd gnd 0.07fF
C958 gnd gnd 0.05fF
C959 g1 gnd 0.06fF
C960 b0 gnd 0.03fF
C961 sum3 cla_0/5or_0/a_0_n44# 0.05fF
C962 gnd gnd 0.05fF
C963 vdd p2 0.09fF
C964 vdd g1 0.07fF
C965 gnd p3 0.07fF
C966 g2 gnd 0.01fF
C967 gnd vdd 0.76fF
C968 vdd b1 0.13fF
C969 cla_0/4and_0/a_13_5# t3_4and 0.05fF
C970 p2 gnd 0.04fF
C971 gnd t4_2and 0.06fF
C972 vdd vdd 0.05fF
```

```
C973 vdd cla_0/3and_1/a_13_5# 0.08fF
C974 g0 p2 0.08fF
C975 g1 p1 0.13fF
C976 g0 gnd 0.01fF
C977 gnd gnd 0.10fF
C978 carry2 sumblock_0/xor1_0/a_32_n47# 0.28fF
C979 p0 vdd 0.23fF
C980 sum3 p3 0.01fF
C981 p2 gnd 0.04fF
C982 vdd c_in 0.12fF
C983 gnd gnd 0.15fF
C984 vdd gnd 0.03fF
C985 p0 p2 0.08fF
C986 cla_0/5and_0/a_13_5# p2 0.08fF
C987 t4_2and t4_5and 0.08fF
C988 g0 gnd 0.06fF
C989 gnd p0 0.12fF
C990 t1_2and gnd 0.04fF
C991 gnd gnd 0.14fF
C992 b0 gnd 0.06fF
C993 gnd gnd 0.05fF
C994 t1_2and gnd 0.06fF
C995 vdd vdd 0.03fF
C996 c_in sumblock_0/xor1_3/a_n12_n44# 0.20fF
C997 gnd g0 0.07fF
C998 gnd c_in 0.15fF
C999 gnd gnd 0.03fF
C1000 a2 vdd 0.23fF
C1001 b2 propgen_0/xor1_1/a_32_n47# 0.28fF
C1002 vdd t3_4and 0.03fF
C1003 vdd p3 0.06fF
C1004 sumblock_0/xor1_2/a_n12_n44# p1 0.08fF
C1005 p3 gnd 0.04fF
C1006 cla_0/3and_0/a_13_5# vdd 0.13fF
C1007 gnd p2 0.09fF
C1008 b1 vdd 0.05fF
C1009 propgen_0/2and_3/a_13_5# vdd 0.08fF
C1010 p0 cla_0/2and_0/a_13_5# 0.17fF
C1011 t3_3and g2 1.02fF
C1012 vdd gnd 0.07fF
C1013 p1 vdd 0.04fF
C1014 p3 cla_0/4and_1/a_13_5# 0.12fF
C1015 g1 p2 1.50fF
C1016 c_in cla_0/2and_0/a_13_5# 0.04fF
C1017 gnd Gnd 2.01fF
C1018 vdd Gnd 3.60fF
C1019 gnd Gnd 0.15fF
C1020 gnd Gnd 0.31fF
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C1021 gnd Gnd 0.12fF
C1022 gnd Gnd 0.02fF
C1023 gnd Gnd 0.12fF
C1024 gnd Gnd 0.02fF
C1025 gnd Gnd 0.29fF
C1026 gnd Gnd 0.14fF
C1027 gnd Gnd 0.17fF
C1028 gnd Gnd 0.15fF
C1029 vdd Gnd 0.11fF
C1030 gnd Gnd 0.16fF
C1031 vdd Gnd 0.30fF
C1032 vdd Gnd 0.02fF
C1033 vdd Gnd 0.84fF
C1034 gnd Gnd 0.45fF
C1035 gnd Gnd 0.45fF
C1036 gnd Gnd 0.46fF
C1037 gnd Gnd 0.46fF
C1038 gnd Gnd 3.27fF
C1039 gnd Gnd 0.41fF
C1040 p0 Gnd 1.22fF
C1041 vdd Gnd 0.41fF
C1042 propgen_0/xor1_3/a_32_n47# Gnd 0.42fF
C1043 propgen_0/xor1_3/a_n12_n44# Gnd 0.50fF
C1044 b0 Gnd 2.66fF
C1045 a0 Gnd 2.68fF
C1046 vdd Gnd 1.63fF
C1047 gnd Gnd 0.52fF
C1048 vdd Gnd 0.41fF
C1049 propgen_0/xor1_2/a_32_n47# Gnd 0.42fF
C1050 propgen_0/xor1_2/a_n12_n44# Gnd 0.50fF
C1051 b1 Gnd 3.27fF
C1052 a1 Gnd 2.69fF
C1053 vdd Gnd 1.63fF
C1054 gnd Gnd 0.49fF
C1055 p2 Gnd 1.36fF
C1056 vdd Gnd 0.41fF
C1057 propgen_0/xor1_1/a_32_n47# Gnd 0.42fF
C1058 propgen_0/xor1_1/a_n12_n44# Gnd 0.50fF
C1059 b2 Gnd 2.66fF
C1060 a2 Gnd 2.70fF
C1061 vdd Gnd 1.63fF
C1062 gnd Gnd 0.54fF
C1063 p3 Gnd 1.08fF
C1064 vdd Gnd 0.54fF
C1065 propgen_0/xor1_0/a_32_n47# Gnd 0.42fF
C1066 propgen_0/xor1_0/a_n12_n44# Gnd 0.50fF
C1067 b3 Gnd 2.66fF
C1068 a3 Gnd 2.72fF
```

```
C1069 vdd Gnd 1.63fF
C1070 gnd Gnd 0.34fF
C1071 g0 Gnd 0.41fF
C1072 vdd Gnd 0.36fF
C1073 propgen_0/2and_3/a_13_5# Gnd 0.37fF
C1074 b0 Gnd 0.32fF
C1075 a0 Gnd 0.28fF
C1076 vdd Gnd 0.43fF
C1077 vdd Gnd 0.67fF
C1078 gnd Gnd 0.34fF
C1079 vdd Gnd 0.36fF
C1080 propgen_0/2and_2/a_13_5# Gnd 0.37fF
C1081 b1 Gnd 0.32fF
C1082 a1 Gnd 0.28fF
C1083 vdd Gnd 0.43fF
C1084 vdd Gnd 0.67fF
C1085 gnd Gnd 0.34fF
C1086 g2 Gnd 0.43fF
C1087 vdd Gnd 0.27fF
C1088 propgen_0/2and_1/a_13_5# Gnd 0.37fF
C1089 b2 Gnd 0.32fF
C1090 a3 Gnd 0.28fF
C1091 vdd Gnd 0.43fF
C1092 vdd Gnd 0.67fF
C1093 gnd Gnd 0.34fF
C1094 p3 Gnd 0.42fF
C1095 vdd Gnd 0.36fF
C1096 propgen_0/2and_0/a_13_5# Gnd 0.37fF
C1097 b3 Gnd 0.32fF
C1098 a3 Gnd 0.28fF
C1099 vdd Gnd 0.43fF
C1100 vdd Gnd 0.67fF
C1101 vdd Gnd 0.12fF
C1102 gnd Gnd 1.29fF
C1103 sum0 Gnd 0.78fF
C1104 vdd Gnd 0.43fF
C1105 sumblock_0/xor1_3/a_32_n47# Gnd 0.42fF
C1106 sumblock_0/xor1_3/a_n12_n44# Gnd 0.50fF
C1107 c_in Gnd 1.74fF
C1108 p0 Gnd 1.50fF
C1109 vdd Gnd 1.63fF
C1110 gnd Gnd 0.54fF
C1111 sum1 Gnd 0.93fF
C1112 vdd Gnd 0.43fF
C1113 sumblock_0/xor1_2/a_32_n47# Gnd 0.42fF
C1114 sumblock_0/xor1_2/a_n12_n44# Gnd 0.50fF
C1115 carry0 Gnd 1.85fF
C1116 vdd Gnd 1.63fF
```

```
C1117 gnd Gnd 0.54fF
C1118 sum2 Gnd 0.91fF
C1119 vdd Gnd 0.43fF
C1120 sumblock_0/xor1_1/a_32_n47# Gnd 0.42fF
C1121 sumblock_0/xor1_1/a_n12_n44# Gnd 0.50fF
C1122 carry1 Gnd 1.73fF
C1123 p2 Gnd 1.44fF
C1124 vdd Gnd 1.63fF
C1125 gnd Gnd 0.54fF
C1126 sum3 Gnd 0.92fF
C1127 vdd Gnd 0.43fF
C1128 sumblock_0/xor1_0/a_32_n47# Gnd 0.42fF
C1129 sumblock_0/xor1_0/a_n12_n44# Gnd 0.50fF
C1130 carry2 Gnd 1.75fF
C1131 p3 Gnd 1.68fF
C1132 vdd Gnd 1.63fF
C1133 gnd Gnd 0.28fF
C1134 gnd Gnd 0.23fF
C1135 gnd Gnd 0.07fF
C1136 gnd Gnd 0.00fF
C1137 gnd Gnd 0.12fF
C1138 gnd Gnd 0.42fF
C1139 gnd Gnd 0.48fF
C1140 gnd Gnd 0.11fF
C1141 vdd Gnd 0.64fF
C1142 vdd Gnd 0.30fF
C1143 gnd Gnd 0.57fF
C1144 gnd Gnd 0.81fF
C1145 gnd Gnd 0.11fF
C1146 vdd Gnd 0.11fF
C1147 gnd Gnd 0.91fF
C1148 vdd Gnd 0.25fF
C1149 vdd Gnd 0.71fF
C1150 gnd Gnd 1.42fF
C1151 gnd Gnd 0.19fF
C1152 gnd Gnd 0.15fF
C1153 vdd Gnd 0.11fF
C1154 vdd Gnd 1.64fF
C1155 vdd Gnd 2.46fF
C1156 vdd Gnd 0.08fF
C1157 gnd Gnd 0.82fF
C1158 p1 Gnd 3.71fF
C1159 vdd Gnd 0.19fF
C1160 gnd Gnd 0.39fF
C1161 t4_4and Gnd 0.14fF
C1162 vdd Gnd 0.38fF
C1163 cla_0/4and_1/a_13_5# Gnd 0.52fF
C1164 p3 Gnd 0.29fF
```

```
C1165 p2 Gnd 0.40fF
C1166 g0 Gnd 0.48fF
C1167 vdd Gnd 0.43fF
C1168 vdd Gnd 0.99fF
C1169 gnd Gnd 0.34fF
C1170 t3_4and Gnd 0.23fF
C1171 vdd Gnd 0.25fF
C1172 cla_0/4and_0/a_13_5# Gnd 0.52fF
C1173 p2 Gnd 0.64fF
C1174 p1 Gnd 0.65fF
C1175 p0 Gnd 0.62fF
C1176 vdd Gnd 0.43fF
C1177 vdd Gnd 0.99fF
C1178 gnd Gnd 0.18fF
C1179 sum1 Gnd 0.26fF
C1180 vdd Gnd 0.31fF
C1181 cla_0/3or_0/a_0_n30# Gnd 0.46fF
C1182 t2_2and Gnd 0.34fF
C1183 t2_3and Gnd 0.29fF
C1184 vdd Gnd 1.21fF
C1185 gnd Gnd 0.41fF
C1186 t4_5and Gnd 0.14fF
C1187 vdd Gnd 0.46fF
C1188 cla_0/5and_0/a_13_5# Gnd 0.62fF
C1189 p3 Gnd 0.69fF
C1190 p2 Gnd 0.37fF
C1191 p1 Gnd 1.16fF
C1192 p0 Gnd 1.75fF
C1193 vdd Gnd 0.43fF
C1194 vdd Gnd 1.18fF
C1195 vdd Gnd 0.31fF
C1196 vdd Gnd 0.28fF
C1197 cla_0/2or_0/a_0_n30# Gnd 0.35fF
C1198 t1_2and Gnd 0.29fF
C1199 g0 Gnd 0.23fF
C1200 vdd Gnd 1.03fF
C1201 sum3 Gnd 0.25fF
C1202 vdd Gnd 0.31fF
C1203 cla_0/5or_0/a_0_n44# Gnd 0.65fF
C1204 g3 Gnd 0.89fF
C1205 t4_2and Gnd 0.61fF
C1206 t4_3and Gnd 0.55fF
C1207 t4_4and Gnd 0.51fF
C1208 t4_5and Gnd 0.45fF
C1209 vdd Gnd 1.55fF
C1210 gnd Gnd 0.33fF
C1211 t4_2and Gnd 0.17fF
C1212 vdd Gnd 0.28fF
```

```
C1213 cla_0/2and_3/a_13_5# Gnd 0.37fF
C1214 p3 Gnd 0.53fF
C1215 g2 Gnd 1.27fF
C1216 vdd Gnd 0.43fF
C1217 vdd Gnd 0.67fF
C1218 gnd Gnd 0.31fF
C1219 t3_2and Gnd 0.11fF
C1220 vdd Gnd 0.28fF
C1221 cla_0/2and_2/a_13_5# Gnd 0.37fF
C1222 p2 Gnd 0.52fF
C1223 vdd Gnd 0.43fF
C1224 vdd Gnd 0.67fF
C1225 gnd Gnd 0.33fF
C1226 t2_2and Gnd 0.17fF
C1227 vdd Gnd 0.36fF
C1228 cla_0/2and_1/a_13_5# Gnd 0.37fF
C1229 p1 Gnd 0.51fF
C1230 g0 Gnd 0.46fF
C1231 vdd Gnd 0.43fF
C1232 vdd Gnd 0.67fF
C1233 gnd Gnd 0.29fF
C1234 t1_2and Gnd 0.17fF
C1235 cla_0/2and_0/a_13_5# Gnd 0.37fF
C1236 p0 Gnd 0.36fF
C1237 vdd Gnd 0.43fF
C1238 vdd Gnd 0.67fF
C1239 gnd Gnd 0.37fF
C1240 t4_3and Gnd 0.17fF
C1241 vdd Gnd 0.33fF
C1242 cla_0/3and_2/a_13_5# Gnd 0.43fF
C1243 p3 Gnd 0.46fF
C1244 p2 Gnd 0.59fF
C1245 g1 Gnd 1.71fF
C1246 vdd Gnd 0.43fF
C1247 vdd Gnd 0.83fF
C1248 gnd Gnd 0.32fF
C1249 t3_3and Gnd 0.18fF
C1250 vdd Gnd 0.06fF
C1251 cla_0/3and_1/a_13_5# Gnd 0.43fF
C1252 p2 Gnd 0.57fF
C1253 g0 Gnd 0.45fF
C1254 vdd Gnd 0.43fF
C1255 vdd Gnd 0.83fF
C1256 gnd Gnd 0.36fF
C1257 sum2 Gnd 0.23fF
C1258 vdd Gnd 0.28fF
C1259 cla_0/4or_0/a_0_n37# Gnd 0.54fF
C1260 t3_3and Gnd 0.51fF
```

```
C1261 t3_2and Gnd 0.37fF
C1262 t3_4and Gnd 0.31fF
C1263 vdd Gnd 1.39fF
C1264 gnd Gnd 0.36fF
C1265 t2_3and Gnd 0.14fF
C1266 vdd Gnd 0.39fF
C1267 cla_0/3and_0/a_13_5# Gnd 0.43fF
C1268 p1 Gnd 0.43fF
C1269 p0 Gnd 0.37fF
C1270 c_in Gnd 0.29fF
C1271 vdd Gnd 0.43fF
C1272 vdd Gnd 0.83fF

.tran 0.05n 320n

.control
run

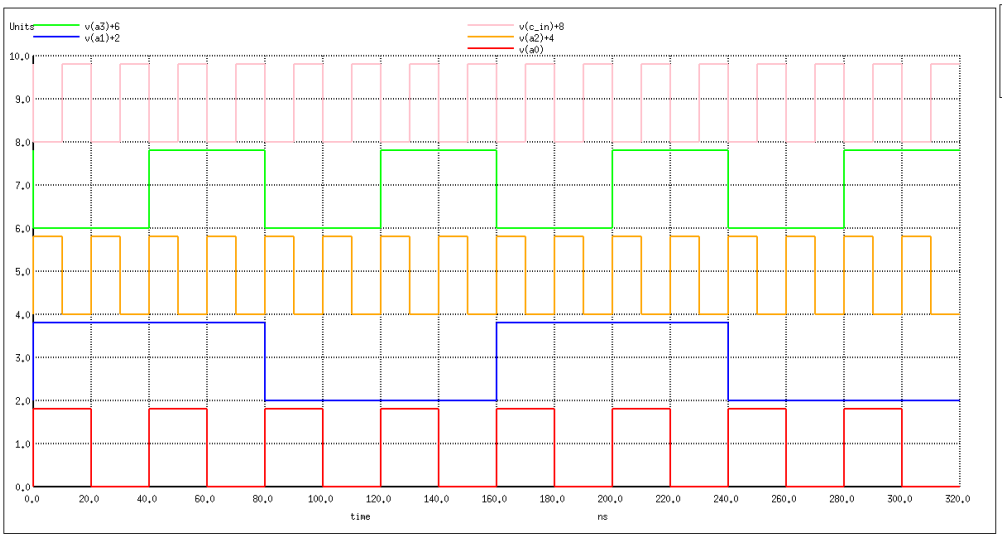
set color0 = white
set color1 = black

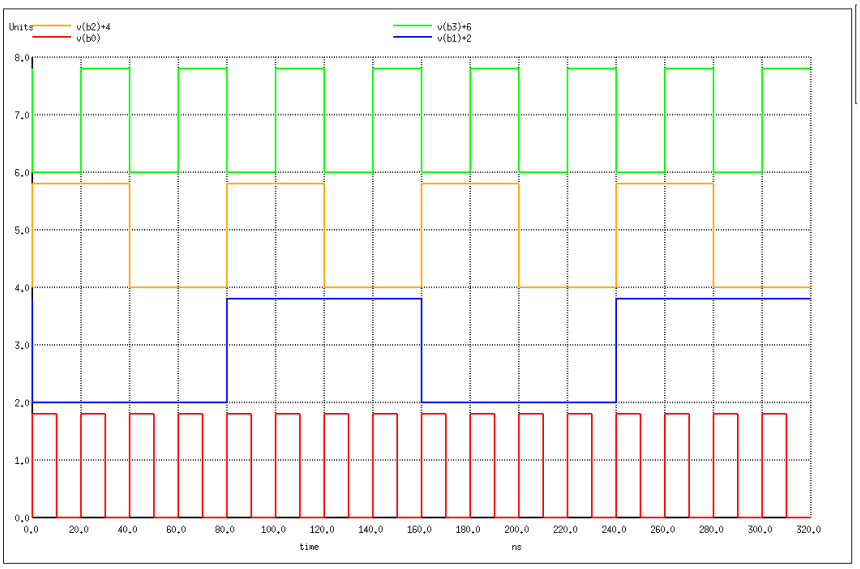
plot (v(carry3)*16 +v(sum3)*8 + v(sum2)*4 +v(sum1)*2 +v(sum0))/1.8
plot (v(a3)*8+v(a2)*4+v(a1)*2+v(a0)+v(b3)*8+v(b2)*4+v(b1)*2+v(b0)+v(c_in))/1.8

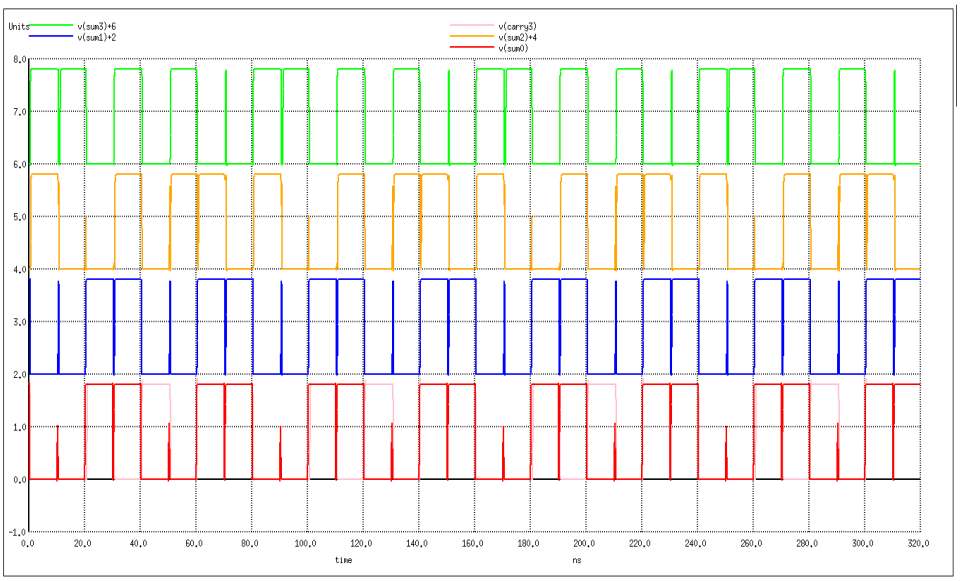
*plot v(p1) v(a1)+2 v(b1)+4

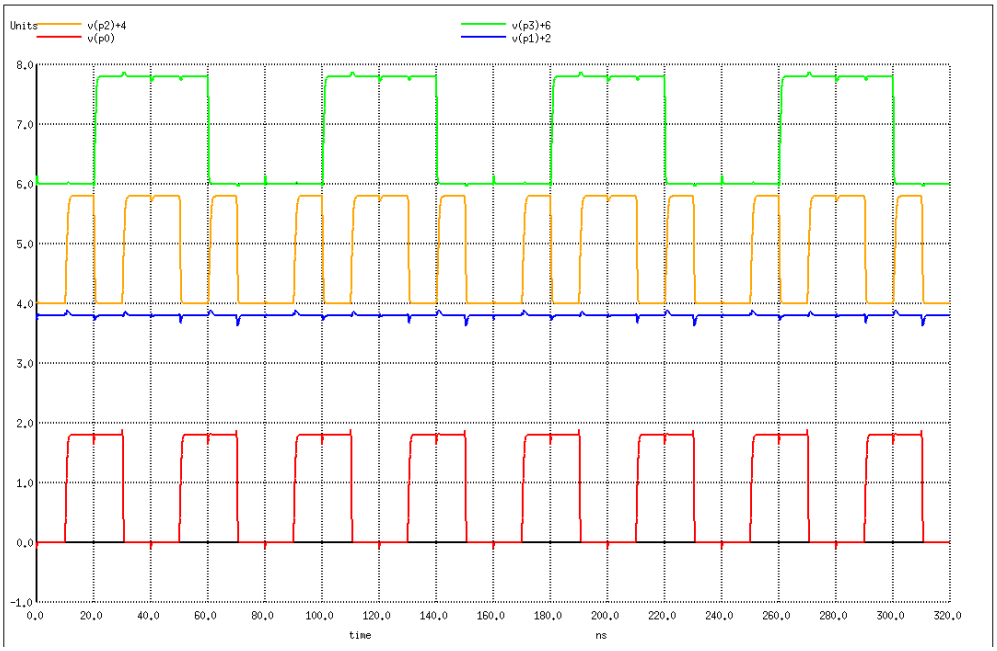

.endc
.end
```

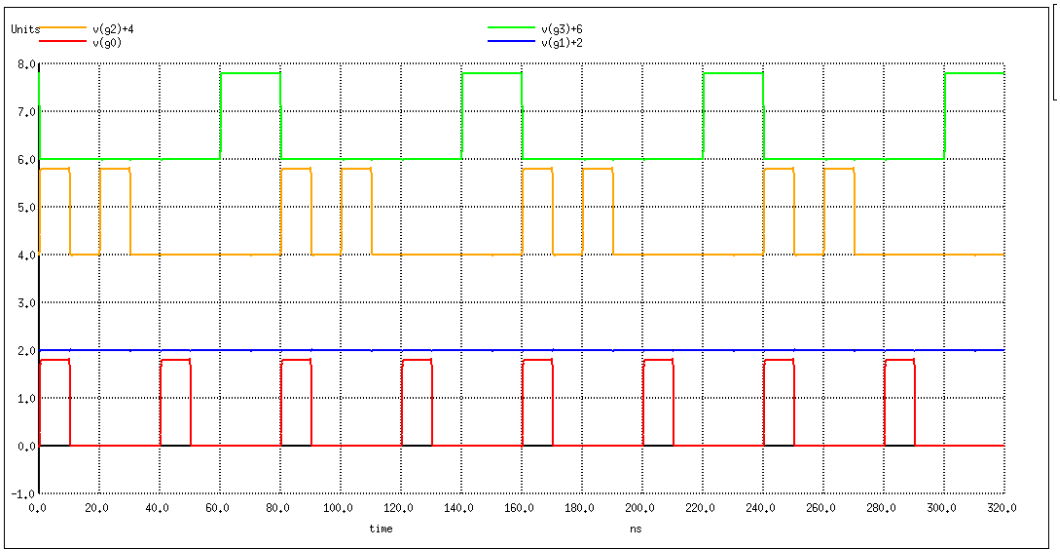
The outputs are given below,

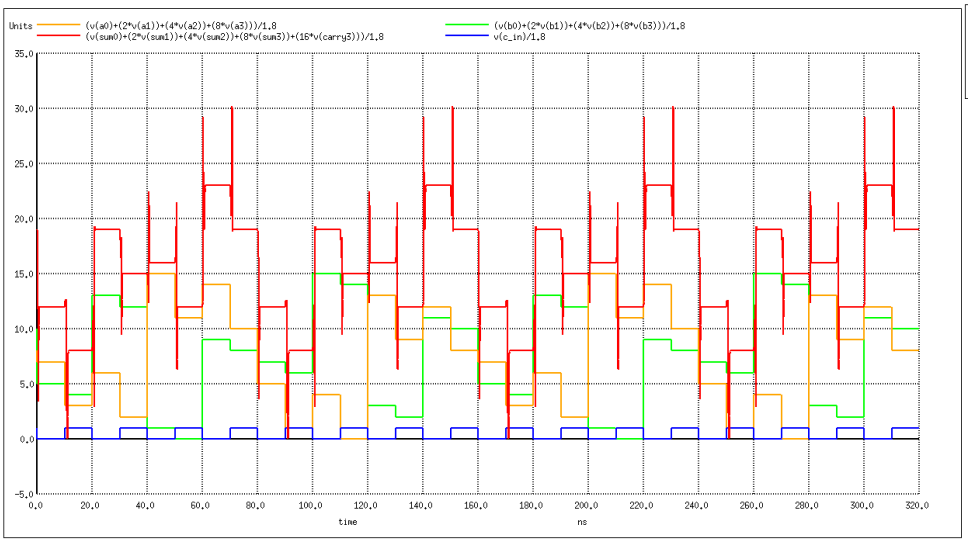



Units
v(b2)+4
v(b0)
v(b3)+6
v(b1)+2
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0
320.0
time
ns


Units
v(sum3)+6
v(sum1)+2
v(carry3)
v(sum2)+4
v(sum0)
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0
320.0
time
ns


Units
v(p2)+4
v(p0)
v(p3)+6
v(p1)+2
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0
320.0
time
ns


Units
v(g2)+4
v(g0)
v(g3)+6
v(g1)+2
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0
320.0
time
ns



Question 10

The structural Verilog code for the CLA adder is given below.

```
// 4-Bit Carry Look-Ahead Adder
module CLA (a,b,Cin,sum,carry);

    // Inputs
    input [3:0] a;
    input [3:0] b;
    input Cin;

    //Outputs
    output [3:0] sum;
    output [3:0] carry;

    //Intermediates
    //Propagate
    wire [3:0] p;
    //Generate
    wire [3:0] g;
    wire w1,w2,w3,w4;

    //Generate g_i = a_i AND b_i
    and GEN0(g[0],a[0],b[0]);
    and GEN1(g[1],a[1],b[1]);
    and GEN2(g[2],a[2],b[2]);
```

```
    and GEN3(g[3],a[3],b[3]);

    //Propagate p_i = a_i XOR b_i
    xor PROP0(p[0],a[0],b[0]);
    xor PROP1(p[1],a[1],b[1]);
    xor PROP2(p[2],a[2],b[2]);
    xor PROP3(p[3],a[3],b[3]);

    //Carry carry_{i+1} = (p_i AND c_i) OR g_i
    and AND0(w0,p[0],Cin);
    or OR0(carry[0],w0,g[0]);

    and AND11(w11,p[1],p[0],Cin);
    and AND12(w12,p[1],g[0]);
    or OR1(carry[1],w11,w12,g[1]);
    //and AND1(w2,p[1],carry[0]);
    //or OR1(carry[1],w2,g[1]);

    and AND21(w21,p[2],p[1],p[0],Cin);
    and AND22(w22,p[2],p[1],g[0]);
    and AND23(w23,p[2],g[1]);
    or OR2(carry[2],w21,w22,w23,g[2]);
    //and AND2(w3,p[2],carry[1]);
    //or OR2(carry[2],w3,g[2]);

    and AND31(w31,p[3],p[2],p[1],p[0],Cin);
    and AND32(w32,p[3],p[2],p[1],g[0]);
    and AND33(w33,p[3],p[2],g[1]);
    and AND34(w34,p[3],g[2]);
    or OR3(carry[3],w31,w32,w33,w34,g[3]);
    //and AND3(w4,p[3],carry[2]);
    //or OR3(Cout,w4,g[3]);

    //Sum sum_i = p_i XOR carry_i
    xor SUM0(sum[0],p[0],Cin);
    xor SUM1(sum[1],p[1],carry[0]);
    xor SUM2(sum[2],p[2],carry[1]);
    xor SUM3(sum[3],p[3],carry[2]);

endmodule
```

The test bench is given below,

```
`timescale 1ns/1ps
module CLA_clked_testbench();

    reg CLK;
```

```
    reg [3:0] a;
    reg [3:0] b;
    reg Cin;
    output [3:0] sum;
    output Cout;

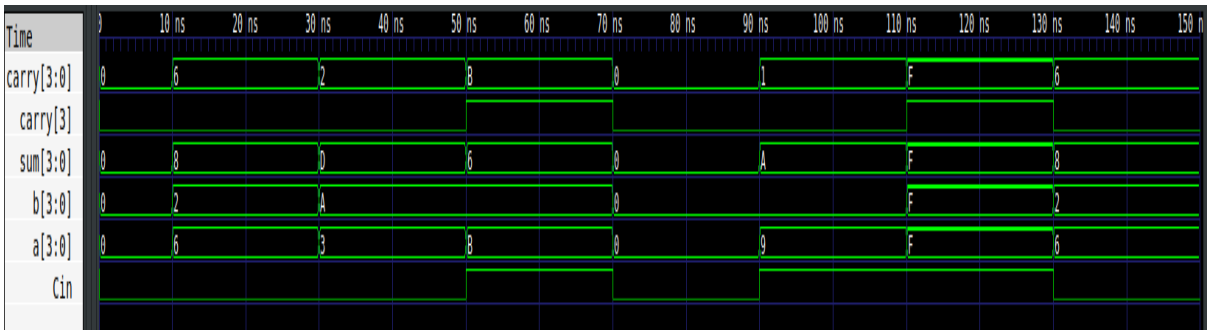
    CLA_clked abc(.CLK(CLK),.a(a),.b(b),.Cin(Cin),.sum(sum),.Cout(Cout));

    initial begin
        $dumpfile("CLA_clked.vcd");
        $dumpvars(0,CLA_clked_testbench);
        a = 0;
        b = 0;
        Cin = 0;
        CLK = 0;
        #10 a = 4'd3; b = 4'd2; Cin = 1;
        $monitor( "a = %b, b = %b , Cin = %b , Cout = %b, sum =
%b",a,b,Cin,Cout,sum);
        #20 a = 4'd15; b = 4'd15; Cin = 1;
        $monitor( "a = %b, b = %b , Cin = %b , Cout = %b, sum =
%b",a,b,Cin,Cout,sum);
        #20 a = 4'd5; b = 4'd5; Cin = 0;
        $monitor( "a = %b, b = %b , Cin = %b , Cout = %b, sum =
%b",a,b,Cin,Cout,sum);
        #20 a = 4'd15; b = 4'd1; Cin = 1;
        $monitor( "a = %b, b = %b , Cin = %b , Cout = %b, sum =
%b",a,b,Cin,Cout,sum);
        #20
        $finish;
    end

    always #10 CLK = ~CLK;

endmodule
```

The output waveform is given below,



The behavioural code for the CLA adder with flip flops is given below,

```
// 4-Bit Carry Look-Ahead Adder with D Flip-Flops
module CLA_clked (
    // Inputs
    input CLK,
    input [3:0] a,
    input [3:0] b,
    input Cin,

    //Outputs
    output reg [3:0] sum,
    output reg Cout
    // Cout = carry[3];
    );

    //Intermediates
    reg [3:0] Q_a;
    reg [3:0] Q_b;
    wire [3:0] D_sum;
    wire D_Cout;

    always @(posedge CLK)
    begin
        //Input D flip-flops
        Q_a = a;
        Q_b = b;
    end

    //CLA
    CLA abc(.a(Q_a),.b(Q_b),.Cin(Cin),.sum(D_sum),.Cout(D_Cout));

    always @(posedge CLK)
    begin
        //Output D flip-flops
        sum = D_sum;
        Cout = D_Cout;
    end
endmodule
```

```
`timescale 1ns/1ps
module CLA_clked_testbench();

    reg CLK;
    reg [3:0] a;
    reg [3:0] b;
```

```
    reg Cin;
    output [3:0] sum;
    output Cout;

    CLA_clked abc(.CLK(CLK),.a(a),.b(b),.Cin(Cin),.sum(sum),.Cout(Cout));

    initial begin
        $dumpfile("CLA_clked.vcd");
        $dumpvars(0,CLA_clked_testbench);
        a = 0;
        b = 0;
        Cin = 0;
        CLK = 0;
        #10 a = 4'd3; b = 4'd2; Cin = 1;
        $monitor( "a = %b, b = %b , Cin = %b , Cout = %b, sum =
%b",a,b,Cin,Cout,sum);
        #20 a = 4'd15; b = 4'd15; Cin = 1;
        $monitor( "a = %b, b = %b , Cin = %b , Cout = %b, sum =
%b",a,b,Cin,Cout,sum);
        #20 a = 4'd5; b = 4'd5; Cin = 0;
        $monitor( "a = %b, b = %b , Cin = %b , Cout = %b, sum =
%b",a,b,Cin,Cout,sum);
        #20 a = 4'd15; b = 4'd1; Cin = 1;
        $monitor( "a = %b, b = %b , Cin = %b , Cout = %b, sum =
%b",a,b,Cin,Cout,sum);
        #20
        $finish;
    end

    always #10 CLK = ~CLK;

endmodule
```

And the output waveform is,