A Level-Crossing Sampling Scheme For A/D Conversion

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1 Abstract

A/D (Analog to Digital) conversion can be viewed as representing a signal in-terms of a mapping between discrete time values and their corresponding amplitude values, which belong to a finite set of real numbers, which is called sampling. A new type of sampling scheme is introduced based on multiple level-crossings, where samples instants are recorded when the signal crosses any of the user-defined quantization levels. This results in generation of non-uniform samples, which have to converted to uniform samples in order to be used in most of the real-life applications. Nyquist rate sampling would need a large number of quantization levels to receive high resolution (while using a small bandwidth), while zero-crossing sampling would require us to know the crossing instants with high precision, for proper reconstruction of the signal. The non-uniform samples are first passed through to a polynomial interpolator to generate uniform samples and then passed through a decimator to improve the resolution. The paper analyses the performance of such a sampling scheme along with its tradeoffs in terms of speed, resolution, and real time implementations. We try to find various parameters which on altering we can improve our SNR.

2.1 Sampling and Its Need

Analog signals in real life are continuous and there are infinitely many points and amplitude levels between any given time intervals in the signal. So, theoretically, it would take infinite memory and infinite computation time if we were to store and process these signals. Computers and other digital applications have finite memory and computational limitations. So, storing and processing analog signals in its raw form is not a viable method to process them. Here comes the need of sampling.

Sampling is the process of converting continuous-time signals into discrete-time signals by representing it as a sequence of samples. The most common and primitive method to do sampling to take samples at uniform time intervals. So, the continuous-time signal is converted into discrete-time signal as,

$$x[n] = x(nT_s)$$

Where T_s is the sampling frequency. Since we are taking samples at different time points, we lose information about the original continuous-time signal if sampling is not done methodically.

2.2 Nyquist-Shannon Sampling Theorem

The Nyquist-Shannon sampling theorem states that it is possible to perfectively reconstruct a bandlimited signal from its samples provided that the sampling frequency is at

least twice the maximum frequency present in the signal. This quantity is referred to as the Nyquist rate of the signal and is given by

$$\omega_s > 2\omega_m$$

Where ω_m is the maximum frequency of the signal.

2.3 Analog-to-Digital Converter (ADC)

For practical applications, analog signals are converted into digital signals using Analog-to-Digital Converters. However, ADCs are prone to quantization errors, and ultimately, the performance of the ADC is represented by the SNR it can produce and its resolution. An ADC typically has certain quantization levels associated with it.

2.4 Signal-to-Noise Ratio (SNR)

SNR is defined as the signal power to the noise power. Typically, it is expressed in terms of decibels (dB).

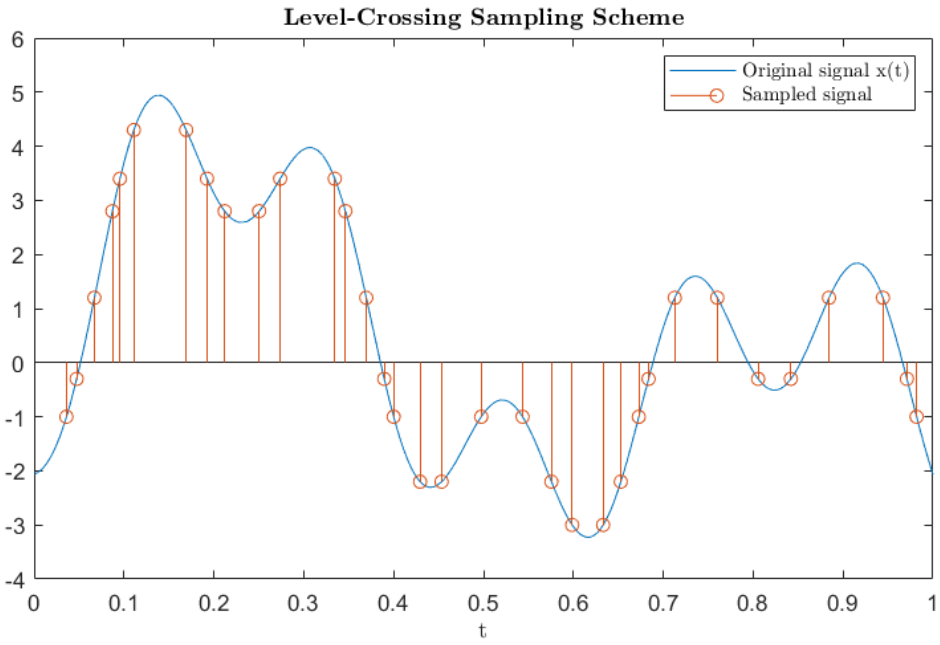
$$\text{SNR} = \frac{P_{signal}}{P_{noise}}$$

3 Level-Crossing Sampling and A/D Conversion

3.1 Level-Crossing Sampling

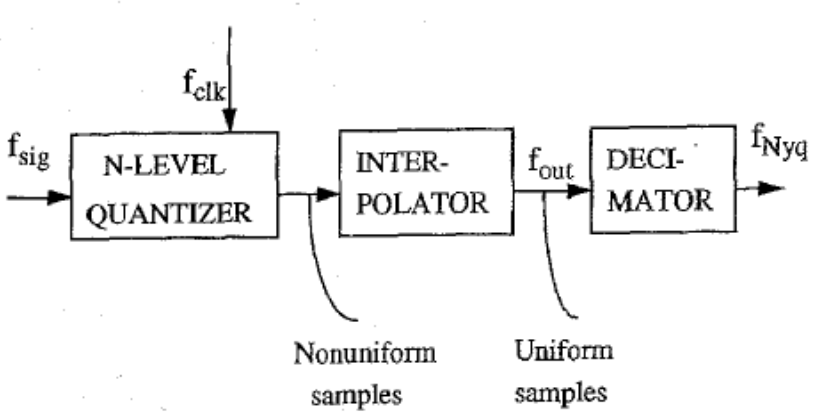
Although uniform sampling above the Nyquist rate is a very good sampling techniques, there are certain situations where other sampling techniques might perform better. If we to implement uniform sampling using an ADC, we would most probably require a large number of quantization levels to achieve the desired ADC resolution. Other sampling techniques such as the zero-crossing sampling where the signal is represented as instants where it crosses a pre-specified value might require extremely high time resolution to achieve the desired ADC performance. These two samplings can be thought of as lying on opposite ends of the sampling spectrum, and naturally a question arises whether it is possible to design and implement a sampling scheme intermediate between these two, and one which has characteristics similar to these sampling schemes.

Our assigned paper proposes one such sampling scheme called the ‘Level-Crossing’ sampling scheme. The idea behind the sampling technique is simple. Samples are recorded as instants where the signal crosses certain pre-determined quantization levels. This resultants in samples that are non-uniformly spaced in time, where each sample is represented as an amplitude-time ordered pair. One major advantage of the level-crossing sampling scheme over traditional sampling schemes is that the sampling is dynamic. If a high frequency signal is sampled, since it would cross the pre-determined quantization levels a large number of times, a large number of samples will be recorded. On the contrary, if the signal has a low frequency, it would cross the quantization levels lesser number of times and fewer samples will be recorded.



3.2 A/D Conversion Using the Level-Crossing Sampling Scheme

The paper also implements the sampling scheme in an ADC. An ADC employing this sampling scheme would not need as much amplitude resolution as the uniform sampling scheme or levels of time resolution required for the zero-crossing sampling scheme. The quantizer that is used to employ the level-crossing sampling scheme and generates non-uniform samples can be further extended to include other components for extended applications that might require uniform samples. The architecture of such an A/D converter is given below.



So, the extended ADC can be thought to have three primary parts – the quantizer, the interpolator and the decimator. The process of analog to digital conversion can be expressed as three key steps –

1. Signal Acquisition and Quantization Stage

The analog signal is fed into the N-Level quantizer. The quantizer employs the level crossing sampling scheme, and records samples each time the signal crosses any of the pre-defined quantization levels as amplitude-time ordered pairs where the amplitude is the quantization level that is crossed, and the time is the time instant at which quantization level was crossed. This generates non-uniform samples.

2. Interpolator Stage

   The non-uniform samples are fed into the interpolator which interpolates the samples and outputs uniformly spaced samples at a pre-defined sampling frequency of f_{out}. Typically, polynomial interpolation is carried out with a certain interpolation order.

3. Decimator Stage

   The uniform samples coming out from the interpolator are passed into a decimator which removes any noise that may have crept in through the process and down-samples the uniform samples to a sampling frequency which may be chosen as the Nyquist frequency f_{Nyq}. Decimators will typically increase the resolution of ADCs by filtering out the noise present.

If the ADC is to be implemented practically, we need account for a variety of parameters. The quantizer will have certain amplitude resolution associated with it, and hence the quantization levels are known only within a certain uncertainty limit. We denote the maximum uncertainty as δ_a. Typically, for a quantizer that has L bits of resolution, L can be express as,

$$L = -\log_2(2\delta_a)$$

where the signal amplitude is scaled to unity. The number of quantization levels present in the quantizer will typically be less than 2^L. The uncertainty in the quantization levels can be thought to be uniformly distributed in the range $(-\delta_a, \delta_a)$. The quantizer will also have a certain clock frequency f_{clk} to measure the time instants. So, samples generated from the level-crossings will also have certain time resolution associated with it, along with the amplitude resolution. Consider that $T = \frac{1}{\mathrm{f_{clk}}}$. Then T will be determined by the time resolution R of the quantizer. Since R is a measure of the time accuracy, T is inversely proportional to R. Then, R can be expressed as,

$$R = \frac{f_{clk}}{f_s}$$

where f_s is the frequency of the input signal. So, the time instants can be recorded only as integer multiples of T, wherein lies the time error. The number of quantization levels, R and L are tradeoffs associated with the cost, speed, and efficiency of the quantizer and hence their choice will affect the performance of the ADC. R and L jointly constitute to the quantization error equally and hence increasing one value while the other is kept fixed will increase the resolution of the quantizer only by very tiny margins that tend to a saturation value.

The interpolator will have a pre-defined interpolation order with which it performs polynomial interpolation. Typically, polynomial interpolation will introduce truncation errors, as opposed to the rounding off errors associated with the quantizer. We observe that the

truncation errors are more prominent when the interpolation order is above 4 and so, most polynomial interpolators employ an interpolation order of 2, which gives decent interpolation. Hence, the choice of interpolation order also will affect the performance of the ADC.

The extent of resolution increase the decimator brings will primarily depend on the noise band present. The extent of decimation depends upon the decimation factor DF, which is expressed as,

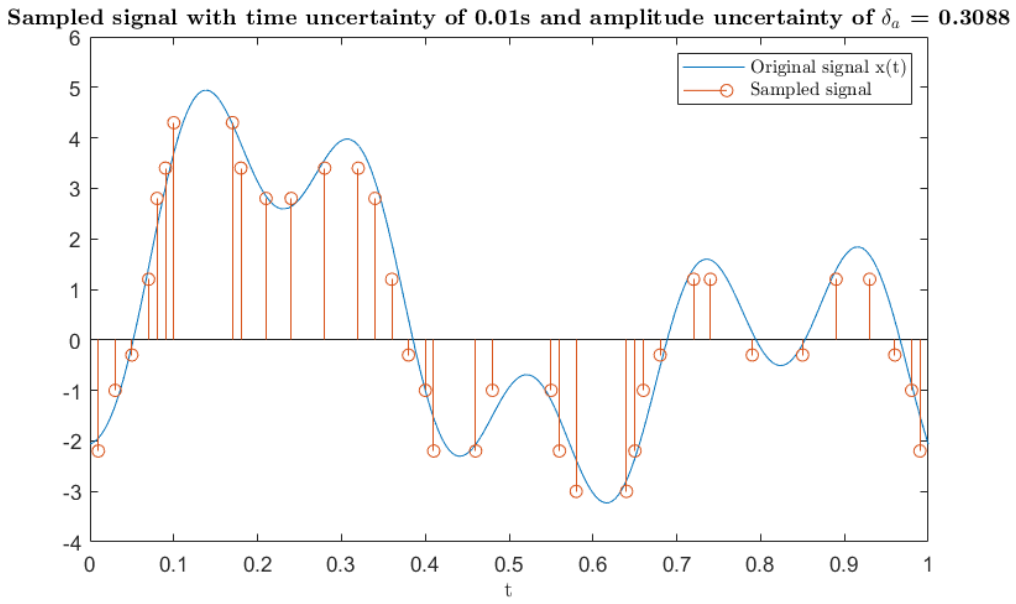
$$DF = \frac{f_{out}}{f_{Nyq}}$$

Higher the decimation factor, better is the performance of the decimator, which comes with increased execution times. So, DF is a tradeoff associated with the ADC. The paper discusses these tradeoffs through various plots and simulations and suggests an optimal design procedure to attain the desired values of these parameters.

4 Simulations and Results

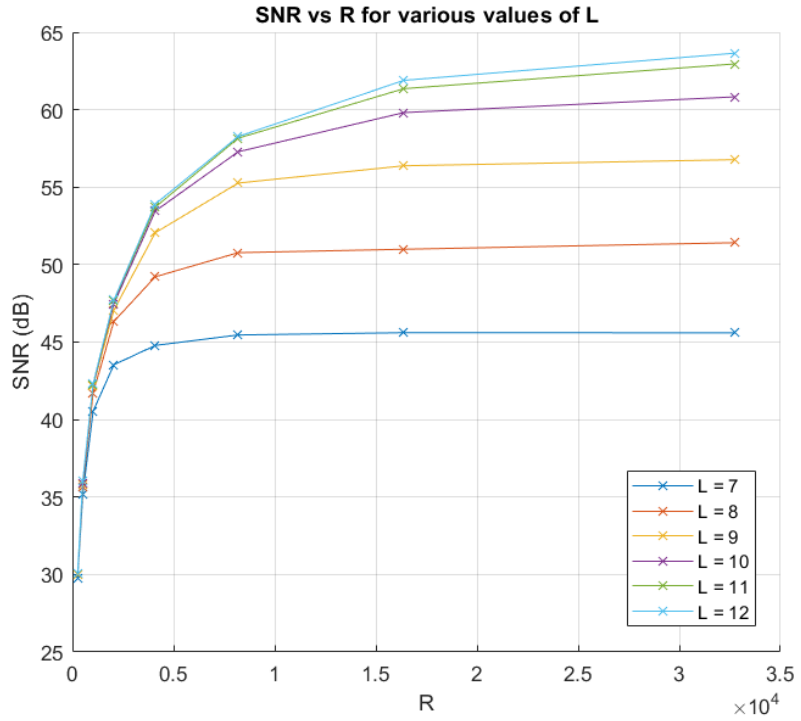
So, the ADC can be designed keeping in mind the number of quantization levels, R, L, interpolation order and DF. We wish to implement the level-crossing sampling scheme and design the ADC and discuss these tradeoffs using MATLAB codes, simulations, and plots.

The quantizer with a certain value of R and L will not perfectly record the samples of the input signal. When the quantizer was set up with a time uncertainty of 0.01s and an amplitude uncertainty of 0.3088, the quantizer output was as follows,

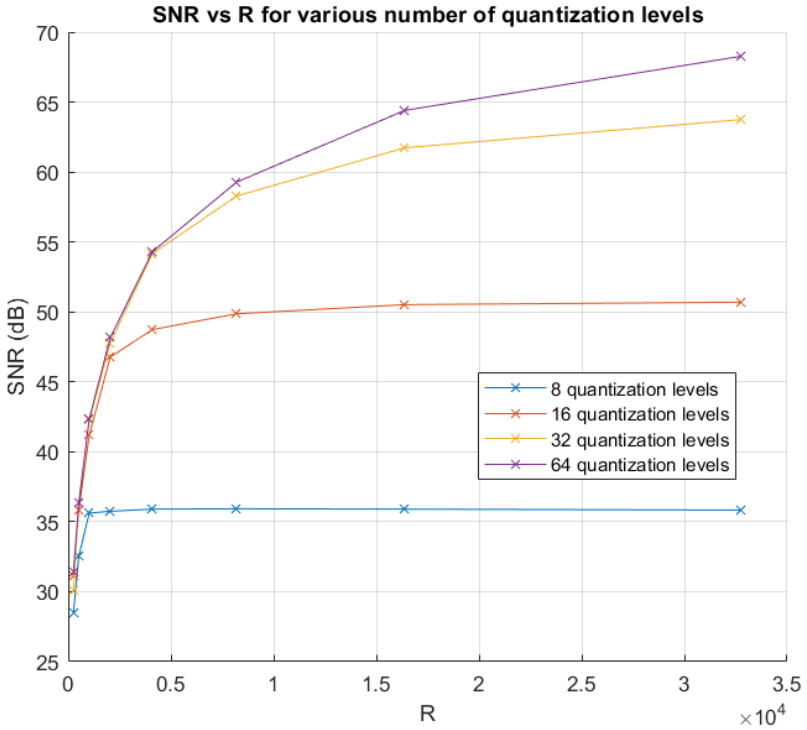


We can observe that the samples are shifted to the left slightly, and the amplitude levels are also off by a margin. Note that this is a case when R and L were taken to be much lower than what an actual ADC might have. The quantizer output in practical implementations will only differ slightly from the ideal values.

Through our simulations, we could observe that the performance of the quantizer for a fixed value of L, the SNR output greatly varied with R.



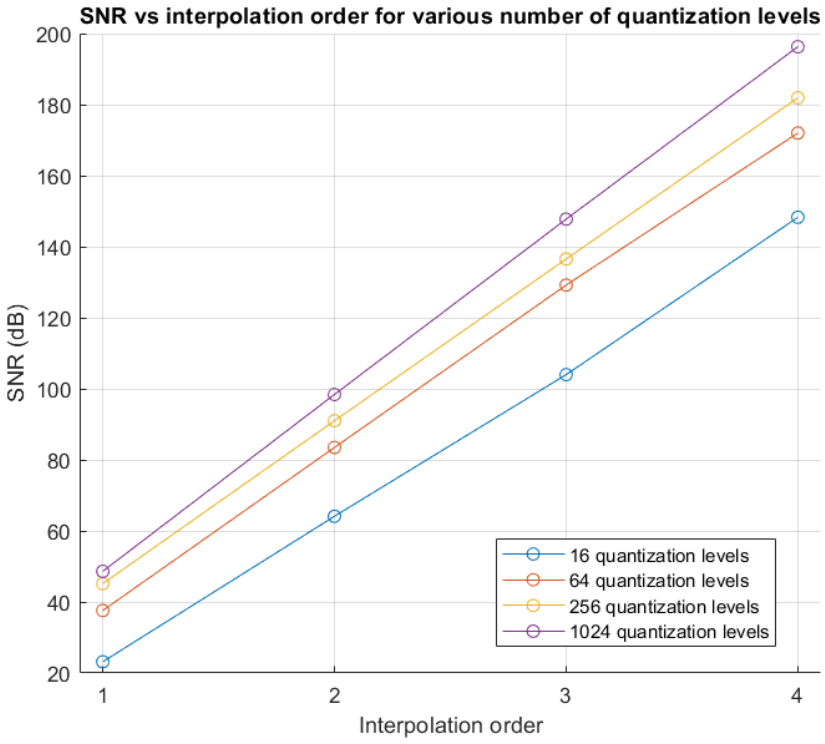
However, for all values of L, the SNR reaches a saturation value as R is varied. This behaviour is expected since L is a measure of amplitude resolution and without further increase in L, increase in R won't change the SNR much. The increase in time resolution is worthless unless the amplitude resolution is increased. This behaviour can also be seen with quantization levels, as depicted below.



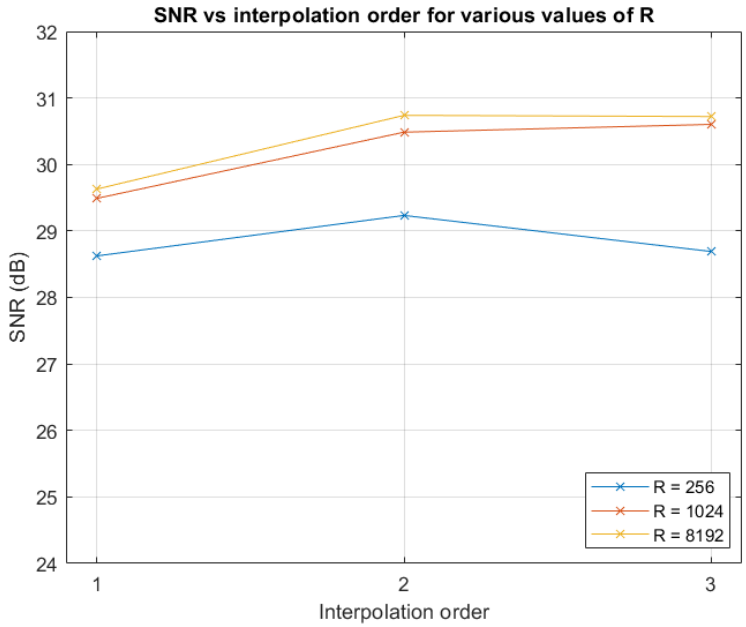
So, the number of quantization levels play a key role in SNR output. The increase in time resolution is worthless unless there are enough quantization levels (i.e., the level-crossings), to record the samples.

So, there is a need for a good balance between R, L and number of quantization levels, which will ultimately decide the performance of the quantizer part of the ADC.

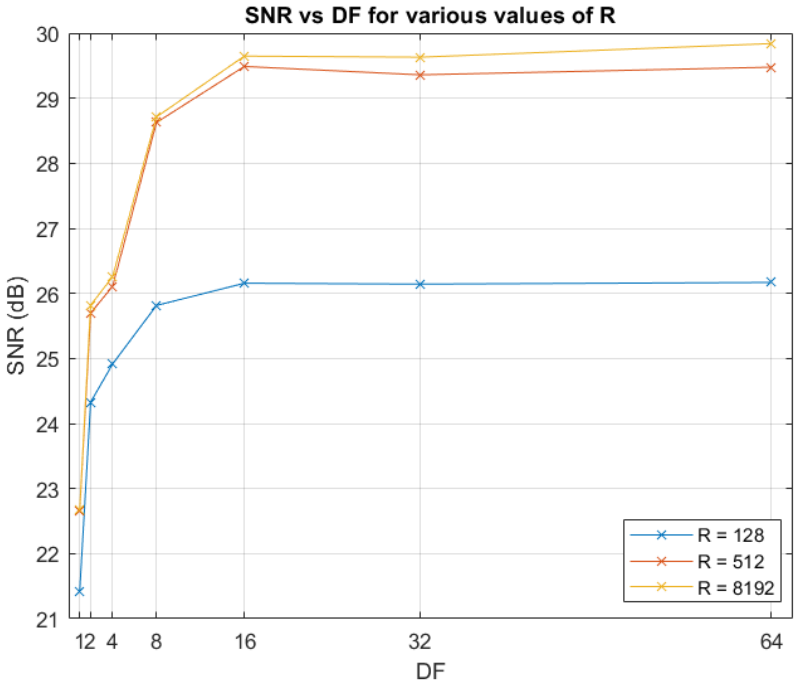
The performance of the interpolator for the extended applications depends upon the interpolation order used for polynomial interpolation. Through our simulations, we could find that there is a direct correlation between increasing the number of quantization levels, increasing the interpolation order (to an extent) and increasing the SNR output, when little or no amplitude uncertainty was present and for a fixed time resolution as depicted in the figure given below. There is a linear increase in SNR (in dB scale) when the interpolation order is increased by one. However, we could observe that this behaviour breaks slightly with interpolation orders of 5 and above. As discussed in the paper, interpolation order introduces truncation error, the uncertainty of which grows with increasing interpolation order. So, the SNR values varied largely and most of the times, it was much than the SNR output for lower interpolation order.



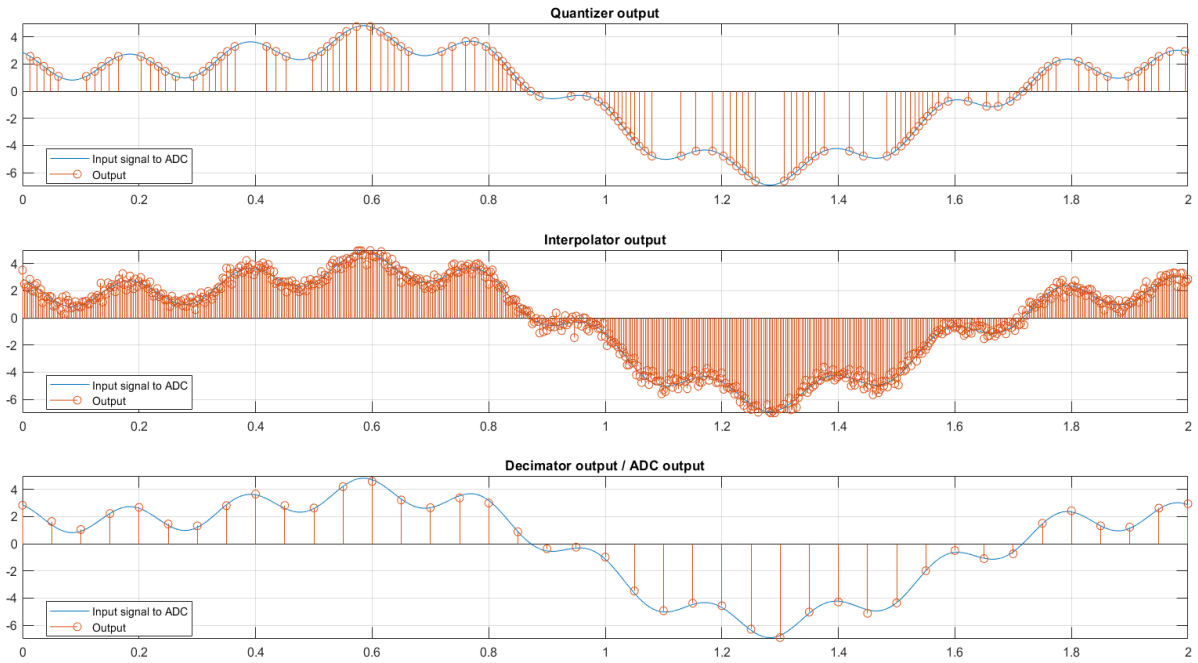
On keeping the quantization levels as constant and varying the time resolution and interpolation order, we could observe that beyond an interpolation order of 2, there was no or very slight increase in the SNR values, on increasing R. This is primarily due to increased truncation errors that come into play when the interpolation order is increased beyond 4.



The performance of the decimator depends upon the decimation factor DF which could be thought of as the down-sampling scale, while also filtering out any noise that may have crept in due to the circuitry in a practical ADC. Based on our simulations, the SNR reaches a saturation value when DF is about 16 to 32, on introducing noise into the interpolator, as beyond a frequency limit, the noise power is limited.



So, based on our simulations, for reasonable ADC performance for simple sinusoidal inputs, to obtain an SNR of around 27-29, the optimal minimum values are 32 quantization levels, L = 8, R = 2048, DF = 16 and an interpolation order of 2.



5 Conclusion

We have discussed about the level-crossing sampling scheme, which we can see is a general form of sampling where Nyquist rate and zero crossing sampling are just specific cases. We have defined the design architecture of an A/D converter that utilises our level crossing sampling scheme with three primary stage – the quantizer which employs the level-crossing sampling scheme, the interpolator, and the decimator; where each stage was briefly analysed along with defining the parameters that affect our SNR. We have plotted and discussed how our SNR changes when we change the values of R (time resolution), L (measure of amplitude resolution), the number of quantization levels, the interpolation order, and the decimation factor DF, so that we can choose the appropriate in order to design an ADC for a particular application (based on the requirements and the areas where we can compromise). Most of the real-life applications that use a polynomial interpolator (while making sure that it has quantization levels beyond a minimum value to ensure maximum SNR) has an interpolation order of around 2, and as we can see from our plots that the SNR doesn't significantly improve beyond order 2 for a particular value of R.

References

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