



[Designing with a complete simulation test bench for op amps, Part 3: Input-referred errors](#)

[Ian Williams](#) - September 13, 2018

Previous installments of this series discussed the need to verify SPICE model accuracy and how to measure the [output impedance](#) and [small-signal bandwidth](#) of [operational amplifier](#) (op amp) models. In part 3, I'll show how to measure some of the most common input-referred error sources that affect both DC and AC accuracy: common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR), input offset voltage (V_{os}), input bias current (I_b), and input offset current (I_{os}).

Common-mode rejection ratio

An op amp is designed to amplify the differential signal applied across its input pins while rejecting any common-mode signal present. Put simply, a differential signal is created when a voltage difference exists between nodes of a circuit. A common-mode signal, on the other hand, describes a signal that is common to two or more nodes of a circuit. The input common-mode voltage of an op amp is formally defined as the average voltage present across its two inputs, since either input may change over time.

Figure 1 gives an example of differential versus common-mode signals. In this case, the differential signal (V_{diff}) is the difference between the voltage present at $IN+$ and the voltage present at $IN-$. The common-mode signal (V_{cm}) is the 2.5V DC voltage present on both inputs.

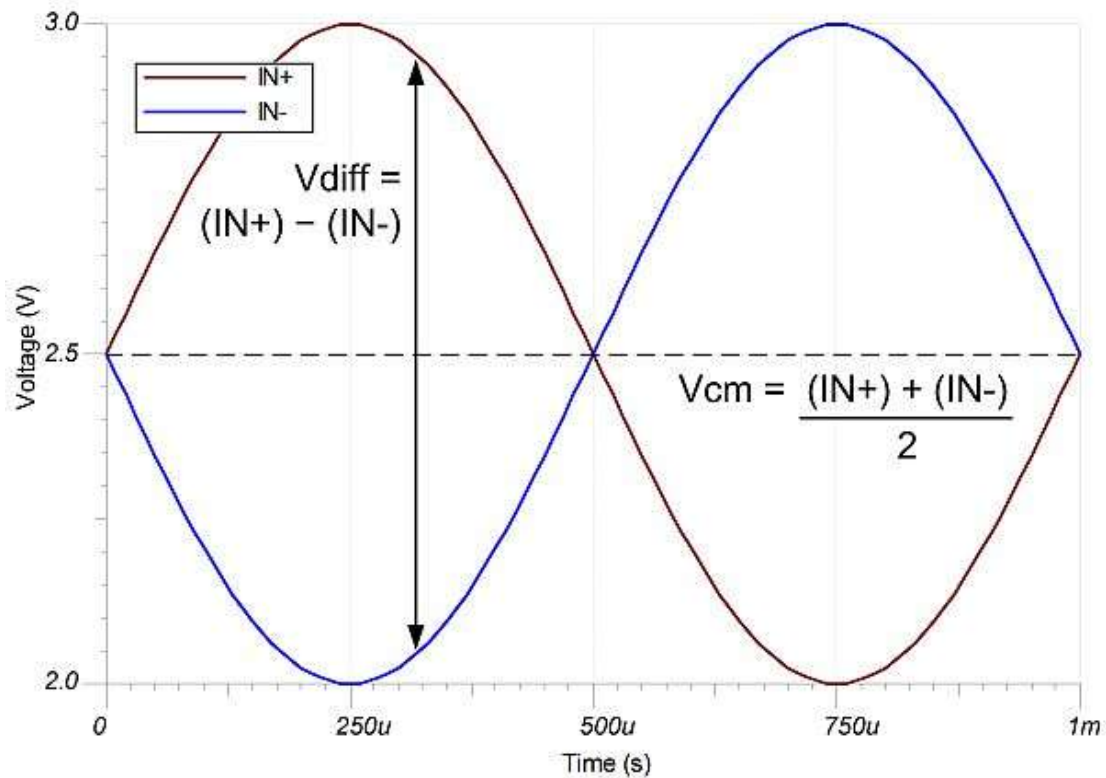


Figure 1 Differential signal vs. common-mode signal

Some typical examples of common-mode signals in op amp circuits are DC bias voltages and coupled noise from electromagnetic fields or parasitic circuit paths. You want an op amp to reject these common-mode input signals, because if they were amplified instead, the resulting output could cause major issues in the circuit's operation. The amplification of a large DC bias voltage could cause the amplifier output to exhibit a large offset or saturate at either of the power-supply rails. If noise was amplified, the true output signal could deteriorate or even be lost in the resulting noise at the amplifier output.

CMRR quantifies how well an op amp rejects these common-mode signals. When defined as a rejection in this manner, a higher value is better, since that means more of the common-mode signal is rejected and it will therefore have less effect on the op amp. However, since no real op amp has infinite CMRR, common-mode signals do have some measurable effect on an op amp's behavior.

Let's revisit the simplified small-signal model of an op amp, shown in **Figure 2**. CMRR is modeled as an error voltage source (V_{cmrr}) connected in series with the noninverting input. This error voltage changes with the applied common-mode voltage according to the CMRR specification of the op amp. Since CMRR is input-referred, V_{cmrr} is amplified by the closed-loop gain of the op amp circuit along with the differential input signal (V_e) to create the total output voltage (V_{out}).

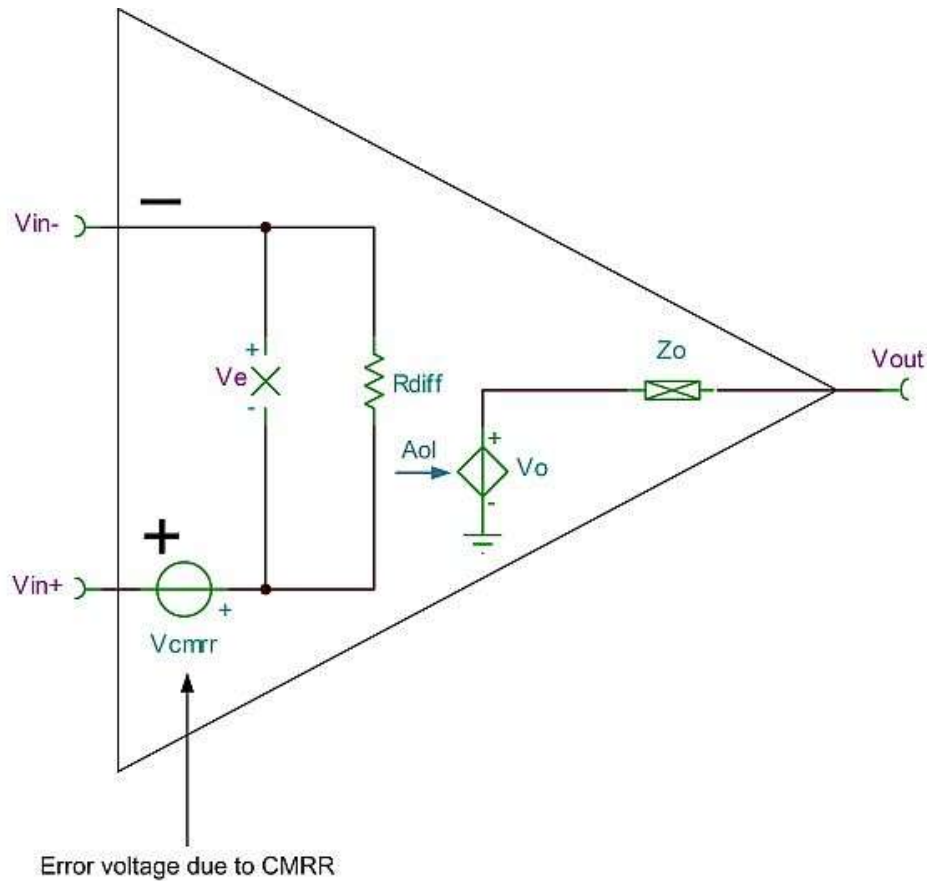


Figure 2 Simplified input-referred CMRR model

An op amp's common-mode rejection also changes over frequency. CMRR is highest at low frequencies, with most op amps exhibiting between 80dB (100 μ V of input-referred error per 1V of V_{cm}) and 160dB (10nV of input-referred error per 1V of V_{cm}) of common-mode rejection. The level of rejection rolls off at higher frequencies as the op amp runs out of bandwidth, so take care when selecting a device to ensure that CMRR performance is sufficient at the frequencies of interest.

Figure 3 is a typical CMRR vs. frequency curve.

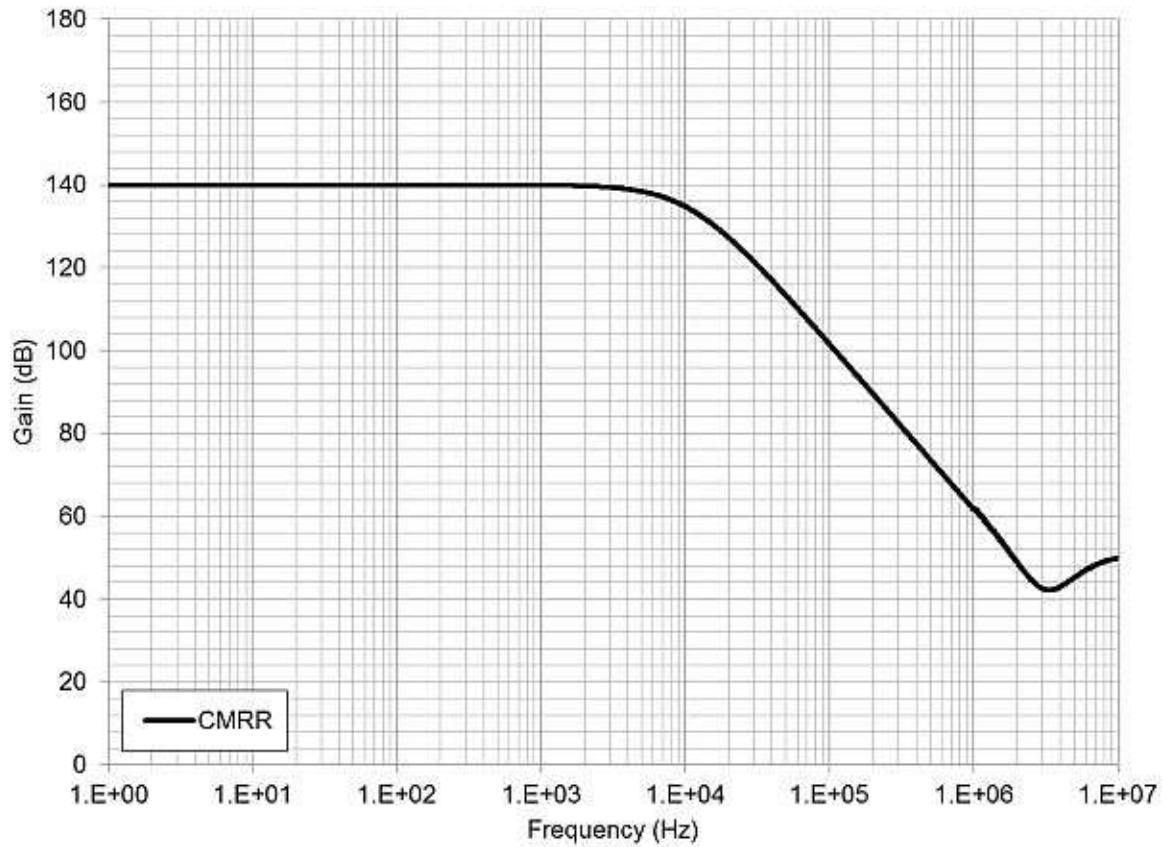


Figure 3 Typical CMRR vs. frequency curve

Let's use an example calculation to show how the curve in **Figure 3** translates to an input-referred error voltage. If a common-mode input signal is present with a frequency of 100kHz (1E+05Hz), you can see from the curve that the op amp has approximately 100dB of CMRR at that frequency. Equation 1 converts 100dB into an attenuation factor given in linear voltage gain units (V/V):

$$\text{CMRR(V/V)} = 10^{\frac{-\text{CMRR(dB)}}{20}} = 10^{\frac{-100}{20}} = 10^{-5} = 10\mu\text{V/V} \quad (1)$$

Now it's possible to compute the input-referred error voltage induced by the common-mode signal at 100kHz. Simply multiply the amplitude of the common-mode signal by the linear CMRR attenuation factor of 10μV/V to determine the input-referred error voltage. Equation 2 is an example of a common-mode signal with an amplitude equal to 1Vpp.

$$V_{\text{CMRR}} = V_{\text{cm}} * \text{CMRR(V/V)} = 1\text{Vpp} * 10\mu\text{V/V} = 10\mu\text{Vpp} \quad (2)$$

Therefore, a common-mode input signal with an amplitude of 1Vpp and a frequency of 100kHz generates an input-referred error signal of approximately 10μVpp. Keep in mind that this calculation is only valid at 100kHz, and would need to be repeated for different frequencies according to the CMRR characteristic given in **Figure 3**.

From a measurement perspective, CMRR is defined as the ratio of an op amp's open-loop differential gain to its open-loop common-mode gain. In the real world, these two gain characteristics can be tricky to isolate from one another, but the power of simulation allows you to do this effectively.

Figure 4 shows the recommended test circuit.

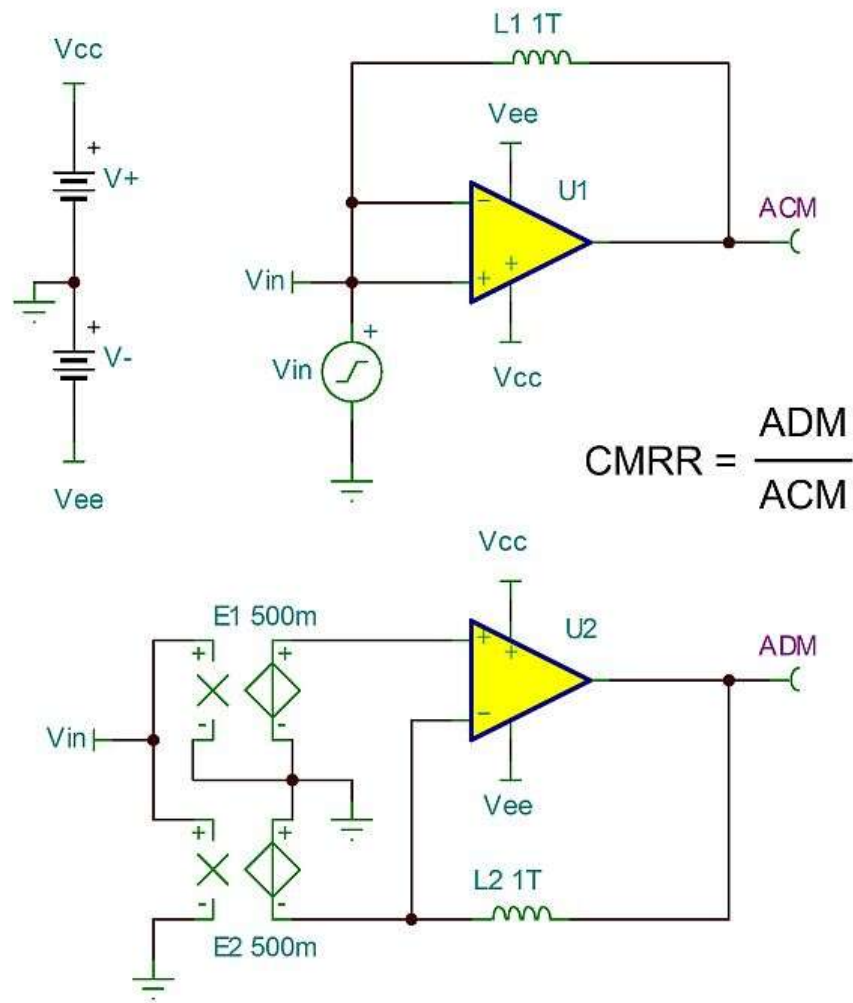


Figure 4 CMRR test circuit

This unique test circuit uses two identical copies of the op amp under test to measure the open-loop differential gain and open-loop common-mode gain separately. In the top circuit, AC source V_{in} is applied equally to both inputs of op amp U1 to create a purely common-mode input signal. Inductor L1 acts as a short circuit at DC, enabling SPICE to compute a valid DC operating point. At AC, L1 acts as an open circuit, placing U1 in an open-loop configuration to measure its open-loop common-mode gain (ACM).

In the bottom circuit, AC source V_{in} is routed to a single-ended-to-differential conversion circuit made up of voltage-controlled voltage sources E1 and E2. This generates a differential version of V_{in} biased around 0V, which is then applied to the inputs of op amp U2. Like in the top circuit, inductor L2 acts as a short circuit at DC and an open circuit at AC to allow for both a valid DC operating point and measurement of the open-loop differential gain (ADM).

As usual, I recommend verifying that the op amp is operating in its linear region by running a DC operating point test. Make sure to match the specified data-sheet conditions for power-supply voltage and input common-mode voltage.

To measure CMRR, run an AC transfer function over the desired frequency range and plot the magnitude in decibels of ACM and ADM. Use your simulator's post-processing function to generate a curve for ADM/ACM , the definition of CMRR.

Let's use this circuit to test the CMRR of the [OPA2187 SPICE model](#). The [OPA2187](#) is a zero-drift, low-power precision op amp from Texas Instruments. **Figure 5** shows the results.

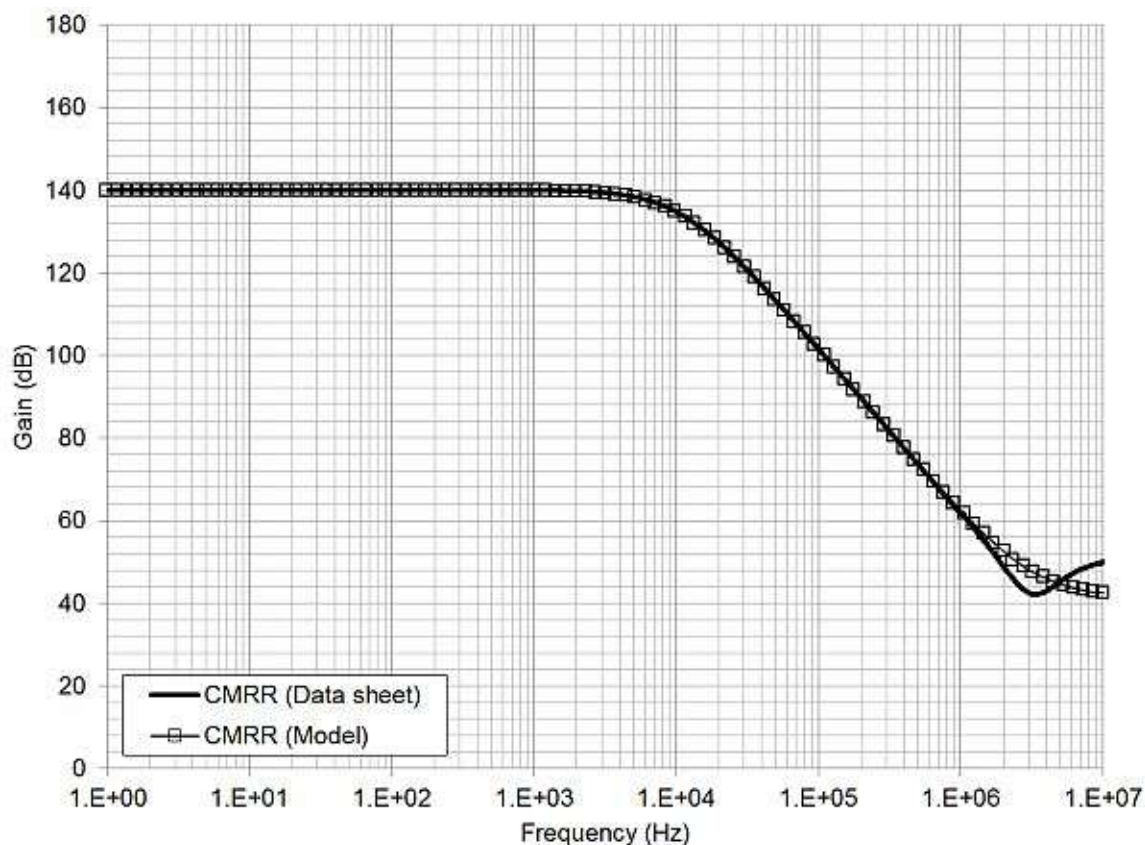


Figure 5 OPA2187 CMRR test results

Based on this test, the op amps CMRR is modeled very closely to the data-sheet curve throughout the majority of the measured frequency range. At frequencies approaching and above the unity-gain bandwidth of the amplifier - around 1MHz in this example - measured CMRR is dominated by parasitic components and higher-order behavior and becomes difficult to model. For more information on CMRR, watch the TI Precision Labs [Op Amps: Common Mode Rejection video](#).

Power supply rejection ratio

Power supply rejection ratio

You also want an op amp to reject any signals present at its power supplies. Op amps are used in all kinds of environments with all kinds of power-supply sources, from high-accuracy linear regulators to switching step-down converters to simple diode clamps and resistor dividers. A variety of conditions - like noise coupling, transients caused by poor load or line regulation, or high ripple - can cause unwanted signals to be applied to an op amp's power-supply pins instead of the perfect DC voltages that you hope for.

PSRR describes how well an op amp rejects the signals present at its power-supply pins. PSRR can also be modeled as an error voltage source (V_{psrr}) in series with the op amp noninverting input, as shown in **Figure 6**. This error voltage changes with the applied power-supply voltage according to the PSRR specification of the op amp. Since PSRR is input-referred, V_{psrr} is amplified by the closed-loop gain of the op amp circuit along with V_e and V_{cmrr} to generate V_{out} .

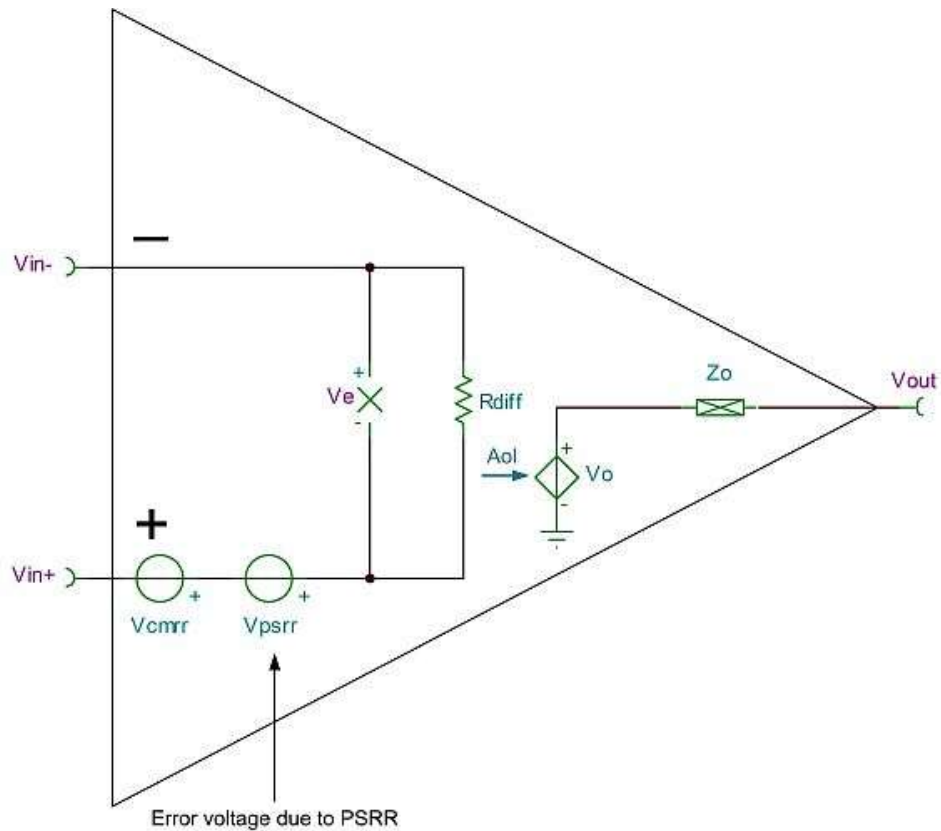


Figure 6 Simplified input-referred PSRR model

Also like CMRR, PSRR changes over frequency, with the most rejection at low frequencies and less at higher frequencies as the op amp runs out of bandwidth. This can be a concern when using switching power supplies that switch at frequencies above the unity-gain bandwidth of the op amp, so make sure to use appropriate filtering and decoupling.

Figure 7 is a typical PSRR vs. frequency curve. Note that separate curves are provided for the positive and negative supply in this example. Some devices give only one PSRR curve in their data sheet, implying that the same characteristic applies to both supplies. You can calculate the input-referred error voltage induced by a power-supply signal at a certain frequency in the same way that I showed earlier for CMRR.

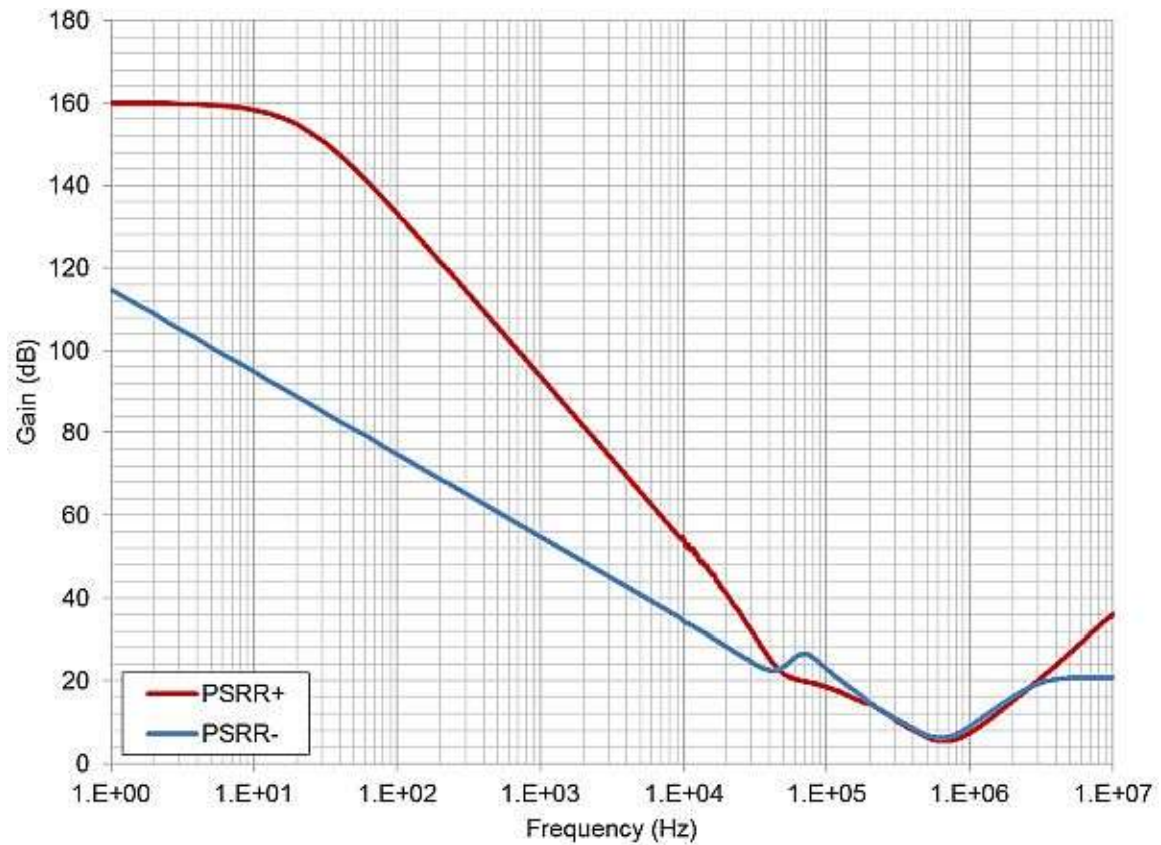


Figure 7 Typical PSRR vs. frequency curve

PSRR is defined as the ratio of the signal applied to either op-amp power-supply pin versus the resulting input offset voltage. **Figure 8** shows the recommended test circuit for positive PSRR (PSRR+), while Figure 9 shows the circuit for negative PSRR (PSRR-).

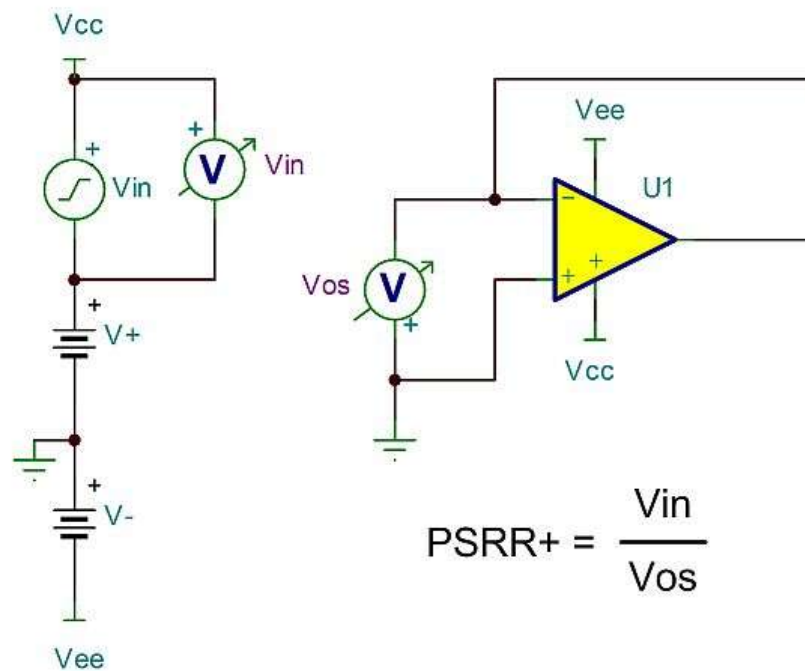


Figure 8 PSRR+ test circuit

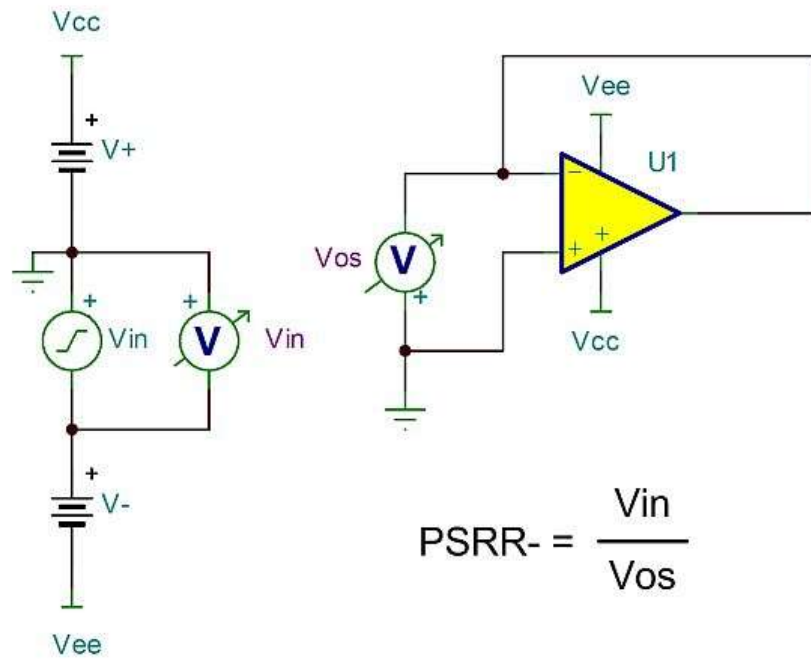


Figure 9 PSRR– test circuit

In these test circuits, adding AC source V_{in} in series with one of the power-supply voltages generates the DC + AC test signal. The op amp is placed in a standard unity-gain buffer configuration with its noninverting input shorted directly to ground, and the induced offset voltage across the op amp input pins (V_{os}) is measured.

To plot PSRR, run an AC transfer function over the desired frequency range and plot the magnitude in decibels of V_{in} and V_{os} . Use your simulator's post-processing function to generate a curve for V_{in}/V_{os} , the definition of PSRR.

Let's use this circuit to test the PSRR of the [OPA2187](#) SPICE model. As always, make sure to match the specified data-sheet conditions for power-supply voltage and input common-mode voltage and check the DC operating point to verify that the op amp is operating in the linear region. **Figure 10** shows the results.

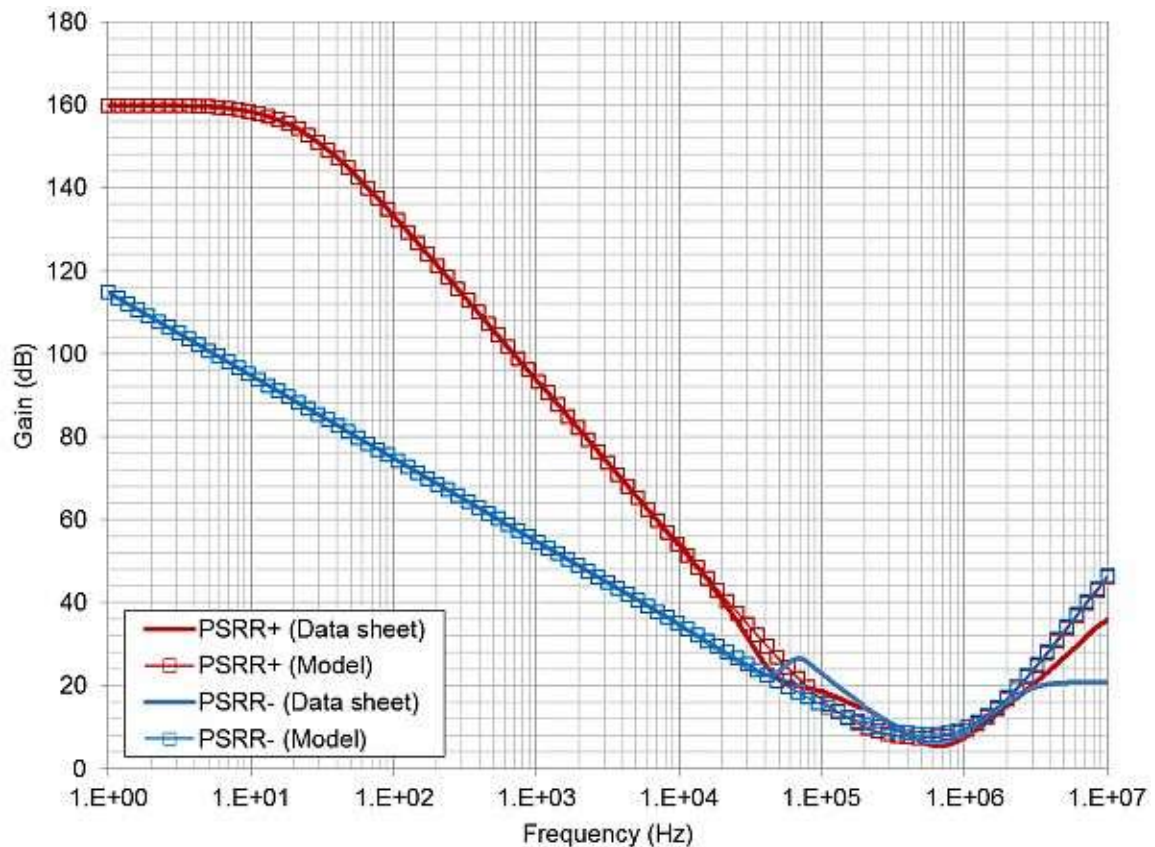


Figure 10 OPA2187 PSRR results

The test results show that the op amp's PSRR is modeled very closely to the data-sheet curve throughout the majority of the measured frequency range. As with CMRR, the parasitic and higher-order effects at high frequencies are problematic to model and cause some deviation between the data-sheet curves and the measured simulation characteristics in that region. For more information on PSRR, watch the TI Precision Labs [Op Amps: Power Supply Rejection video](#).

Input offset voltage, input bias current, input offset current

Input offset voltage, input bias current, input offset current - V_{os} , I_b , I_{os}

For many precision circuits, V_{os} and I_b are among the first parameters considered when selecting an op amp. V_{os} is an error voltage caused by the slight mismatch of transistors in the differential input pair of the op amp. IC designers employ various methods to reduce this error, such as laser trimming internal resistors and adding sophisticated switching and filtering networks, but all op amps have some amount of inherent offset voltage.

Like CMRR and PSRR, V_{os} is modeled as a DC error voltage in series with the op amp noninverting input. This voltage does not change over frequency, but it does drift over temperature. As with all input-referred error sources, it will add to any externally applied input signals and be amplified by the closed-loop gain of the op amp circuit before appearing at the output.

I_b is the current flowing into the inputs of an op amp. For bipolar amplifiers, this current flow is caused by the base current of the input transistors, and for FET amplifiers it's usually a result of the leakage current from input electrostatic discharge (ESD) protection diodes. Ideally, the current flowing into each op amp input pin would be equal and cancel out; however, for most devices this is not the case. The difference in bias current between the noninverting and inverting inputs of the op amp is called I_{os} .

I_b is modeled as a DC current source flowing from each op amp input pin to ground. Like V_{os} , these do not change significantly over frequency but exhibit temperature drift. With low impedances connected around the op amp, I_b and I_{os} may not cause measurable errors in a circuit's performance. However, if you're using large input or feedback resistors, the resulting voltage drop across those resistors may cause DC errors. **Figure 11** shows the op amp small-signal model, now updated to include V_{os} and I_b .

Keep in mind that the error sources from CMRR, PSRR, and V_{os} can have either positive or negative polarity for most devices. Because these errors are uncorrelated and follow Gaussian distributions, you can combine them using the root-sum-of-squares method for easier total error analysis.

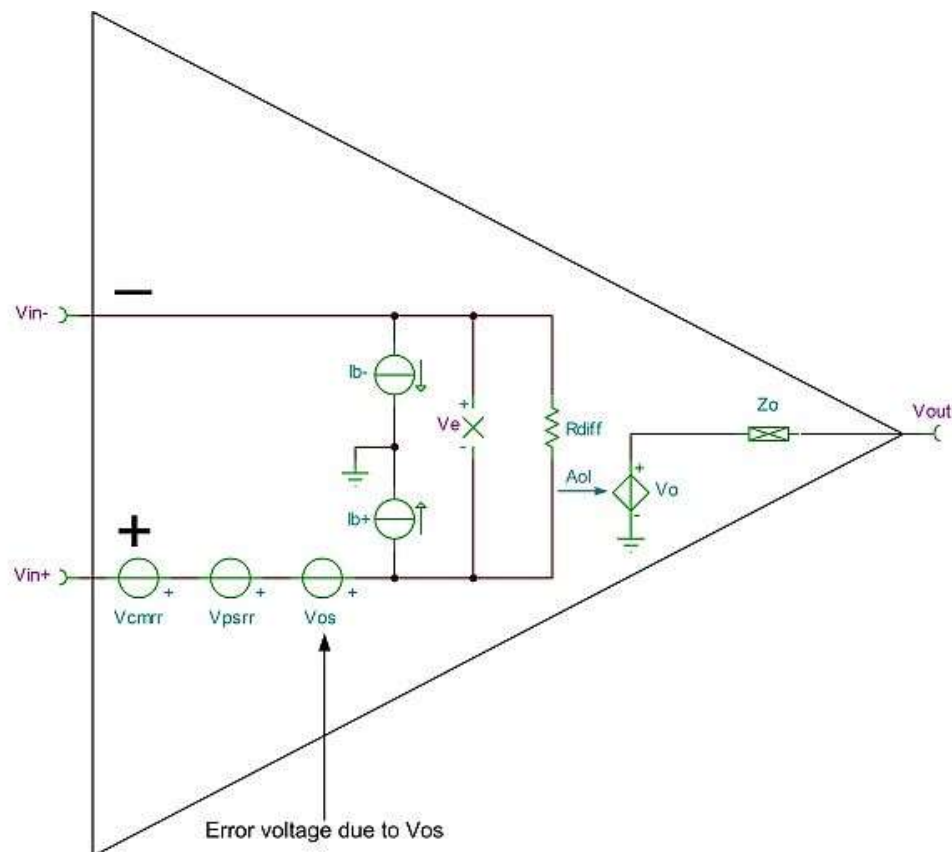


Figure 11 Simplified input-referred V_{os} , I_b , I_{os} model

V_{os} , I_b and I_{os} are specified in the electrical characteristics table of an op amp data sheet. **Figure 12**, taken from the OPA2187 data sheet, shows an example table giving both typical and maximum values. Op amp SPICE models are commonly designed to show typical behavior, not maximum, but check with the manufacturer if there's any confusion about a particular model.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
V _{OS}	Input offset voltage		±1	±15	μV
INPUT BIAS CURRENT					
I _B	Input bias current	V _{CM} = V _S / 2	±100	±350	pA
I _{OS}	Input offset current		±100	±500	pA

Figure 12 Example V_{os} , I_b , I_{os} specifications

Verifying V_{os} , I_b and I_{os} in simulation is quite straightforward. **Figure 13** shows the recommended test circuit.

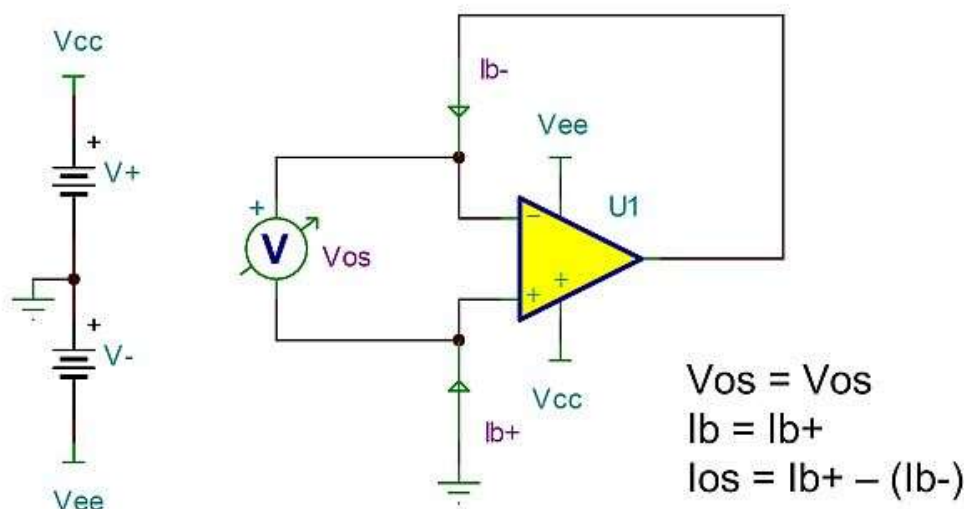


Figure 13 Vos, Ib, Ios test circuit

In this test circuit, the op amp is placed in a unity-gain buffer configuration with its noninverting input grounded. Current meters are placed at both op amp inputs in order to measure I_{b+} and I_{b-} , and differential voltmeter V_{os} is connected across the op amp pins to measure the input offset voltage. To measure V_{os} , I_b , and I_{os} , simply run a DC operating point simulation and observe the values reported by all three meters. If the model includes temperature drift characteristics, you can sweep the ambient temperature and measure the change in V_{os} , I_b , and I_{os} as well.

Let's use this circuit to verify the V_{os} , I_b , and I_{os} of the OPA2187. Of course, ensure that the power-supply voltage and input common-mode voltage match the test conditions given in the op amp data sheet. **Figure 14** shows the results.

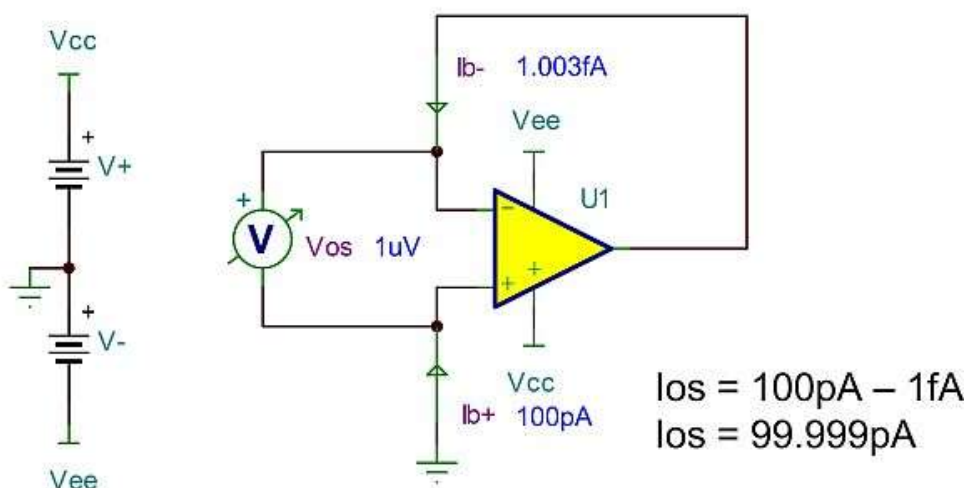


Figure 14 OPA2187 Vos, Ib, Ios test results

Comparing the measured results to **Figure 12**, you can see that V_{os} , I_b , and I_{os} are modeled exactly to their typical specifications. Note that V_{os} and I_b are directly observable, while you must calculate I_{os} by taking the difference of I_{b+} and I_{b-} . In this case, 100pA minus 1fA equals 99.999pA , or 100pA .

For more information on V_{os} and I_b , including example error calculations, watch the TI Precision

Labs [Op Amps: Vos and Ib video](#).

In summary:

- CMRR defines how well an op amp rejects common-mode signals present at its input pins. It can be modeled as an error voltage source at the op amp's noninverting input, which changes over frequency.
- PSRR defines how well an op amp rejects signals present at its power-supply pins. It can also be modeled as an error voltage source at the op amp's noninverting input, which changes over frequency.
- Vos is an inherent DC voltage caused by a mismatch in the op amp's input transistors. It is modeled as an error voltage source at the op amp's noninverting input, which is constant over frequency but varies over temperature.
- Ib is a current flowing into the op amp pins caused by the base current of bipolar transistors or leakage current of input ESD protection diodes. It is modeled as a current source from each op amp input to ground, which is constant over frequency but varies over temperature.
- Ios is the difference in bias current between the noninverting and inverting inputs of the op amp.

Thank you for reading the third installment of this series. In part 4, I'll show you how to verify the noise behavior of an op amp model, including input voltage noise density (e_n), input current noise density (i_n), and total integrated noise.

[Ian Williams](#) is an applications engineer and SPICE model developer for the Precision Amplifiers group at Texas Instruments.

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