Designing with a complete simulation test bench for op amps, Part 2: Small-signal bandwidth

Ian Williams - July 26, 2018

Open-loop gain/phase – Aol

The first installment of this article series discussed the need to verify SPICE model accuracy and how to measure the open- and closed-loop small-signal AC output impedance of operational amplifier (op amp) models. Here in part 2, I'll explain how to verify the parameters of an op amp that define its small-signal bandwidth or frequency response while the op amp is in its linear operating region: open-loop gain/phase (Aol), closed-loop gain (Acl) and small-signal step response.

Open-loop gain/phase – Aol

Aol is the gain stage that acts on the differential signal applied to the op amp input pins and is undoubtedly the most fundamental parameter of any op amp. It affects nearly all aspects of small-signal or linear operation, including gain-bandwidth product, stability response, rise and fall time, settling time, and even input offset voltage. In essence, Aol is what makes an amplifier an amplifier. To reiterate a point from the first installment in this series, Aol interacts with the open-loop small-signal output impedance (Zo) across frequency to create the op amp's overall AC response.

Let's return to our simplified small-signal open-loop model of an op amp from part 1, shown in **Figure 1**.

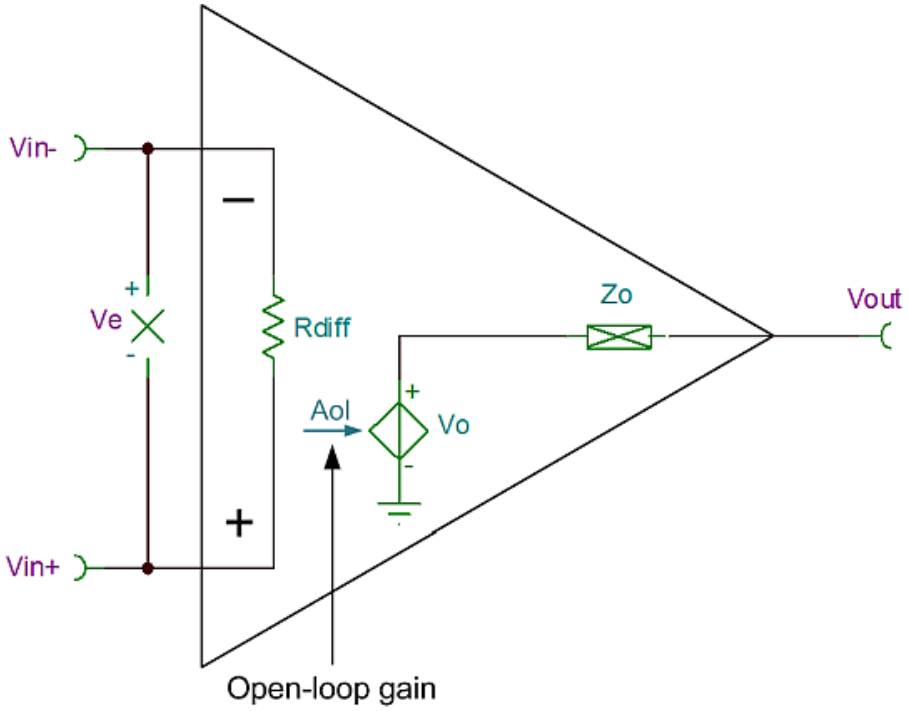

Figure 1 Simplified op amp small-signal model (open-loop)

In this model, a differential input signal (Ve) develops across the op amp's input resistance (Rdiff). Aol amplifies Ve to generate the ideal output voltage (Vo), which flows through Zo before appearing at the output pin (Vout).

As implied earlier, Aol is not simply an ideal gain block that behaves the same at all frequencies. In practice, real-world limitations and choices of modern op amp design cause most products to exhibit an Aol response with predictable gain and phase components, as shown in **Figure 2**. Both gain and phase curves are represented on the same set of axes, with the gain curve labeled G and the phase curve labeled φ.

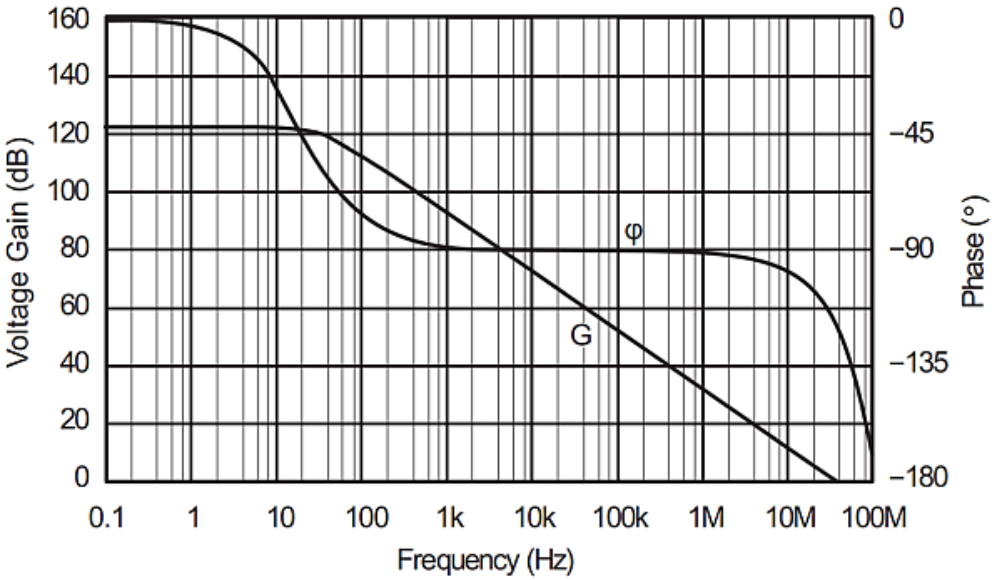

Figure 2 Typical open-loop gain/phase plot

To better analyze the characteristics of open-loop gain, let's divide **Figure 2** into three distinct regions, as shown in **Figure 3**.

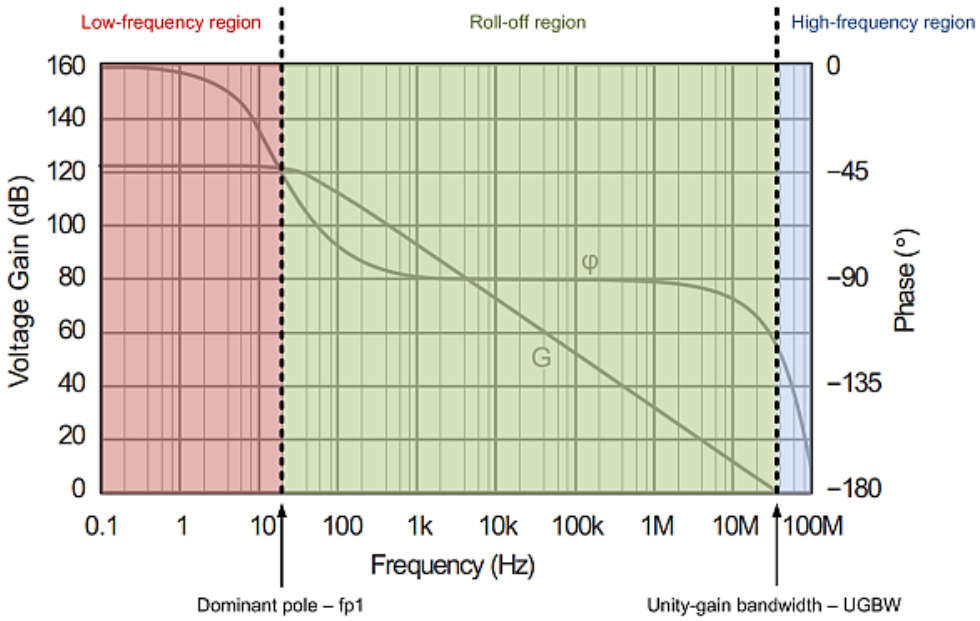

Figure 3 Regions of Aol

The first region is the low-frequency region, highlighted in red. In this region, the gain and phase components are both fairly constant. An op amp operating on signals at these low frequencies is as close as possible to ideal, with a very large maximum gain (usually >100dB or 100,000V/V) and no serious concerns in terms of stability.

The low-frequency region ends at a point in frequency known as the dominant pole (fp1). At this frequency, a pole placed in Aol by design causes the gain and phase curves to change. Right at fp1, the gain reduces by −3dB and the phase shifts by −45 degrees. After fp1, the gain continues to roll off at −20dB per decade and the phase shifts by a total of -90 degrees before remaining constant.

Let's call this second region the roll-off region, highlighted in green; it is in this region where op amps most commonly operate. In the roll-off region, it's possible to configure op amps with negative feedback for stable operation with various amounts of closed-loop gain (Acl), as long as the desired Acl is less than Aol at that frequency.

The roll-off region ends at a frequency called the unity-gain bandwidth (UGBW). At this frequency, the gain curve has rolled off to 0dB, or 1V/V. Since the gain curve continues to roll off above the UGBW, frequencies higher than this cannot pass through the op amp without some degree of attenuation. At the UGBW, the amount of phase shift remaining before reaching a total of -180 degrees is called the phase margin and is a primary indicator of the general stability response of the op amp for a closed-loop gain of 1V/V.

Let's call this third region the high-frequency region, highlighted in blue. In the high-frequency region, higher-order poles and zeroes act on the op amp's small-signal response, causing the phase to shift rapidly and making the overall system more complex to characterize. It's common in this region for Zo, input capacitance (Cin), PCB parasitics and other higher-order characteristics to start to significantly influence the op amp's AC response. For all of these reasons, I do not recommend attempting to operate an op amp in this region.

For a review on poles, zeroes and how they occur in op amps, watch the TI Precision Labs – Op Amps video series on bandwidth. For a deeper discussion about op amp stability, watch the TI Precision Labs – Op Amps video series on stability.

It should now be evident that it's important to verify the Aol behavior of your op amp SPICE models.

Figure 4 shows the recommended test circuit.

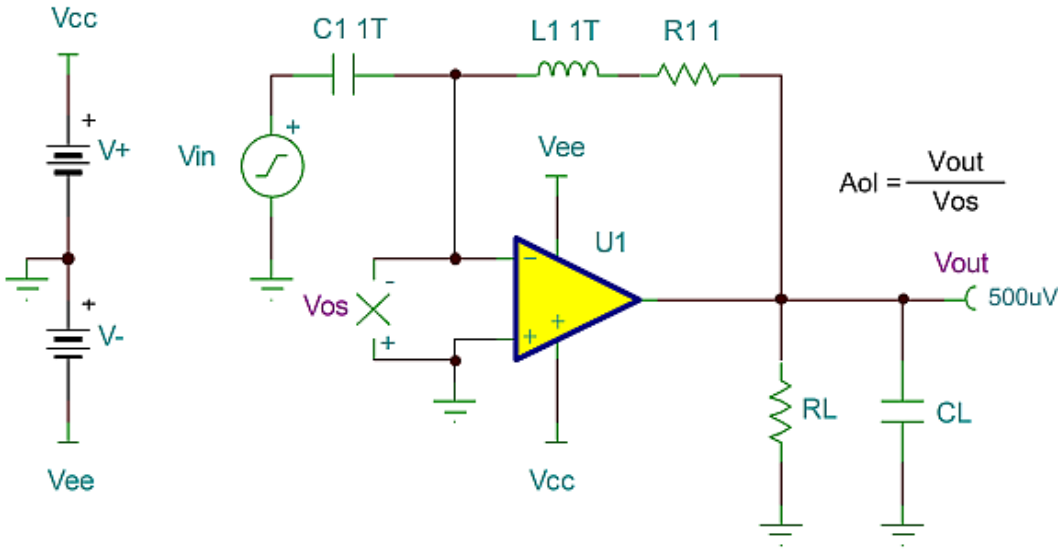

Figure 4 Open-loop gain/phase test circuit

The test circuit is very similar to the one used to measure open-loop output impedance. Inductor L1 creates closed-loop feedback at DC while allowing for open-loop AC analysis, while R1 provides a small amount of series resistance in the feedback loop to make the circuit more "real" and prevent mathematical errors in the analysis. Capacitor C1 shorts the op amp's inverting input to signal source Vin at AC in order to receive the appropriate AC stimulus but acts as an open circuit at DC.

As explained by Bruce Trump in his classic blog post, "Offset Voltage and Open-Loop Gain – they're cousins," you can think of Aol as an offset voltage that changes with output voltage. Therefore, to measure Aol, run an AC transfer function over the desired frequency range and plot the gain and phase of Vout/Vos. The op amp must be in its linear operating region (as shown in **Figure 4**), where Vout is equal to a small offset voltage. Make sure to match the specified data-sheet conditions for the power-supply voltage, input common-mode voltage, load resistance and load capacitance.

Most simulators default to showing the results for gain in decibels and phase in degrees. Since these are the units you wish to see, you only need to make minimal adjustments to the results window. Let's use this circuit to test the Aol of the OPA1678 SPICE model. The OPA1678 is a low-distortion, low-noise, general-purpose audio op amp from Texas Instruments. **Figure 5** gives the results.

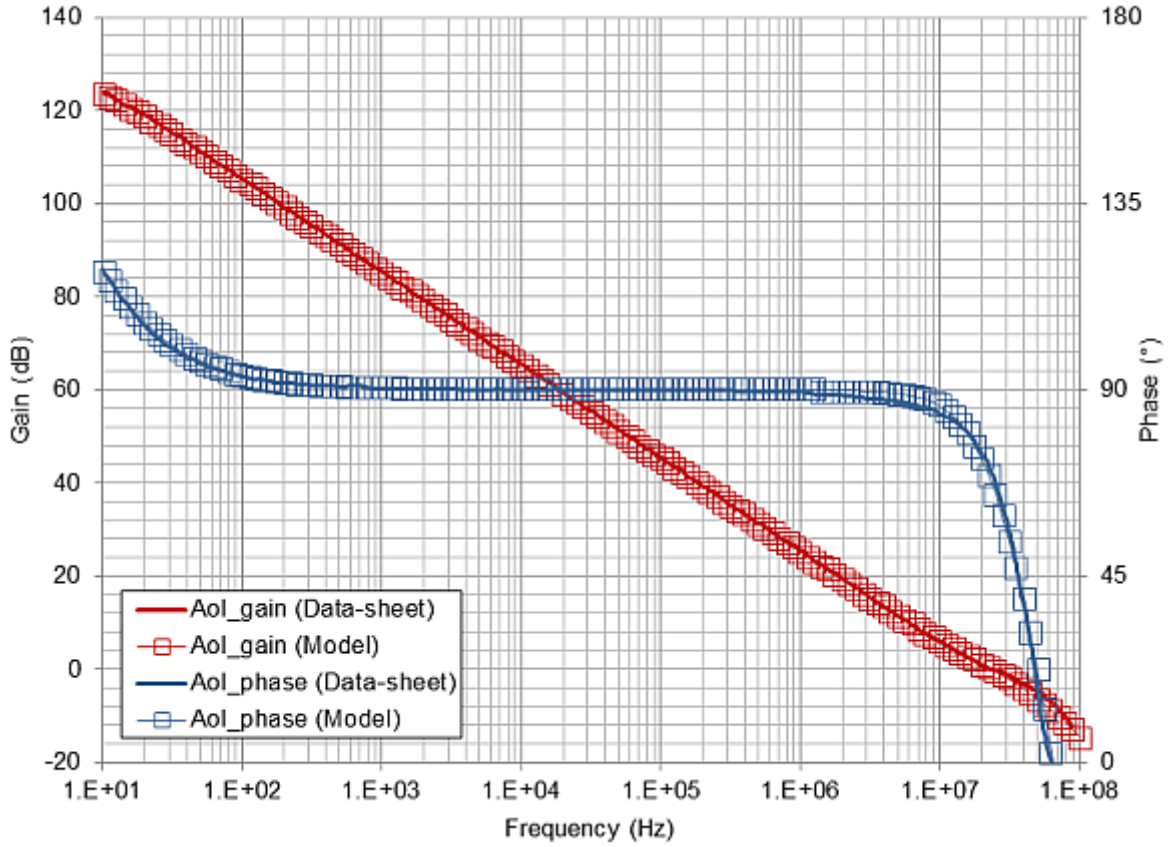

Figure 5 OPA1678 Aol Results

In this case, the op amp's Aol models very closely to the data-sheet curve and can be used for small-signal analysis to achieve results that will match the real world.

Closed-loop gain – Acl
Closed-loop gain – Acl

Closed-loop gain (Acl) is the AC response of an op amp when it is placed in a closed-loop configuration with negative feedback. Unlike Aol, which is an inherent property of the op amp and remains relatively fixed (for the most part) with variations in load or feedback, Acl is a function of Aol, Zo and β, the feedback factor set by the feedback network. This should sound familiar, as it is very similar to the relationship between Zo and Zout.

Let's return to the op amp small-signal model, now expanded to represent a closed-loop circuit, shown in **Figure 6**.

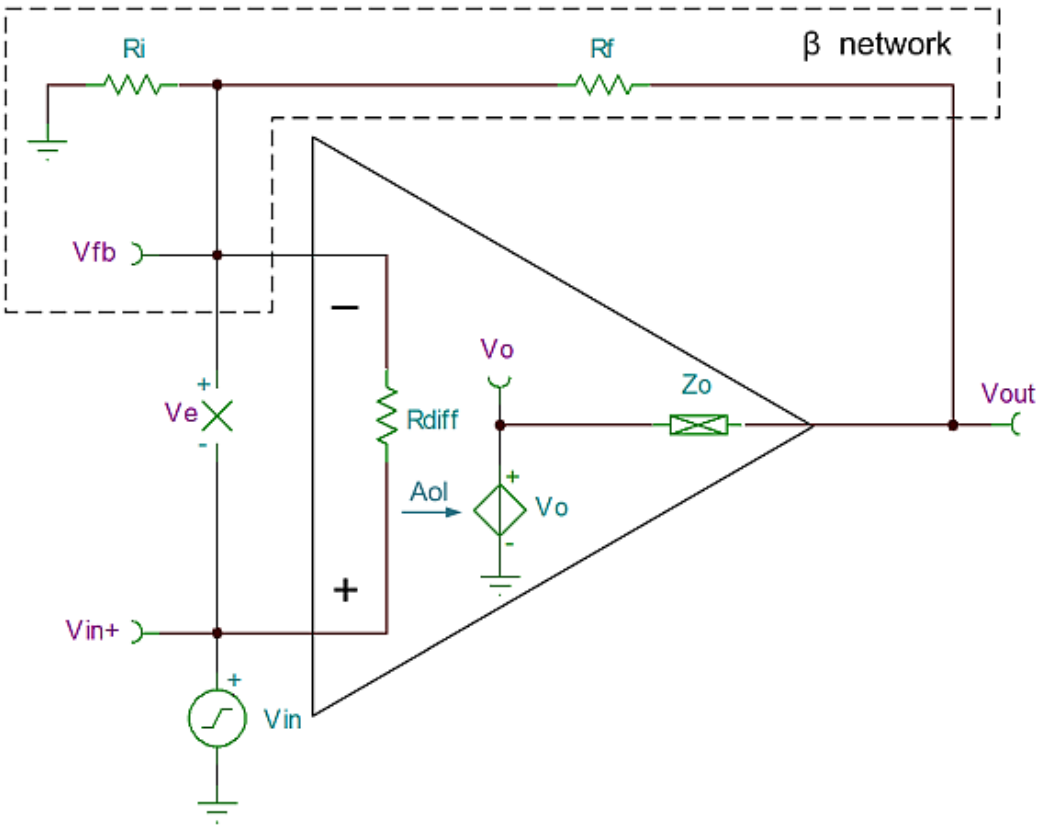

Figure 6 Simplified op amp small-signal model (closed-loop)

Our goal is to solve for the transfer function of this system, or Vout/Vin, which is equivalent to Acl.

First, recall that feedback factor β is the ratio of the voltage that appears at feedback node Vfb vs. the output voltage Vout. The standard resistor divider equation given in the numerator of Equation 1 computes the voltage at Vfb:

$$\beta = \frac{Vfb}{Vout} = \frac{Vout * \frac{Ri}{(Rf + Ri)}}{Vout} = \frac{Ri}{Rf + Ri} \qquad (1)$$

Since the noninverting input of the op amp is grounded, Ve, or the error voltage between the op amp input pins, is equal to Vfb. By rearranging the terms of Equation 1, you can determine that Vfb is equal to Vout multiplied by β, as shown in Equation 2:

$$Ve = Vfb = Vout * \beta \qquad (2)$$

To continue the analysis and solve for Acl, let's change the representation of the closed-loop op amp circuit to the control theory model given in **Figure 7**. For simplicity, assume that Zo is a short circuit, so Vo is equal to Vout. In reality, Zo also influences the AC response.

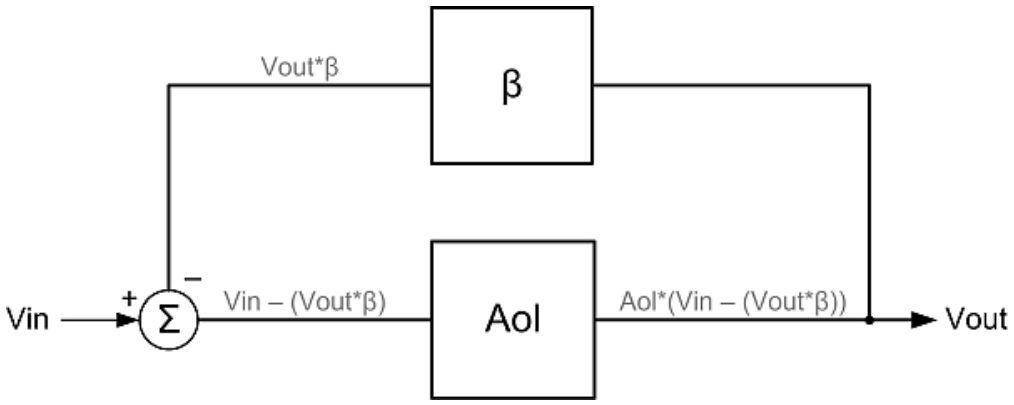

Figure 7 Closed-loop op amp control theory model

By stepping through the control system, you can identify the values at each node. The negative input of the summing node is the same as the inverting input of the op amp, or Vfb, and from Equation 2, you know that Vfb is equal to Vout * β. Therefore, the voltage to the right of the summing junction is equal to the difference of Vin and Vfb, as given by Equation 3:

$$\text{Vin} - \text{Vfb} = \text{Vin} - (\text{Vout} * \beta) \quad (3)$$

The voltage at Vout is then equal to the voltage to the right of the summing junction multiplied by Aol, as given by Equation 4:

$$\text{Vout} = \text{Aol} * (\text{Vin} - (\text{Vout} * \beta)) \quad (4)$$

Rearranging terms and solving for Acl, or Vout/Vin, gives the relationship shown in Equation 5:

$$\text{Acl} = \frac{\text{Vout}}{\text{Vin}} = \frac{\text{Aol}}{1 + \text{Aol} * \beta} \quad (5)$$

This definition reveals that closed-loop gain is a result of Aol being reduced by Aol * β, the loop gain of the op amp. This consequence of applying negative feedback enables circuit designers to reduce the huge open-loop gain of the op amp to a more usable level. Since Aol is so large, taking the limit of Acl as Aol approaches infinity leads to an even simpler definition of closed-loop gain, as given by Equation 6:

$$\text{Acl} = \lim_{\text{Aol}\to\infty} \left(\frac{\text{Aol}}{1 + \text{Aol} * \beta}\right) = \frac{1}{\beta} \quad (6)$$

Circuit designers commonly use this simpler definition of Acl, and it is a valid approximation at low and middle frequencies where Aol is large. However, remember that Aol rolls off starting at frequency fp1, the dominant pole, so at higher frequencies the roll-off is visible in Acl as well.

Most op amp manufacturers specify closed-loop gain at several gain settings, or several values of β.

Figure 8 shows the closed-loop gain vs. frequency curve for the OPA1678.

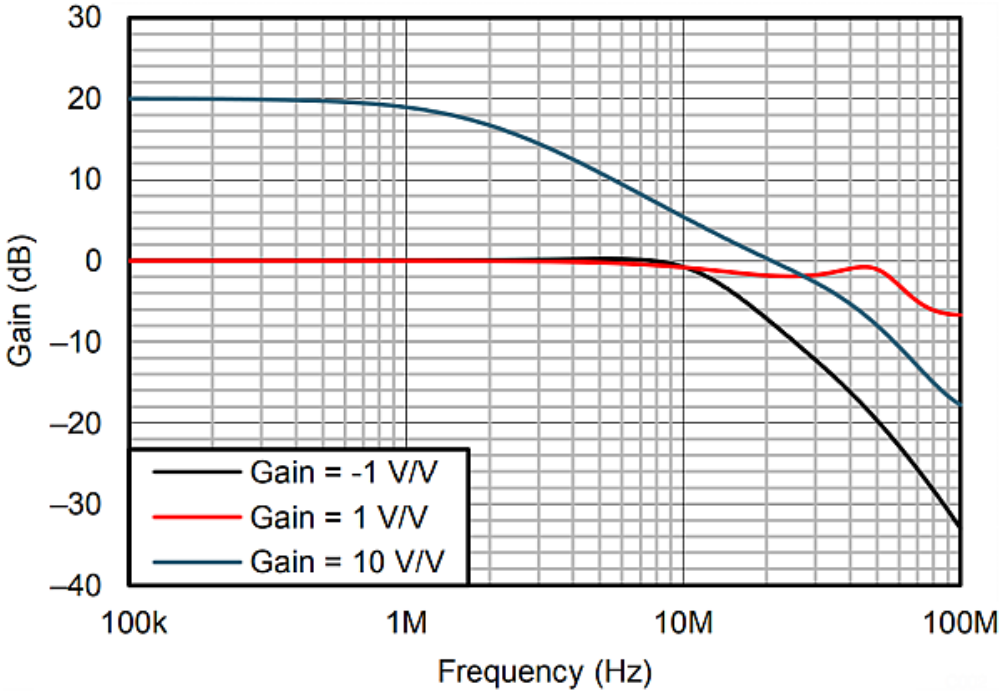

Figure 8 Closed-loop gain of the OPA1678

Notice how the closed-loop gain remains flat at low and middle frequencies but rolls off at higher frequencies. Also note that as the DC value of Acl increases from ±1V/V to 10V/V, the roll-off occurs at a lower frequency. Finally, observe how the higher-order effects of Zo, Cin and PCB parasitics influence Acl at higher frequencies. Because of how diverse the open-loop gain and output impedance of different op amps can be, the high-frequency closed-loop gain will look quite different from one device to the next.

Figure 9 shows the recommended test circuits for verifying Acl at three different gain settings.

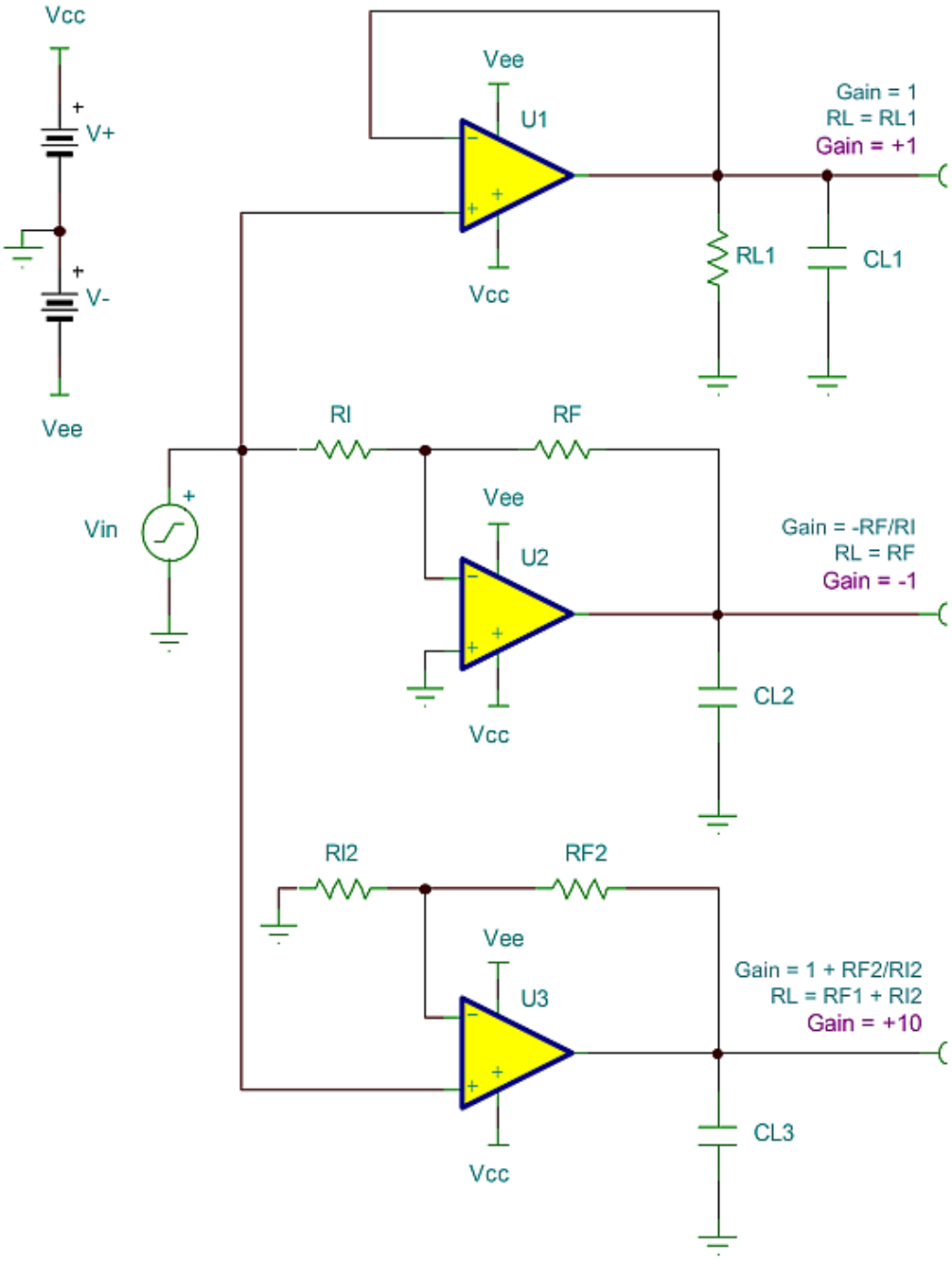

Figure 9 Closed-loop gain test circuits

In these test circuits, feedback resistors RF and RI close the loop around the op amps to create test conditions that match the model used in the derivation of Acl. To plot Acl, run an AC transfer function over the desired range and plot the voltages at output nodes Gain = +1, Gain = -1 and Gain = +10.

For Gain = +1, RF has been replaced with a short circuit and RI with an open circuit. For Gain = −1, set RF = RI. For Gain = +10, set RF = 10 * RI. Let's use this circuit to test the Acl of the OPA1678 SPICE model at Gain = +1, −1 and +10. As always, make sure to match the specified data-sheet conditions for power-supply voltage, input common-mode voltage, load resistance and load capacitance.

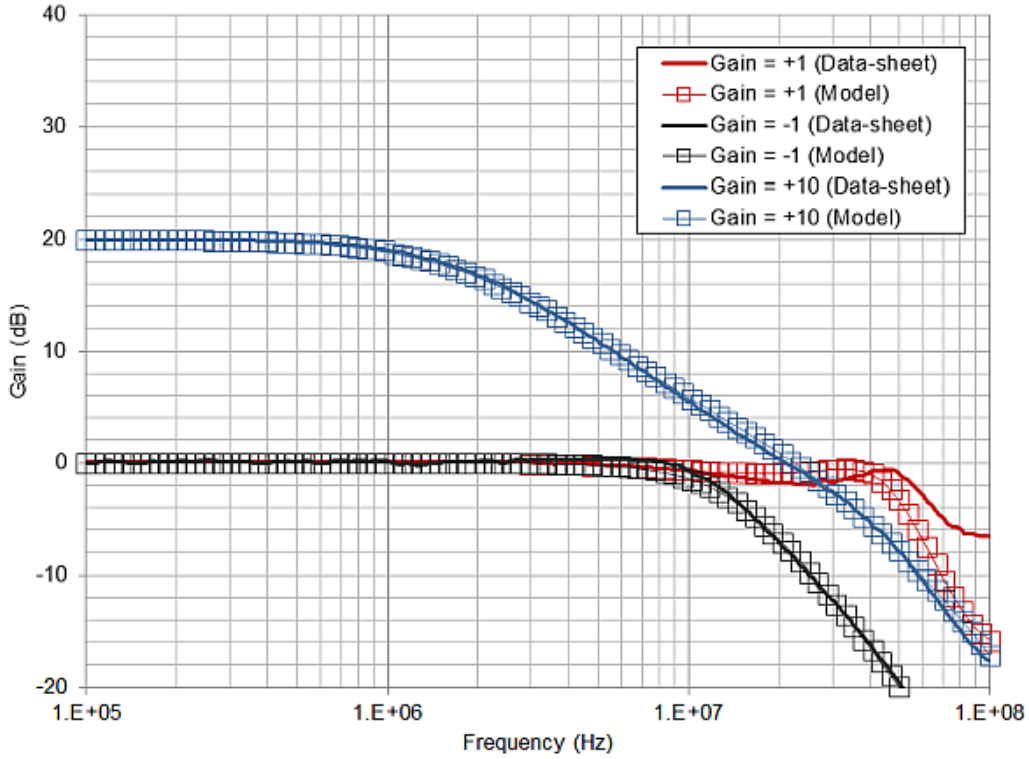

Figure 10 OPA1678 Acl results

The closed-loop gain of the model matches the data-sheet curves quite closely at Gain = −1 and Gain = +10. The high-frequency behavior when Gain = +1 is not as good of a match, however. This may be somewhat surprising, as the open-loop gain of the OPA1678 model matches the data-sheet spec perfectly, as shown earlier in **Figure 5**.

Remember that Acl is not an inherent and independent property of the op amp but a combined effect of Aol, Zo, Cin and all external circuit components. If any test conditions in the simulation circuit are different than those the validation engineers used when generating the data-sheet curves, the results will not match. The case where Gain = +1 is particularly sensitive to this, since β = 1 and its influence drops out of the equation.

Keep in mind that all units of the same device number are not exactly the same. Every spec is different, but there's always some level of tolerance present in the value listed in the data-sheet table. For example, the differential input capacitance (C_diff) of the OPA1678 is given with a typical value of 6pF. No minimum and maximum values are guaranteed, so it's reasonable to assume a variation of up to ±20% across all shipped units. Let's plot Acl again at Gain = +1 for the typical value of C_diff as well as the typical value ±20%. **Figure 11** shows the results.

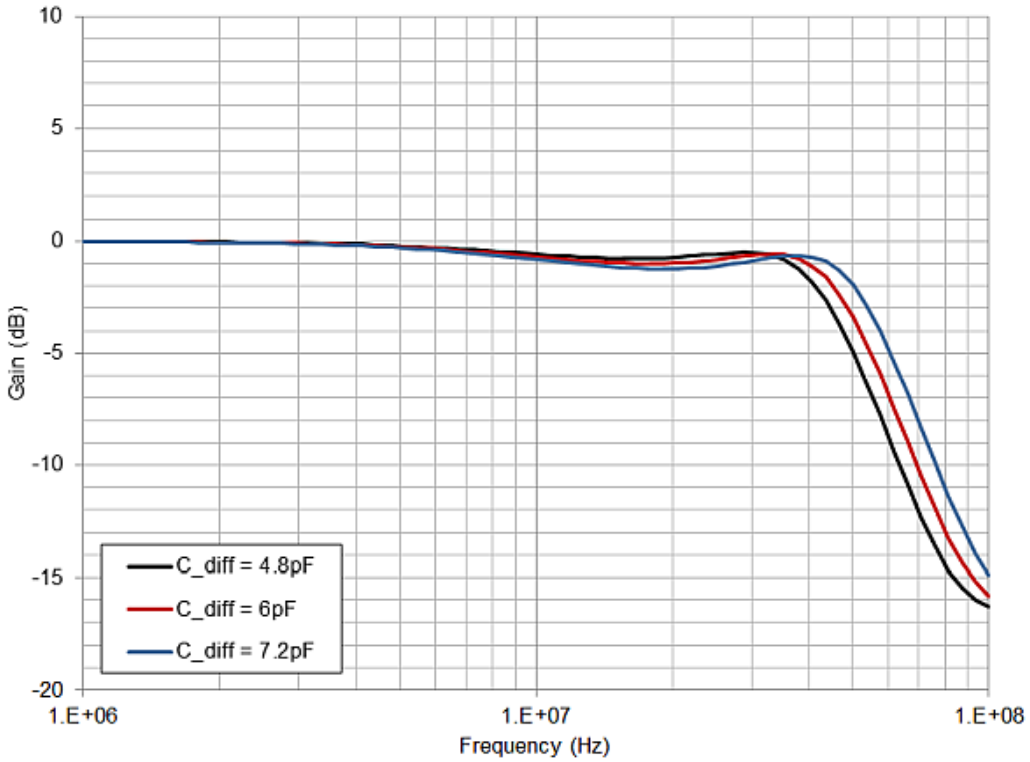

Figure 11 OPA1678 Acl vs. C_diff, Gain = +1

As you can see, the severity of the "dip" above 10MHz and the location of the high-frequency roll-off change quite significantly across this range of input capacitance. Varying the values of load capacitance and feedback resistance will give similar results. Unfortunately, op amp manufacturers do not usually provide the exact values of all external components (much less PCB parasitics) for this and other closed-loop tests. My recommendation is to simply check that the −3dB frequency of the model matches within ±20% of the data-sheet curve and that the shape of the high-frequency roll-offs are similar.

Small-signal step response

Small-signal step response

Open- and closed-loop gain are op amp properties considered to be in the frequency (or AC) domain. The small-signal bandwidth of an op amp can also be quantified in the time domain through the small-signal step response test. For this test, you place the op amp in a closed-loop configuration, apply a small-signal step function or square wave to its input, and measure the output voltage. The limit of what's considered "small-signal" varies from engineer to engineer, but a good rule of thumb is that a small signal must have an amplitude less than or equal to 100mVpp.

The behavior of the output voltage waveform in this test gives useful information about the closed-loop op amp circuit. As described in the "Analog Engineer's Pocket Reference Guide," (You will need to use or create a myTI account) the rise and fall time of the output indicate the closed-loop bandwidth of the system, and the percent overshoot of the output corresponds to the phase margin of the system. The phase margin relationship is especially useful in the real world, as this closed-loop, small-signal step response test is much simpler to perform on the bench with standard test equipment than any open-loop test to check stability.

Figure 12 gives the small-signal step response curves for the OPA1678 at Gain = +1 and Gain = −1.

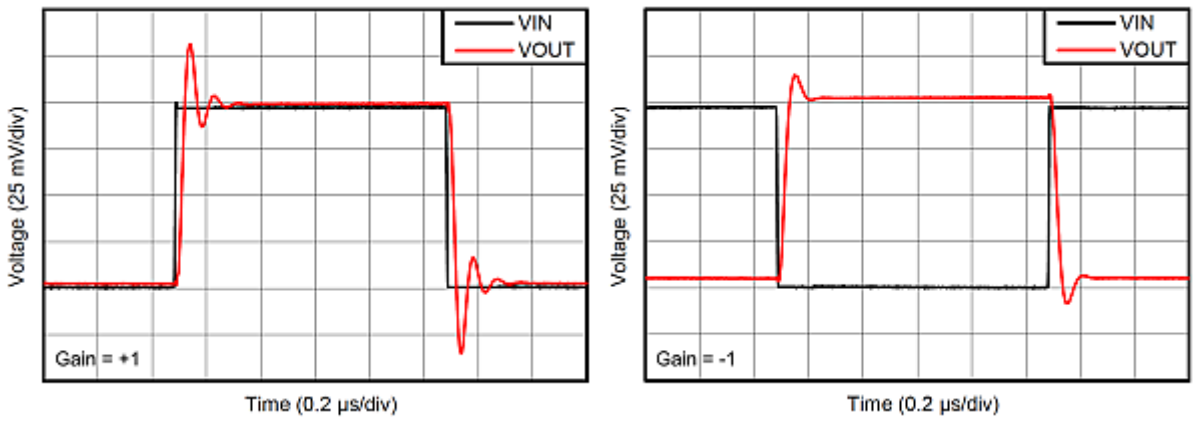

Figure 12 Small-signal step response of the OPA1678

Figure 13 shows the test circuits for verifying small-signal step response at Gain = +1 and Gain = −1.

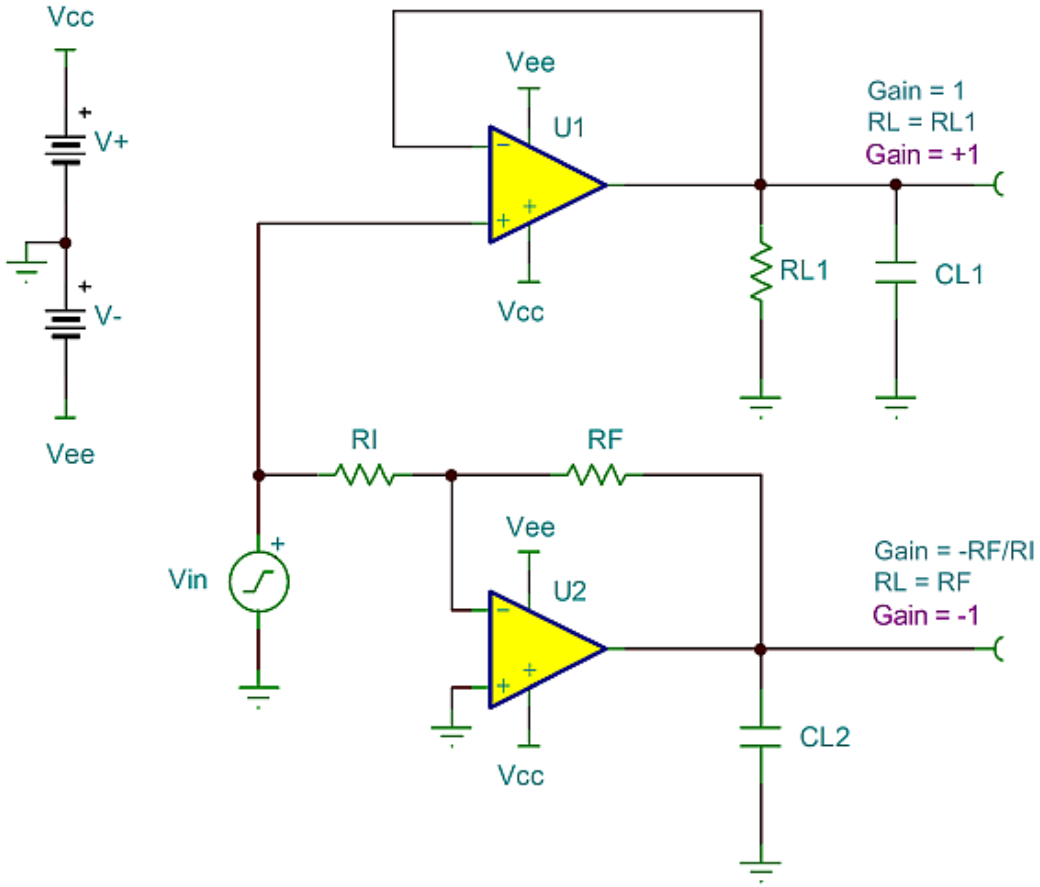

Figure 13 Small-signal step response test circuits

These test circuits should look familiar, as they're exactly the same as the closed-loop gain test circuits for Gain = +1 and Gain = −1. This is no coincidence, as small-signal step response and closed-loop gain describe the same condition but in different domains.

To plot the small-signal step response, run a transient analysis over the desired time range and plot the voltage at output nodes Gain = +1 and Gain = −1. In addition to matching all of the usual data-sheet test conditions, also take care to match the amplitude and frequency of the input signal (Vin). In this case, the input amplitude is 100mVpp and the frequency is 1MHz, as shown in **Figure 12**.

Let’s use these test circuits to verify the small-signal step response of the OPA1678. **Figures 14 and 15** give the results.

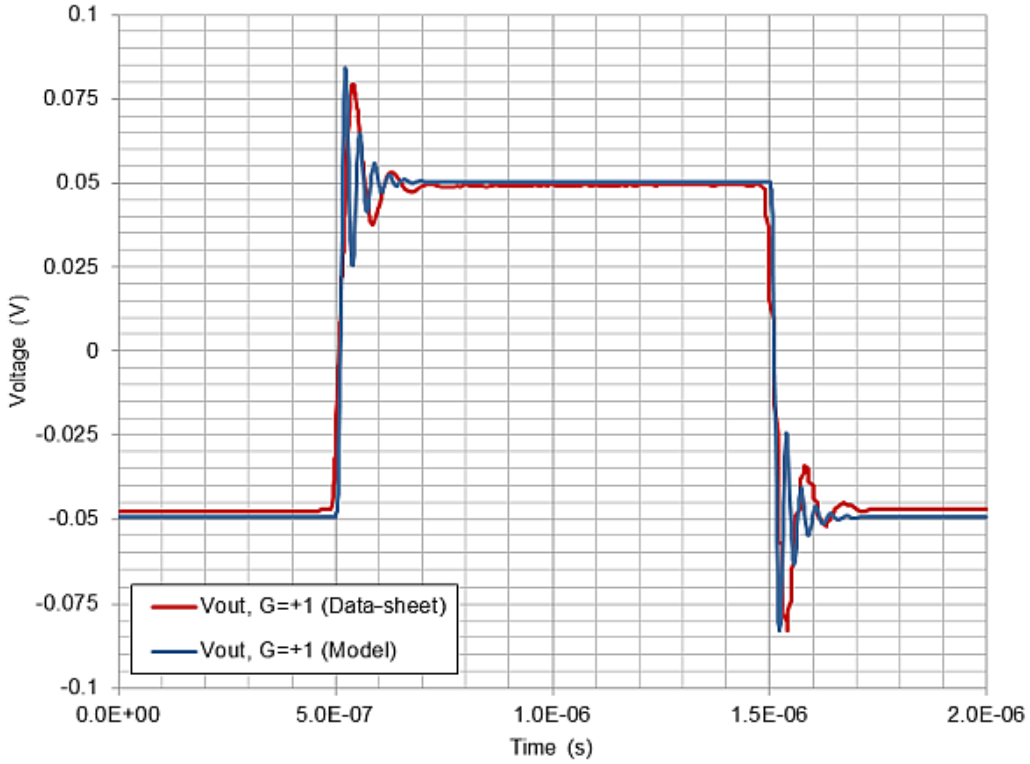

Figure 14 OPA1678 small-signal step response results, G = +1

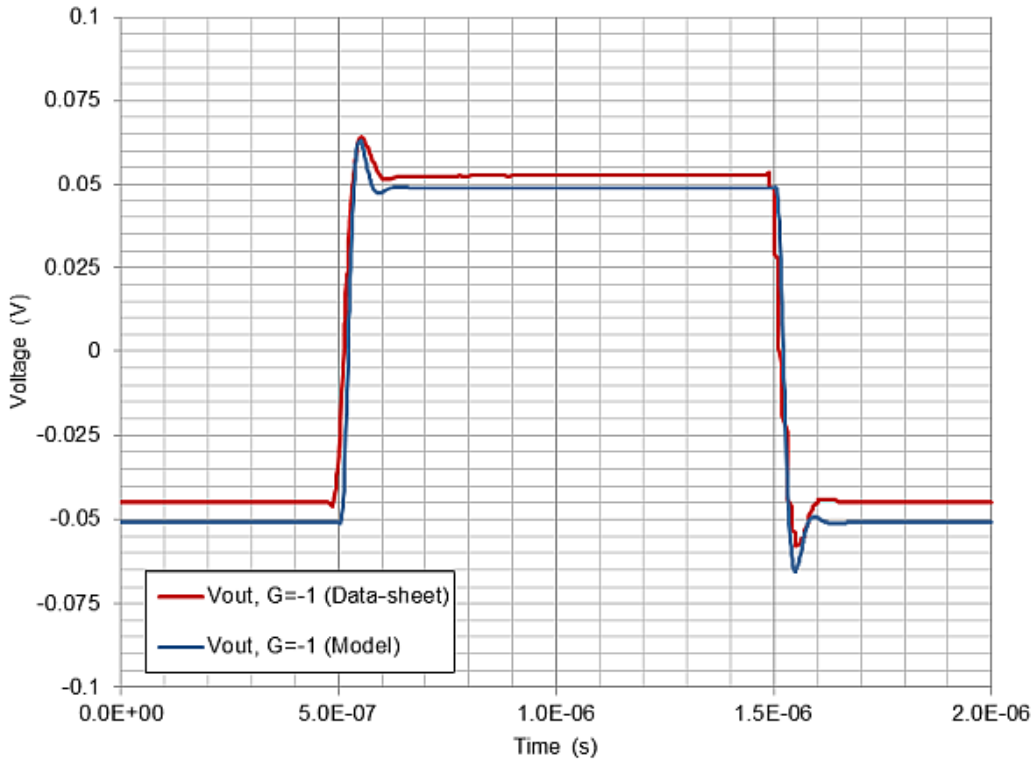

Figure 15 OPA1678 small-signal step response results, G = -1

For both Gain = +1 and Gain = −1, the rise time and percent overshoot of the OPA1678 model match closely with the data-sheet curves. Based on the results of the three parameters discussed and measured in this installment, you can conclude that the small-signal bandwidth of the OPA1678 SPICE model is accurate and gives results that closely match the behavior of real silicon.

In summary:

- Aol is the open-loop gain of an op amp, or the AC transfer function without any feedback applied. Most op amps have an Aol curve that follows a predictable response in both gain and phase. Aol is an inherent characteristic of the op amp design and does not change significantly based on feedback or load.
- Acl is the closed-loop gain of an op amp, or the AC transfer function with a specific feedback network (β) and other external circuit components connected. At low and middle frequencies, Acl is approximately equal to 1/β. At high frequencies, Acl is highly influenced by higher-order effects and external circuit elements.
- The small-signal step response is the representation of closed-loop gain in the time domain. In this response, the rise and fall time of the output voltage indicate closed-loop bandwidth, and the percent overshoot of the output voltage indicates phase margin or stability.

Thank you for reading the second installment in this series. In part 3, I'll show how to verify the input-referred error sources of an op amp, including common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR), input offset voltage (Vos), input bias current (Ib) and input offset current (Ios).

Ian Williams is an applications engineer and SPICE model developer for the precision amplifiers group at Texas Instruments.

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