**MIPS64 Processor Synthesis**

**External Architecture Specification**

John Dawson

256 37th street

Pittsburgh PA, 15201

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# Introduction

This document details the design of a custom 64 bit MIPS soft core processor for use within Altera FPGA devices.

## References

This section outlines the references used for this document.

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| --- | --- |
| MIPS64Instruction Set | *http://equipe.nce.ufrj.br/gabriel/arqcomp2/MIPS64\_Instruction\_Set\_v0.95.pdf* |
| Computer Organization and Design |  |
| See Mips Run Linux |  |
|  |  |
|  |  |

## Glossary of Terms

## Revision History

| **Version** | **Date** | **Changed By** | **Modifications** |
| --- | --- | --- | --- |
| 0.1 | 9Sept02 | J. Dawson | Initial draft. |

# Overview

# Pipeline Detailed Design

## Instruction Fetch (IF)

## Instruction Decode (ID)

### Overview

### Register Block

### Control Table

## Instruction Execute (IE)

### Overview

### ALU

## Memory Access (MEM)

### Overview

## Writeback (WB)

### Overview

## Data Forwarding Unit

## Hazard Unit

# Coprocessor 0 Detailed Design

## Overview

## Control Register Set

# Coprocessor 1 Detailed Design

## Overview

## Control Register Set