

**MIPS64 Processor Verification**

**External Architecture Specification**

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Table of Contents

[1. Introduction 4](#_Toc397423189)

[1.1 References 4](#_Toc397423190)

[1.2 Glossary of Terms 4](#_Toc397423191)

[1.3 Revision History 4](#_Toc397423192)

[2. Overview 5](#_Toc397423193)

[3. Block Simulation Strategies 6](#_Toc397423194)

[3.1 Instruction Fetch (IF) Block 6](#_Toc397423195)

[3.2 Instruction Decode (ID) Block 6](#_Toc397423196)

[3.3 Instruction Execute (IE) Block 6](#_Toc397423197)

[3.4 Memory Access (MEM) Block 6](#_Toc397423198)

[3.5 Writeback (WB) Block 6](#_Toc397423199)

[3.6 Data Forwarding Unit Block 6](#_Toc397423200)

[3.7 Hazard Unit Block 6](#_Toc397423201)

[4. CPU Simulation Strategy 7](#_Toc397423202)

[5. Coprocessor 0 Simulation Strategy 8](#_Toc397423203)

[6. Coprocessor 1 Simulation Strategy 9](#_Toc397423204)

# Introduction

This document details the hardware verification strategy used with the MIPS64 IP design.

## References

This section outlines the references used for this document.

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| MIPS64Instruction Set | *http://equipe.nce.ufrj.br/gabriel/arqcomp2/MIPS64\_Instruction\_Set\_v0.95.pdf* |
| Computer Organization and Design |  |
| See Mips Run Linux |  |
|  |  |
|  |  |

## Glossary of Terms

## Revision History

| **Version** | **Date** | **Changed By** | **Modifications** |
| --- | --- | --- | --- |
| 0.1 | 9Sept02 | J. Dawson | Initial draft.d |

# Overview

# Block Simulation Strategies

## Instruction Fetch (IF) Block

## Instruction Decode (ID) Block

## Instruction Execute (IE) Block

## Memory Access (MEM) Block

## Writeback (WB) Block

## Data Forwarding Unit Block

## Hazard Unit Block

# CPU Simulation Strategy

# Coprocessor 0 Simulation Strategy

# Coprocessor 1 Simulation Strategy