

**MIPS64 Processor Verification**

**External Architecture Specification**

John Dawson

256 37th street

Pittsburgh PA, 15201

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# Introduction

This document details the hardware verification strategy used with the MIPS64 IP design.

## References

This section outlines the references used for this document.

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| MIPS64Instruction Set | *http://equipe.nce.ufrj.br/gabriel/arqcomp2/MIPS64\_Instruction\_Set\_v0.95.pdf* |
| Computer Organization and Design |  |
| See Mips Run Linux |  |
|  |  |
|  |  |

## Glossary of Terms

## Revision History

| **Version** | **Date** | **Changed By** | **Modifications** |
| --- | --- | --- | --- |
| 0.1 | 9Sept02 | J. Dawson | Initial draft. |

# Overview

# Block Simulation Strategies

## Instruction Fetch (IF) Block

## Instruction Decode (ID) Block

## Instruction Execute (IE) Block

## Memory Access (MEM) Block

## Writeback (WB) Block

## Data Forwarding Unit Block

## Hazard Unit Block

# CPU Simulation Strategy

# Coprocessor 0 Simulation Strategy

# Coprocessor 1 Simulation Strategy