

# Foenix F256jr User's Manual

Peter Weingartner

October 1, 2022

# Contents

<b>1</b>	<b>Introduction</b>	<b>3</b>
<b>2</b>	<b>F256jr Basics</b>	<b>4</b>
<b>3</b>	<b>Memory Management</b>	<b>5</b>
3.0.1	Example: Setting up a LUT . . . . .	6
<b>4</b>	<b>The Text Screen</b>	<b>8</b>
4.1	Text Matrix . . . . .	8
4.1.1	Example: Print an A to the Screen . . . . .	8
4.2	Text Color LUTs . . . . .	9
4.3	Color Matrix . . . . .	9
4.3.1	Example: Make That “A” Yellow on Blue . . . . .	10
4.4	Entering Text Mode . . . . .	10
4.5	Text Fonts . . . . .	11
<b>5</b>	<b>Bitmap Graphics</b>	<b>12</b>
<b>6</b>	<b>Sprites</b>	<b>13</b>
<b>7</b>	<b>Tiles</b>	<b>14</b>
<b>8</b>	<b>Sound</b>	<b>15</b>
8.1	CODEC . . . . .	15
8.2	Using the PSGs . . . . .	16
8.2.1	Attenuation . . . . .	17
8.2.2	Tones . . . . .	17
8.2.3	Noise . . . . .	17
8.3	Using the SIDs . . . . .	18
8.3.1	Ring Modulation . . . . .	19
8.3.2	Synchronization . . . . .	19
<b>9</b>	<b>Interrupt Controller</b>	<b>20</b>
<b>10</b>	<b>Tracking Time</b>	<b>23</b>
10.1	Interval Timers . . . . .	23
10.2	Real Time Clock . . . . .	23
<b>11</b>	<b>Memory Maps</b>	<b>26</b>

# List of Tables

3.1	C256jr memory layout . . . . .	5
3.2	CPU Memory Banks . . . . .	5
3.3	I/O Banks . . . . .	6
3.4	MMU Registers . . . . .	6
4.1	Text Color Lookup Tables . . . . .	9
4.2	VICKY Master Control Registers . . . . .	10
4.3	A sample character . . . . .	11
8.1	CODEC Control Registers . . . . .	16
8.2	SN76489 Channel Registers . . . . .	16
8.3	SN76489 Command Formats . . . . .	16
8.4	SN76489 Noise Frequencies . . . . .	17
8.5	SID Registers . . . . .	19
10.1	MMU Registers . . . . .	23
10.2	RTC Periodic Interrupt Rates . . . . .	25
11.1	System Memory Map for the F256jr . . . . .	26
11.2	CPU Memory Map for the F256jr . . . . .	27
11.3	I/O Page 0 Addresses . . . . .	28
11.4	Memory Map for I/O Page 1 . . . . .	28

# Chapter 1

## Introduction

This manual is meant to be as complete as possible an introduction to the various hardware features of the F256jr. In it, I will attempt to explain each of the major subsystems of the F256jr and provide simple but practical examples of their use.

One thing this manual will not provide is a tutorial in programming the 65C02 processor at the heart of the F256jr. There are plenty of excellent books and videos explaining how the processor works and how to do assembly programming. While examples will generally be written in assembly, I will try to annotate them fully so that what is happening is very clear even to the novice assembly language coder.

## Chapter 2

# F256jr Basics

## Chapter 3

# Memory Management

The F256jr has 256 KB of system RAM which can be used for programs, data, and graphics. It also has 512 KB of read-only flash memory that can be used by whatever operating system is installed. Now, the 65C02 CPU at the heart of the F256jr has an address space of only 64 KB, so how can it access all this memory, not to mention the I/O devices on the system? The answer is paging. The F256jr has a special memory management unit (MMU) that can swap banks of memory or I/O registers into and out of the memory space of the CPU.

To understand how it all works, we first need to look at how RAM and flash memory are handled by the F256jr. Because there are 768 KB of total storage on the system, the system has a 20-bit address bus to manage the memory. RAM and flash have address on that 20-bit bus as shown in table 3.1.

Start	End	Memory Type
0x00000	0x2FFFF	System RAM (256 KB)
0x30000	0x7FFFF	Reserved for future use (256 KB)
0x80000	0xFFFFF	Flash Memory (512 KB)

Table 3.1: C256jr memory layout

This memory is divided up into “banks” of 8 KB each. The 16-bit address space of the CPU is also divided up into 8 KB banks. The MMU allows the program to assign any bank of system memory to any bank of the CPU’s memory. It does this through the use of memory look-up tables (LUT), which provide the upper bits needed to select the bank out of system memory for any given bank in CPU memory. It takes 13 bits to specify an address within 8 KB, which means for a 16-bit address from the CPU, the upper 3 bits are the bank number. Since the system bus is 20 bits, a bank number there is 7 bits. So a LUT must provide a 7-bit system bank number for each 3-bit bank number provided by the CPU.

The F256jr’s MMU supports up to four LUTs, only one of which is active at any given moment. This allows programs to define four different memory layouts and switch between them quickly, without having to alter a LUT on the fly.

Bank	A[15..13]	Start	End
0	000	0x0000	0x1FFF
1	001	0x2000	0x3FFF
2	010	0x4000	0x5FFF
3	011	0x6000	0x7FFF
4	100	0x8000	0x9FFF
5	101	0xA000	0xBFFF
6	110	0xC000	0xDFFF
7	111	0xE000	0xFFFF

Table 3.2: CPU Memory Banks

Of the eight CPU memory banks, one is special. Bank 6 can be mapped to memory as the rest can,

or it can be mapped to I/O registers, which are not memory mapped in the same way as RAM and flash. All I/O devices on the F256jr therefore live within 0xC000 through 0xDFFF on the CPU, but only if the MMU is set to map I/O to bank 6. There is quite a lot of I/O to access on the F256jr, so there are four different banks of I/O registers and memory that can be mapped to bank 6 (see table 3.3).

I/O Bank	Purpose
0	Low level I/O registers
1	Text display font memory and graphics color LUTs
2	Text display character matrix
3	Text display color matrix

Table 3.3: I/O Banks

Address	Name	7	6	5	4	3	2	1	0
0x0000	MMU_MEM_CTRL	EDIT_EN	RSVD	EDIT_LUT	RSVD	RSVD	RSVD	ACT_LUT	
0x0001	MMU_IO_CTRL	RSVD					IO_DISABLE	IO_PAGE	

Table 3.4: MMU Registers

The MMU is controlled through two main registers, which are always at locations 0x0000 and 0x0001 in the CPU's address space (see table 3.4). These registers allow programs to select an active LUT, edit a LUT, and control bank 6:

**ACT\_LUT** these two bits specify which LUT (0 - 3) is used to translate CPU bus address to system bus addresses.

**EDIT\_EN** if set (1), this bit allows a LUT to be edited by the program, and memory addresses 0x0010 - 0x0017 will be used by the LUT being edited. If clear (0), those memory locations will be standard memory locations and will be mapped like the rest of bank 0.

**EDIT\_LUT** if EDIT\_EN is set, these two bits will specify which LUT (0 - 3) is being edited and will appear in memory addresses 0x0010 - 0x0017.

**IO\_DISABLE** if set (1), bank 6 is mapped like any other memory bank. If clear (0), bank 6 is mapped to I/O memory.

**IO\_PAGE** if IO\_DISABLE is clear, these two bits specify which bank of I/O memory (0 - 3) is mapped to bank 6.

### 3.0.1 Example: Setting up a LUT

In this example, we will set up LUT 1 so that the first six banks of CPU memory map to the first banks of RAM, bank 7 of CPU memory maps to the first bank of flash memory, and bank 6 maps to the first I/O bank.

```

lda #$90      ; Active LUT = 0, Edit LUT#1
sta $0000

ldx #0        ; Start at bank 0
11: txa        ; First 6 banks will just be the first banks of RAM
sta $0010,x   ; Set the LUT mapping for this bank
inx          ; Move to the next bank
cpx #6        ; Until we get to bank 6
bne 11

lda #$40      ; Bank 7 maps to $80000, first bank of flash
sta $0017

```

```
stz $0001      ; Bank 6 should be I/O bank 0

lda #$01       ; Turn off LUT editing, and switch to LUT#1
sta $0000
```



## Chapter 4

# The Text Screen

The display on the F256jr is managed by TinyVicky, which is the smaller member of the Vicky family of display controllers in the other Foenix machines. TinyVicky provides several display engines to let your programs control the screen:

- Text: an old school style text screen where the characters to display are stored in a text matrix, and the shape of those characters comes from font memory. Text mode characters are 8 pixels wide by 8 pixels high.
- Bitmap: a simple pixel graphics mode that can be either 300x240 or 300x200. TinyVicky supports two layers of bitmap
- Sprite: an engine to display small, movable sprites on the screen. [TODO: how many and what resolutions]
- Tile: an engine to display images on the screen made up of tiles from a tile set [TODO: how many layers, tile size]

The bitmap, sprite, and tile engines are considered graphics modes. TinyVicky will let you display either text by itself, a mix of the graphics modes by themselves, or text overlayed on top of the graphics modes.

### 4.1 Text Matrix

The memory for the characters to display on the screen is the text matrix, which is stored in I/O page 2. When this I/O page is swapped into the CPU address space, it appears at 0xC000. Each byte of memory corresponds to a single character on the screen in left to right, top to bottom order. The byte at 0xC000 is the upper left corner of the screen, the byte at 0xC001 is the next character to the right, and so on. The number of bytes per line is set by the base resolution of the screen, but is generally 80. When a border is displayed, while that limits the number of characters displayed, the layout in memory remains the same.

The text screen has two core resolutions, tied to the refresh rate of the screen: 80 by 60 at 60 Hz, and 80 by 50 at 70 Hz. Beyond that, the character display may be made double width or double height, or both. This gives the following possible character displays: 80 × 60, 40 × 60, 80 × 30, 40 × 30, 80 × 50, 40 × 50, 80 × 25, and 40 × 25.

#### 4.1.1 Example: Print an A to the Screen

```
lda $0001      ; Save the current MMU setting
pha

lda #$02       ; Swap I/O Page 2 into bank 6
sta $0001

lda #'A'       ; Write 'A' to the upper left corner
```

```

sta $C000

pla          ; Restore the old MMU setting
sta $0001

```

Note: this example does not set the font or the color, so depending on how your F256jr is initialized, you may not see an actual “A” on the screen.

## 4.2 Text Color LUTs

Characters in TinyVicky text mode have two colors: the foreground and the background. The foreground and background colors are picked for each character out of two different palettes of 16 colors each. The colors in the palettes are picked from the full range of colors F256jr can produce, which is more than 16 million colors. This is all managed through two color lookup tables (LUTs) provided by TinyVicky: a text foreground color LUT, and a text background color LUT.

The text LUTs are stored in I/O page 0. The foreground LUT starts at 0xD800, and the background LUT starts at 0xD840.

Each LUT is a list of 16 entries. Each entry is a set of four bytes: blue, green, red, and alpha. Each byte indicates how much of that primary color is present as a component of the actual color. The values range from 0 (none) to 255 (as much as possible). Currently, the alpha channel is not used and is there for future expansion.

Index	Foreground	Background	0	1	2	3
0	0xD800	0xD840	BLUE_0	GREEN_0	RED_0	X
1	0xD804	0xD844	BLUE_1	GREEN_1	RED_1	X
2	0xD808	0xD848	BLUE_2	GREEN_2	RED_2	X
3	0xD80C	0xD84C	BLUE_3	GREEN_3	RED_3	X
4	0xD810	0xD850	BLUE_4	GREEN_4	RED_4	X
5	0xD814	0xD854	BLUE_5	GREEN_5	RED_5	X
6	0xD818	0xD858	BLUE_6	GREEN_6	RED_6	X
7	0xD81C	0xD85C	BLUE_7	GREEN_7	RED_7	X
8	0xD820	0xD860	BLUE_8	GREEN_8	RED_8	X
9	0xD824	0xD864	BLUE_9	GREEN_9	RED_9	X
10	0xD828	0xD868	BLUE_10	GREEN_10	RED_10	X
11	0xD82C	0xD86C	BLUE_11	GREEN_11	RED_11	X
12	0xD830	0xD870	BLUE_12	GREEN_12	RED_12	X
13	0xD834	0xD874	BLUE_13	GREEN_13	RED_13	X
14	0xD838	0xD878	BLUE_14	GREEN_14	RED_14	X
15	0xD83C	0xD87C	BLUE_15	GREEN_15	RED_15	X

Table 4.1: Text Color Lookup Tables

## 4.3 Color Matrix

The way that text color is selected for each character is through the color matrix. This section of memory is in I/O page 3 and starts at 0xC000 when page 3 is swapped into the CPU’s address space. The layout is precisely the same as the text matrix (e.g. the character at 0xC123 in the text matrix has its color information at 0xC123 in the color matrix).

Each byte in the color matrix specifies two colors by providing an index into each of the two text LUTs. The most significant four bits is the number of the foreground color to use. The number of the least significant four bits is the number of the background color to use.

Let’s say the color value at 0xC123 is 0x45. This means that the foreground color of the character is color 4 from the text foreground LUT, which starts at 0xD810 ( $0xD800 + 4 * 4$ ), and the background color of the character is 5 from the text background LUT, which starts at 0xD854 ( $0xD840 + 4 * 5$ ). If

the bytes at 0xD810 are 0x00, 0x80, 0x80, that means the foreground will be a medium yellow. If the bytes at 0xD854 are 0xFF, 0x00, 0x00, that means the background will be blue.

### 4.3.1 Example: Make That “A” Yellow on Blue

```

lda $0001      ; Save the MMU state
pha

stz $0001      ; Switch in I/O Page #0

stz $D810      ; Set foreground #4 to medium yellow
lda #$80
sta $D811
sta $D812

lda #$FF       ; Set background #5 to blue
sta $D854
stz $D855
stz $D856

lda #$03       ; Switch to I/O page #3 (color matrix)
sta $0001

lda #$45       ; Color will be foreground=4, background=5
sta $C000

pla           ; Restore the MMU state
sta $0001

```

## 4.4 Entering Text Mode

Whether or not text mode is being displayed (and in what resolution) is controlled by the VICKY Master Control Registers (see table 4.2). For now, we’re going to ignore most of the bits, which are used by other display modes. For text mode, we really only care about the TEXT bit, which needs to be set to turn on the text display. The resolution is controlled by DBL\_Y, DBL\_X, and CLK\_70. If we set 0xD000 to 0x01 and 0xD001 to 0x00, that will put us into text mode at 80 × 60.

Address	7	6	5	4	3	2	1	0
0xD000	X	GAMMA	SPRITE	TILE	BITMAP	GRAPH	OVRLY	TEXT
0xD001	X					DBL_Y	DBL_X	CLK_70

Table 4.2: VICKY Master Control Registers

**TEXT** if set (1), text mode display is enabled

**OVRLY** if set, text will be overlaid on graphics

**GRAPH** if set, one or more of the graphics modes may be used

**BITMAP** if set (and GRAPHICS is set), bitmap graphics may be displayed

**TILE** if set (and GRAPHICS is set), tile graphics may be displayed

**SPRITE** if set (and GRAPHICS is set), sprite graphics may be displayed

**GAMMA** if set, gamma correction is enabled

**CLK\_70** if set, the video refresh will be set to 70 Hz mode (640x400 text resolution, 320x200 graphics).  
If clear, the video refresh will be set to 60 Hz (640x480 text resolution, 320x240 graphics).

**DBL\_X** if set, text mode characters will be twice as wide (320 pixels)

**DBL\_Y** if set, text mode characters will be twice as high (240 or 200 pixels, depending on CLK\_70)

## 4.5 Text Fonts

Character shapes (or “glyphs,” if you prefer) are defined in font memory, which is in I/O page 1 and starts at 0xC000. The F256jr treats each character as a square of pixels, 8 pixels on a side. A pixel may be either in the foreground color for the character or in the background color for the character. The way this is managed is that each character has a sequence of eight bytes in the font memory. Each byte represents a row in the character, and each bit represents a pixel in the row (■ for foreground, □ for background).

As an example, let’s say we wanted to have a fancy “F” for character 0:

□	□	□	■	■	■	■	■	0x1F
□	□	■	■	□	□	□	□	0x30
□	□	■	■	□	□	□	□	0x30
□	■	■	■	■	■	□	□	0x7C
□	■	■	□	□	□	□	□	0x60
■	■	□	□	□	□	□	□	0xC0
■	■	□	□	□	□	□	□	0xC0

Table 4.3: A sample character

The glyph to display would be defined by the eight byte sequence 0x1F, 0x30, 0x30, 0x7C, 0x60, 0xC0, 0xC0. We would store that sequence in I/O page 0, starting at 0xC000 (0x1F), through 0xC007 (0xC0). After that was set, any time the byte 0x00 is written to screen memory, the glyph “F” would be displayed in that position.

## Chapter 5

# Bitmap Graphics

## Chapter 6

# Sprites

## Chapter 7

# Tiles

# Chapter 8

## Sound

The F256jr supports two different sound chips, although only one is built-in. The built-in sound chip is the SN76489 (called the “PGS” here), which was used by many vintage machines including the TI99/4A, the BBC Micro, the IBM PCjr, and the Tandy 1000. On the F256jr, the PSG is implemented as two stereo PSGs in the FPGA. The other chip supported is the Commodore SID chip (6581 or 8580). The SID is not installed by default, but the board comes with two sockets for SID chips. The F256jr supports the original 6581, the lower voltage 8580, and the modern SID replacement projects.

### 8.1 CODEC

The F256jr (and indeed all the Foenix computers up to this point) makes use of a WM8776 CODEC chip. You can think of the CODEC as the central switchboard for audio on the F256jr. The CODEC chip has inputs for several different audio channels (both analog and digital), and each audio device on the F256jr is routed to an input on the CODEC. The CODEC then has outputs for audio line level and headphones. The CODEC will convert analog inputs to digital, mix all the audio inputs according to its settings, and then convert the resulting digital audio to analog and drive the outputs. With the CODEC, you can turn on and off the various input channels, control the volume, and mute or enable the different outputs.

The CODEC is a rather complex chip with many features, and the full details are really beyond the scope of this document. Most programs for the F256jr will not need to use it or will only use it in very specific ways. Therefore, this document will really just show how to access it and initialize it and then leave a reference to the data sheet for the chip that has the complete data on the chip.

Raw access to the CODEC chip is fairly complex. Fortunately, the FPGA on the F256jr provides three registers to simply access for programs. The FPGA takes care of the actual timing of transmitting data to the CODEC, serializing the data correctly, and so on. All the program needs to know about are the correct format for the 16-bit command words that are sent to the CODEC, and then a status register to monitor.

The CODEC commands are based around a number of registers. Each command is really just writing values to those registers. The command words are 16-bits wide, with the 7 most significant bits being the number of the register to write, and the 9 least significant bits being the data to write. For instance, there is a register to enable and disable the headphone output. Bit 0 of the register controls whether or not the headphone output is enabled (0 = enabled, 1 = disabled). The register number is 13. So, to disable the output on the headphones, we would need to write 000000001 to register 13. The register number in binary is 0001101, So the command word we would need to send is 0001101000000001\ or 0x1A01.

The registers for the CODEC on the F256jr are:

Bit 0 of the status/control register both triggers sending the command (on a write) and indicates if the CODEC is busy receiving a command (writing a 1 triggers the sending of the command, reading a 1 indicates that the CODEC is busy).

So to mute the headphones, we would issue the following:

```
wait:  lda $D622      ; Wait for the CODEC to be ready
        and #$01
        cmp #$01
```



Address	R/W	7	6	5	4	3	2	1	0	Purpose
0xD620	W	D7	D6	D5	D4	D3	D2	D1	D0	Command Low
0xD621	W	R6	R5	R4	R3	R2	R1	R0	D8	Command High
0xD622	R	X							BUSY	Status
0xD622	W	X							START	Control

Table 8.1: CODEC Control Registers

```

beq wait ; Bit 0 = 1, CODEC is still busy... keep waiting

lda #$01 ; Set command to %0001101000000001, or R13 <- 000000001
sta $D620
lda #$1A
sta $D621

lda #$01 ; Trigger the transmission of the command to the CODEC
sta $D622

```

## 8.2 Using the PSGs

The F256jr has support for dual SN76489 (PSG) sound chips, emulated in the FPGA. The SN76489 was used in several vintage machines, including the TI-99/4A, BBC Micro, IBM PCjr, and Tandy 1000. The chip provides three independent square-wave tone generators and a single noise generator. Each tone generator can produce tones of several frequencies in 16 different volume levels. The noise generator can produce two different types of noise in three different tones at 16 different volume levels.

Access to each PSG is through a single memory address, but that single address allows the CPU to write a value to eight different internal registers. For each tone generator, there is a ten bit frequency (which takes two bytes to set), and a four bit “attenuation” or volume level. For the noise generator, there is a noise control register and a noise attenuation register.

R2	R1	R0	Channel	Purpose
0	0	0	Tone 1	Frequency
0	0	1	Tone 1	Attenuation
0	1	0	Tone 2	Frequency
0	1	1	Tone 2	Attenuation
1	0	0	Tone 3	Frequency
1	0	1	Tone 3	Attenuation
1	1	0	Noise	Control
1	1	1	Noise	Attenuation

Table 8.2: SN76489 Channel Registers

There are four basic formats of bytes that can be written to the port:

D7	D6	D5	D4	D3	D2	D1	D0	Purpose
1	R2	R1	R0	F3	F2	F1	F0	Set the low four bits of the frequency
0	X	F9	F8	F7	F6	F5	F4	Set the high seven bits of the frequency
1	1	1	0	X	FB	F1	F0	Set the type and frequency of the noise generator
1	R2	R1	R0	A3	A2	A1	A0	Set the attenuation (four bits)

Table 8.3: SN76489 Command Formats

Note: there is a PSG sound device for the left stereo channel and one for the right. The left channel PSG can be accessed at 0xD600, and the right channel at 0xD610. Both are in I/O page 0.

### 8.2.1 Attenuation

All the channels support attenuation or volume control. The PSG expresses the loudness of the sound with how much it is attenuated or dampened. Therefore, an attenuation of 0 will be the loudest sound, while an attenuation of 15 will make the channel silent.

### 8.2.2 Tones

Each of the three sound channels generates simple square waves. The frequency generated depends upon the system clock driving the chip and the number provided in the frequency register. The relationship is:

$$f = \frac{C}{32n}$$

where  $f$  is the frequency produced,  $C$  is the system clock, and  $n$  is the number provided in the register. Expressed a different way, the value we need to produce a given frequency can be computed as:

$$n = \frac{C}{32f}$$

For the F256jr the system clock is 3.57 MHz, which means:

$$n = \frac{111,563}{f}$$

So, let us say we want channel 1 to produce a concert A, which is 440Hz at maximum volume. The value we need to set for the frequency code is  $111,320/440 = 253$  or 0xFE. We can do that with this code:

```
lda #$90      ; %10010000 = Channel 1 attenuation = 0
sta $D600     ; Send it to left PSG
sta $D610     ; Send it to right PSG

lda #$8E      ; %10001100 = Set the low 4 bits of the frequency code
sta $D600     ; Send it to left PSG
sta $D610     ; Send it to right PSG

lda #$0F      ; %00001111 = Set the high 7 bits of the frequency
sta $D600     ; Send it to left PSG
sta $D610     ; Send it to right PSG
```

To turn it off later, we just need to write:

```
lda #$9F      ; %10011111 = Channel 1 attenuation = 15 (silence)
sta $D600     ; Send it to left PSG
sta $D610     ; Send it to right PSG
```

### 8.2.3 Noise

Noise works differently from tones, since it is random. The noise generator on the PSG can produce two styles of noise determined by the FB bit: white noise (FB = 1), and periodic (FB = 0). The noise has a sort of frequency, based on either the system clock or the current output of tone 3. This frequency is set using the F1 and F0 bits:

F1	F0	Frequency
0	0	$C/512$
0	1	$C/1024$
1	0	$C/2048$
1	1	Tone 3 output

Table 8.4: SN76489 Noise Frequencies

As an example, to set white noise of the highest frequency ( $C/512$  or around 6 kHz), we could use the code:

```

lda #$F0      ; %10010000 = Channel 3 attenuation = 0
sta $D600     ; Send it to left PSG
sta $D610     ; Send it to right PSG

lda #$E4      ; %11100100 = white noise, f = C/512
sta $D600     ; Send it to left PSG
sta $D610     ; Send it to right PSG

```

To turn it off later, we just need to write:

```

lda #$FF      ; %11111111 = Channel 3 attenuation = 15 (silence)
sta $D600     ; Send it to left PSG
sta $D610     ; Send it to right PSG

```

### 8.3 Using the SIDs

The SID is a full-featured analog sound synthesizer, and a full explanation of how to use it is really beyond the scope of this document. In this document, I will provide just an introduction to the chip and list the register addresses for the SID chips that can be installed on the F256jr (see table 8.5).

The SID chip provides three independent voices (so it can play three notes at once). The three voices are almost identical in their features, with voice 3 being the only one different. Each voice can produce one of four basic sound wave forms: randomized noise, square waves, saw tooth waves, and triangle waves. These waves can be generated over a range of frequencies, and for the square waves, the width of the pulse (*i.e.* *duty cycle*) may be adjusted.

The type of wave form produced by a voice is controlled by the NOISE, PULSE, SAW, and TRI bits. If NOISE is set to 1, the output is random noise. If PULSE is set, a square wave is produced. If SAW is set, a saw tooth wave is produced. If TRI is set, the voice produces a triangle wave. If PULSE is set, the duty cycle of the square wave (or pulse width, if you prefer) is set by the PW bits according to the formula  $PW/40.95$  (expressed as a percent).

The frequency of the waveform is set by the bits  $F[15..0]$ . This number sets the actual frequency according to the formula:

$$f_{\text{out}} = \frac{FC}{16777216}$$

where:  $f_{\text{out}}$  is the output frequency,  $F$  is the number set in the registers, and  $C$  is the system clock driving the SIDs. For the F256jr,  $C$  is 1.022714 MHz, so the formula for the F256jr is:

$$f_{\text{out}} = \frac{F}{16.405}$$

or:

$$F = 16.404 f_{\text{out}}$$

For example: concert A, which is 440 Hz, would be:  $F = 16.405 \times 440 \approx 7218$ . So, to play a concert A, you would set the frequency to 7218, or 0x1C32.

Each of the three voices has a sound “envelope” which changes the volume of the sound during the duration of the note. There are four phases to the sound envelope: attack, decay, sustain, and release (ADSR). When the note first starts playing (that is, the GATE bit for the voice is set to 1), it starts at the attack phase when the volume starts at zero and goes up to the current maximum volume. How fast this happens is determined by the attack rate (ATK3-0 in the registers). Once the volume reaches the maximum, the volume goes down again to the sustain volume. This phase is called decay, and the speed at which the volume drops is determined by the DCY3-0 register values. Next, the envelope enters the sustain phase, where the volume is held steady at the sustain level (STN3-0). It stays here until the note is to stop playing (GATE is set to 0). At this point, the envelope enters the release stage, where the volume drops back to zero at the release rate (RLS3-0).

The ADSR envelope allows the SID chip to mimic the qualities of various musical instruments or shape various sound effects. For instance, a pipe organ’s notes are typically either on or off, so the attack, decay, and release rates would be set to be instantaneous, and the sustain level would be set to full. A piano, on the other hand tends to have a sharp, somewhat percussive sound at the beginning with the note holding a long time on release if not dampened.

Voice	Offset	7	6	5	4	3	2	1	0
V1	0	F7	F6	F5	F4	F3	F2	F1	F0
	1	F15	F14	F13	F12	F11	F10	F9	F8
	2	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
	3	X				PW11	PW10	PW9	PW8
	4	NOISE	PULSE	SAW	TRI	TEST	RING	SYNC	GATE
	5	ATK3	ATK2	ATK1	ATK0	DLY3	DLY2	DLY1	DLY0
	6	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
V2	7	F7	F6	F5	F4	F3	F2	F1	F0
	8	F15	F14	F13	F12	F11	F10	F9	F8
	9	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
	10	X				PW11	PW10	PW9	PW8
	11	NOISE	PULSE	SAW	TRI	TEST	RING	SYNC	GATE
	12	ATK3	ATK2	ATK1	ATK0	DLY3	DLY2	DLY1	DLY0
	13	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
V3	14	F7	F6	F5	F4	F3	F2	F1	F0
	15	F15	F14	F13	F12	F11	F10	F9	F8
	16	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
	17	X				PW11	PW10	PW9	PW8
	18	NOISE	PULSE	SAW	TRI	TEST	RING	SYNC	GATE
	19	ATK3	ATK2	ATK1	ATK0	DLY3	DLY2	DLY1	DLY0
	20	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
	21	X					FC2	FC1	FC0
	22	FC10	FC9	FC8	FC7	FC6	FC5	FC4	FC3
	23	RES3	RES2	RES1	RES0	EXT	FILTV3	FILTV2	FILTV1
	24	MUTEV3	HIGH	BAND	LOW	VOL3	VOL2	VOL1	VOL0
	25	paddle x							
	26	paddle y							
	27	oscillator 3							
	28	envelope 3							

Table 8.5: SID Registers

While the different voices are independent, they can be set to alter one another through two different effects: synchronization, and ring modulation. With these features, the voices can interact with each other in the following pairs:

- Voice 1  $\rightarrow$  Voice 2
- Voice 2  $\rightarrow$  Voice 3
- Voice 3  $\rightarrow$  Voice 1

### 8.3.1 Ring Modulation

If a voice's RING bit is set and the voice is set to use the triangle wave form (TRI is set), then the triangle wave will be replaced by the combination of the two voice's frequencies. So if the RING bit of voice 1 is set, the result will be the ring modulation of voice 1 and voice 3. Ring modulation tends to produce harmonics and overtones and can be used for bell like sounds.

### 8.3.2 Synchronization

If a voice's SYNC bit is set, the frequency it produces will be synchronized to the controlling voice. So if voice 1's SYNC bit is set, its frequency will be synchronized to voice 3.

## Chapter 9

# Interrupt Controller

The 65C02 has two interrupts: non-maskable interrupts (NMI) for high priority events, and the regular interrupt request line (IRQ) for normal priority events. Currently, the C256 series of computers do not use NMI for any purpose, so the only interrupt is the IRQ line. There are many devices on the F256jr which can trigger interrupts, so to save the interrupt handler the chore of querying each device in turn, the F256jr provides an interrupt controller module. The individual devices route their interrupt request signals to the interrupt controller. When an interrupt comes in, the controller knows which device it is and decides whether or not to forward the interrupt to the CPU. The interrupt handler can then query the interrupt handler to see which device or devices have interrupts pending and can then acknowledge them once they have been properly handled.

The interrupt controller provides two sets of registers to provide its functionality: interrupt masks, and interrupt pending. The mask registers provide a mask flag for every possible interrupt. If the flag is true (1), the interrupt from that device is masked, and an interrupt coming in from it will not trigger an IRQ on the processor. The pending register provides a pending flag for every possible interrupt. If the flag is true (1) on a read, the device has requested an interrupt, if false (0) there is no interrupt pending from the device. Setting a flag in a pending register to 1 will acknowledge the interrupt and cause the controller to drop the pending flag. Writing a 0 to a flag will have no effect.

NOTE: Some of the devices on the F256jr have their own interrupt enable flags (separate from the mask flags). For example, the 65C22 VIA has an interrupt enable bit in one of its registers and will not send an interrupt to the F256jr's interrupt controller if that bit is not enabled. For such devices, the interrupt enable flag on the device must be set and the corresponding mask bit in the interrupt controller must be clear in order for interrupts to be sent to the CPU. Other devices, like VICKY, do not have a separate enable flag. In their case, only their corresponding mask bits must be cleared to enable their interrupts.

Mask	Pending	Bit	Name	Purpose
0xD666	0xD660	0x01	INT_VKY_SOF	TinyVicky Start Of Frame interrupt <sup>1</sup>
		0x02	INT_VKY_SOL	TinyVicky Start Of Line interrupt <sup>2</sup>
		0x04	INT_PS2_KBD	PS/2 keyboard event
		0x08	INT_PS2_MOUSE	PS/2 mouse event
		0x10	INT_TIMER_0	TIMER0 has reached its target value
		0x20	INT_TIMER_1	TIMER1 has reached its target value
		0x40	INT_DMA	DMA has completed
		0x80	RESERVED	
0xD667	0xD661	0x01	INT_UART	The UART is ready to receive or send data
		0x02	RESERVED	
		0x04	RESERVED	
		0x08	RESERVED	
		0x10	INT_RTC	Event from the real time clock chip
		0x20	INT_VIA	Event from the 65C22 VIA chip
		0x40	INT_IEC	Event from the IEC serial bus
		0x80	INT_SDC_INS	User has inserted an SD card

As an example of working with the interrupt controller, let's try using the SOF interrupt to alter the character in the upper left corner.

To start, we will need to install our interrupt handler to respond to IRQs. For this example, we're going to completely take over interrupt processing, so we'll do some things we wouldn't ordinarily do. Also, since an interrupt could come in while we're setting things up, we need to be careful about how we do things.

1. First, we want to disable IRQs at the CPU level.
2. Then we set the interrupt vector.
3. Next, we want to mask off all but the SOF interrupt, since that is the only one we will process (in real programs, we will either need to handle several interrupts or play nicely with the operating system).
4. Now, there might be interrupts that came in earlier, so will go ahead and just clear all the pending interrupt flags so we start cleanly.
5. Finally, we enable CPU interrupt handling again and loop forever... processing the SOF interrupt when it comes in.

VIRQ = \$FFFE

```
INT_PEND_0 = $D660 ; Pending register for interrupts 0 - 7
INT_PEND_1 = $D661 ; Pending register for interrupts 8 - 15
INT_MASK_0 = $D666 ; Mask register for interrupts 0 - 7
INT_MASK_1 = $D667 ; Mask register for interrupts 8 - 15
```

```
start:      ; Disable IRQ handling
            sei

            ; Load my IRQ handler into the IRQ vector
            ; NOTE: this code just takes over IRQs completely. It could save
            ;       the pointer to the old handler and chain to it when it had
            ;       handled its interrupt. But what is proper really depends on
            ;       what the program is trying to do.
            lda #<my_handler
            sta VIRQ
            lda #>my_handler
            sta VIRQ+1

            ; Mask off all but the SOF interrupt
            lda #$ff
            sta INT_MASK_1
            and #~INT00_VKY_SOF
            sta INT_MASK_0

            ; Clear all pending interrupts
            lda #$ff
            sta INT_PEND_0
            sta INT_PEND_1

            ; Put a character in the upper right of the screen
            lda #SYS_CTRL_TEXT_PG
            sta SYS_CTRL_1

            lda #'@'
            sta $c000

            ; Set the color of the character
```

```

lda #SYS_CTRL_COLOR_PG
sta SYS_CTRL_1

lda #$F0
sta $c000

; Go back to I/O page 0
stz SYS_CTRL_1

; Make sure we're in text mode
lda #$01          ; enable TEXT
sta $D000         ; Save that to VICKY master control register 0
stz $D001

; Re-enable IRQ handling
cli

```

To actually process the interrupt, we need to read and then increment the character at the start of the screen, clear the pending flag for the SOF interrupt, and then return. However, the screen and the interrupt control registers are in different I/O banks, so we'll need to change the I/O bank a couple of times during interrupt processing. So, the first thing we will do is to save the value of the system control register at 0x0001, so we can restore it before we return from the interrupt.

```
SYS_CTRL_1 = $0001
```

```
SYS_CTRL_TEXT_PG = $02
```

```
my_handler: pha
```

```

; Save the system control register
lda SYS_CTRL_1
pha

; Switch to I/O page 0
stz SYS_CTRL_1

; Check for SOF flag
lda #INT00_VKY_SOF
bit INT_PEND_0
beq return          ; If it's zero, exit the handler

; Yes: clear the flag for SOF
sta INT_PEND_0

; Move to the text screen page
lda #SYS_CTRL_TEXT_PG
sta SYS_CTRL_1

; Increment the character at position 0
inc $c000

; Restore the system control register
pla
sta SYS_CTRL_1

; Return to the original code
pla
rti

```

```
return:
```

# Chapter 10

## Tracking Time

### 10.1 Interval Timers

### 10.2 Real Time Clock

For programs needing to keep track of time, F256jr provides a real time clock chip (RTC), the bq4802. This chip, keeps track of the year (including century), month, day, hour (in 12 or 24 hour mode), minute, and second. The coin cell battery on the F256jr motherboard is to provide power to the RTC so it can continue tracking time even when the F256jr is turned off or unplugged. Additionally, the RTC can send interrupts to the CPU, either periodically or at a specific time.

The RTC is relatively straightforward to use, but one potentially tricky thing to keep in mind is that there is a specific procedure to follow when reading or writing the date-time. As well as the registers the CPU can access, the RTC has internal registers which are constantly updating as time progresses. Normally, the internal registers update their external counterparts, but this should not be allowed to happen while the CPU is getting or setting the externally facing registers. So, to access the external registers, the program must first disable the automatic updates to the external registers. Then it can read or write the external registers. Then it can re-enable the automatic updates. If the program has changed the registers, when updates are re-enabled the data in the external registers will be sent to the internal registers in one action. This keeps the time information consistent.

Address	Name	7	6	5	4	3	2	1	0
0xD690	Seconds	0	second 10s digit			second 1s digit			
0xD691	Seconds Alarm	0	second 10s digit			second 1s digit			
0xD692	Minutes	0	minute 10s digit			minute 1s digit			
0xD693	Minutes Alarm	0	minute 10s digit			minute 1s digit			
0xD694	Hours	AM/PM	0	hour 10s digit		hour 1s digit			
0xD695	Hours Alarm	AM/PM	0	hour 10s digit		hour 1s digit			
0xD696	Days	0	0	day 10s digit		day 1s digit			
0xD697	Days Alarm	0	0	day 10s digit		day 1s digit			
0xD698	Day of Week	0	0	0	0	0	day of week digit		
0xD699	Month	0	0	0	month 10s digit	month 1s digit			
0xD69A	Year	year 10s digit				year 1s digit			
0xD69B	Rates	0	WD			RS			
0xD69C	Enables	0	0	0	0	AIE	PIE	PWRIE	ABE
0xD69D	Flags	0	0	0	0	AF	PF	PWRF	BVF
0xD69E	Control	0	0	0	0	UTI	STOP	12/24	DSE
0xD69F	Century	century 10s digit				century 1s digit			

Table 10.1: MMU Registers

There are 16 registers for the RTC (see table 10.1). There is a register each for century, year, month, day of the week (*i.e.* Sunday - Saturday), day, hour, minute, and second. Each one is expressed in binary-coded-decimal, meaning the lower four bits are the ones digit (0 - 9), and the upper bits are the



10s digit. In most cases, the upper digit is limited (*e.g.* seconds and minutes can only have 0 - 6 as the tens digit). For seconds, minutes, hours, and day there is a separate alarm register, which will be described later. Finally, there are the four registers for rates, enabled, flags, and control:

The Enables register has four separate enable bits:

**AIE** if set (1), the alarm interrupt will be enabled. The RTC will raise an interrupt when the current time matches the time specified in the alarm registers.

**PIE** if set (1), the RTC will raise an interrupt periodically, where the period is specified by the RS field.

**PWRIE** if set (1), the RTC will raise an interrupt on a power failure (not relevant to the F256jr).

**ABE** if set (1), the RTC will allow alarm interrupts when on battery backup (not relevant to the F256jr).

The Flags register has four separate flags, which generally reflect why an interrupt was raised:

**AF** if set (1), the alarm was triggered

**PF** if set (1), the periodic interrupt was triggered

**PWRF** if set (1), the power failure interrupt was triggered

**BVF** if set (1), the battery voltage is within safe range. If clear (0), the battery voltage is low, and the time may be invalid.

The Control register has four bits which change how the RTC operates:

**UTI** if set (1), the update of the externally facing registers by the internal timers is inhibited. In order to read or write those registers, the program must first set UTI and then clear it when done.

**STOP** this bit allows for a battery saving feature. If it is clear (0) before the system is powered down, it will avoid draining the battery and may stop tracking the time. If it is set (1), it will keep using the battery as long as possible.

**12/24** sets whether the RTC is using 12 or 24 hour accounting.

**DSE** if set (1), daylight savings is in effect.

The Rates register controls the watchdog timer and the periodic interrupt. The watchdog timer is not really relevant to the F256jr, but it monitors for activity and raises an interrupt if activity has not been seen within a certain amount of time (specified by the WD field). The periodic interrupt will be raised repeatedly, the period of which is set by the RS field (see table 10.2).

RS3	RS2	RS1	RS0	Period
0	0	0	0	None
0	0	0	1	30.5175 $\mu s$
0	0	1	0	61.035 $\mu s$
0	0	1	1	122.070 $\mu s$
0	1	0	0	244.141 $\mu s$
0	1	0	1	488.281 $\mu s$
0	1	1	0	976.5625 $\mu s$
0	1	1	1	1.95315 ms
1	0	0	0	3.90625 ms
1	0	0	1	7.8125 ms
1	0	1	0	15.625 ms
1	0	1	1	31.25 ms
1	1	0	0	62.5 ms
1	1	0	1	125 ms
1	1	1	0	250 ms
1	1	1	1	500 ms

Table 10.2: RTC Periodic Interrupt Rates

## Chapter 11

# Memory Maps

Address	Purpose
0x00000 0x3FFFF	System RAM for programs, data, and graphics (256 KB)
0x40000 0x7FFFF	
0x80000 0xFFFFF	Flash memory (512 KB)

Table 11.1: System Memory Map for the F256jr

Bank	Purpose	
0	0x0000	MMU Memory Control Register
	0x0001	MMU I/O Control Register
	0x0002	RAM or Flash
	0x000F	
	0x0010	RAM, Flash, or MMU LUT Registers
	0x001F	
	0x0020	65C02 Page Zero
	0x00FF	
	0x0100	65C02 Stack
	0x01FF	
	0x0200	RAM or Flash
	0x1FFF	
1	0x2000	RAM or Flash
	0x3FFF	
2	0x4000	RAM or Flash
	0x5FFF	
3	0x6000	RAM or Flash
	0x7FFF	
4	0x8000	RAM or Flash
	0x9FFF	
5	0xA000	RAM or Flash
	0xBFFF	
6	0xC000	RAM, Flash, I/O, Text mode character, or color data
	0xDFFF	
7	0xE000	RAM or Flash
	0xFFFFA	
	0xFFFFA	65C02 NMI Vector
	0xFFFFB	
	0xFFFFC	65C02 Reset Vector
	0xFFFFD	
	0xFFFFE	65C02 IRQ Vector
	0xFFFFF	

Table 11.2: CPU Memory Map for the F256jr

Start	End	Purpose
0xC000	0xC3FF	Gamma Table Blue
0xC400	0xC7FF	Gamma Table Green
0xC800	0xCBFF	Gamma Table Red
0xCC00	0xCFFF	Reserved
0xD000	0xD0FF	VICKY Master Control Registers
0xD100	0xD1FF	VICKY Bitmap Control Registers
0xD200	0xD2FF	VICKY Tile Control Registers
0xD300	0xD3FF	Reserved
0xD400	0xD4FF	SID Left
0xD500	0xD4FF	SID Right
0xD600	0xD60F	PSG Left
0xD610	0xD61F	PSG Right
0xD620	0xD62F	CODEC
0xD630	0xD63F	UART
0xD640	0xD64F	PS/2 Interface
0xD650	0xD65F	Timers
0xD660	0xD66F	Interrupt Controller
0xD670	0xD67F	DIP Switch
0xD680	0xD68F	IEC Controller
0xD690	0xD69F	Real Time Clock
0xD6A0	0xD6AF	System Control Registers
0xD6B0	0xD7FF	Reserved
0xD800	0xD83F	Text Foreground Color LUT
0xD840	0xD87F	Text Background Color LUT
0xD880	0xD8FF	Reserved
0xD900	0xDAFF	VICKY Sprite Control Registers
0xDB00	0xDBFF	Reserved
0xDC00	0xDCFF	65C22 VIA Control Registers
0xDD00	0xDDFF	SD Card Controller
0xDE00	0xDEFF	Integer Math Coprocessor
0xDF00	0xDFFF	DMA Controller

Table 11.3: I/O Page 0 Addresses

Start	End	Purpose
0xC000	0xC7FF	Text Mode Font Memory
0xC800	0xCFFF	Reserved
0xD000	0xD3FF	Graphics Color LUT 0
0xD400	0xD7FF	Graphics Color LUT 1
0xD800	0xDBFF	Graphics Color LUT 2
0xDC00	0xDFFF	Graphics Color LUT 3

Table 11.4: Memory Map for I/O Page 1