Lab 04 – Automatic Sequencer

Students work in pairs with a triple if there is an odd number attending the lab session.

Learning objectives:

1. Design a circuit to generate an endless sequence of 8 assertions that can be used to point to memory locations or to input/output devices.
2. Gain experience in writing a program at the logic device level (machine language level).
3. Gain experience creating and reading logic circuit schematics and generating a bill of materials (BOM).

Required equipment: Lab kit provided by your TA.

Due at the end of this lab session.

1. Give your completed and scored breadboard circuit schematic and BOM to your TA.
2. As much of your constructed and tested breadboard circuit as you can complete before the lab session scheduled time ends but at least demonstrate the working 555 timer output using an LED.

Grading

Before the end of this lab session, do the following to earn up to 20 points.

1. [15 points] Breadboard Circuit Schematic and BOM sheet scored in lab by your TA.
2. [5 points] Demonstrate correct operation on your breadboard of the 555 clock circuit, at least, and any additional portion of the automatic sequencer that you finish in two hours. Then remove all components from the breadboard except the 10 Ohm resistor and power distribution wires and return those parts to the lab kit box.

Overview

An automatic sequencer is a basic building block of all processors. It supports the instruction Fetch-Execute Cycle for sequential reading of machine program instructions stored as an array in memory by the processor. (Fetch of instructions forming an if-else or while loop control structure requires a slightly more complex circuit that can skip ahead or skip backwards in the array index sequence, respectively.)

The automatic sequencer combines three logic circuit functions: Clock (555 DIP), Counter (74163 DIP), and Decoder. (74138 DIP) The 555 clock circuit emits a steady stream of alternating logic levels and is used to control the pacing of circuit operation.

The 74163 counter contains a 4-bit register to store the current count value and an incrementor logic function circuit. Typical operation is to compute new a new 4-bit output, QD QC QB QA, = (QD QC QB QA + 1) modulo 16 with each clock signal rising edge. The 74163 is programmable in the following three ways. It has logic to change the increment amount to 0 to suspend counting. It also includes a synchronous CLR' input and logic to allow the count to be cleared, i.e., QD QC QB QA = 0000, on the next clock rising edge. Finally, QD QC QB QA can be synchronously set to any 4-bit string value using the LOAD' input. The 74163 uses unsigned weighted-positional integer representation.

The 74138 decoder accepts a 3-bit address and three enable signals and outputs an assertion on 0-of-8 (decoder in a disabled state) or 1-of-8 wires (decoder in its enabled state). The enables make the decoder programmable.

Step 1 – Write the "Declaration Statements" in the Sequencer Circuit Diagram

Your TA will provide you with a hardcopy sheet titled "My Breadboard Circuit Schematic and Bill of Materials (BOM)" called Worksheet for simplicity hereinafter.

Using the information in the following two tables, declare all inputs to the 74163 and 74138 chips. These declarations will specify power connections, logic signal paths, and "programming" for the circuit. To get you started, the declaration of all 555 chip inputs are given on the worksheet. Add your declarations in the same style and level of abstraction to accomplish the following for the Sequencer:

1. Enable the 74163 circuit to increment the count value.
2. Allow the initial count value to be whatever random number appears at power ON of the 74163.
3. Enable the decoder to assert its outputs.
4. Have the decoder assert a new output with each rising edge of the 555 clock signal.
5. Display the low-active 74138 outputs by eight LED symbols that point towards the outputs from Ground.
6. If a 74138 or 74163 input pin will not connect to a defined logic signal, draw a short line out from the pin and label that wire "NC" for "no connection".

As you draw declarations on the worksheet for all input pins of the 74163 and 74138 chips, use that information to fill in the quantities for the Bill of Materials (BOM) table.

Flip over the worksheet and complete the computation of the 555 clock signal characteristics: frequency, time high, and time low.

Definition of 74163 to Guide your Input Declarations Choices

The 74163 counter circuit counts rising edges appearing on its clock signal input by incrementing a count value modulo 16. The 74163 outputs a 4-bit count value.

74163 Pin	Name and purpose
1	Clear', an active low device-programming input, that commands the counter to an output of 0000 at any time, called "clearing the count". For this lab, connect Pin 1 to +5 V (Vcc) because the count should sequence modulo 16 at all times and, thus, never be cleared.
2	Clock input. The count value increments when this logic signal has a rising edge.
3, 4, 5, and 6	A, B, C, and D count value initialization inputs to allow setting the count value to an known, i.e., "initial," value. For this lab these pins are Unused. It is safe to leave these pins unconnected, unlike most logic signal inputs, because these inputs are connected to a multiplexer that ignores them when input Load' is not asserted.
7	Enable P. One of two enables for the function, increment the count mod 16.
8	Ground. One of the two terminals necessary to supply power to the package.
9	Load', an active low signal that at the time of the next rising clock edge replaces the current count value with the value present on Data Input wires, A, B, C, and D.
10	Enable T. Second enable for the function, increment the count mod 16.
11, 12, 13, 14	Count value output in unsigned weighted positional representation. Pin 14 is the LSB and has weight 2^0 and pin 11 is the MSB and has weight 2^3.
15	Ripple Carry Output from the count. Allows daisy chaining of multiple 74163 chips to make counters with outputs numbering any multiple of 4 bits and counting modulo 2^{2k} given k linked chips.
16	Vcc. One of the two terminals necessary to supply power to the package.

The 74163 data sheet is available at http://www.futurlec.com/74HC/74HC163.shtml

Definition of 74138 to Guide Your Input Declarations Choices
The 74138 decoder accepts only 3 bits of unsigned integer input, so you must decide which 3 output bits from the 74163 to send to the 74138 so that the 74138 will assert a different output for each clock signal rising edge. To make your three choices, examine how frequently the bits of a 4-bit unsigned integer representation will change as the represented value is incremented (increased by 1) continuously.

74138 Pin	Name and purpose
1, 2, and 3	Pins for the address to be decoded, where Pin 1 is the least significant bit (LSB) and Pin 3 is the most significant bit (MSB) of the unsigned integer representation of the address value.
4, 5, and 6	Enables G1, G'2A, and G'2B. These enable signals allow daisy-chaining this chip with one or three copies to make 4x16 or 5x32 decoder circuits, respectively. To enable 3x8 decoding only, set pins 4, 5, and 6 to LOW, LOW, and HIGH, respectively.
8	Ground.
7, 9, 10, 11, 12, 13, 14, and 15	Pins 15 through 9 correspond to decoder outputs Y0' through Y6', respectively. Pin 7 outputs Y7'. These outputs are active low.
16	Vcc.

The 74138 data sheet is available at http://pdf1.alldatasheet.com/datasheet-pdf/view/51038/FAIRCHILD/74138.html

STEP 1 SCORING [first 15 of 20 available points]: Before lab ends. and when you complete both sides of the worksheet, call your TA for scoring.

BUILD STEP – Use your Schematic Declarations and BOM to Build to Specification

After your TA has scored your worksheet, use that information to build the sequencer circuit on your breadboard. Build as much as you can during lab. Build in the following sequence and according to the following specifications. Test each newly ready logic signal output with an LED as you build.

1. Place pin 1 of the 555 DIP in breadboard row 5 and place pin 4 in row 8.
2. Use the wire color coding given in the Bill of Materials.

3. Complete the 555 circuit. Double check that capacitors C1 and C2 are placed into the circuit with correct polarity orientation.
   Power the circuit and test it using an LED to "printf" the output clock signal on pin 3. Complete any debugging of the 555 circuit before going to step 4. Call your TA to help with debugging now, if needed. Leave the clock signal visualization LED in place on your breadboard.

4. Place pin 1 of the 74163 in row 9, and pin 8 in row 16. Place pin 1 of the 74138 in row 17 and pin 8 in row 24. The reason for this placement is that the next lab will add to this circuit and there must be room for the devices to be added.
5. Make all the wires in your BOM now, while you are in lab and have access to a wire stripper tool.

6. Using your schematic, connect all logic signal inputs to the 74163 counter. Place 4 LEDs on the breadboard to display the active high count value bus signals. Power, then test the combined 555 and 74163 circuit and debug as necessary. Call your TA for help if needed.

7. Using your schematic, connect all inputs for the decoder. Place 8 LEDs in a line (4 of these will be re-purposing the LEDs used to examine the 74163 output value) along pins 15 through 9 of the 74138 and use a wire to bring the 7 pin output across to the line of 8 LEDs. Remember that the 74138 is an active low output circuit,. Thus, the LEDs must be placed with their short terminal wire tied to a decoder output and their long terminal wire (for higher voltage) connected to which reference voltage bus? Test your 3-DIP sequencer circuit. You should see the 8 decoder outputs assert one at a time with each successive LED lighting with the rising clock edge, which causes the clock signal LED to also illuminate. Debug and ask your TA as needed.

STEP 2 SCORING [final 5 points]: Before your lab session ends demonstrate correct operation on your breadboard of the 555 clock circuit, at least, and any additional portion of the automatic sequencer that you finish in two hours.

Appendix – Timing and Waveform Equations and Reference Information for 555 chip

The functions of the 8 pins of the 555 DIP are as follows.

555 Pin	Name and purpose
1	Ground
2	Trigger. When this input falls below 1/2 of the voltage at CTRL (Pin 5) then OUT (Pin 3) emits a rising edge and a timing interval starts
3	Clock. 555 chip output.
4	Reset. Active low. Clock is reset by driving this input to GND. Timing begins when RESET rises above approximately 0.7V.
5	CTRL. Control. Provides control access to the internal voltage divider.
6	Threshold setting. The timing interval ends when the voltage at THR is greater than at CTRL.
7	Discharge. Empties the charge in capacitor C2 through a path internal to the 555 circuit, causing the voltage on pin 2 to fall until the pin 2 Trigger action ends the discharge cycle and starts a new timing interval.
8	Vcc

A 555 datasheet is at http://en.wikipedia.org/wiki/555_timer_IC .

See an animation of 555 operation at http://www.falstad.com/circuit/e-555int.html .

555 Timing and Waveform Equations

The values of the external components R1 and R2 in units of Ohms and C2 in units of Farads control the waveform of the pulses emitted by the 555. Note that C2 has a capacitance of 1000 microFarads (millionths of a Farad).

The frequency, f, of the pulse stream in units of cycles per second, called Hertz, generated by the 555 is given by the equation

f in Hertz = 1 / (0.693*C2*(R1 + 2*R2)).

The time that the signal is at a high voltage within each pulse is

t_high in seconds = 0.693*(R1 + R2)*C2 .

The low voltage time of each pulse is

t_low in seconds = 0.693*R2*C2 .