CS 25000 Computer Architecture PRACTICE Midterm 1 Fall 2025

Name: _____ PU ID: | 0 | 0 | | | | | | | | |
Print name used in Brightspace

During this exam you may not use books, notes, or devices. You may not talk.

Do not ask questions about the examduring the exam.

Write your answers entirely inside the provided boxes.

Points are earned by what is written inside each box only: write legibly, erase diligently.

All boxes have ample space for the correct answer.

Do supporting work on backs of pages.

Midterm 1 may contain a different number of questions than appear in this Practice Midterm 1.

I will neither give nor receive aid on this exam.

Sign here

DO NOT turn the page until told to start the rest of this exam. Thank you.

Check that this document contains all pages. If not, raise your hand to obtain a copy that does have all pages before you proceed.

Only what appears within the answer box will be scored. Write legibly.
For multiple choice questions, answer using the letter of your choice.
Use the back of document pages or the page margins for working out answers.

1. [ ] True or False. Interpreters have been implemented in software and in hardware.

2. [ ] Assembly language syntax matches machine instruction format field order.
   A True
   B False

[ ] 2. An immediate operand is an operand obtained from a register in the register unit.
   A True
   B False

[ ] 3. Which location is not suitable for containing input resulting from program prompts that request input from the program user?
   A Immediate operand field within a machine instruction
   B Register in the CPU register file
   C Main memory
   D No one of answers A, B, and C names a not suitable location.
   E Each one of answers A, B, and C names a not suitable location.

[ ] 4. Sometimes the bit string in the opcode field of a machine instruction representation has no valid meaning. True or False?

5. [ ]

   This device controls which register in the register file has its output bus connected to an input bus of the ALU.

6. Computer hardware executes [ ] language programs.

7. An ordered sequence of bits is called a [ ].

8. What are the weights used in the 5-bit 2's complement integer representation?

[ ]

9. [ ] Write your answer inside the box.

How many of these representations – sign magnitude, unsigned integer, and 2's complement – have two ways to represent the integer zero?

10. [ ]

Modifying computer hardware to point to sixteen times more memory locations than was possible for the original hardware requires

A Adding one more wire to the address bus
B Adding two more wires to the address bus
C Adding four more wires to the address bus
D Increasing the number of address bus wires to sixteen times as many as the original number
E None of the above answers is correct

11. [ ]

How many hexadecimal digits are required to represent a 24-bit bit string?

A 5
B 24
C 16
D The question provides insufficient information to determine its answer.
E None of the above answers is correct.

12. [ ]

If possible, express decimal integer -8 in 4-bit 2's complement representation. Otherwise, answer "Not possible".

13. Answer using an integer only, no units.

If a machine instruction points to two operands and one result that are stored in a collection of 32 locations, how many bits in the machine instruction representation are devoted to pointing to operand locations and the result location?

14.

In total, how many input and output buses does a multiplexer, also called a selector, with an n-bit address bus have?

15.

The n-bit bit string inequality function can be defined using a truth table. How many input columns does this truth table have?

16.

True or False? Sign extension can be used to cast the 4-bit unsigned integer representation to eight bits.

17.

Which is easier to fetch from instruction memory, variable-length machine instructions or fixed-length machine instructions?

18. Write the letter for your answer inside the box.

Which stores a bit string?

A integer adder
B register
C selector
D demultiplexer
E None of the above answers is correct.

19. 0x

Write the bit string 0100111110001011 using hexadecimal notation.

20. [ ] Write your answer in the form of an integer.

2^27 bits is how many Mebibytes?

21. A multiplexer has a total of 9 input and output buses. How many bits wide is its address bus?

[ ]

22. [ ] Answer must have the form 2^k for some k.

A particular 32-bit, fixed-length, machine instruction representation can provide the address bits to a multiplexer that is selecting the result of an ALU function for an ALU containing up to 64 different functions. How many 32-bit bit strings share the same opcode field when paired with this representation?

23. [ ]

A register operand field in a machine language instruction is

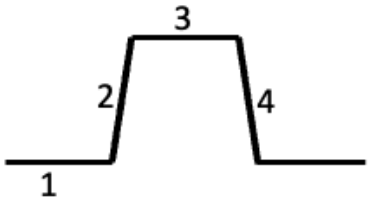
A a pointer.
B a value.
C located immediately following the opcode field.
D the same size as the opcode field.
E a power of two number of bits.

24. [ ]

How many voltage bands are used to represent a bit on a wire?

25. [ ] Write the number in the box

What numbered segment of the logic signal waveform is the rising edge?



26. Which is a LEGv8 instruction that computes z = x + y?
    A ADD X34, X35, X36
    B ADD X1, X2, X3
    C ADDI X1, X2, #y
    D z = x + y
    E None of the other answers is correct.

27. Which is not a valid LEGv8 instruction?
    A ADD X7, X8, X22
    B LDUR X8
    C SUB X7, X7, X7
    D CBNZ X4, L1
    E CBNZ X4, Else

28. Does every S'R' latch circuit built from two 2-input NAND gates and with S' and R' both not asserted output the same Q value when powered on?
    A Yes
    B No

29. To command the S'R' latch so that Q(t) = 1 becomes Q(t+1) = 0 which input is required?
    A S'R' = 00
    B S'R' = 01
    C S'R' = 10
    D S'R' = 11
    E More than one of the above answers will command the stated latch output transition.

30. If a clock signal rising edge is used to indicate the time at which it is safe to write a result bus bit string into a result register, then the time interval between consecutive clock signal rising edges _____ the worst case propagation delay of the combinatorial circuit computing that result bus bit string. Choose the answer that correctly fills in the blank.
    A must be greater than or equal to
    B must be less than
    C must be equal to
    D must be twice
    E must be at least one gate delay more than