Design of a Dual-Antenna and Dual-Band GPS Receiver for CubeSats

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***Abstract*—During the last few years, there has been a rise in the use of nanosatellites because they offer a low cost and short development time alternative to larger satellites intended for long-duration missions. The use of commercial components (COTS) instead of the expensive space-grade components required for long missions is one of the main reasons of the popularity of the nanosatellites. This paper presents the hardware design of a GPS receiver compatible with the CubeSat standard. The receiver has two antenna inputs and is capable of operating on the L1 and L2 bands. Since the proposed design is based on non-space qualified components, a tolerance and fault mitigation scheme for SEU and SEL events produced by the effect of radiation is implemented.**

I. Introduction

The access to the space has been significantly changed since the creation of nanosatellites, in particular the CubeSats. The CubeSat standard, developed by the Polytechnic University of California about eighteen years ago, has allowed hundreds of educational or private organizations to carry out scientific and commercial space missions [1] [2].

Compared to traditional satellites, nanosatellites usually use low orbits (LEO) and require small volume and low manufacturing costs. In addition, the electronic modules of a CubeSat are usually built with commercial components (COTS) instead of radiation-tolerant components that are extremely costly and difficult to acquire.

In the space environment the radiation manifests itself in a random and instantaneous way through Single Event Upsets (SEU) and Single Event Latch-ups (SEL), causing transient failures in the COTS. There is another kind of radiation effect known as Total Ionizing Dose (TID) which can produce permanent faults on the components. The amount of damage due to TID depend on the exposure time of the component to the radiation. For CubeSats TID effect is usually negligible because of the short duration of most missions.

SEUs occur when a charged particle impacts a storage element causing a change in its logic state, generating a data error. SEUs can be mitigated using error correction codes (EDAC) on memory devices and data scrubbing for RAM memories and SRAM FPGAs.

SELs are more dangerous than SEUs since they increase the supply current of an affected device and can cause permanent damage to it. Mitigation of SELs is complex, since a device power-on reset must be performed to stop the short circuit. However, in some cases this may not be effective. The occurrence of SEUs and SELs depends on the level of radiation in the environment, the design of the integrated circuit and the technology used for its construction. In particular, CMOS circuits are very vulnerable to this type of events.

In some applications the CubeSat position needs to be known accurately, such as for the orbital tracking of the satellite path. The recent advances in development of digital cameras suitable for CubeSats allow implementing earth observation missions. In order to determine the region of the planet pointed by the camera, the systems on-board the CubeSat should determine its position. On the other hand, segmented satellite architectures require absolute and relative position and speed of each member vehicle in order to guarantee the proper functioning of the satellite network. For example, for distributed synthetic aperture radar (SAR) imaging it is necessary to know the position of the satellites to obtain a correct integration of the joint image.

In this type of applications, the satellites should have a global navigation satellite system (GNSS) receiver on-board. A GNSS receiver uses medium-orbit (MEOs) satellite constellations to determine its position and speed. Currently the only two fully operational GNSS constelations are GPS and GLONASS, which transmit several ranging signals on different frequency bands called L1, L2 and L5 [3]. A multiband GPS receiver can calculate the navigation solution, i.e. position and speed, with greater accuracy than a monoband receiver [4].

This paper presents the hardware design of a L1/L2 GPS receiver able to operate with one or two antennas. The proposed design is suitable for CubeSats because it has the required form factor, although its use in other types of small satellites is also possible. On the other hand, this design can operate with some commercial CubeSats on-board computers (OBC) [5] [6]. The use of more than one antenna increases the reliability of the navigation solution since it allows improving the reception of the signals of the GPS satellites. In addition, having the navigation solution of two antennas permits, under certain conditions of satellite visibility, to estimate the orientation of the satellite [7].

The rest of this paper is organized as follows. Section II presents the proposed design. Section III discusses the failure mitigation scheme. Section IV details the design of the printed circuit board and its mechanical fit in a CubeSat frame. Finally,

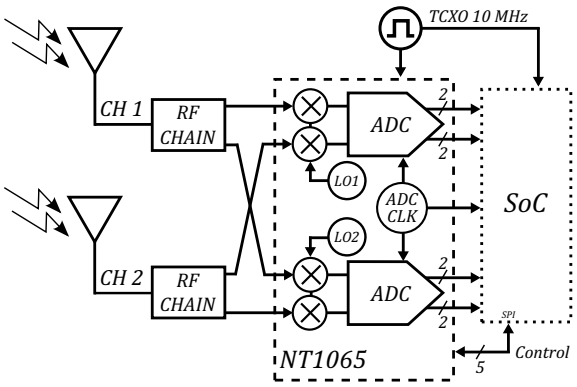

Fig. 1. Receiver block diagram.

the conclusion is in Section V.

II. Proposed design

The proposed design is based on the typical architecture of a GPS receiver, consisting of a radiofrequency (RF) stage and a digital signal processing platform [8] [9]. The RF stage receives the signals from the antennas and provides the necessary amplification and filtering. The RF signals are then converted to a lower intermediate frequency (IF) to perform analog to digital conversion. The digital processing platform receives the samples, performs the necessary correlations to acquire the satellites present in the antenna, demodulates the data and calculates the navigation solution, which is sent to another device by means of a communication interface.

Due to the size limitations, emphasis was placed on reducing the size of the RF front-end. There are COTS in the market that perform the functions of a GPS RF front-end, like the one used in [10]. For this work, the integrated circuit chosen to implement the RF front-end is the NT1065 of NTLab [11]. The main virtue of this chip is that it has four independent RF channels, which makes it suitable for implementing a multi-antenna or multi-band receiver. Moreover, this chip has a very low power consumption compared to an RF front-end implemented with discrete components, which makes it ideal for a CubeSat application. These characteristics justify the choice of the NT1065 to implement the receiver.

A block diagram of the proposed design is shown in Fig. 1. In the RF chain, the signals received by the antenna are amplified and separated into two channels by an RF splitter. Then, each channel is filtered with a SAW filter tuned at the center frequency of the desired GPS band, i.e. L1 or L2. The filtered signals are down-converted and sampled using the NT1065, which provides two bit per sample (magnitude and sign) for each IF signal. These samples and the sampling clock signal are processed by a SoC (System-on-Chip) synthesized in an FPGA. The SoC consists of a processor and a dedicated hardware for GPS signal processing. For the SoC implementation, the FPGA has external SRAM and FLASH memories. For debugging purposes, JTAG and USB-UART interfaces are available. The main communication interfaces are an RS-422 rx/tx channel and an isolated I2C bus. The interfaces are used to send the navigation information to the satellite OBC.

The design of the digital signal processing stage is based on a commercial Artix 7 SRAM type FPGA [12]. This kind of FPGAs have larger logical capacity than their space qualified counterparts. In addition, they consume less power and are much cheaper. Despite this FPGA is not a radiation tolerant component, is adequate because the CubeSat missions are not critical and have a typical duration of a few months.

The temperature of a satellite varies depending on the exposition to the sun. These variations may affect the electronic components. Particularly, the frequency of a crystal oscillator is modified if its temperature changes. In GPS receivers, the reference frequency variations can highly degrade the quality of the navigation solution. For this reason in the proposed design the frequency reference is provided by a temperature compensated crystal oscillator (TXCO), which has the required frequency stability to ensure the proper functioning of the receiver [13]. The RF and the signal processing stages use both the same frequency reference of 10 MHz.

To achieve mechanical compatibility with commercial modules for CubeSats, the receiver has the form factor indicated in [14]. For electrical compatibility two 52-pin connectors are used to support the PC-104 standard, which is typically adopted to interconnect CubeSat's modules. The modules are placed one on top of the other, forming a vertical structure. The number of modules determines the volume of the satellite. The volume is measured in units of CubeSat, being one standard unit (1U) 10cm$\times$10cm$\times$10cm. There are CubeSats of 1,2,3,6 and up to 12U.

The proposed design can support both active and passive antennas, however an active antenna is recommended to obtain a better performance. It is noted that a L1/L2 antenna is needed for dual-band operation. If the application does not require the use of two independent antennas, the receiver can operate with only one antenna. For example, the space or the consumption required for a dual antenna operation may not be compatible with a CubeSat of size 1U or 2U. To choose the gain of the antennas, it should be taken into account that the RF chain of each channel has a gain of about 15 dB and the recommended overall gain is between 15 dB and 35 dB. For this reason, a resistive attenuator is placed to adjust the gain for the chosen antenna.

The receiver is designed to operate from a 5V supply, which is provided by the satellite power conversion module through the PC-104 connector. To generate the voltages needed for the digital circuits of the receiver, three switching regulators are used. The power for the RF stage is provided by a linear regulator in order to avoid noise figure degradation.

The proposed design has circuits capable of detecting and mitigating SEL and SEU, that are described in the next section.

III. Reliability

As mentioned above, the main challenge for COTS in space is radiation, which causes component failure or even destruction. In LEO orbits the radiation is mainly manifested

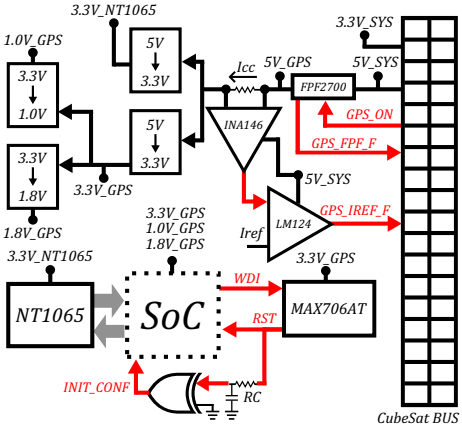

Fig. 2. Failure detection and mitigation scheme.

by the impact of protons on the electronic equipment. Because of the duration of a typical Cubesat mission, the reliability analysis carried out only considers SEU and SEL events.

NASA categorizes CubeSats missions as type D, where the acceptable risk is high because low cost and low complexity are prioritized [15][16]. Therefore, the proposed mitigation scheme is according to class D missions. We propose to reduce the number of elements that detect the occurrence of both SEU and SEL, since these components will also be commercial and therefore vulnerable to radiation. For SEL mitigation, we decided to use the OBC to turn the receiver on and off, since it is assumed that the OBC module will have greater or equal fault tolerance. Regarding operating faults due to SEU, the receiver will be responsible for mitigating them using an external watchdog that will monitor the behavior of the processor. The proposed scheme for detecting and mitigating receiver faults can be seen in Fig. 2.

A. Failures due to SEL:

In order to save a receiver fault caused by a SEL, the proposed design has the FPF2700 integrated circuit that allows the OBC to control the power of the whole module through the signal GPS_ON. This chip has a current limit, as well as temperature and short circuit protection [17]. The FPF2700 is widely used in CubeSats, therefore its behavior in a radiation environment has been studied [18]. If an event triggers the chip protection, the receiver's power supply is turned off and the OBC is notified of the fault by means of the logic signal GPS_FPF_F. In addition, the receiver has a current measuring circuit composed of a differential amplifier INA146 and an LM124 operational amplifier operating as a comparator, which allows to set a current limit according to the maximum total consumption of the receiver. This value is approximately 350 mA at 5V, which is lower than the FPF2700 threshold [17]. The output of the comparator is connected to the satellite PC-104 connector, in order to inform the OBC, which can make a decision according to the current measurement. The choice of INA146 and LM124 is based on the information about their radiation tolerance presented in [19].

B. Failures due to SEU:

Three techniques are usually used to mitigate faults due to SEU. The most used consist on monitoring the processor that runs the software of the module and reseting it when a fault occurs. This is achieved by means a watchdog that can be internal or external to the processor. Another technique is the detection and correction of errors in the memories through additional parity bits. The third technique is used in SRAM type memories and SRAM FPGAs. It consists of monitoring the RAM and correcting errors by sector in order to avoid losing functionality. This is also known as scrubbing.

In this work an external watchdog circuit is used to trigger the reconfiguration of the FPGA device, which produces a complete reset of the receiver. The operation is as follows. The processor periodically sends a pulse to the watchdog circuit. When a failure occurs, the processor stops and therefore the periodic pulses cease. If after one second the watchdog does not detect a pulse input, it will reset the receiver. In order to guarantee the effectiveness of the system reset it is important to take into account the timing of the signals that command the reconfiguration of the FPGA. To do this, the configuration start signal, INIT_CONF, must be set high after the RESET signal. To ensure a correct relative timing between these two signals, a delay of 1 ms is introduced given by the RC circuit placed at the input of the XOR gate as shown in Fig. 2.

IV. Printed Circuit Board Design

The printed circuit board (PCB) design consists of ten layers on a substrate of FR4 material. Four signal layers were used, two of them were internal. In order to improve the signal integrity, four ground planes were placed to minimize inductive coupling. The distribution of the voltages required by the receiver was carried out using two power planes [20]. The ground planes are interspersed between signal layers, and above and below the power planes, forming a scheme that enhance the signal integrity. The complete design of the top layer of the PCB is shown in Fig. 3.

The dimensions of the board follow the guidelines described in [14]. For practical and electromagnetic compatibility reasons, all the necessary connectors were located on the periphery of the board. The components used in this design are surface mount technology, due to their good qualities for high speed digital designs and their small size that is needed for reducing the board area. Most of the integrated circuits were placed on the top layer, leaving the bottom layer for the passive components, such as capacitors and resistors. The average trace width is 6 mils, which is mostly determined by the BGA package of the FPGA which has 484 balls. All the vias are plated through hole with a hole diameter of 0.2mm and a pad diameter of 0.46mm. The antenna input traces have a characteristic impedance of 50 Ω. For this purpose, a microstrip transmission line was implemented on the top and bottom layers using a trace width of 7 mils and a separation between the signal layer and the ground plane of 4 mils. Other signals of interest are the system and sampling clocks, as well as the differential pairs of USB and RS-422. For the single

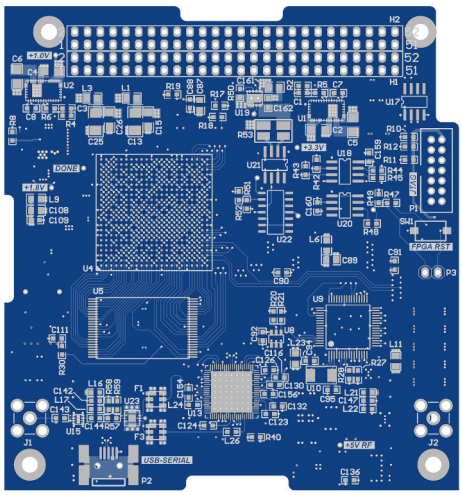

Fig. 3. Top layer of the designed PCB.

ended lines, the value of an eventual termination resistor was calculated using time-domain signal simulation. For example, the system clock signal that comes from a buffer and enters to the FPGA uses a 33 Ω series resistor in order to remove ringing caused by the reflections in the line. The value was calculated by simulations using IBIS models of the buffer and the FPGA [21].

To detect mechanical interferences, the 3D model of the receiver was integrated with the 3D model of a typical 1U structure of a CubeSat. The correct mechanical connection of the receiver with other modules was verified. The height of the receiver does not exceed the height of the PC-104 connector, therefore the CubeSat standard of 15 mm spacing between modules is needed. Fig. 4 shows a full 3D render of the proposed design in a frame next to a commercial OBC [6].

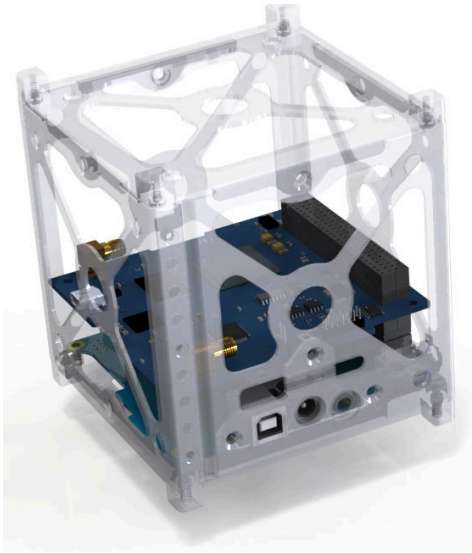

Fig. 4. 3D view of the proposed design above a commercial OBC module in a CubeSat 1U frame.

V. Conclusions

The hardware design of a multi-band GPS receiver with two antenna inputs compatible with the CubeSat standard and with different commercial modules available in the market was presented. According to the CubeSat philosophy, which consist of minimizing the cost and complexity of the hardware, the proposed design is based on COTS. Because in missions of relative short duration in LEO orbits such as CubeSats missions, radiation affects COTS mainly through SEU and SEL events, a fault mitigation scheme was implemented. The design process is finished and the obtained simulation results are satisfactory, which justify the fabrication of a prototype to perform the final validation tests and measurements.

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