This is a great explaination of FPGA resource usage … need to work this into the questions

<https://forums.xilinx.com/t5/Implementation/Vivado-utilization-report/td-p/317517>

Can not go to far trying to throw trivial verilog code at vivado. It will throw random resource utilization at you. It doesn’t try to use a single CLB, it randomly does what it feels like. Our goal is to write verilog code and predict its behavior.

<https://forums.xilinx.com/t5/Synthesis/Question-about-LUT-usage-in-a-very-very-simple-combinatorial/td-p/221143>