RESET

RESET SWITCH

100Ω

7414

Z80 CPU

26 RESET

$\overline{RD}$ 21
$\overline{WR}$ 22
$\overline{MREQ}$ 19
$\overline{M1}$ 27

Jumper used to tie /INT high if no interrupt circuit is implemented.

16 $\overline{INT}$

1nF

47K

10K

INTER-RUPT

A15 5
A14 4
A13 3
A12 2
A11 1
A10 40
A9 39
A8 38
A7 37
A6 36
A5 35
A4 34
A3 33
A2 32
A1 31
A0 30

Address bus

POWER LED

280Ω

10K

24 $\overline{WAIT}$

+

10K

17 $\overline{NMI}$

74138

10K

G1 6

G2A 4
G2B 5

20 $\overline{IORQ}$

I/O Device Select

$\overline{DS7}$ 7 Y7
$\overline{DS6}$ 9 Y6
$\overline{DS5}$ 10 Y5
$\overline{DS4}$ 11 Y4
$\overline{DS3}$ 12 Y3
$\overline{DS2}$ 13 Y2
$\overline{DS1}$ 14 Y1
$\overline{DS0}$ 15 Y0

CLK

6 CLK

Oscillator 10 Mhz

25 $\overline{BUSRQ}$
28 $\overline{BUSAK}$

N/C 23 $\overline{RFSH}$
N/C 18 $\overline{HALT}$

D7 13
D6 10
D5 9
D4 7
D3 8
D2 12
D1 15
D0 14

Data bus

A 1
B 2
C 3

Cosam 3Z: CPU and Address Decoding	
Steve Maddsion	02/04/2007

SRAM
62LV1027

21	DQ7
20	DQ6
19	DQ5
18	DQ4
17	DQ3
15	DQ2
14	DQ1
13	DQ0

31	A15
3	A14
28	A13
4	A12
25	A11
23	A10
26	A9
27	A8
5	A7
6	A6
7	A5
8	A4
9	A3
10	A2
11	A1
12	A0

CS2   30   10K

1   N/C

A16   2

OE̅   24
WE̅   29
CS̅1̅   22

FLASH
28F2000TPC

21	DQ7
20	DQ6
19	DQ5
18	DQ4
17	DQ3
15	DQ2
14	DQ1
13	DQ0

28	A13
4	A12
25	A11
23	A10
26	A9
27	A8
5	A7
6	A6
7	A5
8	A4
9	A3
10	A2
11	A1
12	A0

R̅P̅   30   10K

W̅E̅   31   10K

VPP   1   N/C

A14   29
A15   3
A16   2

OE̅   24

CE̅   22

Z80 Bus

D7
D6
D5
D4
D3
D2
D1
D0

A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0

M̅R̅E̅Q̅

W̅R̅

R̅D̅

| Cosam 3Z: Memory and memory decoding | |
| Steve Maddsion | 03/04/2007 |

UART
16C550

D7	8	DQ7		
D6	7	DQ6		
D5	6	DQ5		
D4	5	DQ4		
D3	4	DQ3		
D2	3	DQ2		
D1	2	DQ1		
D0	1	DQ0		

CS0   12   10K

CS1   13   10K

X2	17	N/C
DDIS	23	N/C
$\overline{TXRDY}$	24	N/C
$\overline{RXRDY}$	29	N/C
$\overline{OUT2}$	31	N/C
$\overline{RTS}$	32	N/C
$\overline{OUT1}$	34	N/C
$\overline{CTS}$	36	N/C
$\overline{DCD}$	38	N/C
$\overline{RI}$	39	N/C

$\overline{DS1}$	14	$\overline{CS2}$
RESET	35	RES
$\overline{WR}$	18	$\overline{WR}$
$\overline{RD}$	21	$\overline{RD}$
A2	26	A2
A1	27	A1
A0	28	A0

$\overline{DTR}$	33	Ain
$\overline{DSR}$	37	Bout
TX	11	Cin
RX	10	Dout

INT   30   IRQ1

RCLK   9
BOUT   15

RD   22
WR   19
$\overline{AS}$ 25

CLK   16   X1

Oscillator
1.8432 Mhz

1µF   1µF

VCC
16

2   C++   MAX-232   C--   6   1µF

C+   1   1µF
C-   3

C+   4   1µF
C-   5

Bin   13   DSR
Din   8   RX
Cout   7   TX
Aout   14   DTR

RS-232
DB9 (male)

DSR 6
RX 2
7
TX 3
8
DTR 4
9
GND 5

Can be left
N/C if no
interrupt
circuit is
present.

Cosam 3Z: Serial Interface	
Steve Maddsion	09/04/2007

Cosam 3Z: IDE Interface

Steve Maddsion   31/03/2007

Cosam 3Z: Front Panel Address/Data Logic

Steve Maddsion 04/02/2008

Display

D0 D1 D2 D3 D4 D5 D6 D7

1K 150Ω (×8)

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

1K 150Ω (×16)

$\overline{DS1}$

150Ω

1K

Serial

	Cosam 3Z: Blinkenlights	
Steve Maddsion		25/01/2008

Address
Bus

1	A0
3	A1
5	A2
7	A3
9	A4
11	A5
13	A6
15	A7
17	A8
19	A9
21	A10
23	A11
25	A12
27	A13
29	A14
31	A15

$\overline{DS0}$ — 2 — RTC
$\overline{DS1}$ — 4 — UART
$\overline{DS2}$ — 6 — IDE
$\overline{DS3}$ — 8
$\overline{DS4}$ — 10
$\overline{DS5}$ — 12
$\overline{DS6}$ — 14
$\overline{DS7}$ — 16

I/O device
selection

IRQ0 — 18 — Timer
IRQ1 — 20 — UART
IRQ2 — 22 — IDE
IRQ3 — 24
IRQ4 — 26
IRQ5 — 28
IRQ6 — 30
IRQ7 — 32

Interrupt request
from I/O devices

| 33 | RESET |

$\overline{RESET}$ — 34 — Control Bus

Control
Bus

35	$\overline{INT}$
37	$\overline{M1}$
39	$\overline{BUSRQ}$
41	$\overline{BUSACK}$
43	$\overline{MREQ}$
45	$\overline{IORQ}$
47	$\overline{WR}$
49	$\overline{RD}$

D7 — 36
D6 — 38
D5 — 40
D4 — 42
D3 — 44
D2 — 46
D1 — 48
D0 — 50

Data
Bus

50-pin DIL header

Cosam 3Z: Expansion Bus Connector	
Steve Maddsion	04/02/2008