Arbitrary Delay for FIFO P3F

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Since we can clock the read clock (`RCLK`) and write clock (`WCLK`) for the FIFO independently, we can make the delay be an arbitrary function of state if

$$f_{\text{WCLK}} = k\dot{\tau} + f_{\text{RCLK}}$$

This may be achieved with the circuit of Fig. 1.

I have already ordered some prototype parts that could be used to create this circuit in hardware. They should be in the cardboard box of parts and stuff that I left in the lab.

- `TL082` JFET-input opamps (on breakout boards).
- A VCO (voltage-controlled oscillator) part by TI.
- A 4 MHz crystal oscillator.
- A binary ripple-counter part (CD-series).
- Some MUXes (maybe on breakout boards).

We just need to use opamps to differentiate $\tau(y)$ and then suitably offset and scale that signal so that when $\dot{\tau} = 0\,\text{s}\,\text{s}^{-1}$, the input voltage to the VCO will cause the VCO to generate a clock at f_{RCLK}. Alternatively, make the differentiator inverting and switch the role of `WCLK` and RCLK.

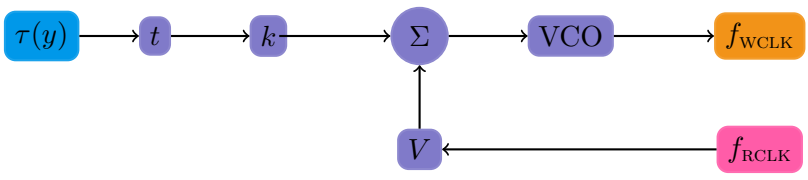

Figure 1: Arbitrary delay circuit block diagram.