

LMx93-N, LM2903-N Low-Power, Low-Offset Voltage, Dual Comparators

1 Features

- Wide Supply
 - Voltage Range: 2.0 V to 36 V
 - Single or Dual Supplies: ± 1.0 V to ± 18 V
- Very Low Supply Current Drain (0.4 mA) — Independent of Supply Voltage
- Low Input Biasing Current: 25 nA
- Low Input Offset Current: ± 5 nA
- Maximum Offset voltage: ± 3 mV
- Input Common-Mode Voltage Range Includes Ground
- Differential Input Voltage Range Equal to the Power Supply Voltage
- Low Output Saturation Voltage: 250 mV at 4 mA
- Output Voltage Compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Available in the 8-Bump (12 mil) DSBGA Package
- See AN-1112 ([SNVA009](#)) for DSBGA Considerations
- Advantages
 - High Precision Comparators
 - Reduced V_{OS} Drift Over Temperature
 - Eliminates Need for Dual Supplies
 - Allows Sensing Near Ground
 - Compatible with All Forms of Logic
 - Power Drain Suitable for Battery Operation

2 Applications

- Battery Powered Applications
- Industrial Applications

3 Description

The LM193-N series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193-N series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM19-N series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

The LM393 and LM2903 parts are available in TI's innovative thin DSBGA package with 8 (12 mil) large bumps.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM193-N	TO-99 (8)	9.08 mm x 9.08 mm
LM293-N		
LM393-N	SOIC (8)	4.90 mm x 3.91 mm
	DSBGA (8)	1.54 mm x 1.54 mm
LM2903-N	SOIC (8)	4.90 mm x 3.91 mm
	DSBGA (8)	1.54 mm x 1.54 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

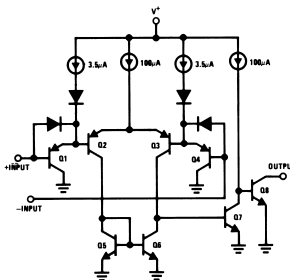


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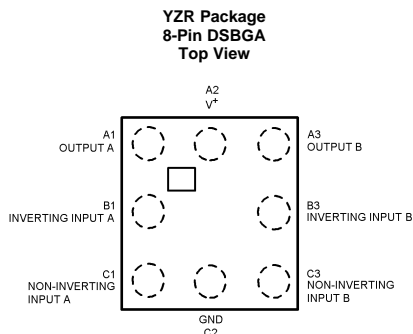
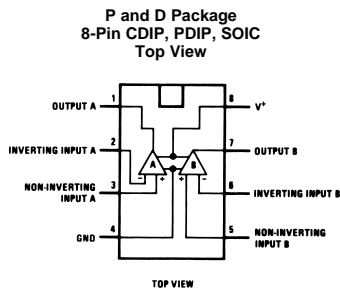
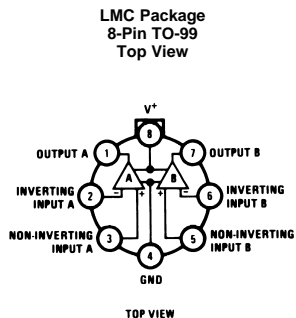
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (December 2014) to Revision G	Page
Added DSBGA packages inadvertently omitted from Device Info table during format conversion	1
Changes from Revision E (March 2013) to Revision F	Page
Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
Changes from Revision D (March 2013) to Revision E	Page
Changed layout of National Data Sheet to TI format	1

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	PDIP/SOIC/TO-99	DSBGA		
OUTA	1	A1	O	Output, Channel A
-INA	2	B1	I	Inverting Input, Channel A
+INA	3	C1	I	Noninverting Input, Channel A
GND	4	C2	P	Ground
+INB	5	C3	I	Noninverting Input, Channel B
-INB	6	B3	I	Inverting Input, Channel B
OUTB	7	A3	O	Output, Channel B
V+	8	A2	P	Positive power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

			MIN	MAX	UNIT
Differential Input Voltage ⁽⁴⁾				36	V
Input Voltage			-0.3	36	V
Input Current (V _{IN} <-0.3 V) ⁽⁵⁾				50	mA
Power Dissipation ⁽⁶⁾	PDIP			780	mW
	TO-99			660	mW
	SOIC			510	mW
	DSBGA			568	mW
Output Short-Circuit to Ground ⁽⁷⁾				Continu ous	
Lead Temperature (Soldering, 10 seconds)				260	°C
Soldering Information	PDIP Package Soldering (10 seconds)			260	°C
	SOIC Package	Vapor Phase (60 seconds)		215	°C
		Infrared (15 seconds)		220	°C
Storage temperature, T _{stg}			-65	150	°C

- Absolute Maximum Ratings* indicate limits beyond which damage may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.
- Refer to RETS193AX for LM193AH military specifications and to RETS193X for LM193H military specifications.
- If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
- This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.
- For operating at high temperatures, the LM393 and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.
- Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+ .

6.2 ESD Ratings

	VALUE	UNIT
V_{ESD} Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1300	V

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (V^+) - Single Supply	2.0		36	V
Supply Voltage (V^+) - Dual Supply	±1.0		±18	V
Operating Input Voltage on (V_{IN} pin)	0	(V^+)	-1.5V	V
Operating junction temperature, T_J : LM193/LM193A	-55		125	°C
Operating junction temperature, T_J : LM2903	-40		85	°C
Operating junction temperature, T_J : LM293	-25		85	°C
Operating junction temperature, T_J : LM393	0		70	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LMx93	UNIT
	TO-99	
	8 PINS	
R _{θJA} Junction-to-ambient thermal resistance	170	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics: LM193A V⁺ = 5 V, T_A = 25°C

Unless otherwise stated.

PARAMETER	TEST CONDITIONS	LM193A			UNIT
		MIN	TYP	MAX	
Input Offset Voltage	See ⁽¹⁾ .	1.0	2.0		mV
Input Bias Current	I _{IN} (+) or I _{IN} (-) with Output In Linear Range, V _{CM} = 0 V ⁽²⁾	25	100		nA
Input Offset Current	I _{IN} (+)–I _{IN} (-) V _{CM} = 0 V	3.0	25		nA
Input Common Mode Voltage Range	V ₊ = 30 V ⁽³⁾	0	V ⁺ –1.5		V
Supply Current	R _L =∞ V ⁺ =5 V	0.4	1		mA
	V ⁺ =36 V	1	2.5		mA
Voltage Gain	R _L ≥15 kΩ, V ⁺ =15 V V _O = 1 V to 11 V	50	200		V/mV
Large Signal Response Time	V _{IN} =TTL Logic Swing, V _{REF} =1.4 V V _{RL} =5V, R _L =5.1 kΩ	300			ns
Response Time	V _{RL} =5V, R _L =5.1 kΩ ⁽⁴⁾	1.3			μs
Output Sink Current	V _{IN} (-) = 1V, V _{IN} (+) = 0, V _O ≤ 1.5 V	6.0	16		mA
Saturation Voltage	V _{IN} (-) = 1V, V _{IN} (+) = 0, I _{SINK} ≤ 4 mA	250	400		mV
Output Leakage Current	V _{IN} (-) = 0, V _{IN} (+) = 1V, V _O = 5 V	0.1			nA

- (1) At output switch point, V_O=1.4V, R_S= 0 Ω with V⁺ from 5V to 30V; and over the full input common-mode range (0V to V⁺–1.5V), at 25°C.
- (2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- (3) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V⁺–1.5 V at 25°C, but either or both inputs can go to 36 V without damage, independent of the magnitude of V⁺.
- (4) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see [LMx93 and LM193A Typical Characteristics](#).

6.6 Electrical Characteristics: LM193A (V₊ = 5 V)⁽¹⁾

PARAMETER	TEST CONDITIONS	LM193A			UNIT
		MIN	TYP	MAX	
Input Offset Voltage	See ⁽²⁾		4.0		mV
Input Offset Current	I _{IN} (+)–I _{IN} (-), V _{CM} =0 V		100		nA
Input Bias Current	I _{IN} (+) or I _{IN} (-) with Output in Linear Range, V _{CM} =0 V ⁽³⁾		300		nA
Input Common Mode Voltage Range	V ⁺ =30 V ⁽⁴⁾	0	V ⁺ –2.0		V
Saturation Voltage	V _{IN} (-) = 1V, V _{IN} (+) = 0, I _{SINK} ≤ 4 mA		700		mV
Output Leakage Current	V _{IN} (-) = 0, V _{IN} (+) = 1V, V _O = 30 V		1.0		μA
Differential Input Voltage	Keep All V _{IN} ≥ 0 V (or V ⁺ , if Used), ⁽⁵⁾		36		V

- (1) These specifications are limited to –55°C≤T_A≤+125°C, for the LM193/LM193A. With the LM293 all temperature specifications are limited to –25°C≤T_A≤+85°C and the LM393 temperature specifications are limited to 0°C≤T_A≤+70°C. The LM2903 is limited to –40°C≤T_A≤+85°C.
- (2) At output switch point, V_O=1.4V, R_S= 0 Ω with V⁺ from 5V to 30V; and over the full input common-mode range (0V to V⁺–1.5V), at 25°C.
- (3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- (4) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V⁺–1.5 V at 25°C, but either or both inputs can go to 36 V without damage, independent of the magnitude of V⁺.
- (5) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than –0.3V (or 0.3V below the magnitude of the negative power supply, if used).

6.7 Electrical Characteristics: LMx93 and LM2903 V⁺ = 5 V, T_A = 25°C

Unless otherwise stated.

PARAMETER	TEST CONDITIONS	LM193-N			LM293-N, LM393-N			LM2903-N			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MI N	TYP	MAX	
Input Offset Voltage	See ⁽¹⁾	1.0	5.0		1.0	5.0		2.0	7.0		mV
Input Bias Current	I _{IN} (+) or I _{IN} (-) with Output In Linear Range, V _{CM} = 0 V ⁽²⁾	25	100		25	250		25	250		nA
Input Offset Current	I _{IN} (+)–I _{IN} (-) V _{CM} = 0 V	3.0	25		5.0	50		5.0	50		nA
Input Common Mode Voltage Range	V ₊ = 30 V ⁽³⁾	0	V ₊ –1.5		0	V ₊ –1.5		0	V ₊ –1.5		V
Supply Current	R _L =∞ V ⁺ =5 V	0.4	1		0.4	1		0.4	1.0		mA
	V ⁺ =36 V	1	2.5		1	2.5		1	2.5		mA
Voltage Gain	R _L ≥15 kΩ, V ⁺ =15 V V _O = 1 V to 11 V	50	200		50	200		25	100		V/mV
Large Signal Response Time	V _{IN} =TTL Logic Swing, V _{REF} =1.4 V V _{RL} =5 V, R _L =5.1 kΩ	300			300			300			ns
Response Time	V _{RL} =5 V, R _L =5.1 kΩ ⁽⁴⁾	1.3			1.3			1.5			μs
Output Sink Current	V _{IN} (-) = 1 V, V _{IN} (+) = 0, V _O ≤ 1.5 V	6.0	16		6.0	16		6.0	16		mA
Saturation Voltage	V _{IN} (-) = 1 V, V _{IN} (+) = 0, I _{SINK} ≤ 4 mA	250	400		250	400		250	400		mV
Output Leakage Current	V _{IN} (-) = 0, V _{IN} (+) = 1V, V _O = 5 V	0.1			0.1			0.1			nA

- (1) At output switch point, V_O=1.4V, R_S= 0 Ω with V⁺ from 5V to 30V; and over the full input common-mode range (0V to V⁺–1.5V), at 25°C.
- (2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- (3) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V⁺–1.5 V at 25°C, but either or both inputs can go to 36 V without damage, independent of the magnitude of V⁺.
- (4) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see [LMx93 and LM193A Typical Characteristics](#).

6.8 Electrical Characteristics: LMx93 and LM2903 (V₊ = 5 V)⁽¹⁾

PARAMETER	TEST CONDITIONS	LM193-N			LM293-N, LM393-N			LM290-N			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	See ⁽²⁾			9			9		9	15	mV
Input Offset Current	I _{IN(+)} – I _{IN(–)} , V _{CM} = 0 V			100			150		50	200	nA
Input Bias Current	I _{IN(+)} or I _{IN(–)} with Output in Linear Range, V _{CM} = 0 V ⁽³⁾			300			400		200	500	nA
Input Common Mode Voltage Range	V ⁺ = 30 V ⁽⁴⁾	0		V ⁺ – 2.0	0		V ⁺ – 2.0	0		V ⁺ – 2.0	V
Saturation Voltage	V _{IN(–)} = 1 V, V _{IN(+)} = 0, I _{SINK} ≤ 4 mA			700			700		400	700	mV
Output Leakage Current	V _{IN(–)} = 0, V _{IN(+)} = 1 V, V _O = 30 V			1.0			1.0		1.0		μA
Differential Input Voltage	Keep All V _{IN} 's ≥ 0 V (or V [–] , if Used), ⁽⁵⁾			36			36		36		V

- (1) These specifications are limited to –55°C ≤ T_A ≤ +125°C, for the LM193/LM193A. With the LM293 all temperature specifications are limited to –25°C ≤ T_A ≤ +85°C and the LM393 temperature specifications are limited to 0°C ≤ T_A ≤ +70°C. The LM2903 is limited to –40°C ≤ T_A ≤ +85°C.
- (2) At output switch point, V_O = 1.4 V, R_S = 0 Ω with V⁺ from 5 V to 30 V; and over the full input common-mode range (0 V to V⁺ – 1.5 V), at 25°C.
- (3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- (4) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V⁺ – 1.5 V at 25°C, but either or both inputs can go to 36 V without damage, independent of the magnitude of V⁺.
- (5) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than –0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

6.9 Typical Characteristics: LMx93 and LM193A

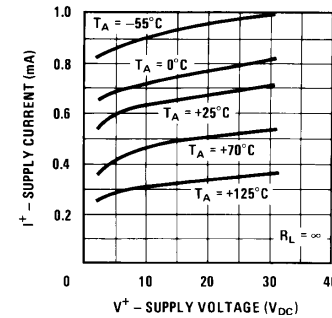


Figure 1. Supply Current

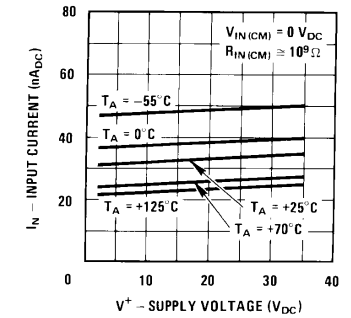


Figure 2. Input Current

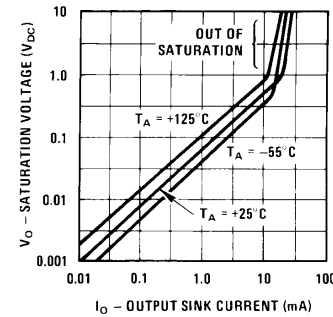


Figure 3. Output Saturation Voltage

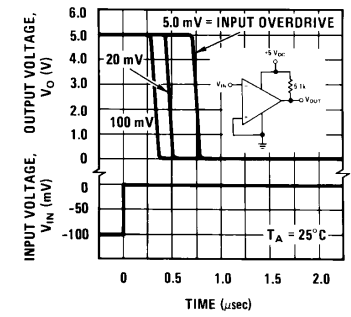


Figure 4. Response Time for Various Input Overdrives—Negative Transition

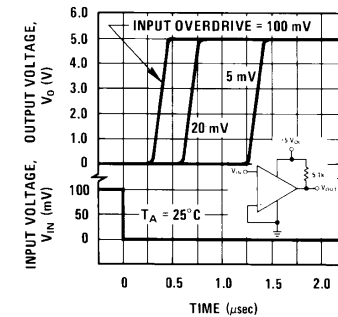


Figure 5. Response Time for Various Input Overdrives—Positive Transition

6.10 Typical Characteristics: LM2903

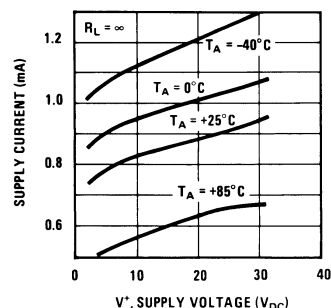


Figure 6. Supply Current

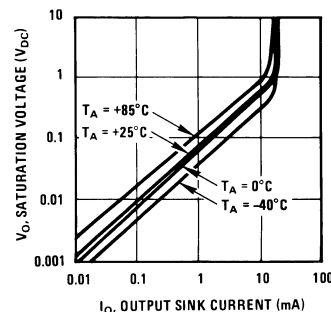


Figure 8. Output Saturation Voltage

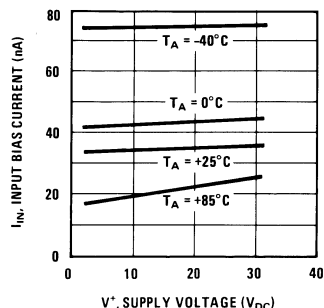


Figure 7. Input Current

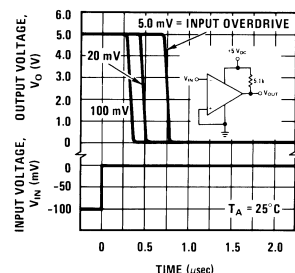


Figure 9. Response Time for Various Input Overdrives—Negative Transition

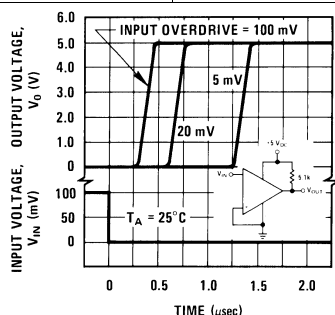


Figure 10. Response Time for Various Input Overdrives—Positive Transition

7 Detailed Description

7.1 Overview

The LM139 provides two independently functioning, high-precision, low V_{OS} drift, low input bias current comparators in a single package. The low power consumption of 0.4 mA at 5 V and the 2.0 V supply operation makes the LM139 suitable for battery powered applications.

7.2 Functional Block Diagram

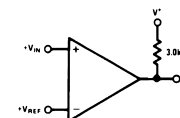


Figure 11. Basic Comparator

7.3 Feature Description

The input bias current of 25 nA enables the LM193 to use even very high impedance nodes as inputs. The differential voltage input range equals the supply voltage range.

The LM193 can be operated with a single supply, where V_+ can be from 2.0 V to 36 V, or in a dual supply voltage configuration, where GND pin is used as a V_- supply. The supply current draws only 0.4 mA for both comparators.

The output of each comparator in the LM193 is the open collector of a grounded-emitter NPN output transistor which can typically draw up to 16 mA.

7.4 Device Functional Modes

A basic comparator circuit is used for converting analog signals to a digital output. The output is HIGH when the voltage on the non-inverting (+IN) input is greater than the inverting (-IN) input. The output is LOW when the voltage on the non-inverting (+IN) input is less than the inverting (-IN) input. The inverting input (-IN) is also commonly referred to as the "reference" or "VREF" input. All pins of any unused comparators should be tied to the negative supply.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\text{ k}\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All input pins of any unused comparators should be tied to the negative supply.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC} .

The differential input voltage may be larger than V^+ without damaging the device [Typical Applications](#). Protection should be provided to prevent the input voltages from going negative more than $-0.3\text{ V}_{\text{DC}}$ (at 25°C). An input clamp diode can be used as shown in [Typical Applications](#).

The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pullup resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pullup resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately $60\text{ }\Omega\text{ }r_{\text{SAT}}$ of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

8.2 Typical Applications

8.2.1 Basic Comparator

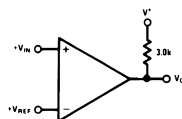


Figure 12. Basic Comparator

8.2.1.1 Design Requirements

The basic usage of a comparator is to indicate when a specific analog signal has exceeded some predefined threshold. In this application, the negative input (IN-) is tied to a reference voltage, and the positive input (IN+) is connected to the input signal. The output is pulled up with a resistor to the logic supply voltage, V^+ with a pullup resistor.

For an example application, the supply voltage is 5V. The input signal varies between 1 V and 3 V, and we want to know when the input exceeds $2.5\text{ V} \pm 1\%$. The supply current draw should not exceed 1 mA.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

First, we determine the biasing for the 2.5-V reference. With the 5-V supply voltage, we would use a voltage divider consisting of one resistor from the supply to IN- and an second resistor from IN-. The 25 nA of input current bias should be $< 1\%$ of the bias current for Vref. With a $100\text{-k}\Omega$ resistor from IN- to V^+ and an additional $100\text{-k}\Omega$ resistor from IN- to ground, there would be 25 μA of current through the two resistors. The $3\text{-k}\Omega$ pullup shown will need $5\text{ V}/3\text{ k}\Omega \rightarrow 1.67\text{ mA}$, which exceeds our current budget.

With the $400\text{-}\mu\text{A}$ supply current and 25 μA of VREF bias current, there is 575 μA remaining for output pullup resistor; with 5-V supply, we need a pullup larger than $8.7\text{ k}\Omega$. A $10\text{-k}\Omega$ pullup is a value that is commonly available and can be used here.

8.2.1.3 Application Curve

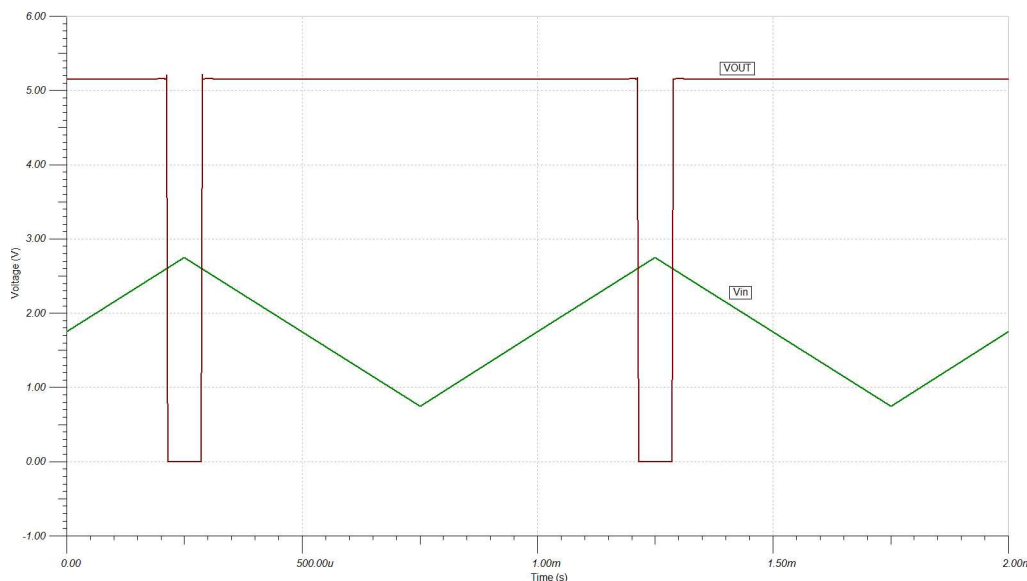
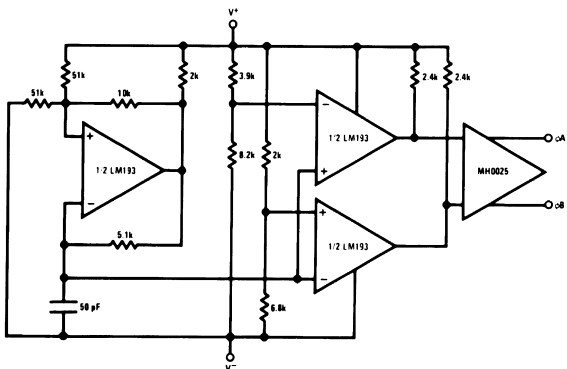


Figure 13. Basic Comparator Response

Typical Applications (continued)

8.2.2 System Examples

8.2.2.1 Split-Supply Application



($V_+ = -15 V_{DC}$ and $V_- = -15 V_{DC}$)

Figure 14. MOS Clock Driver

8.2.2.2 $V_+ = 5.0 V_{DC}$ Application Circuits

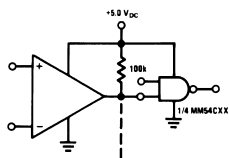


Figure 15. Driving CMOS

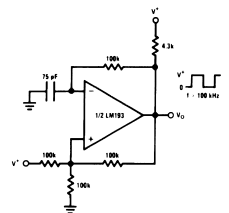


Figure 17. Squarewave Oscillator

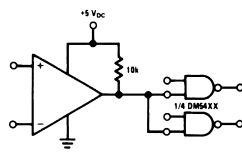


Figure 16. Driving TTL

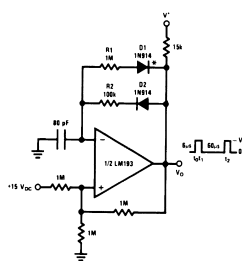


Figure 18. Pulse Generator

* For large ratios of R_1/R_2 ,
D1 can be omitted.

Typical Applications (continued)

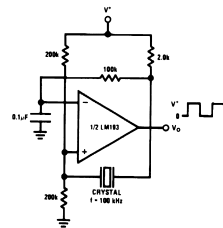


Figure 19. Crystal Controlled Oscillator

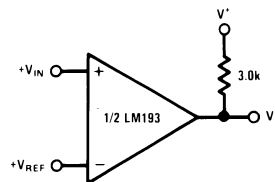


Figure 21. Basic Comparator

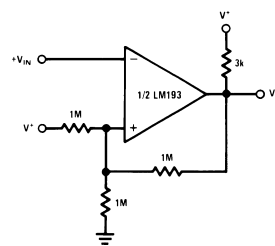


Figure 23. Inverting Comparator With Hysteresis

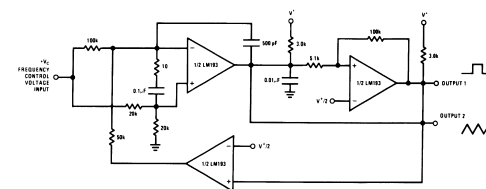


Figure 20. Two-Decade High Frequency VCO

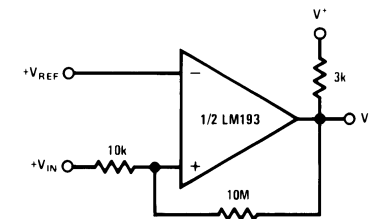
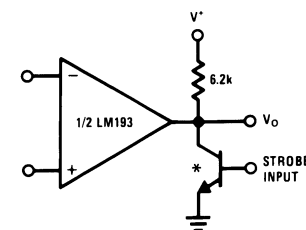


Figure 22. Non-Inverting Comparator With Hysteresis



* OR LOGIC GATE
WITHOUT PULL-UP RESISTOR

Figure 24. Output Strobing

Typical Applications (continued)

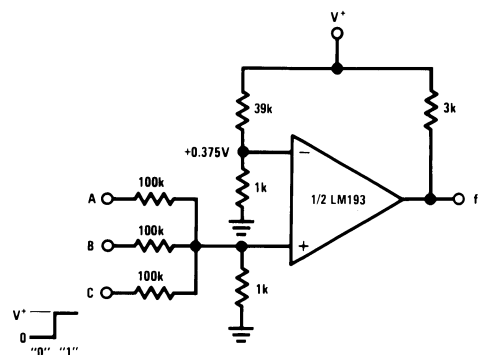


Figure 25. And Gate

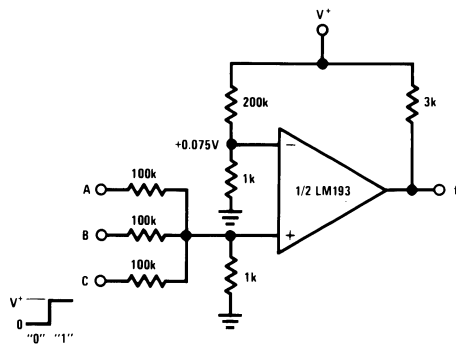


Figure 26. Or Gate

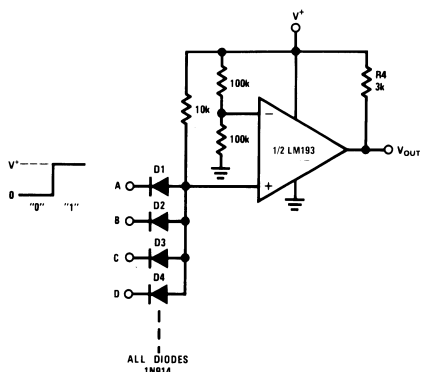


Figure 27. Large Fan-In and Gate

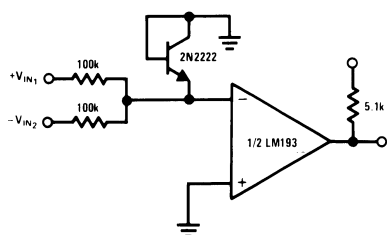


Figure 29. Comparing Input Voltages of Opposite Polarity

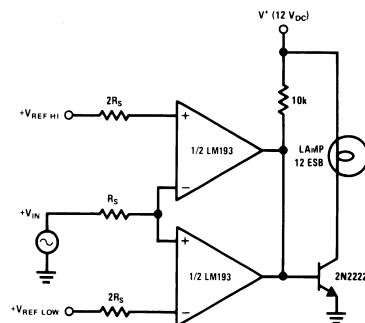


Figure 28. Limit Comparator

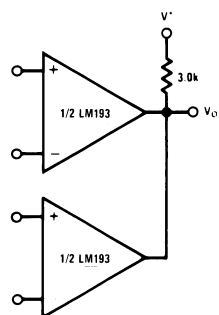


Figure 30. Oring the Outputs

Typical Applications (continued)

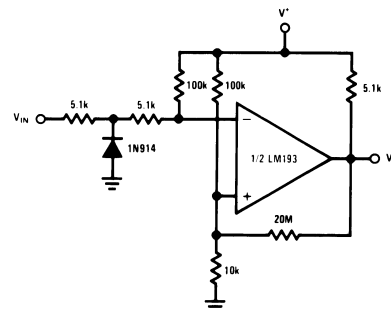


Figure 31. Zero Crossing Detector (Single Power Supply)

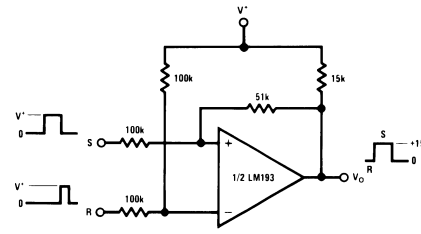


Figure 33. Bi-Stable Multivibrator

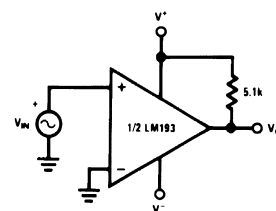


Figure 35. Zero Crossing Detector

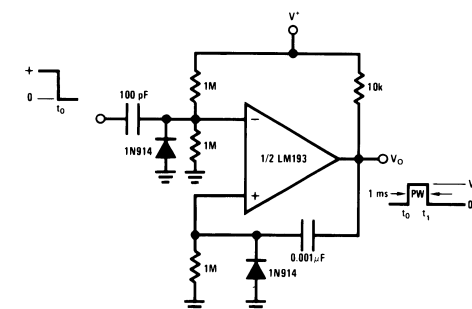


Figure 32. One-Shot Multivibrator

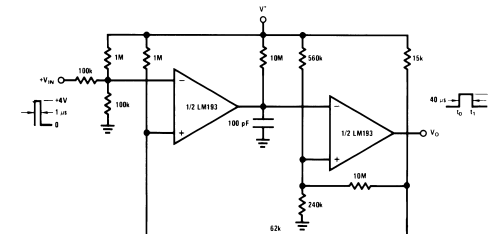


Figure 34. One-Shot Multivibrator With Input Lock Out

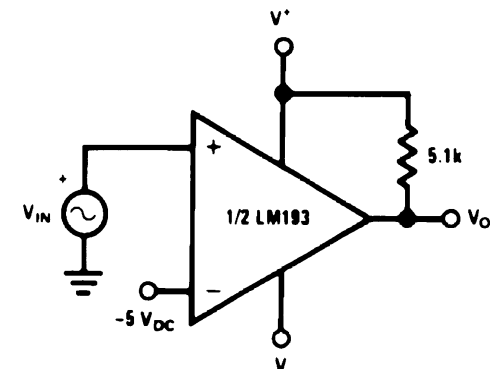


Figure 36. Comparator With a Negative Reference

Typical Applications (continued)

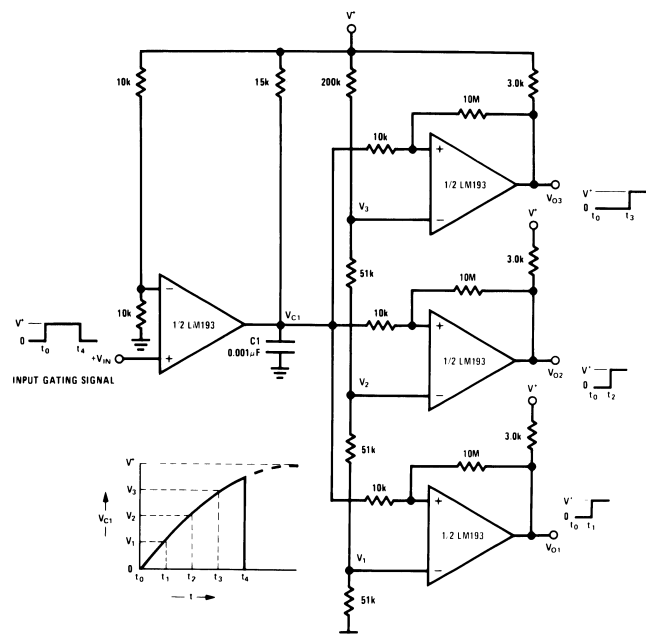


Figure 37. Time Delay Generator

9 Power Supply Recommendations

Even in low frequency applications, the LM139-N can have internal transients which are extremely quick. For this reason, bypassing the power supply with 1.0 µF to ground will provide improved performance; the supply bypass capacitor should be placed as close as possible to the supply pin and have a solid connection to ground. The bypass capacitor should have a low ESR and also a SRF greater than 50MHz.

10 Layout

10.1 Layout Guidelines

Try to minimize parasitic impedances on the inputs to avoid oscillation. Any positive feedback used as hysteresis should place the feedback components as close as possible to the input pins. Care should be taken to ensure that the output pins do not couple to the inputs. This can occur through capacitive coupling if the traces are too close and lead to oscillations on the output. The optimum placement for the bypass capacitor is closest to the V+ and ground pins. Take care to minimize the loop area formed by the bypass capacitor connection between V+ and ground. The ground pin should be connected to the PCB ground plane at the pin of the device. The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

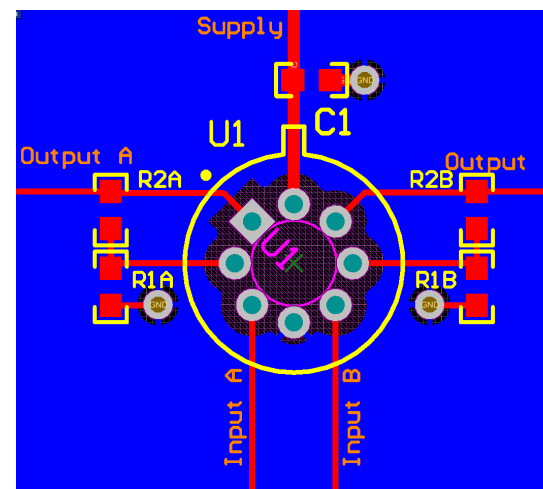


Figure 38. Layout Example