# A checklist for designing RF-sampling receivers

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The modern, advanced CMOS direct radio frequency (RF)-sampling data converter has been eagerly awaited by system design engineers for several major end-equipment manufacturers. This includes manufacturers of communications infrastructure, software-defined radios (SDRs), radar systems, or test and measurement products. Recently introduced data converters are delivering the high dynamic range comparable to high-performance intermediate frequency (IF)-sampling data converters. Additionally, these converters integrate on-chip digital filtering (DDC), which reduces the output data rate from 3-4 GSPS sampling rate to something more manageable similar to traditional IF-sampling data converters.

Two major factors are driving the quick adoption of these ultra-high-speed data converters. The ever increasing demand for wider bandwidth naturally requires faster sampling rates, while higher density and integration is accomplished by removing one down conversion stage from the receiver, for example. Modern SDRs or cellular base stations need to be able to cover multiple frequency bands simultaneously, for example, to support carrier aggregation across multiple licensed Long-Term Evolution (LTE) bands to enable faster data traffic. Rather than expending one radio-per-band system, designers want to shrink the product form factor and build a multiband- capable radio. The RF sampling data converter removes the intermediate frequency (IF) stage saving printed circuit board (PCB) area and power consumption, while its wide Nyquist zone enables sampling multiple bands simultaneously.
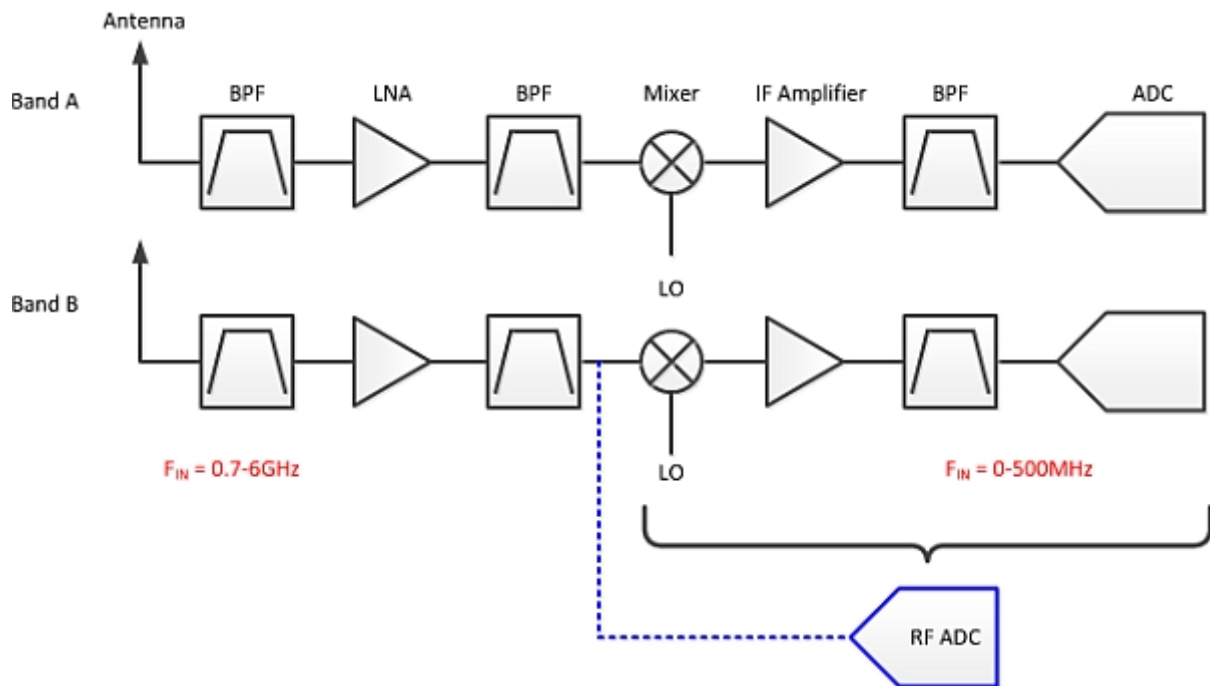
Figure 1: One RF-sampling analog-to-digital converter (ADC) can replace multiple IF-sampling signal chains.

System designers who are considering switching from IF- to RF-sampling need to solve four primary challenges on their checklist:

1. Receiver sensitivity
2. Radio performance in presence of in-band interferer
3. Filter requirements for out-of-band blocker
4. Performance of the sampling clock source

Depending on their application, some may be more critical than others.

Let us examine these challenges using two different types of analog-to-digital converters (ADCs) and compare the results. The first data converter is the ADS4249, a14-bit, 250 MSPS analog-to-digital converter (ADC) used for an IF-sampling system. The second is the ADC32RF45, a 14-bit, 3 GSPS ADC for a RF-sampling system.

Receiver sensitivity

One basic performance metric of the receiver is its *sensitivity*, which means what is the weakest signal power that it can successfully recover and process. Weak input signals cannot be demodulated if the noise of the receiver within the demodulated bandwidth is larger than the

received signal itself. The noise floor of the receiver typically is expressed as a noise figure (NF) in decibel (dB), or the difference to the absolute thermal noise normalized to 1 Hz bandwidth. The most common way to improve an ADC's noise figure is to add an amplifier before the ADC.
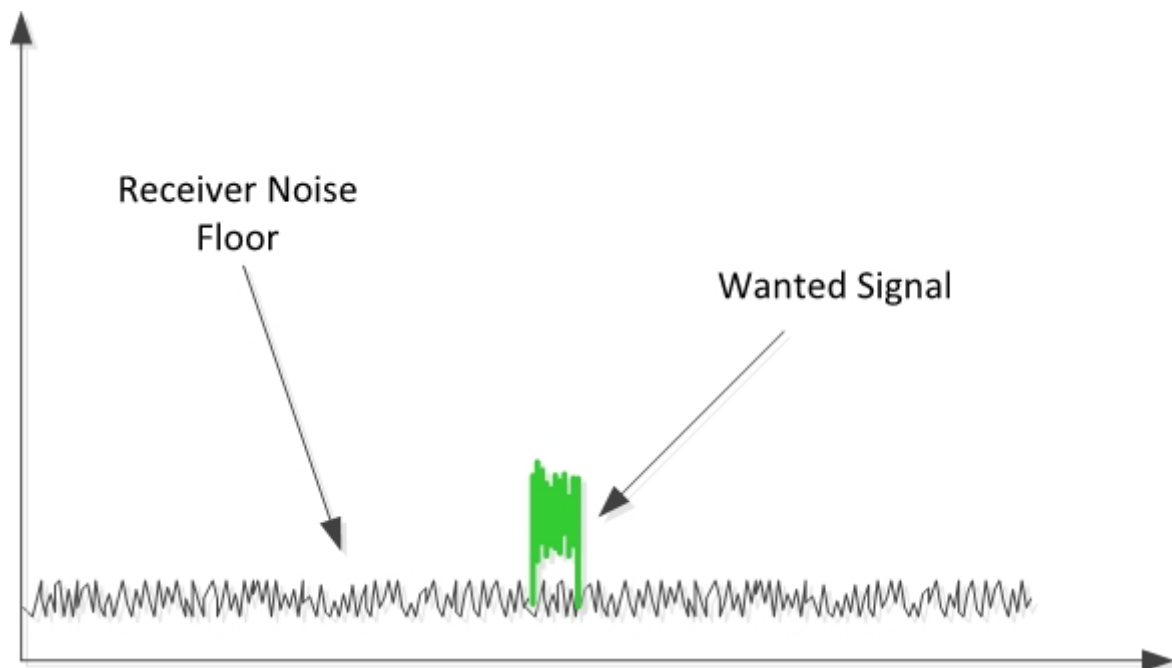
Figure 2: Small wanted signal in sensitivity case.

The noise figures of the IF- and RF-sampling converters can be calculated to:

Table 1: Noise figure comparison between IF- and RF-sampling data converters.

Parameter	IF sampling ADC	RF sampling ADC
Sampling rate (FS)	250 MSPS	3 GSPS
Input full-scale (V_{PP})	2 V_{PP}	1.35 V_{PP}
Thermal noise	72.8 dB	62 dB
Input impedance (Zin)	200 Ω (external)	50 Ω (internal)
Calculated noise figure	24.2 dB	26.8 dB

While the noise figures of both converters are close, the IF-sampling data converter has significant external gain from the mixer and IF digital variable gain amplifier (DVGA), which substantially reduces the impact of the ADC noise figure to the receiver sensitivity. Hence, the RF-sampling ADC requires additional front-end gain (an additional low-noise amplifier or LNA) to minimize its impact

on receiver sensitivity as well.

In-band blocking performance

Sometimes interferers manage to get within the front-end filter passband. The receiver in-band blocking performance is a measure of how well the receiver can demodulate weak signals in the presence of such an in-band interferer. The automatic gain control (AGC) of the receiver ensures that the interferer power level stays below the ADC input full scale to avoid saturation. However, the blocker harmonics generated inside the ADC during the sampling process can still fall on top of the weak wanted signals, reducing the receiver's ability to demodulate.

Since the input frequency is much lower, the IF-sampling data converter offers substantially better low-order harmonic (such as HD2,3) performance as shown in **Table 2**.

Table 2: Spurious-free dynamic range performance of both IF- and RF-sampling data converters.

Parameter	IF-sampling ADC F_{IN} = 170 MHz	RF-sampling ADC F_{IN} = 1.8 GHz
HD2, typ	80 dBc	63 dBc
HD3, typ	80 dBc	67 dBc
Non HD2, 3 typ	88 dBc	80-85 dBc

However, system designers are taking advantage of the high sampling rate of RF-sampling converters. Designers can either select the input frequency range (for example, military SDR operating in the L-Band), or the sampling clock frequency (such as communications infrastructure with fixed-RF frequency bands) in order to avoid low-order harmonics to fall in-band. The high-order distortion performance of modern RF-sampling converters is fairly comparable to that of high-performance IF-sampling converters. This method is also known as *frequency planning*.

The frequency planning concept is illustrated in **Figure 3**. A 60-MHz wide spectrum is centered at an IF of 180 MHz with a 250-Msps ADC. The harmonics of the in-band interferer cannot be avoided. In contrast, the same 60 MHz centered at 1.75 GHz sampled at 3 Gsps provides in-band spurious-free dynamic range (SFDR) that is free of low-order harmonics and interleaving spurs (**Figure 4**).
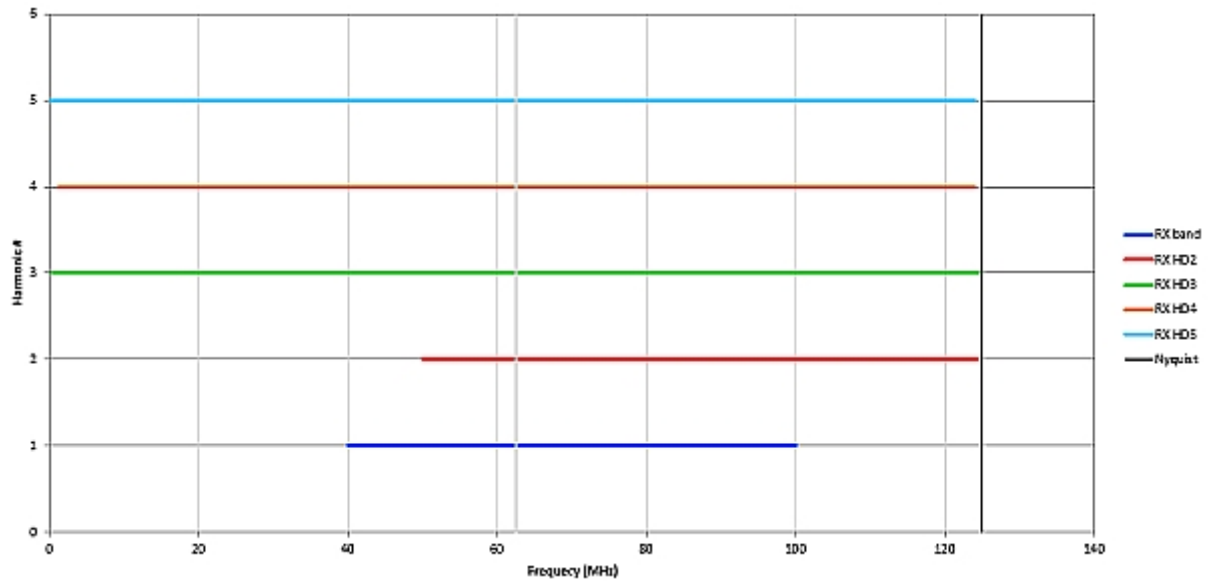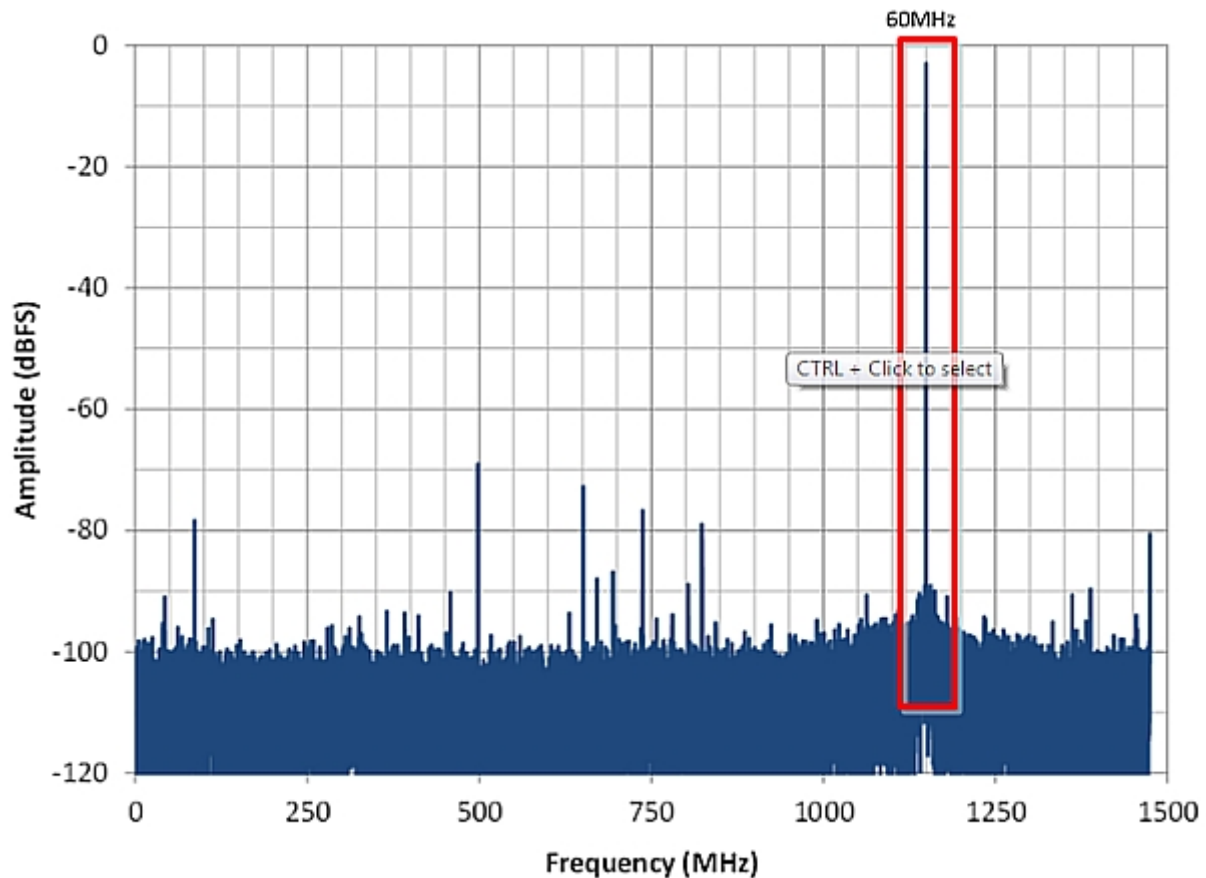
(a)
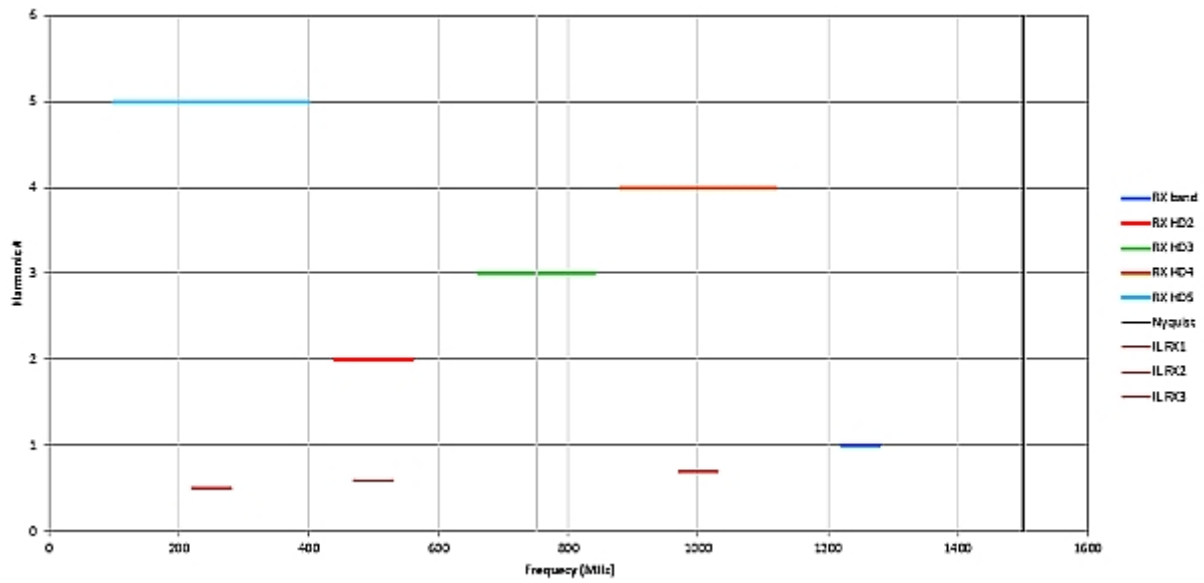
(b)

Figure 3: Frequency spectrum of 60 MHz bandwidth with IF sampling (Fs = 250 Msps centered at 180 MHz) (a); versus RF sampling (Fs = 3 Gsps centered at 1750 MHz) (b).

Figure 4: FFT plot of an ADC, Fs = 3 Gsps, F_{IN} = 1.75 GHz.

External blocker filter requirements

Independent of architecture, the ADC input must be protected from large, out-of-band interferers because that would either alias the in-band to exceed the ADC full scale and saturate the receiver, or generate harmonics that would overlap with a small, in-band wanted signal.

Intermediate frequency-sampling systems have a relatively small Nyquist zone, therefore, the alias bands and mixing images are fairly close by. Since it is difficult to design a RF filter with sharp rolloff, the filter attenuation is typically split between RF and IF bandpass filters.

The filter design for RF-sampling systems is a little bit more relaxed when frequency planning is applied. There are no mixer images or LO spurs to worry about but low-order harmonics, or interleaving spurs of out-of-band interferers, still need to be considered.

Sampling clocking performance requirement

The sampling clock for the RF ADC is equivalent to the local oscillator in a heterodyne receiver. Clock phase noise requirements are highly dependent on the application. Generally, it is better to specify the phase noise at application-specific offset frequencies, versus integrating the clock phase noise across the entire (rather large) Nyquist zone for a representative clock jitter number.

Furthermore, the clock is now a RF signal and faces additional challenges, such as increased amplitude attenuation with increased frequency. ADCs require clock amplitude to be as high as possible for lowest noise floor and tough skew management in multi-channel systems.

Similar to suitable RF- and IF-sampling ADCs, there are fewer high-quality, low-phase noise clocking solutions available for clock rates above 1 Gsps. Therefore, system designers may need to rely on using low-phase noise Los, such as the [LMX2582](#), as the RF ADC clock source.

Summary

The availability of high dynamic range RF-sampling converters, such as the ADC32RF45, enables direct RF-sampling receiver implementations for a wide range of applications. When transitioning from a traditional heterodyne design to a direct RF conversion, the designer should not have to compromise on radio performance. However, attention still needs to be given to the four major design challenges discussed in this article.

References

- Download these datasheets: [ADC12J4000](#), [ADC32RF45](#), [LMX2582](#)
- Neu, Tommy. [Direct RF conversion: From vision to reality](#), Texas Instruments White Paper, May 2015
- Keller, Robert. [Signal chain basics #45: Is high-speed ADC clock jitter being over-specified for communication systems?](#), Planet Analog, September 2, 2010