TPS22810, 2.7-18-V, 2-A, 79-mΩ On-Resistance Load Switch with Thermal Protection

1 Features

- Integrated Single Channel Load Switch
- Ambient Operating Temperature: –40°C to +105°C
  - 2-A Maximum Continuous Current [1]
- Input Voltage Range: 2.7 V to 18 V
- Absolute Maximum Input Voltage: 20 V
- On-Resistance (R_{ON})
  - R_{ON} = 79 mΩ (typical) at V_{IN} = 12 V
- Quiescent Current
  - 62 µA (typical) at V_{IN} = 12 V
- Shutdown Current
  - 500 nA (typical) at V_{IN} = 12 V
- Thermal Shutdown
- Undervoltage Lock-Out (UVLO)
- Adjustable Quick Output Discharge (QOD)
- Configurable Rise Time With CT Pin
- SOT23-6 Package
  - 2.9-mm × 2.8-mm, 0.95-mm Pitch, 1.45-mm Height (DBV)
- WSON Package
  - 2-mm × 2-mm, 0.65-mm Pitch, 0.75-mm Height (DRV)
- ESD Performance Tested per JESD 22
  - ±2-kV HBM and ±1-kV CDM

(1) Thermal performance must be considered

2 Applications

- HD TV
- Industrial Systems
- Set Top Box
- Surveillance systems

3 Description

The TPS22810 is a single channel load switch with configurable rise time and with an integrated quick output discharge (QOD). In addition, the device features thermal shutdown to protect the device against high junction temperature. Because of this, safe operating area of the device is inherently ensured. The device contains an N-channel MOSFET that can operate over an input voltage range of 2.7 V to 18 V and can support a maximum continuous current of 2 A. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals.

The configurable rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. Undervoltage lock-out is used to turn off the device if the VIN voltage drops below a threshold value, ensuring that the downstream circuitry is not damaged by being supplied by a voltage lower than intended. The configurable QOD pin controls the fall time of the device to allow design flexibility for power down.

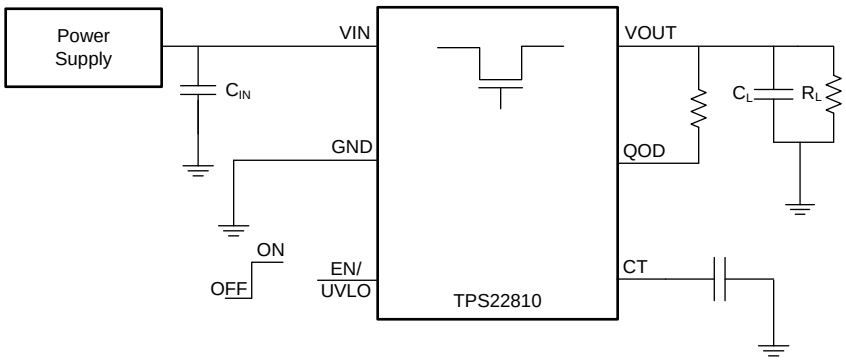
The TPS22810 is available in a leaded, SOT-23 package (DBV) which allows to visually inspect solder joints, as well as a SON package (DRV). The device is characterized for operation over the free-air temperature range of –40˚C to +105˚C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22810	SOT-23 (6)	2.90 mm × 2.80 mm
	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

Changes from Original (December 2016) to Revision A **Page**

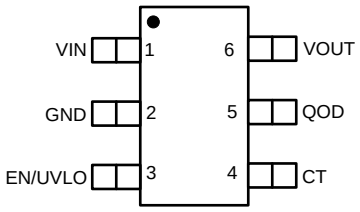
- Deleted I_{MAX} and I_{PLS} from the *Absolute Maximum Ratings* table ... 4
- Changed the Quiescent current MAX value From: 70 µA To: 80 µA in the *Electrical Characteristics* table ... 5
- Changed the Quiescent current MAX value for V_{IN} = 2.7 V From: 60 µA To: 70 µA in the *Electrical Characteristics* table ... 5
- Changed the Shutdown current MAX value From: 2.25 µA To: 2.3 µA in the *Electrical Characteristics* table ... 5

5 Device Comparison Table

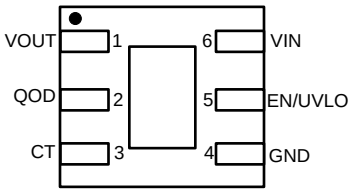
DEVICE	R_{ON} at 12 V	Package	QUICK OUTPUT DISCHARGE	T_A	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22810	79 mΩ	DBV	Configurable	105°C	2 A	Active High
TPS22810	79 mΩ	DRV	Configurable	105°C	2 A	Active High

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



DRV Package
6-Pin WSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO,			
	SOT23	WSON		
CT	4	3	O	Switch slew rate control. Can be left floating
EN/UVLO	3	5	I	Active high switch control input and UVLO adjustment. Do not leave floating
GND	2	4	—	Device ground
QOD	5	2	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways. • Placing an external resistor between VOUT and QOD • Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin floating See the *Quick Output Discharge (QOD)* for more information
VIN	1	6	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND
VOUT	6	1	O	Switch output

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	20	V
V_{OUT}	Output voltage	–0.3	min(VIN + 0.3, 20)	V
$V_{EN/UVLO}$	EN/UVLO voltage	–0.3	20	V
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	2.7	18	V
$V_{EN/UVLO}$	EN/UVLO voltage	0	18	V
V_{OUT}	Output voltage		V_{IN}	V
IMAX	Maximum continuous switch current, T_A = 65°C		2	A
T_A	Operating free-air temperature (1)	–40	105	°C
C_{IN}	Input capacitor	1 (2)		µF

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(MAX)}$], the maximum power dissipation of the device in the application [$P_{D(MAX)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(MAX)} = T_{J(MAX)} – (\theta_{JA} \times P_{D(MAX)})$.
(2) See the *Detailed Description* section.

7.4 Thermal Information

THERMAL METRIC (1)		TPS22810		UNIT
		DBV (SOT23)	DRV (WSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182	74.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.2	80.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.9	44.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.4	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.3	44.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the following ambient operating temperature –40°C ≤ T_A ≤ +105°C. Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q, VIN}$	Quiescent current	V = 18 V, I = 0 A	V_{IN} = 18 V	–40°C to +85°C		62	80	µA
				–40°C to +105°C			85	
			V_{IN} = 12 V	–40°C to +85°C		62	80	
				–40°C to +105°C			85	
			V_{IN} = 5 V	–40°C to +85°C		59	80	
				–40°C to +105°C			85	
			V_{IN} = 3.3 V	–40°C to +85°C		53	80	
				–40°C to +105°C			85	
			V_{IN} = 2.7 V	–40°C to +85°C		49	70	
				–40°C to +105°C			85	
$I_{SD, VIN}$	Shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 18 V	–40°C to +85°C		0.5	2.3	µA
				–40°C to +105°C			3.8	
			V_{IN} = 12 V	–40°C to +85°C		0.5	2.3	
				–40°C to +105°C			3.8	
			V_{IN} = 5 V	–40°C to +85°C		0.5	2.3	
				–40°C to +105°C			3.8	
			V_{IN} = 3.3 V	–40°C to +85°C		0.5	2.3	
				–40°C to +105°C			3.8	
			V_{IN} = 2.7 V	–40°C to +85°C		0.5	2.3	
				–40°C to +105°C			3.8	
$I_{EN/UVLO}$	EN/UVLO pin input leakage current	V_{IN} = 18 V, I_{OUT} = 0 A		–40°C to +105°C			0.1	µA
V_{UVR}	VIN UVLO threshold, rising			–40°C to +105°C	2	2.54	2.62	V
V_{UVhyst}	VIN UVLO hysteresis			–40°C to +105°C		5%		
V_{ENR}	EN threshold voltage, rising			–40°C to +105°C	1.13	1.23	1.3	V
V_{ENF}	EN threshold voltage, falling			–40°C to +105°C	1.08	1.13	1.18	V
V_{SHUTF}	EN threshold voltage for low IQ shutdown			–40°C to +105°C	0.5	0.75	0.9	V

Electrical Characteristics (continued)

Unless otherwise noted, the specification in the following table applies over the following ambient operating temperature –40°C ≤ T_A ≤ +105°C. Typical values are for T_A = 25°C.

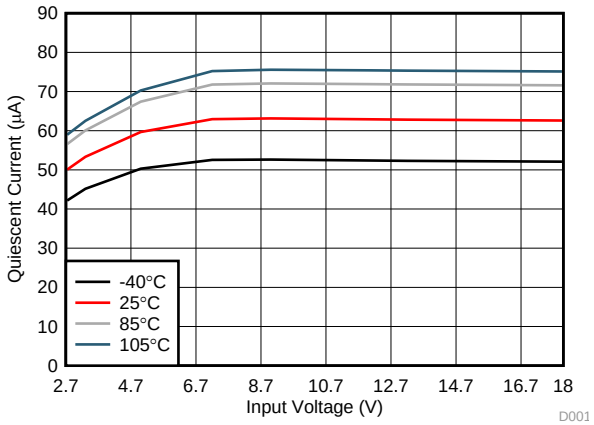
PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
R_{ON}	On-resistance	V_{IN} = 18 V, I_{OUT} = –200 mA	25°C		79	86	mΩ
			–40°C to +85°C			105	
			–40°C to +105°C			115	
		V_{IN} = 12 V, I_{OUT} = –200 mA	25°C		79	86	
			–40°C to +85°C			105	
			–40°C to +105°C			115	
		V_{IN} = 9 V, I_{OUT} = –200 mA	25°C		79	86	
			–40°C to +85°C			105	
			–40°C to +105°C			115	
		V_{IN} = 5 V, I_{OUT} = –200 mA	25°C		79	86	
			–40°C to +85°C			105	
			–40°C to +105°C			115	
		V_{IN} = 3.3 V, I_{OUT} = –200 mA	25°C		83	92	
			–40°C to +85°C			115	
			–40°C to +105°C			125	
		V_{IN} = 2.7 V, I_{OUT} = –200 mA	25°C		86	95	
			–40°C to +85°C			120	
			–40°C to +105°C			130	
R_{PD}	Output pull down resistance	V_{IN} = V_{OUT} = 18 V, $V_{EN/UVLO}$ = 0 V	–40°C to +105°C		290	350	Ω
		V_{IN} = V_{OUT} = 12 V, $V_{EN/UVLO}$ = 0 V	–40°C to +105°C		265	350	
		V_{IN} = V_{OUT} = 5 V, $V_{EN/UVLO}$ = 0 V	–40°C to +105°C		250	400	
TS	Thermal shutdown	Threshold, VIN = 18 V	–40°C to +105°C		160		°C
TSHDN Hyst	Thermal shutdown hysteresis	TSD hysteresis, VIN = 18 V	–40°C to +105°C		30		°C

7.6 Switching Characteristics

Refer to the timing test circuit in Figure 16 (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN is already in steady state condition before the EN/UVLO pin is asserted high.

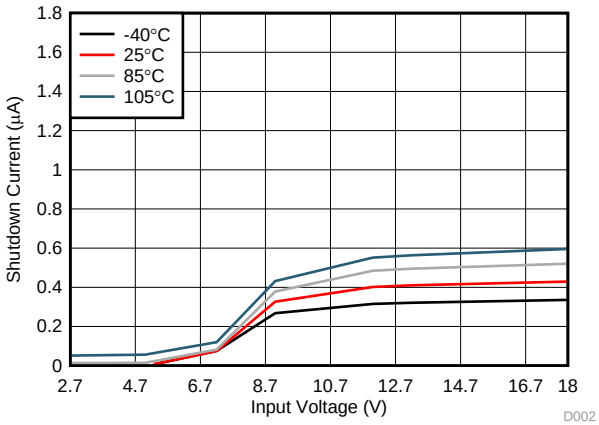
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 18 V, $V_{EN/UVLO}$ = 5 V, T_A = 25 °C (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		520		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		3.3		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		700		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		2		
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		180		
V_{IN} = 12 V, $V_{EN/UVLO}$ = 5 V, T_A = 25 °C (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		380		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		3.3		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		460		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		150		
V_{IN} = 3.3 V, $V_{EN/UVLO}$ = 5 V, T_A = 25 °C (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		185		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		3.3		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		120		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, CT = 2200 pF		130		

7.7 Typical DC Characteristics



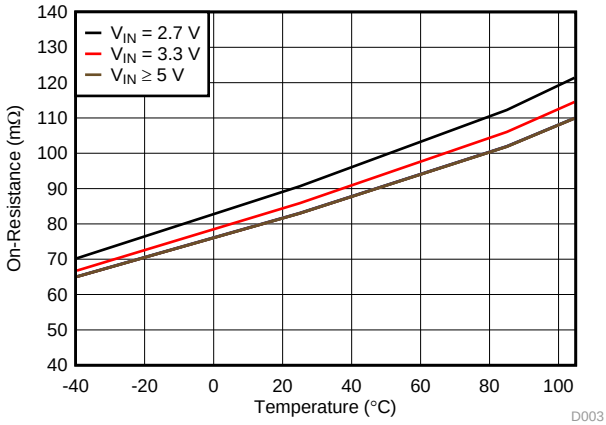
$V_{EN/UVLO}$ = 5 V I_{OUT} = 0 A

Figure 1. Quiescent Current vs Input Voltage



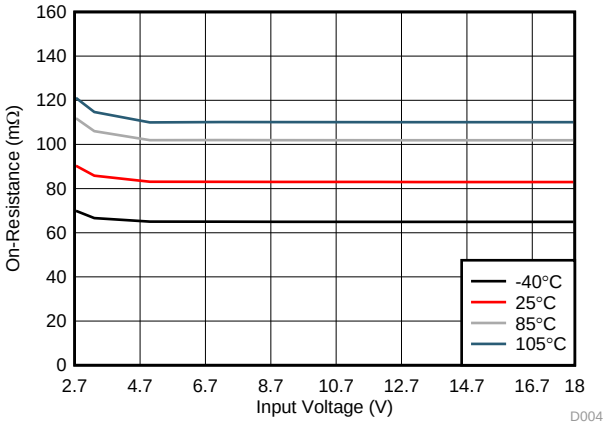
$V_{EN/UVLO}$ = 0 V I_{OUT} = 0 A

Figure 2. Shutdown Current vs Input Voltage



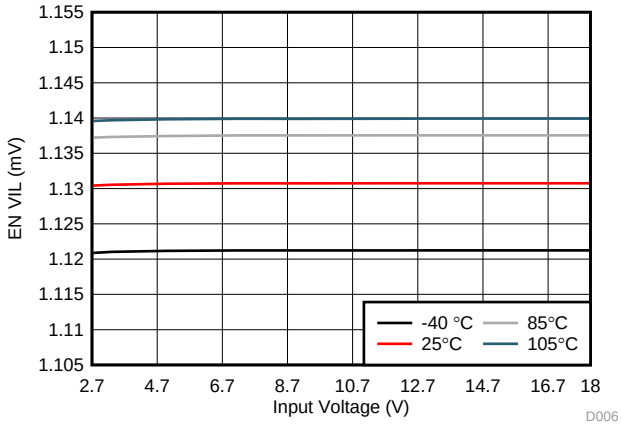
$V_{EN/UVLO}$ = 5 V I_{OUT} = –200 mA

Figure 3. On-Resistance vs Temperature



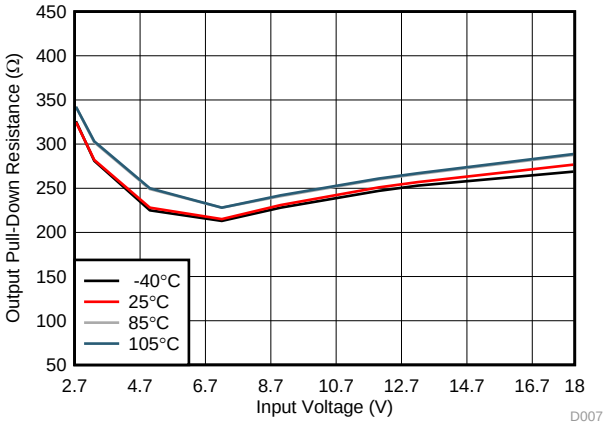
$V_{EN/UVLO}$ = 5 V I_{OUT} = –200 mA

Figure 4. On-Resistance vs Input Voltage



I_{OUT} = 0 A

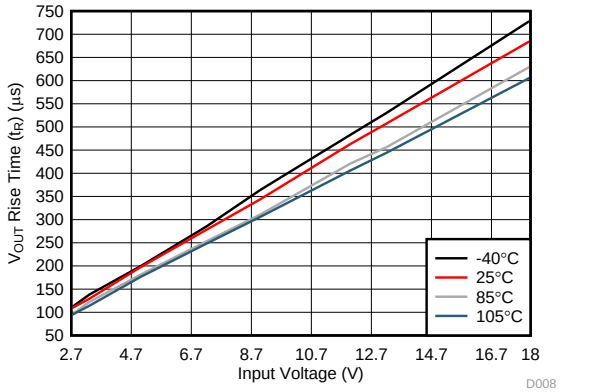
Figure 5. EN VIL vs Input Voltage



V_{IN} = V_{OUT} $V_{EN/UVLO}$ = 0 V

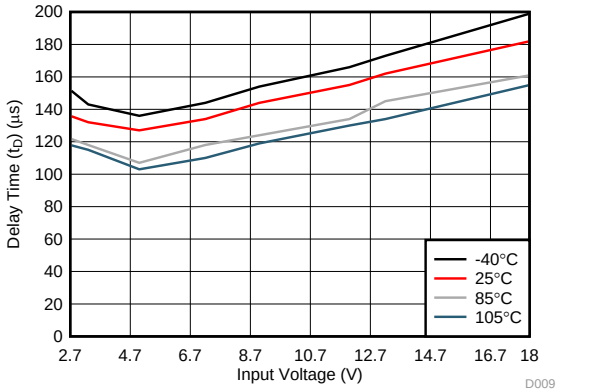
Figure 6. Output Pull-Down Resistance vs Input Voltage

7.8 Typical AC Characteristics



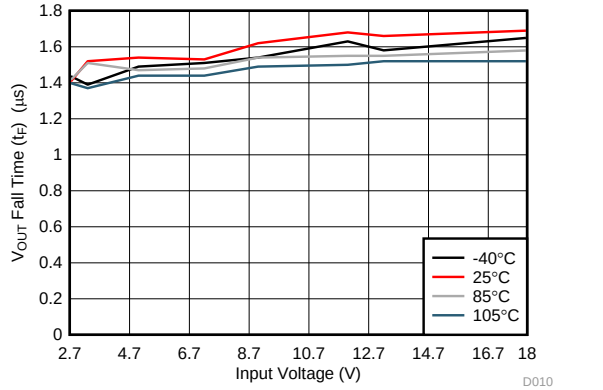
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF
CT = 2200 pF

Figure 7. V_{OUT} Rise Time (t_R) vs Input Voltage



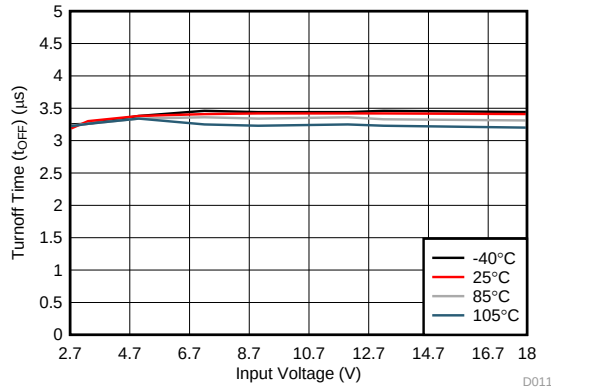
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF
CT = 2200 pF

Figure 8. Delay Time (t_D) vs Input Voltage



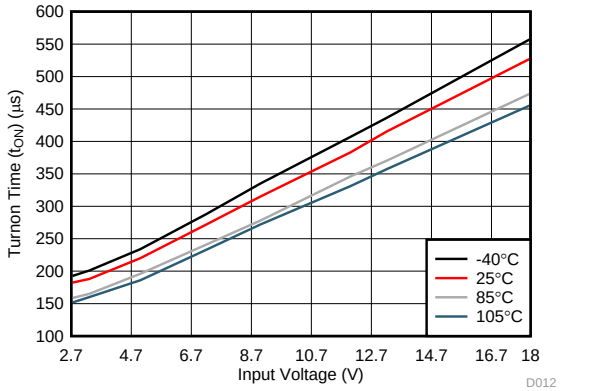
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 9. V_{OUT} Fall Time (t_F) vs Input Voltage



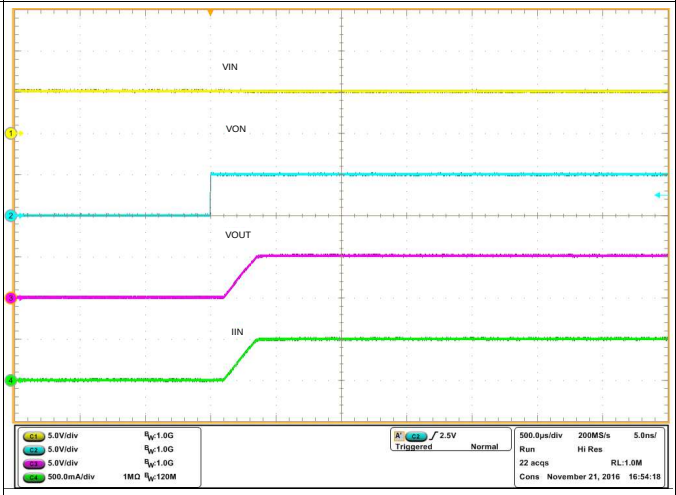
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 10. Turnoff Time (t_{OFF}) vs Input Voltage



C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF
CT = 2200 pF

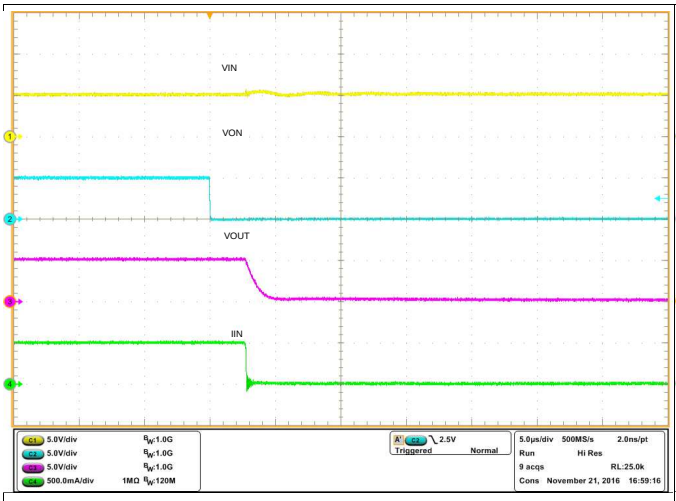
Figure 11. Turnon Time (t_{ON}) vs Input Voltage



V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω CT = 2200 pF

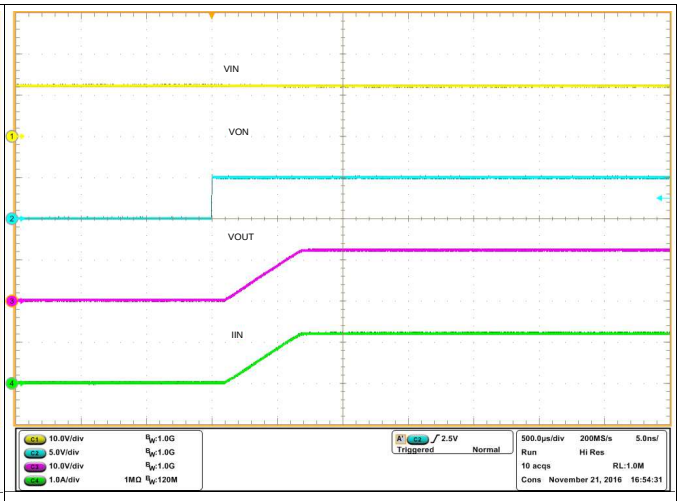
Figure 12. Rise Time t_R at V_{IN} = 5 V

Typical AC Characteristics (continued)



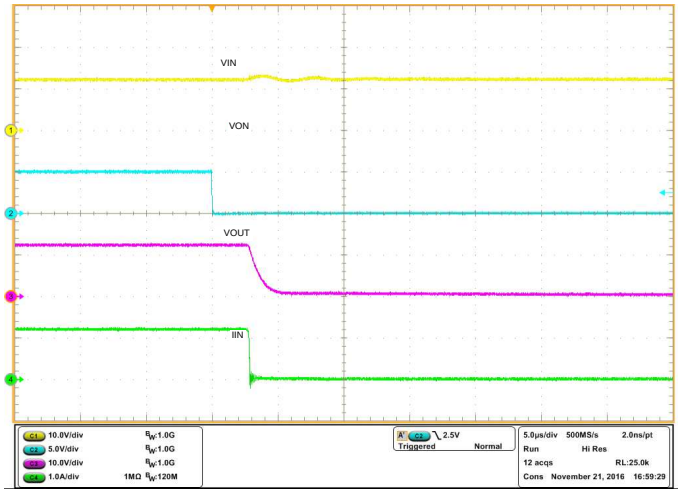
V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω QOD = Open

Figure 13. Fall Time t_F at V_{IN} = 5 V



V_{IN} = 12 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω CT = 2200 pF

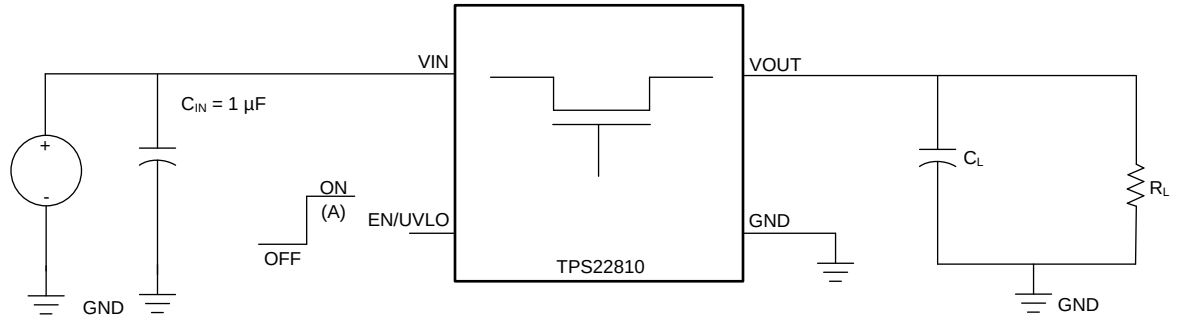
Figure 14. Rise Time t_R at V_{IN} = 12 V



V_{IN} = 12 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω QOD = Open

Figure 15. Fall Time t_F at V_{IN} = 12 V

8 Parameter Measurement Information



A. Rise and fall times of the control signal are 100 ns

Figure 16. Test Circuit

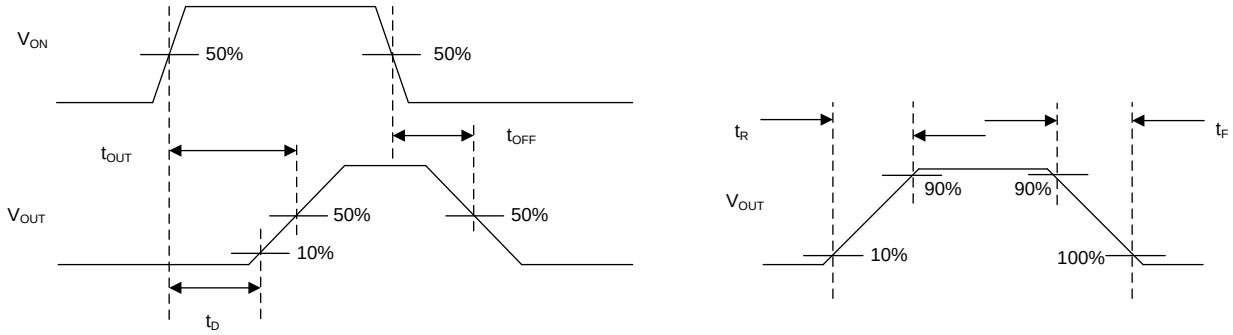


Figure 17. Timing Waveforms

9 Detailed Description

9.1 Overview

The TPS22810 is a 6-pin, 2.7-18-V, 2-A load switch with thermal protection in two separate package options. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage across the device.

The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold (VUVR), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device starts conducting and allow current to flow from VIN to VOUT. When EN/UVLO is held low (below VENF), internal MOSFET is turned off.

A voltage V(EN/UVLO) < V(ENF) on this pin turns off the internal FET, thus disconnecting VIN from VOUT, while voltage below V(SHUTF) takes the device into shutdown mode, with IQ less than 1 μA to ensure minimal power loss.

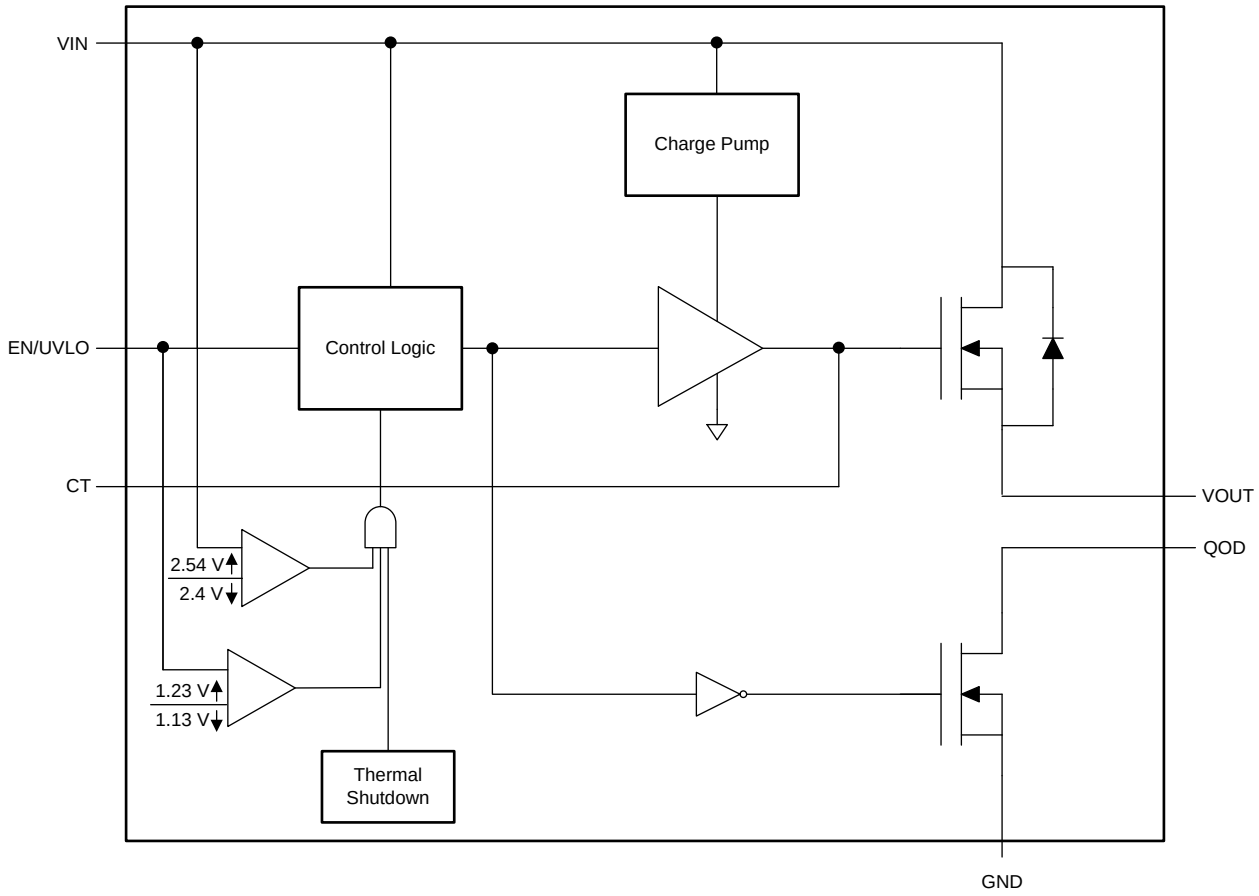
The device has a configurable slew rate which helps reduce or eliminate power supply droop because of large inrush currents. The device also features an internal RPD resistor, which discharges VOUT once the switch is disabled.

During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The device also features a QOD pin, which allows the configuration of the discharge rate of VOUT once the switch is disabled.

The device has a thermal protection feature. Due to this device protects itself against thermal damage due to over-temperature and over-current conditions. Safe Operating Area (SoA) requirements are thus inherently met without any special design consideration by the board designer.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 On and Off Control

TThe EN/UVLO pin controls the state of the switch. EN/UVLO is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The EN/UVLO pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

9.3.2 Quick Output Discharge (QOD)

The TPS22810 includes a QOD feature. The QOD pin can be configured in one of three ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal resistance R_{PD}. The value of this resistance is listed in the *Electrical Characteristics* table.
- QOD pin connected to VOUT pin using an external resistor R_{EXT}. After the switch becomes disabled, the discharge rate is controlled by the value of the total resistance of the QOD. To adjust the total QOD resistance, Equation 1 can be used.

$$R_{QOD} = R_{PD} + R_{EXT} \quad (1)$$

where

- R_{QOD} is the total output discharge resistance
- R_{PD} is the internal pulldown resistance
- R_{EXT} is the external resistance placed between the VOUT and QOD pin.

Feature Description (continued)

- QOD pin is unused and left floating. Using this method, there is no quick output discharge functionality, and the output remains floating after the switch is disabled.

Note that during thermal shutdown, the QOD functionality is not available. The device does not discharge the load as RPD does not become engaged.

The fall times of the device depend on many factors including the total resistance of the QOD, V_{IN}, and the output capacitance. When QOD is connected to VOUT, the fall time changes over V_{IN} as the internal R_{PD} varies over V_{IN}. To calculate the approximate fall time of V_{OUT} for a given R_{QOD}, use Equation 2 and Table 1.

$$V_{CAP} = V_{IN} \times e^{-t/\tau} \quad (2)$$

where

- V_{CAP} is the voltage across the capacitor (V)
- t is the time since power supply removal (s)
- τ is the time constant equal to $R_{QOD} \times C_L$

The fall times' dependency on V_{IN} becomes minimal as the QOD value increases with additional external resistance. See Table 1 for QOD fall times.

Table 1. QOD Fall Times

V_{IN} (V)	FALL TIME (µs) 90% - 10%, C_{IN} = 1 µF, I_{OUT} = 0 A , V_{IN} = 0 V, ON = 0 V(1)					
	T_A = 25°C			T_A = 85°C		
	C_L = 1 µF	C_L = 10 µF	C_L = 100 µF	C_L = 1 µF	C_L = 10 µF	C_L = 100 µF
18	470	4700	47000	470	4700	47000
12	450	4500	45000	450	4500	45000
9	440	4400	44000	440	4400	44000
5	500	5000	50000	480	4800	48000
3.3	600	6000	60000	570	5700	57000

(1) TYPICAL VALUES WITH QOD SHORTED TO VOUT

9.3.2.1 QOD when System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor, C_{IN}, discharges at VIN. Past the set UVLO level, the pull-down resistance RPD becomes disabled and the output no longer becomes discharged. If there is still remaining charge on the output capacitor, this results in longer fall times. Care must be taken such that C_{IN} is large enough to meet the device UVLO settings.

9.3.2.2 Internal QOD Considerations

Special considerations must be taken when using the internal R_{PD} by shorting the QOD pin to the VOUT pin. The internal R_{PD} is a pulldown resistance designed to quickly discharge a load after the switch has been disabled. Care must be used to ensure that excessive current does not flow through R_{PD} during discharge so that the maximum T_J of 125°C is not exceeded. When using only the internal R_{PD} to discharge a load, the total capacitive load must not exceed 200 uF. Otherwise, an external resistor, R_{EXT}, must be used to ensure the amount of current flowing through R_{PD} is properly limited and the maximum T_J is not exceeded. To ensure the device is not damaged, the remaining charge from C_L needs to decay naturally through the internal QOD resistance and must not be driven.

9.3.3 EN/UVLO

As an input pin, EN/UVLO controls the ON and OFF state of the internal MOSFET. In its high state, the internal MOSFET is enabled. A low on this pin turns off the internal MOSFET. High and Low levels are specified in the parametric table of the datasheet

A voltage V(EN/UVLO < V(ENF) on this pin turns off the internal FET, thus disconnecting VIN from VOUT, while voltage below V(SHUTF) takes the device into shutdown mode, with IQ less than 1 µA to ensure minimal power loss.

The EN/UVLO pin can be directly driven by a 1.8 V, 3.3 V or 5 V general purpose output pin.

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (2.5 μs typical) for quick detection of power failure. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

The undervoltage lock out can be programmed by using an external resistor divider from supply VIN terminal to EN/UVLO terminal to GND as shown in Figure 18. When an undervoltage or input power fail event is detected, the internal FET is quickly turned off. If the Under-Voltage Lock-Out function is not needed, the EN/UVLO terminal must be connected to the VIN terminal. EN/UVLO terminal must not be left floating.

The device also implements internal undervoltage-lockout (UVLO) circuitry on the VIN terminal. The device disables when the VIN terminal voltage falls below internal UVLO Threshold V(UVF). The internal UVLO threshold has a hysteresis of 125 mV (5% of V(UVR)). See Figure 19 and Figure 20.

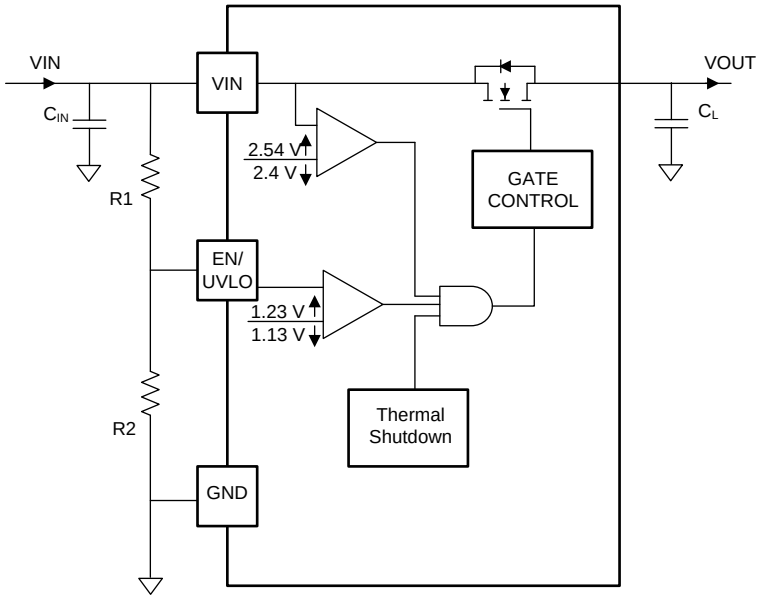


Figure 18. Configuring UVLO with External Resistor Network

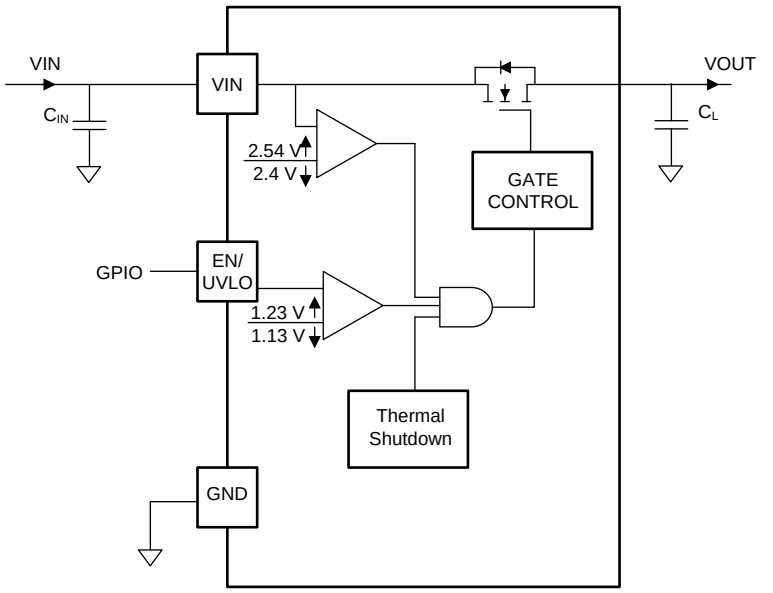


Figure 19. Using 1.8 V/3.3 V GPIO Signal Directly from Processor

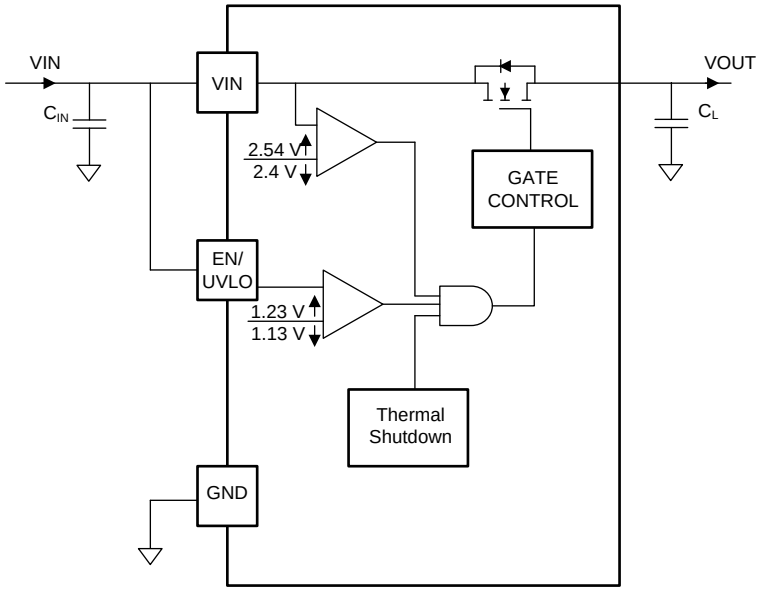


Figure 20. Default UVLO Threshold V(UVR) Using No Additional External Components

9.3.4 Adjustable Rise Time (CT)

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 12 V; therefore, the minimum voltage rating for the CT capacitor must be 25 V for optimal performance. An approximate formula for the relationship between CT and slew rate is shown in Equation 3. This equation accounts for 10% to 90% measurement on VOUT and does NOT apply for CT < 1 nF.

Use Table 2 to determine rise times for when Ct ≥ 1 nF.

$$SR = 46.62 / Ct$$

where

- SR is the slew rate (in V/µs)
- CT is the the capacitance value on the CT pin (in pF)
- The units for the constant a are µs/V. The units for the constant b are µs/(V × pF). (3)

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 2 contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where VIN is already in steady state condition before the EN/UVLO pin is asserted high.

Table 2. Rise Time Table

CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω				
	VIN = 18 V	VIN = 12 V	VIN = 9 V	VIN = 5 V	VIN = 3.3 V
0	115	91	78	60	98
470	136	94	80	63	98
1000	310	209	158	91	102
2200	688	464	345	198	135
4700	1430	957	704	397	265
10000	3115	2085	1540	864	550
27000	8230	5460	4010	2245	1430

9.3.5 Thermal Shutdown

The switch disables when the junction temperature (T_J) rises above the thermal shutdown threshold, T_{SD}. The switch re-enables once the temperature drops below the $T_{SD} – T_{SD,HYS}$ value.

9.4 Device Functional Modes

The features of the TPS22810 depend on the operating mode. Table 3 summarizes the Device Functional Modes.

Table 3. Function Table

EN/UVLO	Device State
L	Disabled
H	Enabled

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com (See the *Device Support* section for more information).

10.1.1 ON and OFF Control

The EN/UVLO pin controls the state of the switch. Asserting EN/UVLO high enables the switch. EN/UVLO is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The EN/UVLO pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

10.1.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

10.1.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause VOUT to exceed VIN when the system supply is removed. This can result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) can cause slightly more VIN dip upon turnon due to inrush currents.

This can be mitigated by increasing the capacitance on the CT pin for a longer rise time.

10.2 Typical Application

This typical application demonstrates how the TPS22810 can be used to power downstream modules.

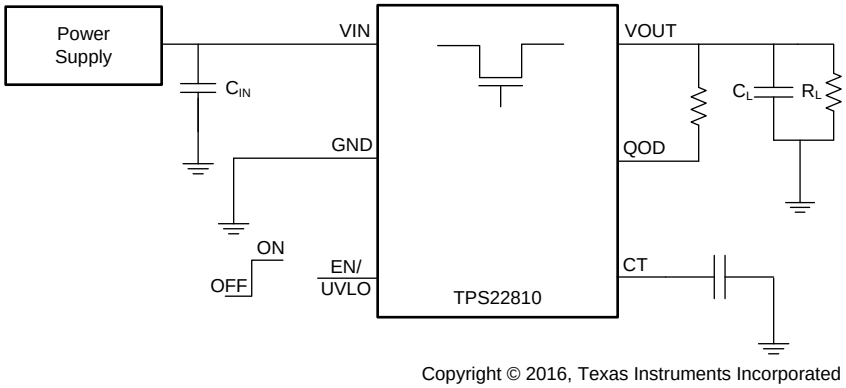


Figure 21. Typical Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the values listed in Table 4 as the design parameters:

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	12 V
Load current	2 A
C_L	22 µF
Desired fall time	20 ms
Maximum acceptable inrush current	400 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Shutdown Sequencing During Unexpected Power Loss

Using the adjustable Quick Output Discharge function of the TPS22810, adding a load switch to each power rail can be used to manage the power down sequencing in the event of an unexpected power loss (that is battery removal). To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down. Next, consult Table 1 to determine appropriate C_L and R_{QOD} values for each power rail's load switch so that the load switches' fall times correspond to the order in which they need to be powered down. In the above example, we must have this power rail's fall time to be 4 ms. Using Equation 2, we can determine the appropriate R_{QOD} to achieve our desired fall time.

Since fall times are measured from 90% of V_{OUT} to 10% of V_{OUT}, using Equation 2, we get Equation 4 and Equation 5.

$$1.2V = 10.8V \times e^{-(20ms)/(R_{QOD} \times (22\mu F))} \quad (4)$$

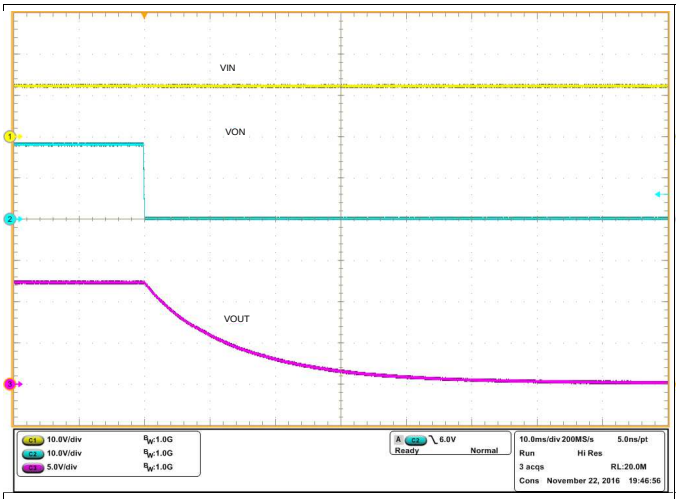
$$R_{QOD} = 413.7\ \Omega \quad (5)$$

Consulting Figure 6, R_{PD} at V_{IN} = 12 V is approximately 250 Ω. Using Equation 1, the required external QOD resistance can be calculated as shown in Equation 6 and Equation 7.

$$413.7\ \Omega = 250\ \Omega + R_{EXT} \quad (6)$$

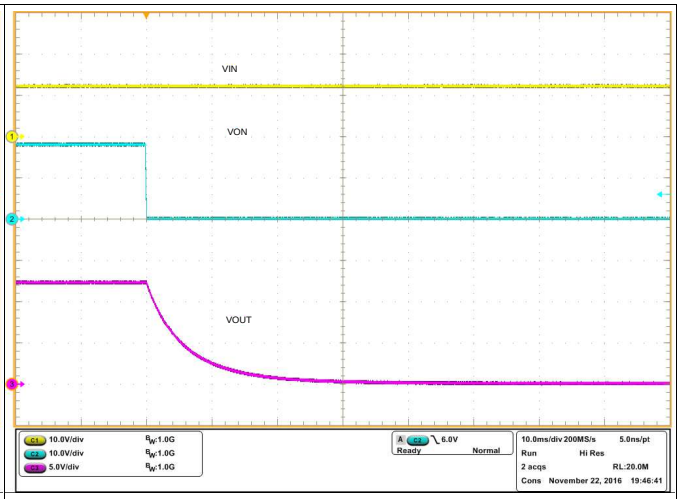
$$R_{EXT} = 163.7\ \Omega \quad (7)$$

Figure 22 through Figure 25 are scope shots demonstrating an example of the QOD functionality when power is removed from the device (both ON and VIN are disconnected simultaneously). In the scope shots, the V_{IN} = 12 V and correspond to when R_{QOD} = 1000 Ω, R_{QOD}= 500 Ω, and QOD = VOUT with two values of C_L = 10 µF and 22 µF.



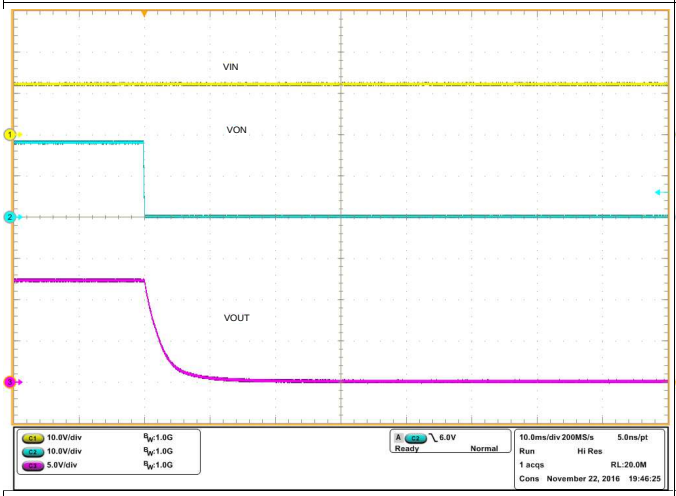
V_{IN} = 12 V C_{IN} = 1 µF C_L = 10 µF

Figure 22. Fall Time t_F at V_{IN} = 12 V, R_{QOD} = 1000 Ω



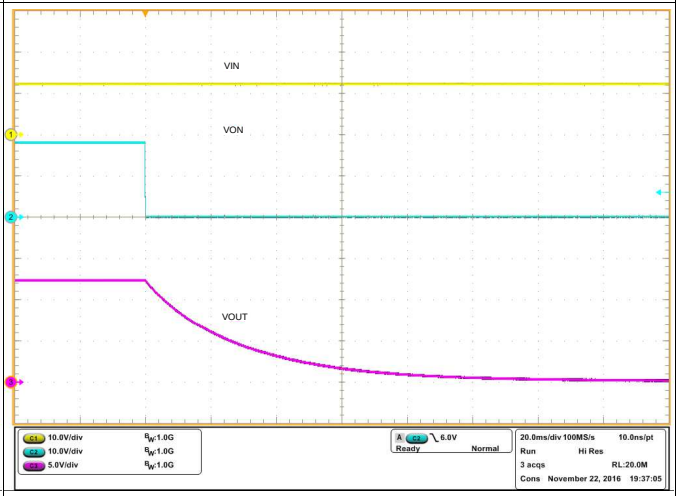
V_{IN} = 12 V C_{IN} = 1 µF C_L = 10 µF

Figure 23. Fall Time t_F at V_{IN} = 12 V, R_{QOD} = 500 Ω



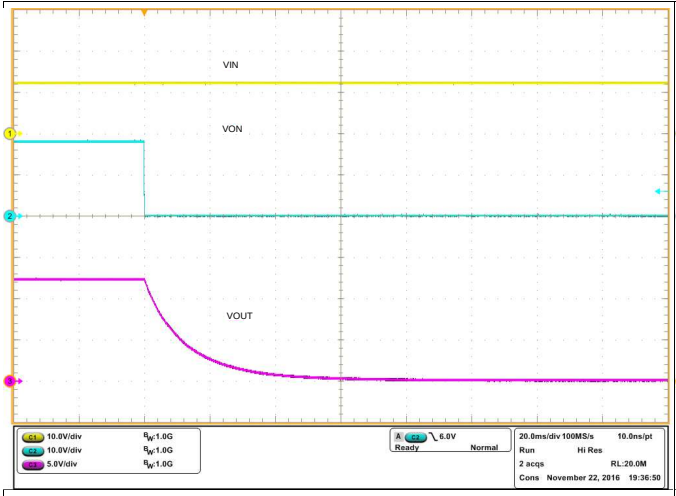
V_{IN} = 12 V C_{IN} = 1 µF C_L = 10 µF

Figure 24. t_F at V_{IN} = 12 V , QOD = V_{OUT}



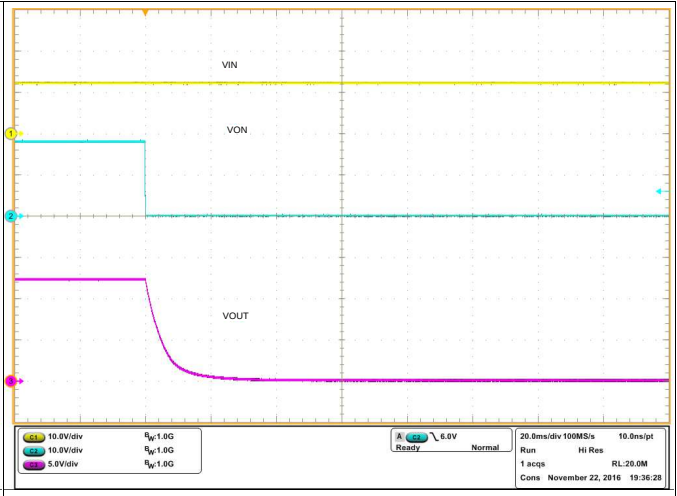
V_{IN} = 12 V C_{IN} = 1 µF C_L = 22 µF

Figure 25. t_F at V_{IN} = 12 V, R_{QOD} = 1000 Ω



V_{IN} = 12 V C_{IN} = 1 µF C_L = 22 µF

Figure 26. t_F at V_{IN} = 12 V, R_{QOD} = 500 Ω



V_{IN} = 12 V C_{IN} = 1 µF C_L = 22 µF

Figure 27. t_F at V_{IN} = 12 V, QOD = V_{OUT}

10.2.2.2 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics* table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use Equation 8 to calculate the VIN to VOUT voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \quad (8)$$

where

- ΔV is the voltage drop from VIN to VOUT
- I_{LOAD} is the load current
- R_{ON} is the On-resistance of the device for a specific V_{IN}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.2.2.3 Inrush Current

To determine how much inrush current is caused by the C_L capacitor, use Equation 9.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \quad (9)$$

where

- I_{INRUSH} is the amount of inrush caused by C_L
- C_L is the capacitance on VOUT
- dt is the Output Voltage rise time during the ramp up of VOUT when the device is enabled
- dV_{OUT} is the change in V_{OUT} during the ramp up of VOUT when the device is enabled

The appropriate rise time can be calculated using the design requirements and the inrush current equation. As we calculate the rise time (measured from 10% to 90% of V_{OUT}), we account for this in our d_{VOUT} parameter (80% of V_{OUT} = 9.6 V) as shown in Equation 10 and Equation 11.

$$400\ mA = 22\ \mu F \times 9.6\ V/dt \quad (10)$$

$$dt = 528\ \mu s \quad (11)$$

To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 528 µs. Consulting Table 2 at V_{IN} = 12 V, CT = 4700 pF provides a typical rise time of 957 µs. Using this rise time and voltage into Equation 9, yields Equation 12 and Equation 13.

$$I_{Inrush} = 22\ \mu F \times 9.6\ V/\ 957\ \mu s \quad (12)$$

$$_{Inrush} = 220\ mA \quad (13)$$

An appropriate C_L value must be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

10.2.3 Application Curves

See the oscilloscope captures below for an example of how the CT capacitor can be used to reduce inrush current for V_{IN} = 12 V. See the *Adjustable Rise Time (CT)* section for rise times for corresponding CT values.

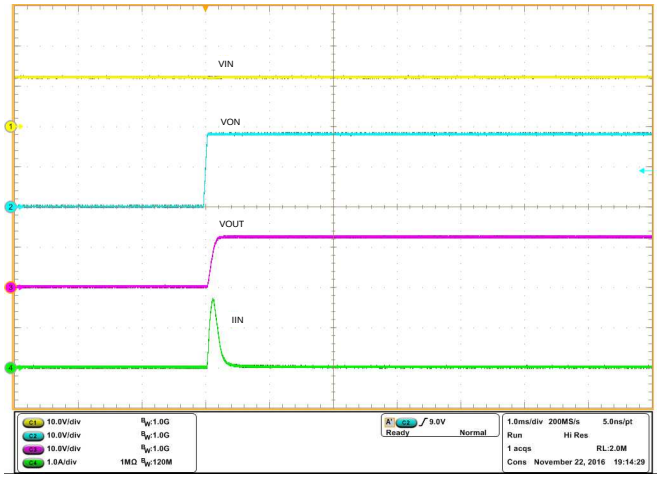


Figure 28. TPS22810 Inrush Current with C_L = 22 µF, CT = 0 pF

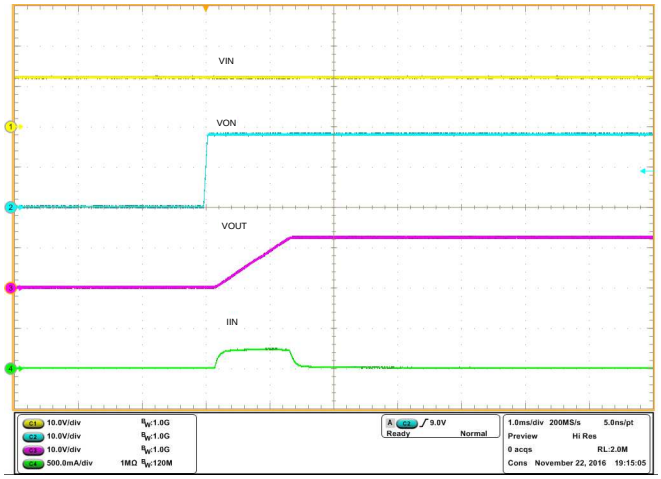


Figure 29. TPS22810 Inrush Current with C_L = 22 µF, CT = 4700 pF

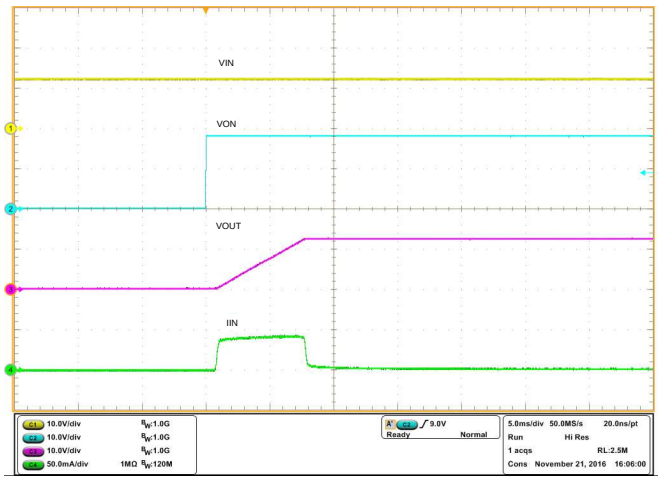


Figure 30. TPS22810 Inrush Current with C_L = 22 µF, CT = 27000 pF

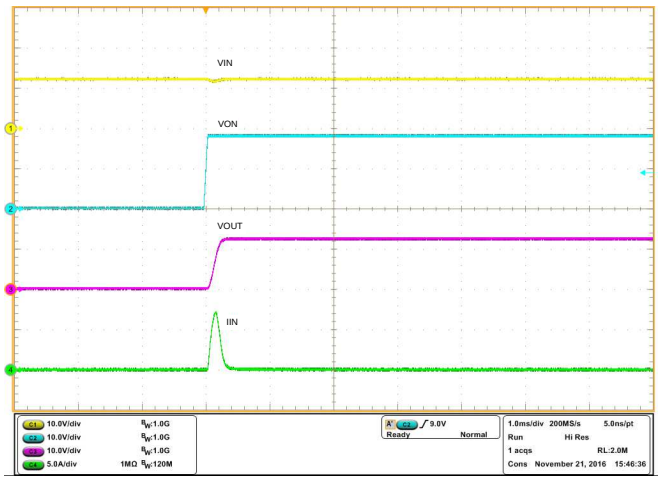


Figure 31. TPS22810 Inrush Current with C_L = 100 µF, CT = 0 pF

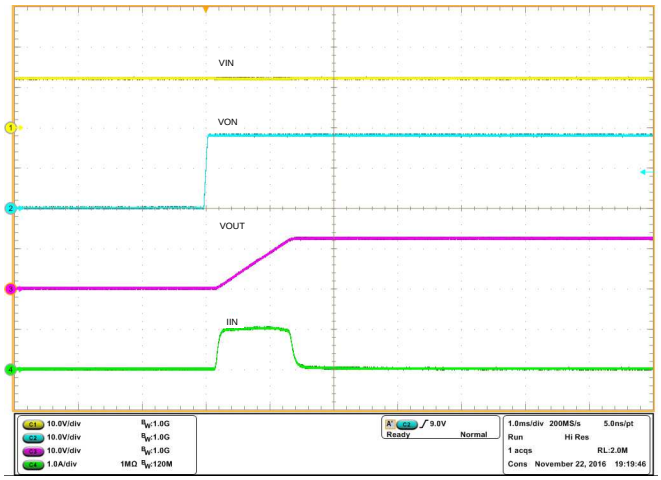


Figure 32. TPS22810 Inrush Current with C_L = 100 µF, CT = 4700 pF

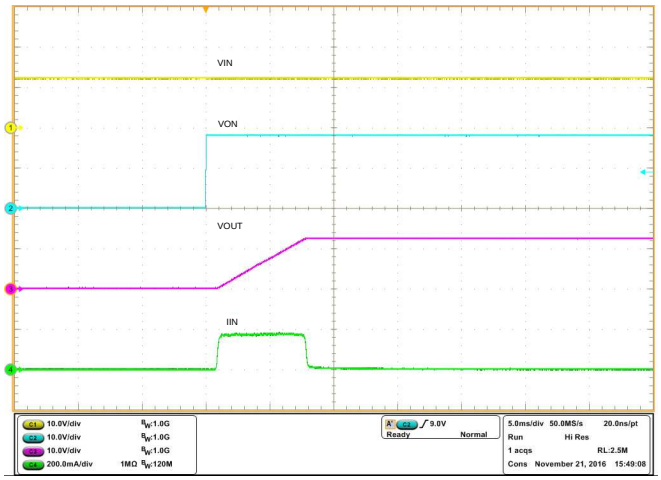


Figure 33. TPS22810 Inrush Current with C_L = 100 µF, CT = 27000 pF

11 Power Supply Recommendations

The device is designed to operate from a VIN range of 2.7 V to 18 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 µF may be sufficient.

The TPS22810 operates regardless of power sequencing order. The order in which voltages are applied to V_{IN} and ON does not damage the device as long as the voltages do not exceed the absolute maximum operating conditions.

12 Layout

12.1 Layout Guidelines

1. VIN and VOUT traces must be as short and wide as possible to accommodate for high current.
2. The VIN pin must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-μF ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.

12.2 Layout Example

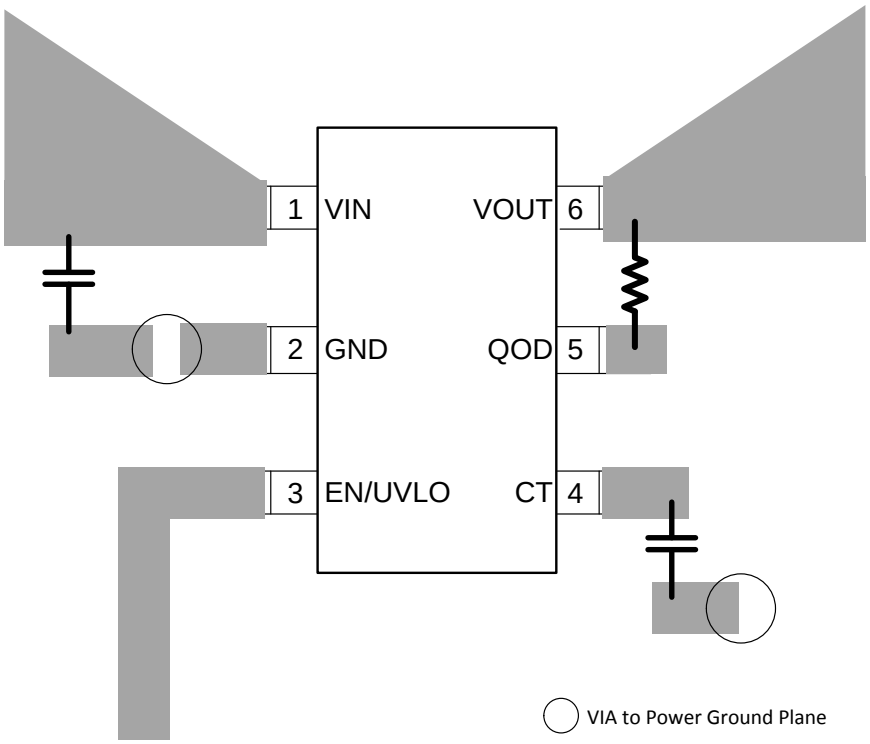


Figure 34. Recommended Board Layout

12.3 Thermal Considerations

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 14.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (14)$$

where

- $P_{D(MAX)}$ is the maximum allowable power dissipation
- $T_{J(MAX)}$ is the maximum allowable junction temperature (150°C for the TPS22810)
- T_A is the ambient temperature of the device
- θ_{JA} is the junction to air thermal impedance. Refer to the *Thermal Information* table. This parameter is highly dependent upon board layout.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Developmental Support

For the TPS22810 PSpice Transient Model, see *TPS22810 PSpice Transient Model*

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

TPS22810 Load Switch Evaluation Module

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22810DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	19HF	Samples
TPS22810DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	19HF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

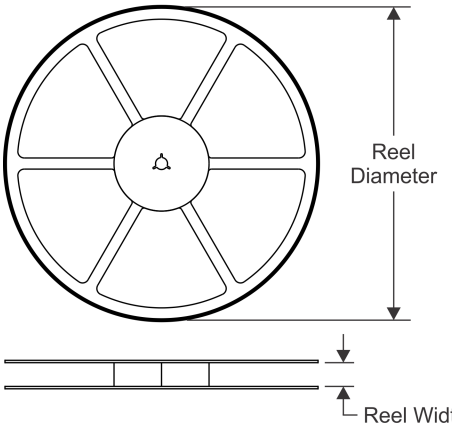
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

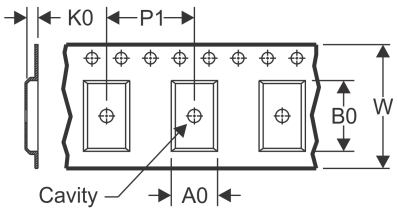
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

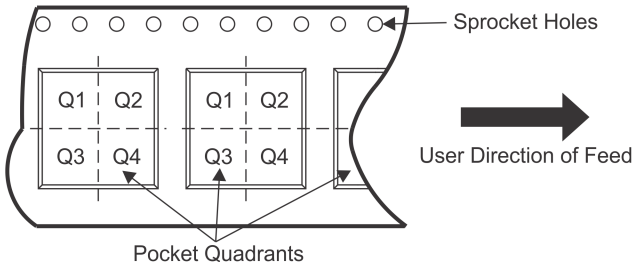


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

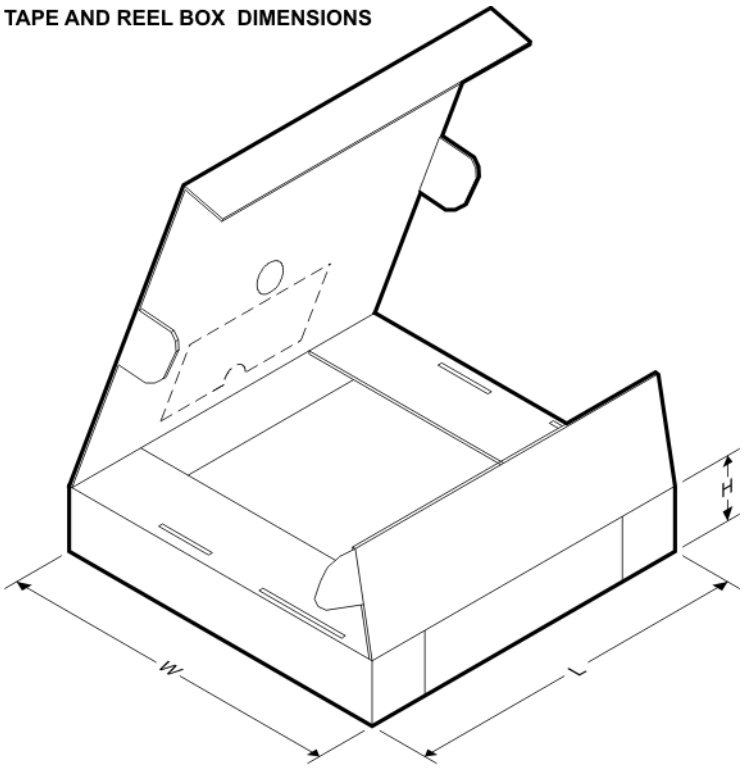
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22810DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22810DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

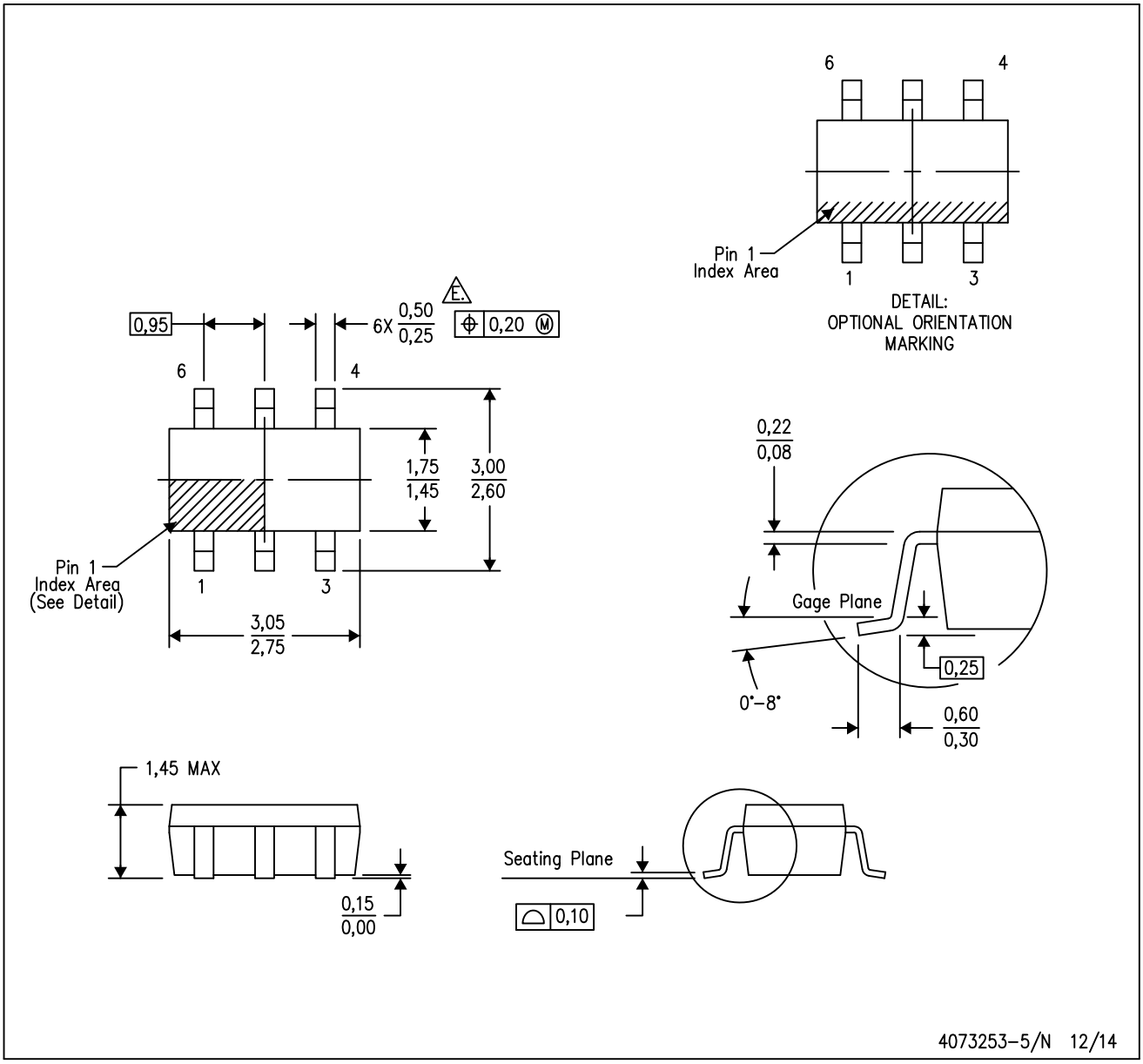
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22810DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS22810DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

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