5. DC Characteristics and Timing Specifications

CII51005-4.0

Operating Conditions

Cyclone® II devices are offered in commercial, industrial, automotive, and extended temperature grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the parameter values in this chapter apply to all Cyclone II devices. AC and DC characteristics are specified using the same numbers for commercial, industrial, and automotive grades. All parameters representing voltages are measured with respect to ground.

Tables 5–1 through 5–4 provide information on absolute maximum ratings.

Table 5–1. Cyclone II Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Output supply voltage		–0.5	4.6	V
V_{CCA_PLL} [1..4]	PLL supply voltage		–0.5	1.8	V
V_{IN}	DC input voltage *(3)*	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin	—	–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias	—	125	°C

Notes to Table 5–1:

(1) Conditions beyond those listed in this table cause permanent damage to a device. These are stress ratings only. Functional operation at these levels or any other conditions beyond those specified in this chapter is not implied. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effect on the device reliability.

(2) Refer to the *Operating Requirements for Altera Devices Data Sheet* for more information.

(3) During transitions, the inputs may overshoot to the voltage shown in Table 5–4 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transition, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5–2 specifies the recommended operating conditions for Cyclone II devices. It shows the allowed voltage ranges for V_{CCINT}, V_{CCIO}, and the operating junction temperature (T_J). The LVTTL and LVCMOS inputs are powered by V_{CCIO} only. The LVDS and LVPECL input buffers on dedicated clock pins are powered by V_{CCINT}. The SSTL, HSTL, LVDS input buffers are powered by both V_{CCINT} and V_{CCIO}.

Table 5–2. Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(1)*	1.15	1.25	V
V_{CCIO} *(2)*	Supply voltage for output buffers, 3.3-V operation	*(1)*	3.135 (3.00)	3.465 (3.60) *(3)*	V
	Supply voltage for output buffers, 2.5-V operation	*(1)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(1)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(1)*	1.425	1.575	V
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C
		For extended temperature use	–40	125	°C
		For automotive use	–40	125	°C

Notes to Table 5–2:

(1) The V_{CC} must rise monotonically. The maximum V_{CC} (both V_{CCIO} and V_{CCINT}) rise time is 100 ms for non-A devices and 2 ms for A devices.

(2) The V_{CCIO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCIO} range specific to each of the single-ended I/O standards is given in Table 5–6, and those specific to the differential standards is given in Table 5–8.

(3) The minimum and maximum values of 3.0 V and 3.6 V, respectively, for V_{CCIO} only applies to the PCI and PCI-X I/O standards. Refer to Table 5–6 for the voltage range of other I/O standards.

Table 5–3. DC Characteristics for User I/O, Dual-Purpose, and Dedicated Pins (Part 1 of 2)

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Unit
V_{IN}	Input voltage	*(1)*, *(2)*		–0.5	—	4.0	V
I_i	Input pin leakage current	$V_{IN} = V_{CCIOmax}$ to 0 V *(3)*		–10	—	10	µA
V_{OUT}	Output voltage	—		0	—	V_{CCIO}	V
I_{OZ}	Tri-stated I/O pin leakage current	$V_{OUT} = V_{CCIOmax}$ to 0 V *(3)*		–10	—	10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_{IN} = ground, no load, no toggling inputs T_J = 25° C Nominal V_{CCINT}	EP2C5/A	—	0.010	*(4)*	A
			EP2C8/A	—	0.017	*(4)*	A
			EP2C15A	—	0.037	*(4)*	A
			EP2C20/A	—	0.037	*(4)*	A
			EP2C35	—	0.066	*(4)*	A
			EP2C50	—	0.101	*(4)*	A
			EP2C70	—	0.141	*(4)*	A
I_{CCIO0}	V_{CCIO} supply current (standby)	V_{IN} = ground, no load, no toggling inputs T_J = 25° C V_{CCIO} = 2.5 V	EP2C5/A	—	0.7	*(4)*	mA
			EP2C8/A	—	0.8	*(4)*	mA
			EP2C15A	—	0.9	*(4)*	mA
			EP2C20/A	—	0.9	*(4)*	mA
			EP2C35	—	1.3	*(4)*	mA
			EP2C50	—	1.3	*(4)*	mA
			EP2C70	—	1.7	*(4)*	mA

Table 5–3. DC Characteristics for User I/O, Dual-Purpose, and Dedicated Pins (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{CONF} *(5) (6)*	Value of I/O pin pull-up resistor before and during configuration	V_{IN} = 0 V; V_{CCIO} = 3.3 V	10	25	50	kΩ
		V_{IN} = 0 V; V_{CCIO} = 2.5 V	15	35	70	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.8 V	30	50	100	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.5 V	40	75	150	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.2 V	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	*(7)*	—	1	2	kΩ

Notes to Table 5–3:

(1) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltages shown in Table 5–4, based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

(3) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(4) Maximum values depend on the actual T_J and design utilization. See the Excel-based PowerPlay Early Power Estimator (www.altera.com) or the Quartus II PowerPlay Power Analyzer feature for maximum values. Refer to "Power Consumption" on page 5–13 for more information.

(5) R_{CONF} values are based on characterization. $R_{CONF} = V_{CCIO}/I_{RCONF}$. R_{CONF} values may be different if V_{IN} value is not 0 V. Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.

(6) Minimum condition at –40°C and high V_{CC}, typical condition at 25°C and nominal V_{CC} and maximum condition at 125°C and low V_{CC} for R_{CONF} values.

(7) These values apply to all V_{CCIO} settings.

Table 5–4 shows the maximum V_{IN} overshoot voltage and the dependency on the duty cycle of the input signal. Refer to Table 5–3 for more information.

Table 5–4. V_{IN} Overshoot Voltage for All Input Buffers

Maximum V_{IN} (V)	Input Signal Duty Cycle
4.0	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

Single-Ended I/O Standards

Tables 5–6 and 5–7 provide operating condition information when using single-ended I/O standards with Cyclone II devices. Table 5–5 provides descriptions for the voltage and current symbols used in Tables 5–6 and 5–7.

Table 5–5. Voltage and Current Symbol Definitions

Symbol	Definition
V_{CCIO}	Supply voltage for single-ended inputs and for output drivers
V_{REF}	Reference voltage for setting the input switching threshold
V_{IL}	Input voltage that indicates a low logic level
V_{IH}	Input voltage that indicates a high logic level
V_{OL}	Output voltage that indicates a low logic level
V_{OH}	Output voltage that indicates a high logic level
I_{OL}	Output current condition under which V_{OL} is tested
I_{OH}	Output current condition under which V_{OH} is tested
V_{TT}	Voltage applied to a resistor termination as specified by HSTL and SSTL standards

Table 5–6. Recommended Operating Conditions for User I/O Pins Using Single-Ended I/O Standards Note (1) (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{IL} (V)	V_{IH} (V)
	Min	Typ	Max	Min	Typ	Max	Max	Min
3.3-V LVTTL and LVCMOS	3.135	3.3	3.465	—	—	—	0.8	1.7
2.5-V LVTTL and LVCMOS	2.375	2.5	2.625	—	—	—	0.7	1.7
1.8-V LVTTL and LVCMOS	1.710	1.8	1.890	—	—	—	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$
1.5-V LVCMOS	1.425	1.5	1.575	—	—	—	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$
PCI and PCI-X	3.000	3.3	3.600	—	—	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$
SSTL-2 class I	2.375	2.5	2.625	1.19	1.25	1.31	$V_{REF} - 0.18$ (DC) $V_{REF} - 0.35$ (AC)	$V_{REF} + 0.18$ (DC) $V_{REF} + 0.35$ (AC)
SSTL-2 class II	2.375	2.5	2.625	1.19	1.25	1.31	$V_{REF} - 0.18$ (DC) $V_{REF} - 0.35$ (AC)	$V_{REF} + 0.18$ (DC) $V_{REF} + 0.35$ (AC)
SSTL-18 class I	1.7	1.8	1.9	0.833	0.9	0.969	$V_{REF} - 0.125$ (DC) $V_{REF} - 0.25$ (AC)	$V_{REF} + 0.125$ (DC) $V_{REF} + 0.25$ (AC)

Table 5–6. Recommended Operating Conditions for User I/O Pins Using Single-Ended I/O Standards *Note (1)* ***(Part 2 of 2)***

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{IL} (V)	V_{IH} (V)
	Min	Typ	Max	Min	Typ	Max	Max	Min
SSTL-18 class II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.125 (DC) V_{REF} – 0.25 (AC)	V_{REF} + 0.125 (DC) V_{REF} + 0.25 (AC)
1.8-V HSTL class I	1.71	1.8	1.89	0.85	0.9	0.95	V_{REF} – 0.1 (DC) V_{REF} – 0.2 (AC)	V_{REF} + 0.1 (DC) V_{REF} + 0.2 (AC)
1.8-V HSTL class II	1.71	1.8	1.89	0.85	0.9	0.95	V_{REF} – 0.1 (DC) V_{REF} – 0.2 (AC)	V_{REF} + 0.1 (DC) V_{REF} + 0.2 (AC)
1.5-V HSTL class I	1.425	1.5	1.575	0.71	0.75	0.79	V_{REF} – 0.1 (DC) V_{REF} – 0.2 (AC)	V_{REF} + 0.1 (DC) V_{REF} + 0.2 (AC)
1.5-V HSTL class II	1.425	1.5	1.575	0.71	0.75	0.79	V_{REF} – 0.1 (DC) V_{REF} – 0.2 (AC)	V_{REF} + 0.1 (DC) V_{REF} + 0.2 (AC)

Note to Table 5–6:
(1) Nominal values (Nom) are for T_A = 25° C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5, 1.8, 2.5, and 3.3 V.

Table 5–7. DC Characteristics of User I/O Pins Using Single-Ended Standards *Notes (1), (2)* ***(Part 1 of 2)***

I/O Standard	Test Conditions		Voltage Thresholds	
	I_{OL} (mA)	I_{OH} (mA)	Maximum V_{OL} (V)	Minimum V_{OH} (V)
3.3-V LVTTL	4	–4	0.45	2.4
3.3-V LVCMOS	0.1	–0.1	0.2	V_{CCIO} – 0.2
2.5-V LVTTL and LVCMOS	1	–1	0.4	2.0
1.8-V LVTTL and LVCMOS	2	–2	0.45	V_{CCIO} – 0.45
1.5-V LVTTL and LVCMOS	2	–2	0.25 × V_{CCIO}	0.75 × V_{CCIO}
PCI and PCI-X	1.5	–0.5	0.1 × V_{CCIO}	0.9 × V_{CCIO}
SSTL-2 class I	8.1	–8.1	V_{TT} – 0.57	V_{TT} + 0.57
SSTL-2 class II	16.4	–16.4	V_{TT} – 0.76	V_{TT} + 0.76
SSTL-18 class I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL-18 class II	13.4	–13.4	0.28	V_{CCIO} – 0.28
1.8-V HSTL class I	8	–8	0.4	V_{CCIO} – 0.4
1.8-V HSTL class II	16	–16	0.4	V_{CCIO} – 0.4

Table 5–7. DC Characteristics of User I/O Pins Using Single-Ended Standards Notes (1), (2) **(Part 2 of 2)**

I/O Standard	Test Conditions		Voltage Thresholds	
	I_{OL} (mA)	I_{OH} (mA)	Maximum V_{OL} (V)	Minimum V_{OH} (V)
1.5-V HSTL class I	8	–8	0.4	V_{CCIO} – 0.4
1.5V HSTL class II	16	–16	0.4	V_{CCIO} – 0.4

Notes to Table 5–7:

(1) The values in this table are based on the conditions listed in Tables 5–2 and 5–6.

(2) This specification is supported across all the programmable drive settings available as shown in the *Cyclone II Architecture* chapter of the *Cyclone II Device Handbook*.

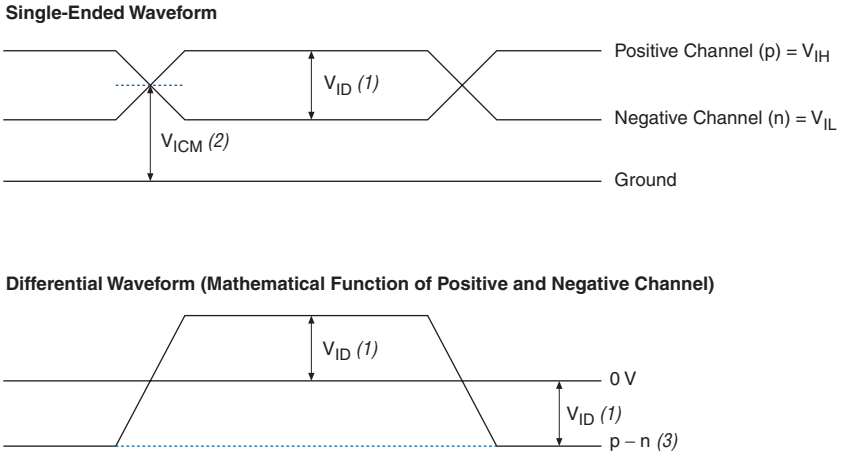
Differential I/O Standards

The RSDS and mini-LVDS I/O standards are only supported on output pins. The LVDS I/O standard is supported on both receiver input pins and transmitter output pins.

For more information on how these differential I/O standards are implemented, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook*.

Figure 5–1 shows the receiver input waveforms for all differential I/O standards (LVDS, LVPECL, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards



Notes to Figure 5–1:

(1) V_{ID} is the differential input voltage. $V_{ID} = |p - n|$.

(2) V_{ICM} is the input common mode voltage. $V_{ICM} = (p + n)/2$.

(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–8 shows the recommended operating conditions for user I/O pins with differential I/O standards.

Table 5–8. Recommended Operating Conditions for User I/O Pins Using Differential Signal I/O Standards

I/O Standard	V_{CCIO} (V)			V_{ID} (V) *(1)*			V_{ICM} (V)			V_{IL} (V)		V_{IH} (V)	
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	2.375	2.5	2.625	0.1	—	0.65	0.1	—	2.0	—	—	—	—
Mini-LVDS *(2)*	2.375	2.5	2.625	—	—	—	—	—	—	—	—	—	—
RSDS *(2)*	2.375	2.5	2.625	—	—	—	—	—	—	—	—	—	—
LVPECL *(3) (6)*	3.135	3.3	3.465	0.1	0.6	0.95	—	—	—	0	2.2	2.1	2.88
Differential 1.5-V HSTL class I and II *(4)*	1.425	1.5	1.575	0.2	—	V_{CCIO} + 0.6	0.68	—	0.9	—	V_{REF} – 0.20	V_{REF} + 0.20	—
Differential 1.8-V HSTL class I and II *(4)*	1.71	1.8	1.89	—	—	—	—	—	—	—	V_{REF} – 0.20	V_{REF} + 0.20	—
Differential SSTL-2 class I and II *(5)*	2.375	2.5	2.625	0.36	—	V_{CCIO} + 0.6	0.5 × V_{CCIO} – 0.2	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.2	—	V_{REF} – 0.35	V_{REF} + 0.35	—
Differential SSTL-18 class I and II *(5)*	1.7	1.8	1.9	0.25	—	V_{CCIO} + 0.6	0.5 × V_{CCIO} – 0.2	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.2	—	V_{REF} – 0.25	V_{REF} + 0.25	—

Notes to Table 5–8:

(1) Refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook* for measurement conditions on V_{ID}.

(2) The RSDS and mini-LVDS I/O standards are only supported on output pins.

(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

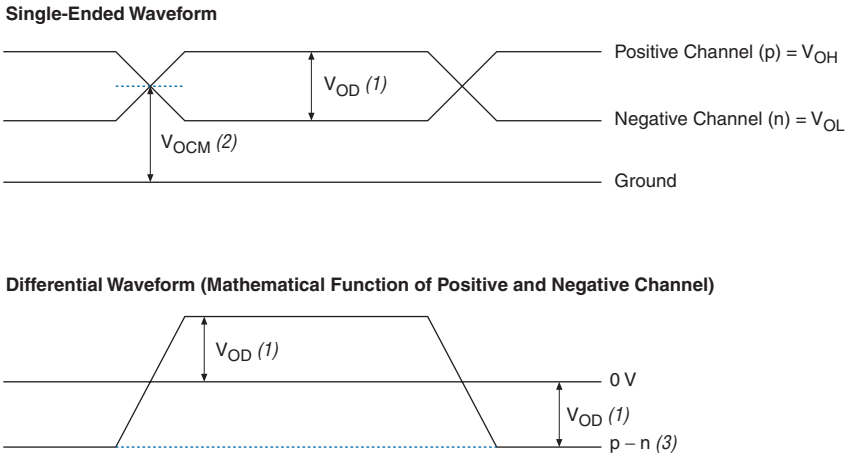
(4) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

(5) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(6) The LVPECL clock inputs are powered by V_{CCINT} and support all V_{CCIO} settings. However, it is recommended to connect V_{CCIO} to typical value of 3.3V.

Figure 5–2 shows the transmitter output waveforms for all supported differential output standards (LVDS, mini-LVDS, RSDS, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards



Notes to Figure 5–2:
(1) V_{OD} is the output differential voltage. $V_{OD} = |p - n|$.
(2) V_{OCM} is the output common mode voltage. $V_{OCM} = (p + n)/2$.
(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–9 shows the DC characteristics for user I/O pins with differential I/O standards.

Table 5–9. DC Characteristics for User I/O Pins Using Differential I/O Standards Note (1) (Part 1 of 2)

I/O Standard	V_{OD} (mV)			ΔV_{OD} (mV)		V_{OCM} (V)			V_{OH} (V)		V_{OL} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	250	—	600	—	50	1.125	1.25	1.375	—	—	—	—
mini-LVDS (2)	300	—	600	—	50	1.125	1.25	1.375	—	—	—	—
RSDS (2)	100	—	600	—	—	1.125	1.25	1.375	—	—	—	—
Differential 1.5-V HSTL class I and II (3)	—	—	—	—	—	—	—	—	V_{CCIO} – 0.4	—	—	0.4

Table 5–9. DC Characteristics for User I/O Pins Using Differential I/O Standards Note (1) *(Part 2 of 2)*

I/O Standard	V_{OD} (mV)			ΔV_{OD} (mV)		V_{OCM} (V)			V_{OH} (V)		V_{OL} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max
Differential 1.8-V HSTL class I and II (3)	—	—	—	—	—	—	—	—	V_{CCIO} – 0.4	—	—	0.4
Differential SSTL-2 class I (4)	—	—	—	—	—	—	—	—	V_{TT} + 0.57	—	—	V_{TT} – 0.57
Differential SSTL-2 class II (4)	—	—	—	—	—	—	—	—	V_{TT} + 0.76	—	—	V_{TT} – 0.76
Differential SSTL-18 class I (4)	—	—	—	—	—	0.5 × V_{CCIO} – 0.125	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.125	V_{TT} + 0.475	—	—	V_{TT} – 0.475
Differential SSTL-18 class II (4)	—	—	—	—	—	0.5 × V_{CCIO} – 0.125	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.125	V_{CCIO} – 0.28	—	—	0.28

Notes to Table 5–9:

(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
(2) The RSDS and mini-LVDS I/O standards are only supported on output pins.
(3) The differential 1.8-V HSTL and differential 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.
(4) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

DC Characteristics for Different Pin Types

Table 5–10 shows the types of pins that support bus hold circuitry.

Table 5–10. Bus Hold Support

Pin Type	Bus Hold
I/O pins using single-ended I/O standards	Yes
I/O pins using differential I/O standards	No
Dedicated clock pins	No
JTAG	No
Configuration pins	No

Table 5–11 specifies the bus hold parameters for general I/O pins.

Table 5–11. Bus Hold Parameters *Note (1)*

Parameter	Conditions	V_{CCIO} Level						Unit
		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$(maximum)	30	—	50	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IL}$(minimum)	–30	—	–50	—	–70	—	µA
Bus-hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	200	—	300	—	500	µA
Bus-hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–200	—	–300	—	–500	µA
Bus-hold trip point *(2)*	—	0.68	1.07	0.7	1.7	0.8	2.0	V

Notes to Table 5–11:
(1) There is no specification for bus-hold at V_{CCIO} = 1.5 V for the HSTL I/O standard.
(2) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

On-Chip Termination Specifications

Table 5–12 defines the specifications for internal termination resistance tolerance when using series or differential on-chip termination.

Table 5–12. Series On-Chip Termination Specifications

Symbol	Description	Conditions	Resistance Tolerance			
			Commercial Max	Industrial Max	Extended/ Automotive Temp Max	Unit
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3V	±30	±30	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 2.5V	±30	±30	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8V	±30 *(1)*	±40	±50	%

Note to Table 5–12:
(1) For commercial –8 devices, the tolerance is ±40%.

Table 5–13 shows the Cyclone II device pin capacitance for different I/O pin types.

Table 5–13. Device Capacitance *Note (1)*

Symbol	Parameter	Typical	Unit
C_{IO}	Input capacitance for user I/O pin.	6	pF
C_{LVDS}	Input capacitance for dual-purpose LVDS/user I/O pin.	6	pF
C_{VREF}	Input capacitance for dual-purpose VREF pin when used as VREF or user I/O pin.	21	pF
C_{CLK}	Input capacitance for clock pin.	5	pF

Note to Table 5–13:

(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflectometry (TDR). Measurement accuracy is within ±0.5 pF.

Power Consumption

You can calculate the power usage for your design using the PowerPlay Early Power Estimator and the PowerPlay Power Analyzer feature in the Quartus® II software.

The interactive PowerPlay Early Power Estimator is typically used during the early stages of FPGA design, prior to finalizing the project, to get a magnitude estimate of the device power. The Quartus II software PowerPlay Power Analyzer feature is typically used during the later stages of FPGA design. The PowerPlay Power Analyzer also allows you to apply test vectors against your design for more accurate power consumption modeling.

In both cases, only use these calculations as an estimation of power, not as a specification. For more information on PowerPlay tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *Power Estimation and Analysis* section in volume 3 of the *Quartus II Handbook*.

You can obtain the Excel-based PowerPlay Early Power Estimator at www.altera.com. Refer to Table 5–3 on page 5–3 for typical I_{CC} standby specifications.

The power-up current required by Cyclone II devices does not exceed the maximum static current. The rate at which the current increases is a function of the system power supply. The exact amount of current consumed varies according to the process, temperature, and power ramp rate. The duration of the I_{CCINT} power-up requirement depends on the V_{CCINT} voltage supply rise time.

You should select power supplies and regulators that can supply the amount of current required when designing with Cyclone II devices.

Altera recommends using the Cyclone II PowerPlay Early Power Estimator to estimate the user-mode I_{CCINT} consumption and then select power supplies or regulators based on the values obtained.

Timing Specifications

The DirectDrive™ technology and MultiTrack™ interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone II device densities and speed grades. This section describes and specifies the performance, internal, external, high-speed I/O, JTAG, and PLL timing specifications.

This section shows the timing models for Cyclone II devices. Commercial devices meet this timing over the commercial temperature range. Industrial devices meet this timing over the industrial temperature range. Automotive devices meet this timing over the automotive temperature range. Extended devices meet this timing over the extended temperature range. All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing Specifications

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 5–14 shows the status of the Cyclone II device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 5–14. Cyclone II Device Timing Model Status

Device	Speed Grade	Preliminary	Final
EP2C5/A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C8/A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C15A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C20/A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C35	Commercial/Industrial	—	✓
EP2C50	Commercial/Industrial	—	✓
EP2C70	Commercial/Industrial	—	✓

Performance

Table 5–15 shows Cyclone II performance for some common designs. All performance values were obtained with Quartus II software compilation of LPM, or MegaCore functions for the FIR and FFT designs.

Table 5–15. Cyclone II Performance (Part 1 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
LE	16-to-1 multiplexer *(1)*	21	0	0	385.35	313.97	270.85	286.04
	32-to-1 multiplexer *(1)*	38	0	0	294.2	260.75	228.78	191.02
	16-bit counter	16	0	0	401.6	349.4	310.65	310.65
	64-bit counter	64	0	0	157.15	137.98	126.08	126.27

Table 5–15. Cyclone II Performance (Part 2 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
Memory M4K block	Simple dual-port RAM 128 × 36 bit *(3)*, *(5)*	0	1	0	235.29	194.93	163.13	163.13
	True dual-port RAM 128 × 18 bit *(3)*, *(5)*	0	1	0	235.29	194.93	163.13	163.13
	FIFO 128 × 16 bit *(5)*	32	1	0	235.29	194.93	163.13	163.13
	Simple dual-port RAM 128 × 36 bit *(4)*,*(5)*	0	1	0	210.08	195.0	163.02	163.02
	True dual-port RAM 128x18 bit *(4)*,*(5)*	0	1	0	163.02	163.02	163.02	163.02
DSP block	9 × 9-bit multiplier *(2)*	0	0	1	260.01	216.73	180.57	180.57
	18 × 18-bit multiplier *(2)*	0	0	1	260.01	216.73	180.57	180.57
	18-bit, 4 tap FIR filter	113	0	8	182.74	147.47	127.74	122.98
Larger Designs	8-bit, 16 tap parallel FIR filter	52	0	4	153.56	131.25	110.44	110.57
	8-bit, 1024 pt, Streaming, 3 Mults/5 Adders FFT function	3191	22	9	235.07	195.0	147.51	163.02
	8-bit, 1024 pt, Streaming, 4 Mults/2 Adders FFT function	3041	22	12	235.07	195.0	146.3	163.02
	8-bit, 1024 pt, Single Output, 1 Parallel FFT Engine, Burst, 3 Mults/5 Adders FFT function	1056	5	3	235.07	195.0	147.84	163.02
	8-bit, 1024 pt, Single Output, 1 Parallel FFT Engine, Burst, 4 Mults/2 Adders FFT function	1006	5	4	235.07	195.0	149.99	163.02
	8-bit, 1024 pt, Single Output, 2 Parallel FFT Engines, Burst, 3 Mults/5 Adders FFT function	1857	10	6	200.0	195.0	149.61	163.02
	8-bit, 1024 pt, Single Output, 2 Parallel FFT Engines, Burst, 4 Mults/2 Adders FFT function	1757	10	8	200.0	195.0	149.34	163.02
	8-bit, 1024 pt, Quad Output, 1 Parallel FFT Engine, Burst, 3 Mults/5 Adders FFT function	2550	10	9	235.07	195.0	148.21	163.02

Table 5–15. Cyclone II Performance (Part 3 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
Larger Designs	8-bit, 1024 pt, Quad Output, 1 Parallel FFT Engine, Burst, 4 Mults/2 Adders FFT function	2400	10	12	235.07	195.0	140.11	163.02
	8-bit, 1024 pt, Quad Output, 2 Parallel FFT Engines, Burst, 3 Mults/5 Adders FFT function	4343	14	18	200.0	195.0	152.67	163.02
	8-bit, 1024 pt, Quad Output, 2 Parallel FFT Engines, Burst, 4 Mults/2 Adders FFT function	4043	14	24	200.0	195.0	149.72	163.02
	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Burst, 3 Mults/5 Adders FFT function	7496	28	36	200.0	195.0	150.01	163.02
	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Burst, 4 Mults/2 Adders FFT function	6896	28	48	200.0	195.0	151.33	163.02
	8-bit, 1024 pt, Quad Output, 1 Parallel FFT Engine, Buffered Burst, 3 Mults/5 Adders FFT function	2934	18	9	235.07	195.0	148.89	163.02
	8-bit, 1024 pt, Quad Output, 1 Parallel FFT Engine, Buffered Burst, 4 Mults/2 Adders FFT function	2784	18	12	235.07	195.0	151.51	163.02
	8-bit, 1024 pt, Quad Output, 2 Parallel FFT Engines, Buffered Burst, 3 Mults/5 Adders FFT function	4720	30	18	200.0	195.0	149.76	163.02
	8-bit, 1024 pt, Quad Output, 2 Parallel FFT Engines, Buffered Burst, 4 Mults/2 Adders FFT function	4420	30	24	200.0	195.0	151.08	163.02

Table 5–15. Cyclone II Performance (Part 4 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
Larger Designs	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Buffered Burst, 3 Mults/5 Adders FFT function	8053	60	36	200.0	195.0	149.23	163.02
	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Buffered Burst, 4 Mults/2 Adders FFT function	7453	60	48	200.0	195.0	151.28	163.02

Notes to Table 5–15 :

(1) This application uses registered inputs and outputs.
(2) This application uses registered multiplier input and output stages within the DSP block.
(3) This application uses the same clock source for both A and B ports.
(4) This application uses independent clock sources for A and B ports.
(5) This application uses PLL clock outputs that are globally routed to connect and drive M4K clock ports. Use of non-PLL clock sources or local routing to drive M4K clock ports may result in lower performance numbers than shown here. Refer to the Quartus II timing report for actual performance numbers.
(6) These numbers are for commercial devices.
(7) These numbers are for automotive devices.

Internal Timing

Refer to Tables 5–16 through 5–19 for the internal timing parameters.

Table 5–16. LE_FF Internal Timing Microparameters (Part 1 of 2)

Parameter	–6 Speed Grade *(1)*		–7 Speed Grade *(2)*		–8 Speed Grade *(3)*		Unit
	Min	Max	Min	Max	Min	Max	
TSU	–36	—	–40	—	–40	—	ps
	—	—	–38	—	–40	—	ps
TH	266	—	306	—	306	—	ps
	—	—	286	—	306	—	ps
TCO	141	250	135	277	135	304	ps
	—	—	141	—	141	—	ps
TCLR	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps

Table 5–16. LE_FF Internal Timing Microparameters (Part 2 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TPRE	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps
TCLKL	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps
TCLKH	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps
tLUT	180	438	172	545	172	651	ps
	—	—	180	—	180	—	ps

Notes to Table 5–16:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Table 5–17. IOE Internal Timing Microparameters (Part 1 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TSU	76	—	101	—	101	—	ps
	—	—	89	—	101	—	ps
TH	88	—	106	—	106	—	ps
	—	—	97	—	106	—	ps
TCO	99	155	95	171	95	187	ps
	—	—	99	—	99	—	ps
TPIN2COMBOUT_R	384	762	366	784	366	855	ps
	—	—	384	—	384	—	ps
TPIN2COMBOUT_C	385	760	367	783	367	854	ps
	—	—	385	—	385	—	ps
TCOMBIN2PIN_R	1344	2490	1280	2689	1280	2887	ps
	—	—	1344	—	1344	—	ps

Table 5–17. IOE Internal Timing Microparameters (Part 2 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TCOMBIN2PIN_C	1418	2622	1352	2831	1352	3041	ps
	—	—	1418	—	1418	—	ps
TCLR	137	—	165	—	165	—	ps
	—	—	151	—	165	—	ps
TPRE	192	—	233	—	233	—	ps
	—	—	212	—	233	—	ps
TCLKL	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps
TCLKH	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps

Notes to Table 5–17:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Table 5–18. DSP Block Internal Timing Microparameters (Part 1 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TSU	47	—	62	—	62	—	ps
	—	—	54	—	62	—	ps
TH	110	—	113	—	113	—	ps
	—	—	111	—	113	—	ps
TCO	0	0	0	0	0	0	ps
	—	—	0	—	0	—	ps
TINREG2PIPE9	652	1379	621	1872	621	2441	ps
	—	—	652	—	652	—	ps
TINREG2PIPE18	652	1379	621	1872	621	2441	ps
	—	—	652	—	652	—	ps

Table 5–18. DSP Block Internal Timing Microparameters (Part 2 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TPIPE2OUTREG	47	104	45	142	45	185	ps
	—	—	47	—	47	—	ps
TPD9	529	2470	505	3353	505	4370	ps
	—	—	529	—	529	—	ps
TPD18	425	2903	406	3941	406	5136	ps
	—	—	425	—	425	—	ps
TCLR	2686	—	3572	—	3572	—	ps
	—	—	3129	—	3572	—	ps
TCLKL	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps
TCLKH	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps

Notes to Table 5–18:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Table 5–19. M4K Block Internal Timing Microparameters (Part 1 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KRC	2387	3764	2275	4248	2275	4736	ps
	—	—	2387	—	2387	—	ps
TM4KWERESU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KWEREH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KBESU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps

Table 5–19. M4K Block Internal Timing Microparameters (Part 2 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KBEH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATAASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATAAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KADDRASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KADDRAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATABSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATABH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KRADDRBSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KRADDRBH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATACO1	466	724	445	826	445	930	ps
	—	—	466	—	466	—	ps
TM4KDATACO2	2345	3680	2234	4157	2234	4636	ps
	—	—	2345	—	2345	—	ps
TM4KCLKH	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps
TM4KCLKL	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps

Table 5–19. M4K Block Internal Timing Microparameters (Part 3 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KCLR	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps

Notes to Table 5–19:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Cyclone II Clock Timing Parameters

Refer to Tables 5–20 through 5–34 for Cyclone II clock timing parameters.

Table 5–20. Cyclone II Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP2C5/A Clock Timing Parameters

Tables 5–21 and 5–22 show the clock timing parameters for EP2C5/A devices.

Table 5–21. EP2C5/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.283	1.343	2.329	2.484	2.688	2.688	ns
t_{COUT}	1.297	1.358	2.363	2.516	2.717	2.717	ns
t_{PLLCIN}	–0.188	–0.201	0.076	0.038	0.042	0.052	ns

Table 5–21. EP2C5/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.174	–0.186	0.11	0.07	0.071	0.081	ns

Notes to Table 5–21:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–22. EP2C5/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.212	1.267	2.210	2.351	2.54	2.540	ns
t_{COUT}	1.214	1.269	2.226	2.364	2.548	2.548	ns
t_{PLLCIN}	–0.259	–0.277	–0.043	–0.095	–0.106	–0.096	ns
$t_{PLLCOUT}$	–0.257	–0.275	–0.027	–0.082	–0.098	–0.088	ns

Notes to Table 5–22:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C8/A Clock Timing Parameters

Tables 5–23 and 5–24 show the clock timing parameters for EP2C8/A devices.

Table 5–23. EP2C8/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.339	1.404	2.405	2.565	2.764	2.774	ns
t_{COUT}	1.353	1.419	2.439	2.597	2.793	2.803	ns
t_{PLLCIN}	–0.193	–0.204	0.055	0.015	0.016	0.026	ns

Table 5–23. EP2C8/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.179	–0.189	0.089	0.047	0.045	0.055	ns

Notes to Table 5–23:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–24. EP2C8/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.256	1.314	2.270	2.416	2.596	2.606	ns
t_{COUT}	1.258	1.316	2.286	2.429	2.604	2.614	ns
t_{PLLCIN}	–0.276	–0.294	–0.08	–0.134	–0.152	–0.142	ns
$t_{PLLCOUT}$	–0.274	–0.292	–0.064	–0.121	–0.144	–0.134	ns

Notes to Table 5–24:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C15A Clock Timing Parameters

Tables 5–25 and 5–26 show the clock timing parameters for EP2C15A devices.

Table 5–25. EP2C15A Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.621	1.698	2.590	2.766	3.009	2.989	ns
t_{COUT}	1.635	1.713	2.624	2.798	3.038	3.018	ns
t_{PLLCIN}	–0.351	–0.372	0.045	0.008	0.046	0.016	ns

Table 5–25. EP2C15A Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.337	–0.357	0.079	0.04	0.075	0.045	ns

Notes to Table 5–25:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–26. EP2C15A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.542	1.615	2.490	2.651	2.886	2.866	ns
t_{COUT}	1.544	1.617	2.506	2.664	2.894	2.874	ns
t_{PLLCIN}	–0.424	–0.448	–0.057	–0.107	–0.077	–0.107	ns
$t_{PLLCOUT}$	–0.422	–0.446	–0.041	–0.094	–0.069	–0.099	ns

Notes to Table 5–26:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C20/A Clock Timing Parameters

Tables 5–27 and 5–28 show the clock timing parameters for EP2C20/A devices.

Table 5–27. EP2C20/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.621	1.698	2.590	2.766	3.009	2.989	ns
t_{COUT}	1.635	1.713	2.624	2.798	3.038	3.018	ns
t_{PLLCIN}	–0.351	–0.372	0.045	0.008	0.046	0.016	ns

Table 5–27. EP2C20/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.337	–0.357	0.079	0.04	0.075	0.045	ns

Notes to Table 5–27:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–28. EP2C20/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.542	1.615	2.490	2.651	2.886	2.866	ns
t_{COUT}	1.544	1.617	2.506	2.664	2.894	2.874	ns
t_{PLLCIN}	–0.424	–0.448	–0.057	–0.107	–0.077	–0.107	ns
$t_{PLLCOUT}$	–0.422	–0.446	–0.041	–0.094	–0.069	–0.099	ns

Notes to Table 5–28:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C35 Clock Timing Parameters

Tables 5–29 and 5–30 show the clock timing parameters for EP2C35 devices.

Table 5–29. EP2C35 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.499	1.569	2.652	2.878	3.155	ns
t_{COUT}	1.513	1.584	2.686	2.910	3.184	ns
t_{PLLCIN}	–0.026	–0.032	0.272	0.316	0.41	ns
$t_{PLLCOUT}$	–0.012	–0.017	0.306	0.348	0.439	ns

Table 5–30. EP2C35 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.410	1.476	2.514	2.724	2.986	ns
t_{COUT}	1.412	1.478	2.530	2.737	2.994	ns
t_{PLLCIN}	–0.117	–0.127	0.134	0.162	0.241	ns
$t_{PLLCOUT}$	–0.115	–0.125	0.15	0.175	0.249	ns

EP2C50 Clock Timing Parameters

Tables 5–31 and 5–32 show the clock timing parameters for EP2C50 devices.

Table 5–31. EP2C50 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.575	1.651	2.759	2.940	3.174	ns
t_{COUT}	1.589	1.666	2.793	2.972	3.203	ns
t_{PLLCIN}	–0.149	–0.158	0.113	0.075	0.089	ns
$t_{PLLCOUT}$	–0.135	–0.143	0.147	0.107	0.118	ns

Table 5–32. EP2C50 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.533	2.624	2.791	3.010	ns
t_{COUT}	1.465	1.535	2.640	2.804	3.018	ns
t_{PLLCIN}	–0.261	–0.276	–0.022	–0.074	–0.075	ns
$t_{PLLCOUT}$	–0.259	–0.274	–0.006	–0.061	–0.067	ns

EP2C70 Clock Timing Parameters

Tables 5–33 and 5–34 show the clock timing parameters for EP2C70 devices.

Table 5–33. EP2C70 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.575	1.651	2.914	3.105	3.174	ns
t_{COUT}	1.589	1.666	2.948	3.137	3.203	ns
t_{PLLCIN}	–0.149	–0.158	0.27	0.268	0.089	ns
$t_{PLLCOUT}$	–0.135	–0.143	0.304	0.3	0.118	ns

Table 5–34. EP2C70 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.533	2.753	2.927	3.010	ns
t_{COUT}	1.465	1.535	2.769	2.940	3.018	ns
t_{PLLCIN}	–0.261	–0.276	0.109	0.09	–0.075	ns
$t_{PLLCOUT}$	–0.259	–0.274	0.125	0.103	–0.067	ns

Clock Network Skew Adders

Table 5–35 shows the clock network specifications.

Table 5–35. Clock Network Specifications

Name	Description	Max	Unit
Clock skew adder EP2C5/A, EP2C8/A *(1)*	Inter-clock network, same bank	±88	ps
	Inter-clock network, same side and entire chip	±88	ps
Clock skew adder EP2C15A, EP2C20/A, EP2C35, EP2C50, EP2C70 *(1)*	Inter-clock network, same bank	±118	ps
	Inter-clock network, same side and entire chip	±138	ps

Note to Table 5–35:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

IOE Programmable Delay

Refer to Table 5–36 and 5–37 for IOE programmable delay.

Table 5–36. Cyclone II IOE Programmable Delay on Column Pins *Notes (1), (2)*

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade (4)		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad -> I/O dataout to core	7	0	2233	0	3827	0	4232	0	4349	ps
			0	2344	—	—	0	4088	—	—	ps
Input Delay from Pin to Input Register	Pad -> I/O input register	8	0	2656	0	4555	0	4914	0	4940	ps
			0	2788	—	—	0	4748	—	—	ps
Delay from Output Register to Output Pin	I/O output register -> Pad	2	0	303	0	563	0	638	0	670	ps
			0	318	—	—	0	617	—	—	ps

Notes to Table 5–36:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.

(3) The value in the first row for each parameter represents the fast corner timing parameter for industrial and automotive devices. The second row represents the fast corner timing parameter for commercial devices.

(4) The value in the first row is for automotive devices. The second row is for commercial devices.

Table 5–37. Cyclone II IOE Programmable Delay on Row Pins *Notes (1), (2)* ***(Part 1 of 2)***

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade (4)		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad -> I/O dataout to core	7	0	2240	0	3776	0	4174	0	4290	ps
			0	2352	—	—	0	4033	—	—	ps

Table 5–37. Cyclone II IOE Programmable Delay on Row Pins Notes (1), (2) (Part 2 of 2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade (4)		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Input Register	Pad -> I/O input register	8	0	2669	0	4482	0	4834	0	4859	ps
			0	2802	—	—	0	4671	—	—	ps
Delay from Output Register to Output Pin	I/O output register -> Pad	2	0	308	0	572	0	648	0	682	ps
			0	324	—	—	0	626	—	—	ps

Notes to Table 5–37 :

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.

(3) The value in the first row represents the fast corner timing parameter for industrial and automotive devices. The second row represents the fast corner timing parameter for commercial devices.

(4) The value in the first row is for automotive devices. The second row is for commercial devices.

Default Capacitive Loading of Different I/O Standards

Refer to Table 5–38 for default capacitive loading of different I/O standards.

Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 1 of 2)

I/O Standard	Capacitive Load	Unit
LVTTL	0	pF
LVCMOS	0	pF
2.5V	0	pF
1.8V	0	pF
1.5V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL_2_CLASS_I	0	pF
SSTL_2_CLASS_II	0	pF
SSTL_18_CLASS_I	0	pF

Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 2 of 2)

I/O Standard	Capacitive Load	Unit
SSTL_18_CLASS_II	0	pF
1.5V_HSTL_CLASS_I	0	pF
1.5V_HSTL_CLASS_II	0	pF
1.8V_HSTL_CLASS_I	0	pF
1.8V_HSTL_CLASS_II	0	pF
DIFFERENTIAL_SSTL_2_CLASS_I	0	pF
DIFFERENTIAL_SSTL_2_CLASS_II	0	pF
DIFFERENTIAL_SSTL_18_CLASS_I	0	pF
DIFFERENTIAL_SSTL_18_CLASS_II	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
LVDS	0	pF
1.2V_HSTL	0	pF
1.2V_DIFFERENTIAL_HSTL	0	pF

I/O Delays

Refer to Tables 5–39 through 5–43 for I/O delays.

Table 5–39. I/O Delay Parameters

Symbol	Parameter
t_{DIP}	Delay from I/O datain to output pad
t_{OP}	Delay from I/O output register to output pad
t_{PCOUT}	Delay from input pad to I/O dataout to core
t_{PI}	Delay from input pad to I/O input register

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 1 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
LVTTL	t_{PI}	581	609	1222	1228	1282	1282	ps
	t_{PCOUT}	367	385	760	783	854	854	ps
2.5V	t_{PI}	624	654	1192	1238	1283	1283	ps
	t_{PCOUT}	410	430	730	793	855	855	ps
1.8V	t_{PI}	725	760	1372	1428	1484	1484	ps
	t_{PCOUT}	511	536	910	983	1056	1056	ps
1.5V	t_{PI}	790	828	1439	1497	1556	1556	ps
	t_{PCOUT}	576	604	977	1052	1128	1128	ps
LVCMOS	t_{PI}	581	609	1222	1228	1282	1282	ps
	t_{PCOUT}	367	385	760	783	854	854	ps
SSTL_2_CLASS_I	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
SSTL_2_CLASS_II	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
SSTL_18_CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
SSTL_18_CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 2 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
1.5V_HSTL_CLASS_I	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
1.5V_HSTL_CLASS_II	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
1.8V_HSTL_CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.8V_HSTL_CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
DIFFERENTIAL_SSTL_2_ CLASS_I	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
DIFFERENTIAL_SSTL_2_ CLASS_II	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
DIFFERENTIAL_SSTL_18_ CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
DIFFERENTIAL_SSTL_18_ CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
LVDS	t_{PI}	623	653	1072	1075	1078	1078	ps
	t_{PCOUT}	409	429	610	630	650	650	ps
1.2V_HSTL	t_{PI}	570	597	1263	1324	1385	1385	ps
	t_{PCOUT}	356	373	801	879	957	957	ps

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 3 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
1.2V_DIFFERENTIAL_HSTL	t_{PI}	570	597	1263	1324	1385	1385	ps
	t_{PCOUT}	356	373	801	879	957	957	ps

Notes to Table 5–40 :
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–41. Cyclone II I/O Input Delay for Row Pins (Part 1 of 2)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
LVTTL	t_{PI}	583	611	1129	1160	1240	1240	ps
	t_{PCOUT}	366	384	762	784	855	855	ps
2.5V	t_{PI}	629	659	1099	1171	1244	1244	ps
	t_{PCOUT}	412	432	732	795	859	859	ps
1.8V	t_{PI}	729	764	1278	1360	1443	1443	ps
	t_{PCOUT}	512	537	911	984	1058	1058	ps
1.5V	t_{PI}	794	832	1345	1429	1513	1513	ps
	t_{PCOUT}	577	605	978	1053	1128	1128	ps
LVCMOS	t_{PI}	583	611	1129	1160	1240	1240	ps
	t_{PCOUT}	366	384	762	784	855	855	ps
SSTL_2_CLASS_I	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
SSTL_2_CLASS_II	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
SSTL_18_CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
SSTL_18_CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.5V_HSTL_CLASS_I	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps

Table 5–41. Cyclone II I/O Input Delay for Row Pins (Part 2 of 2)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
1.5V_HSTL_CLASS_II	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
1.8V_HSTL_CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_HSTL_CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
DIFFERENTIAL_SSTL_2_ CLASS_I	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
DIFFERENTIAL_SSTL_2_ CLASS_II	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
DIFFERENTIAL_SSTL_18_ CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
DIFFERENTIAL_SSTL_18_ CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
LVDS	t_{PI}	651	682	1036	1075	1113	1113	ps
	t_{PCOUT}	434	455	669	699	728	728	ps
PCI	t_{PI}	595	623	1113	1156	1232	1232	ps
	t_{PCOUT}	378	396	746	780	847	847	ps
PCI-X	t_{PI}	595	623	1113	1156	1232	1232	ps
	t_{PCOUT}	378	396	746	780	847	847	ps

Notes to Table 5–41 :

(1) These numbers are for commercial devices.

(2) These numbers are for automotive devices.

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 1 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
LVTTL	4 mA	t_{OP}	1524	1599	2903	3125	3341	3348	ps
		t_{DIP}	1656	1738	3073	3319	3567	3567	ps
	8 mA	t_{OP}	1343	1409	2670	2866	3054	3061	ps
		t_{DIP}	1475	1548	2840	3060	3280	3280	ps
	12 mA	t_{OP}	1287	1350	2547	2735	2917	2924	ps
		t_{DIP}	1419	1489	2717	2929	3143	3143	ps
	16 mA	t_{OP}	1239	1299	2478	2665	2844	2851	ps
		t_{DIP}	1371	1438	2648	2859	3070	3070	ps
	20 mA	t_{OP}	1228	1288	2456	2641	2820	2827	ps
		t_{DIP}	1360	1427	2626	2835	3046	3046	ps
	24 mA (1)	t_{OP}	1220	1279	2452	2637	2815	2822	ps
		t_{DIP}	1352	1418	2622	2831	3041	3041	ps
LVCMOS	4 mA	t_{OP}	1346	1412	2509	2695	2873	2880	ps
		t_{DIP}	1478	1551	2679	2889	3099	3099	ps
	8 mA	t_{OP}	1240	1300	2473	2660	2840	2847	ps
		t_{DIP}	1372	1439	2643	2854	3066	3066	ps
	12 mA	t_{OP}	1221	1280	2428	2613	2790	2797	ps
		t_{DIP}	1353	1419	2598	2807	3016	3016	ps
	16 mA	t_{OP}	1203	1262	2403	2587	2765	2772	ps
		t_{DIP}	1335	1401	2573	2781	2991	2991	ps
	20 mA	t_{OP}	1194	1252	2378	2562	2738	2745	ps
		t_{DIP}	1326	1391	2548	2756	2964	2964	ps
	24 mA (1)	t_{OP}	1192	1250	2382	2566	2742	2749	ps
		t_{DIP}	1324	1389	2552	2760	2968	2968	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 2 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
2.5V	4 mA	t_{OP}	1208	1267	2478	2614	2743	2750	ps
		t_{DIP}	1340	1406	2648	2808	2969	2969	ps
	8 mA	t_{OP}	1190	1248	2307	2434	2554	2561	ps
		t_{DIP}	1322	1387	2477	2628	2780	2780	ps
	12 mA	t_{OP}	1154	1210	2192	2314	2430	2437	ps
		t_{DIP}	1286	1349	2362	2508	2656	2656	ps
	16 mA (1)	t_{OP}	1140	1195	2152	2263	2375	2382	ps
		t_{DIP}	1272	1334	2322	2457	2601	2601	ps
1.8V	2 mA	t_{OP}	1682	1765	3988	4279	4563	4570	ps
		t_{DIP}	1814	1904	4158	4473	4789	4789	ps
	4 mA	t_{OP}	1567	1644	3301	3538	3768	3775	ps
		t_{DIP}	1699	1783	3471	3732	3994	3994	ps
	6 mA	t_{OP}	1475	1547	2993	3195	3391	3398	ps
		t_{DIP}	1607	1686	3163	3389	3617	3617	ps
	8 mA	t_{OP}	1451	1522	2882	3074	3259	3266	ps
		t_{DIP}	1583	1661	3052	3268	3485	3485	ps
	10 mA	t_{OP}	1438	1508	2853	3041	3223	3230	ps
		t_{DIP}	1570	1647	3023	3235	3449	3449	ps
	12 mA (1)	t_{OP}	1438	1508	2853	3041	3223	3230	ps
		t_{DIP}	1570	1647	3023	3235	3449	3449	ps
1.5V	2 mA	t_{OP}	2083	2186	4477	4870	5256	5263	ps
		t_{DIP}	2215	2325	4647	5064	5482	5482	ps
	4 mA	t_{OP}	1793	1881	3649	3965	4274	4281	ps
		t_{DIP}	1925	2020	3819	4159	4500	4500	ps
	6 mA	t_{OP}	1770	1857	3527	3823	4112	4119	ps
		t_{DIP}	1902	1996	3697	4017	4338	4338	ps
	8 mA (1)	t_{OP}	1703	1787	3537	3827	4111	4118	ps
		t_{DIP}	1835	1926	3707	4021	4337	4337	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 3 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
SSTL_2_ CLASS_I	8 mA	t_{OP}	1196	1254	2388	2516	2638	2645	ps
		t_{DIP}	1328	1393	2558	2710	2864	2864	ps
	12 mA (1)	t_{OP}	1174	1231	2277	2401	2518	2525	ps
		t_{DIP}	1306	1370	2447	2595	2744	2744	ps
SSTL_2_ CLASS_II	16 mA	t_{OP}	1158	1214	2245	2365	2479	2486	ps
		t_{DIP}	1290	1353	2415	2559	2705	2705	ps
	20 mA	t_{OP}	1152	1208	2231	2351	2464	2471	ps
		t_{DIP}	1284	1347	2401	2545	2690	2690	ps
	24 mA (1)	t_{OP}	1152	1208	2225	2345	2458	2465	ps
		t_{DIP}	1284	1347	2395	2539	2684	2684	ps
SSTL_18_ CLASS_I	6 mA	t_{OP}	1472	1544	3140	3345	3542	3549	ps
		t_{DIP}	1604	1683	3310	3539	3768	3768	ps
	8 mA	t_{OP}	1469	1541	3086	3287	3482	3489	ps
		t_{DIP}	1601	1680	3256	3481	3708	3708	ps
	10 mA	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
	12 mA (1)	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
SSTL_18_ CLASS_II	16 mA	t_{OP}	1454	1525	2905	3088	3263	3270	ps
		t_{DIP}	1586	1664	3075	3282	3489	3489	ps
	18 mA (1)	t_{OP}	1453	1524	2900	3082	3257	3264	ps
		t_{DIP}	1585	1663	3070	3276	3483	3483	ps
1.8V_HSTL_ CLASS_I	8 mA	t_{OP}	1460	1531	3222	3424	3618	3625	ps
		t_{DIP}	1592	1670	3392	3618	3844	3844	ps
	10 mA	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
	12 mA (1)	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 4 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
1.8V_HSTL_ CLASS_II	16 mA	t_{OP}	1449	1520	2936	3107	3271	3278	ps
		t_{DIP}	1581	1659	3106	3301	3497	3497	ps
	18 mA	t_{OP}	1450	1521	2924	3101	3272	3279	ps
		t_{DIP}	1582	1660	3094	3295	3498	3498	ps
	20 mA (1)	t_{OP}	1452	1523	2926	3096	3259	3266	ps
		t_{DIP}	1584	1662	3096	3290	3485	3485	ps
1.5V_HSTL_ CLASS_I	8 mA	t_{OP}	1779	1866	4292	4637	4974	4981	ps
		t_{DIP}	1911	2005	4462	4831	5200	5200	ps
	10 mA	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
	12 mA (1)	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
1.5V_HSTL_ CLASS_II	16 mA (1)	t_{OP}	1750	1836	3844	4125	4399	4406	ps
		t_{DIP}	1882	1975	4014	4319	4625	4625	ps
DIFFERENTIAL_ SSTL_2_CLASS_I	8 mA	t_{OP}	1196	1254	2388	2516	2638	2645	ps
		t_{DIP}	1328	1393	2558	2710	2864	2864	ps
	12 mA (1)	t_{OP}	1174	1231	2277	2401	2518	2525	ps
		t_{DIP}	1306	1370	2447	2595	2744	2744	ps
DIFFERENTIAL_ SSTL_2_CLASS_II	16 mA	t_{OP}	1158	1214	2245	2365	2479	2486	ps
		t_{DIP}	1290	1353	2415	2559	2705	2705	ps
	20 mA	t_{OP}	1152	1208	2231	2351	2464	2471	ps
		t_{DIP}	1284	1347	2401	2545	2690	2690	ps
	24 mA (1)	t_{OP}	1152	1208	2225	2345	2458	2465	ps
		t_{DIP}	1284	1347	2395	2539	2684	2684	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 5 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
DIFFERENTIAL_ SSTL_18_CLASS_I	6 mA	t_{OP}	1472	1544	3140	3345	3542	3549	ps
		t_{DIP}	1604	1683	3310	3539	3768	3768	ps
	8 mA	t_{OP}	1469	1541	3086	3287	3482	3489	ps
		t_{DIP}	1601	1680	3256	3481	3708	3708	ps
	10 mA	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
	12 mA (1)	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
DIFFERENTIAL_ SSTL_18_CLASS_II	16 mA	t_{OP}	1454	1525	2905	3088	3263	3270	ps
		t_{DIP}	1586	1664	3075	3282	3489	3489	ps
	18 mA (1)	t_{OP}	1453	1524	2900	3082	3257	3264	ps
		t_{DIP}	1585	1663	3070	3276	3483	3483	ps
1.8V_DIFFERENTIAL _HSTL_CLASS_I	8 mA	t_{OP}	1460	1531	3222	3424	3618	3625	ps
		t_{DIP}	1592	1670	3392	3618	3844	3844	ps
	10 mA	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
	12 mA (1)	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
1.8V_DIFFERENTIAL _HSTL_CLASS_II	16 mA	t_{OP}	1449	1520	2936	3107	3271	3278	ps
		t_{DIP}	1581	1659	3106	3301	3497	3497	ps
	18 mA	t_{OP}	1450	1521	2924	3101	3272	3279	ps
		t_{DIP}	1582	1660	3094	3295	3498	3498	ps
	20 mA (1)	t_{OP}	1452	1523	2926	3096	3259	3266	ps
		t_{DIP}	1584	1662	3096	3290	3485	3485	ps
1.5V_DIFFERENTIAL _HSTL_CLASS_I	8 mA	t_{OP}	1779	1866	4292	4637	4974	4981	ps
		t_{DIP}	1911	2005	4462	4831	5200	5200	ps
	10 mA	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
	12 mA (1)	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 6 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
1.5V_DIFFERENTIAL _HSTL_CLASS_II	16 mA (1)	t_{OP}	1750	1836	3844	4125	4399	4406	ps
		t_{DIP}	1882	1975	4014	4319	4625	4625	ps
LVDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
RSDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
MINI_LVDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
SIMPLE_RSDS	—	t_{OP}	1221	1280	2258	2435	2605	2612	ps
		t_{DIP}	1353	1419	2428	2629	2831	2831	ps
1.2V_HSTL	—	t_{OP}	2403	2522	4635	5344	6046	6053	ps
		t_{DIP}	2535	2661	4805	5538	6272	6272	ps
1.2V_DIFFERENTIAL _HSTL	—	t_{OP}	2403	2522	4635	5344	6046	6053	ps
		t_{DIP}	2535	2661	4805	5538	6272	6272	ps

Notes to Table 5–42:

(1) This is the default setting in the Quartus II software.
(2) These numbers are for commercial devices.
(3) These numbers are for automotive devices.

Table 5–43. Cyclone II I/O Output Delay for Row Pins (Part 1 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial /Auto-motive	Commer-cial					
LVTTL	4 mA	t_{OP}	1343	1408	2539	2694	2885	2891	ps
		t_{DIP}	1467	1540	2747	2931	3158	3158	ps
	8 mA	t_{OP}	1198	1256	2411	2587	2756	2762	ps
		t_{DIP}	1322	1388	2619	2824	3029	3029	ps
	12 mA	t_{OP}	1156	1212	2282	2452	2614	2620	ps
		t_{DIP}	1280	1344	2490	2689	2887	2887	ps
	16 mA	t_{OP}	1124	1178	2286	2455	2618	2624	ps
		t_{DIP}	1248	1310	2494	2692	2891	2891	ps
	20 mA	t_{OP}	1112	1165	2245	2413	2574	2580	ps
		t_{DIP}	1236	1297	2453	2650	2847	2847	ps
	24 mA (1)	t_{OP}	1105	1158	2253	2422	2583	2589	ps
		t_{DIP}	1229	1290	2461	2659	2856	2856	ps
LVCMOS	4 mA	t_{OP}	1200	1258	2231	2396	2555	2561	ps
		t_{DIP}	1324	1390	2439	2633	2828	2828	ps
	8 mA	t_{OP}	1125	1179	2260	2429	2591	2597	ps
		t_{DIP}	1249	1311	2468	2666	2864	2864	ps
	12 mA (1)	t_{OP}	1106	1159	2217	2383	2543	2549	ps
		t_{DIP}	1230	1291	2425	2620	2816	2816	ps
2.5V	4 mA	t_{OP}	1126	1180	2350	2477	2598	2604	ps
		t_{DIP}	1250	1312	2558	2714	2871	2871	ps
	8 mA (1)	t_{OP}	1105	1158	2177	2296	2409	2415	ps
		t_{DIP}	1229	1290	2385	2533	2682	2682	ps

Table 5–43. Cyclone II I/O Output Delay for Row Pins (Part 2 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial /Auto-motive	Commer-cial					
1.8V	2 mA	t_{OP}	1503	1576	3657	3927	4190	4196	ps
		t_{DIP}	1627	1708	3865	4164	4463	4463	ps
	4 mA	t_{OP}	1400	1468	3010	3226	3434	3440	ps
		t_{DIP}	1524	1600	3218	3463	3707	3707	ps
	6 mA	t_{OP}	1388	1455	2857	3050	3236	3242	ps
		t_{DIP}	1512	1587	3065	3287	3509	3509	ps
	8 mA	t_{OP}	1347	1412	2714	2897	3072	3078	ps
		t_{DIP}	1471	1544	2922	3134	3345	3345	ps
	10 mA	t_{OP}	1347	1412	2714	2897	3072	3078	ps
		t_{DIP}	1471	1544	2922	3134	3345	3345	ps
	12 mA (1)	t_{OP}	1332	1396	2678	2856	3028	3034	ps
		t_{DIP}	1456	1528	2886	3093	3301	3301	ps
1.5V	2 mA	t_{OP}	1853	1943	4127	4492	4849	4855	ps
		t_{DIP}	1977	2075	4335	4729	5122	5122	ps
	4 mA	t_{OP}	1694	1776	3452	3747	4036	4042	ps
		t_{DIP}	1818	1908	3660	3984	4309	4309	ps
	6 mA (1)	t_{OP}	1694	1776	3452	3747	4036	4042	ps
		t_{DIP}	1818	1908	3660	3984	4309	4309	ps
SSTL_2_ CLASS_I	8 mA	t_{OP}	1090	1142	2152	2268	2376	2382	ps
		t_{DIP}	1214	1274	2360	2505	2649	2649	ps
	12 mA (1)	t_{OP}	1097	1150	2131	2246	2354	2360	ps
		t_{DIP}	1221	1282	2339	2483	2627	2627	ps
SSTL_2_ CLASS_II	16 mA (1)	t_{OP}	1068	1119	2067	2177	2281	2287	ps
		t_{DIP}	1192	1251	2275	2414	2554	2554	ps
SSTL_18_ CLASS_I	6 mA	t_{OP}	1371	1437	2828	3018	3200	3206	ps
		t_{DIP}	1495	1569	3036	3255	3473	3473	ps
	8 mA	t_{OP}	1365	1431	2832	3024	3209	3215	ps
		t_{DIP}	1489	1563	3040	3261	3482	3482	ps
	10 mA (1)	t_{OP}	1374	1440	2806	2990	3167	3173	ps
		t_{DIP}	1498	1572	3014	3227	3440	3440	ps

Table 5–43. Cyclone II I/O Output Delay for Row Pins (Part 3 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial /Auto-motive	Commer-cial					
1.8V_HSTL_ CLASS_I	8 mA	t_{OP}	1364	1430	2853	3017	3178	3184	ps
		t_{DIP}	1488	1562	3061	3254	3451	3451	ps
	10 mA	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
	12 mA (1)	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
1.5V_HSTL_ CLASS_I	8 mA (1)	t_{OP}	1657	1738	3642	3917	4185	4191	ps
		t_{DIP}	1781	1870	3850	4154	4458	4458	ps
DIFFERENTIAL_ SSTL_2_ CLASS_I	8 mA	t_{OP}	1090	1142	2152	2268	2376	2382	ps
		t_{DIP}	1214	1274	2360	2505	2649	2649	ps
	12 mA (1)	t_{OP}	1097	1150	2131	2246	2354	2360	ps
		t_{DIP}	1221	1282	2339	2483	2627	2627	ps
DIFFERENTIAL_ SSTL_2_ CLASS_II	16 mA (1)	t_{OP}	1068	1119	2067	2177	2281	2287	ps
		t_{DIP}	1192	1251	2275	2414	2554	2554	ps
DIFFERENTIAL_ SSTL_18_ CLASS_I	6 mA	t_{OP}	1371	1437	2828	3018	3200	3206	ps
		t_{DIP}	1495	1569	3036	3255	3473	3473	ps
	8 mA	t_{OP}	1365	1431	2832	3024	3209	3215	ps
		t_{DIP}	1489	1563	3040	3261	3482	3482	ps
	10 mA (1)	t_{OP}	1374	1440	2806	2990	3167	3173	ps
		t_{DIP}	1498	1572	3014	3227	3440	3440	ps
1.8V_ DIFFERENTIAL_ HSTL_ CLASS_I	8 mA	t_{OP}	1364	1430	2853	3017	3178	3184	ps
		t_{DIP}	1488	1562	3061	3254	3451	3451	ps
	10 mA	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
	12 mA (1)	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
1.5V_ DIFFERENTIAL_ HSTL_ CLASS_I	8 mA (1)	t_{OP}	1657	1738	3642	3917	4185	4191	ps
		t_{DIP}	1781	1870	3850	4154	4458	4458	ps

Table 5–43. Cyclone II I/O Output Delay for Row Pins (Part 4 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial /Auto-motive	Commer-cial					
LVDS	—	t_{OP}	1216	1275	2089	2184	2272	2278	ps
		t_{DIP}	1340	1407	2297	2421	2545	2545	ps
RSDS	—	t_{OP}	1216	1275	2089	2184	2272	2278	ps
		t_{DIP}	1340	1407	2297	2421	2545	2545	ps
MINI_LVDS	—	t_{OP}	1216	1275	2089	2184	2272	2278	ps
		t_{DIP}	1340	1407	2297	2421	2545	2545	ps
PCI	—	t_{OP}	989	1036	2070	2214	2352	2358	ps
		t_{DIP}	1113	1168	2278	2451	2625	2625	ps
PCI-X	—	t_{OP}	989	1036	2070	2214	2352	2358	ps
		t_{DIP}	1113	1168	2278	2451	2625	2625	ps

Notes to Table 5–43:
(1) This is the default setting in the Quartus II software.
(2) These numbers are for commercial devices.
(3) These numbers are for automotive devices.

Maximum Input and Output Clock Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Table 5–44 specifies the maximum input clock toggle rates. Table 5–45 specifies the maximum output clock toggle rates at default load. Table 5–46 specifies the derating factors for the output clock toggle rate for non-default load.

To calculate the output toggle rate for a non-default load, use this formula:

The toggle rate for a non-default load

= 1000 / (1000/toggle rate at default load + derating factor * load value in pF/1000)

For example, the output toggle rate at 0 pF (default) load for SSTL-18 Class II 18mA I/O standard is 270 MHz on a –6 device column I/O pin. The derating factor is 29 ps/pF. For a 10pF load, the toggle rate is calculated as:

1000 / (1000/270 + 29 × 10/1000) = 250 (MHz)

Tables 5–44 through 5–46 show the I/O toggle rates for Cyclone II devices.

Table 5–44. Maximum Input Clock Toggle Rate on Cyclone II Devices (Part 1 of 2)

I/O Standard	Maximum Input Clock Toggle Rate on Cyclone II Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVTTL	450	405	360	450	405	360	420	380	340
2.5V	450	405	360	450	405	360	450	405	360
1.8V	450	405	360	450	405	360	450	405	360
1.5V	300	270	240	300	270	240	300	270	240
LVCMOS	450	405	360	450	405	360	420	380	340
SSTL_2_CLASS_I	500	500	500	500	500	500	500	500	500
SSTL_2_CLASS_II	500	500	500	500	500	500	500	500	500
SSTL_18_CLASS_I	500	500	500	500	500	500	500	500	500
SSTL_18_CLASS_II	500	500	500	500	500	500	500	500	500
1.5V_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.5V_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
1.8V_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.8V_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
PCI	—	—	—	350	315	280	350	315	280
PCI-X	—	—	—	350	315	280	350	315	280
DIFFERENTIAL_SSTL_2_CLASS_I	500	500	500	500	500	500	500	500	500
DIFFERENTIAL_SSTL_2_CLASS_II	500	500	500	500	500	500	500	500	500

Table 5–44. Maximum Input Clock Toggle Rate on Cyclone II Devices (Part 2 of 2)

I/O Standard	Maximum Input Clock Toggle Rate on Cyclone II Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
DIFFERENTIAL_SSTL_18_CLASS_I	500	500	500	500	500	500	500	500	500
DIFFERENTIAL_SSTL_18_CLASS_II	500	500	500	500	500	500	500	500	500
1.8V_DIFFERENTIAL_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.8V_DIFFERENTIAL_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
1.5V_DIFFERENTIAL_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.5V_DIFFERENTIAL_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
LVPECL	—	—	—	—	—	—	402	402	402
LVDS	402	402	402	402	402	402	402	402	402
1.2V_HSTL	110	90	80	—	—	—	110	90	80
1.2V_DIFFERENTIAL_HSTL	110	90	80	—	—	—	110	90	80

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 1 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVTTL	4 mA	120	100	80	120	100	80	120	100	80
	8 mA	200	170	140	200	170	140	200	170	140
	12 mA	280	230	190	280	230	190	280	230	190
	16 mA	290	240	200	290	240	200	290	240	200
	20 mA	330	280	230	330	280	230	330	280	230
	24 mA	360	300	250	360	300	250	360	300	250

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 2 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVCMOS	4 mA	250	210	170	250	210	170	250	210	170
	8 mA	280	230	190	280	230	190	280	230	190
	12 mA	310	260	210	310	260	210	310	260	210
	16 mA	320	270	220	—	—	—	—	—	—
	20 mA	350	290	240	—	—	—	—	—	—
	24 mA	370	310	250	—	—	—	—	—	—
2.5V	4 mA	180	150	120	180	150	120	180	150	120
	8 mA	280	230	190	280	230	190	280	230	190
	12 mA	440	370	300	—	—	—	—	—	—
	16 mA	450	405	350	—	—	—	—	—	—
1.8V	2 mA	120	100	80	120	100	80	120	100	80
	4 mA	180	150	120	180	150	120	180	150	120
	6 mA	220	180	150	220	180	150	220	180	150
	8 mA	240	200	160	240	200	160	240	200	160
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	350	290	240	350	290	240	350	290	240
1.5V	2 mA	80	60	50	80	60	50	80	60	50
	4 mA	130	110	90	130	110	90	130	110	90
	6 mA	180	150	120	180	150	120	180	150	120
	8 mA	230	190	160	—	—	—	—	—	—
SSTL_2_CLASS_I	8 mA	400	340	280	400	340	280	400	340	280
	12 mA	400	340	280	400	340	280	400	340	280
SSTL_2_CLASS_II	16 mA	350	290	240	350	290	240	350	290	240
	20 mA	400	340	280	—	—	—	—	—	—
	24 mA	400	340	280	—	—	—	—	—	—
SSTL_18_CLASS_I	6 mA	260	220	180	260	220	180	260	220	180
	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	270	220	180	270	220	180	270	220	180
	12 mA	280	230	190	—	—	—	—	—	—

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 3 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
SSTL_18_ CLASS_II	16 mA	260	220	180	—	—	—	—	—	—
	18 mA	270	220	180	—	—	—	—	—	—
1.8V_HSTL_ CLASS_I	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	320	270	220	320	270	220	320	270	220
1.8V_HSTL_ CLASS_II	16 mA	230	190	160	—	—	—	—	—	—
	18 mA	240	200	160	—	—	—	—	—	—
	20 mA	250	210	170	—	—	—	—	—	—
1.5V_HSTL_ CLASS_I	8 mA	210	170	140	210	170	140	210	170	140
	10 mA	220	180	150	—	—	—	—	—	—
	12 mA	230	190	160	—	—	—	—	—	—
1.5V_HSTL_ CLASS_II	16 mA	210	170	140	—	—	—	—	—	—
DIFFERENTIAL_ SSTL_2_CLASS_I	8 mA	400	340	280	400	340	280	400	340	280
	12 mA	400	340	280	400	340	280	400	340	280
DIFFERENTIAL_ SSTL_2_CLASS_II	16 mA	350	290	240	350	290	240	350	290	240
	20 mA	400	340	280	—	—	—	—	—	—
	24 mA	400	340	280	—	—	—	—	—	—
DIFFERENTIAL_ SSTL_18_CLASS_I	6 mA	260	220	180	260	220	180	260	220	180
	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	270	220	180	270	220	180	270	220	180
	12 mA	280	230	190	—	—	—	—	—	—
DIFFERENTIAL_SSTL _18_CLASS_II	16 mA	260	220	180	—	—	—	—	—	—
	18 mA	270	220	180	—	—	—	—	—	—
1.8V_ DIFFERENTIAL_HSTL _CLASS_I	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	320	270	220	320	270	220	320	270	220
1.8V_ DIFFERENTIAL_HSTL _CLASS_II	16 mA	230	190	160	—	—	—	—	—	—
	18 mA	240	200	160	—	—	—	—	—	—
	20 mA	250	210	170	—	—	—	—	—	—

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 4 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.5V_ DIFFERENTIAL_HSTL _CLASS_I	8 mA	210	170	140	210	170	140	210	170	140
	10 mA	220	180	150	—	—	—	—	—	—
	12 mA	230	190	160	—	—	—	—	—	—
1.5V_ DIFFERENTIAL_HSTL _CLASS_II	16 mA	210	170	140	—	—	—	—	—	—
LVDS	—	400	340	280	400	340	280	400	340	280
RSDS	—	400	340	280	400	340	280	400	340	280
MINI_LVDS	—	400	340	280	400	340	280	400	340	280
SIMPLE_RSDS	—	380	320	260	380	320	260	380	320	260
1.2V_HSTL	—	80	80	80	—	—	—	—	—	—
1.2V_ DIFFERENTIAL_HSTL	—	80	80	80	—	—	—	—	—	—
PCI	—	—	—	—	350	315	280	350	315	280
PCI-X	—	—	—	—	350	315	280	350	315	280
LVTTL	OCT_25_ OHMS	360	300	250	360	300	250	360	300	250
LVCMOS	OCT_25_ OHMS	360	300	250	360	300	250	360	300	250
2.5V	OCT_50_ OHMS	240	200	160	240	200	160	240	200	160
1.8V	OCT_50_ OHMS	290	240	200	290	240	200	290	240	200
SSTL_2_CLASS_I	OCT_50_ OHMS	240	200	160	240	200	160	—	—	—
SSTL_18_CLASS_I	OCT_50_ OHMS	290	240	200	290	240	200	—	—	—

Note to Table 5–45:
(1) This is based on single data rate I/Os.

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 1 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVTTL	4 mA	438	439	439	338	362	387	338	362	387
	8 mA	306	321	336	267	283	299	267	283	299
	12 mA	139	179	220	193	198	202	193	198	202
	16 mA	145	158	172	139	147	156	139	147	156
	20 mA	65	77	90	74	79	84	74	79	84
	24 mA	19	20	21	14	18	22	14	18	22
LVCMOS	4 mA	298	305	313	197	205	214	197	205	214
	8 mA	190	205	219	112	118	125	112	118	125
	12 mA	43	72	101	27	31	35	27	31	35
	16 mA	87	99	110	—	—	—	—	—	—
	20 mA	36	46	56	—	—	—	—	—	—
	24 mA	24	25	27	—	—	—	—	—	—
2.5V	4 mA	228	233	237	270	306	343	270	306	343
	8 mA	173	177	180	191	199	208	191	199	208
	12 mA	119	121	123	—	—	—	—	—	—
	16 mA	64	65	66	—	—	—	—	—	—
1.8V	2 mA	452	457	461	332	367	403	332	367	403
	4 mA	321	347	373	244	291	337	244	291	337
	6 mA	227	255	283	178	222	266	178	222	266
	8 mA	37	118	199	58	133	207	58	133	207
	10 mA	41	72	103	46	85	123	46	85	123
	12 mA	7	8	10	13	28	44	13	28	44
1.5V	2 mA	738	764	789	540	604	669	540	604	669
	4 mA	499	518	536	300	354	408	300	354	408
	6 mA	261	271	282	60	103	146	60	103	146
	8 mA	22	25	29	—	—	—	—	—	—
SSTL_2_CLASS_I	8 mA	46	47	49	25	40	56	25	40	56
	12 mA	67	69	70	23	42	60	23	42	60

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
SSTL_2_CLASS_II	16 mA	42	43	45	15	29	42	15	29	42
	20 mA	41	42	44	—	—	—	—	—	—
	24 mA	40	42	43	—	—	—	—	—	—
SSTL_18_ CLASS_I	6 mA	20	22	24	46	47	49	46	47	49
	8 mA	20	22	24	47	49	51	47	49	51
	10 mA	20	22	25	23	25	27	23	25	27
	12 mA	19	23	26	—	—	—	—	—	—
SSTL_18_ CLASS_II	16 mA	30	33	36	—	—	—	—	—	—
	18 mA	29	29	29	—	—	—	—	—	—
1.8V_HSTL_ CLASS_I	8 mA	26	28	29	59	61	63	59	61	63
	10 mA	46	47	48	65	66	68	65	66	68
	12 mA	67	67	67	71	71	72	71	71	72
1.8V_HSTL_ CLASS_II	16 mA	62	65	68	—	—	—	—	—	—
	18 mA	59	62	65	—	—	—	—	—	—
	20 mA	57	59	62	—	—	—	—	—	—
1.5V_HSTL_ CLASS_I	8 mA	40	40	41	28	32	36	28	32	36
	10 mA	41	42	42	—	—	—	—	—	—
	12 mA	43	43	43	—	—	—	—	—	—
1.5V_HSTL_ CLASS_II	16 mA	18	20	21	—	—	—	—	—	—
DIFFERENTIAL_SSTL_2 _CLASS_I	8 mA	46	47	49	25	40	56	25	40	56
	12 mA	67	69	70	23	42	60	23	42	60
DIFFERENTIAL_SSTL_2 _CLASS_II	16 mA	42	43	45	15	29	42	15	29	42
	20 mA	41	42	44	—	—	—	—	—	—
	24 mA	40	42	43	—	—	—	—	—	—
DIFFERENTIAL_SSTL_ 18_CLASS_I	6 mA	20	22	24	46	47	49	46	47	49
	8 mA	20	22	24	47	49	51	47	49	51
	10 mA	20	22	25	23	25	27	23	25	27
	12 mA	19	23	26	—	—	—	—	—	—

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 3 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
DIFFERENTIAL_SSTL_18_CLASS_II	16 mA	30	33	36	—	—	—	—	—	—
	18 mA	29	29	29	—	—	—	—	—	—
1.8V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	26	28	29	59	61	63	59	61	63
	10 mA	46	47	48	65	66	68	65	66	68
	12 mA	67	67	67	71	71	72	71	71	72
1.8V_DIFFERENTIAL_HSTL_CLASS_II	16 mA	62	65	68	—	—	—	—	—	—
	18 mA	59	62	65	—	—	—	—	—	—
	20 mA	57	59	62	—	—	—	—	—	—
1.5V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	40	40	41	28	32	36	28	32	36
	10 mA	41	42	42	—	—	—	—	—	—
	12 mA	43	43	43	—	—	—	—	—	—
1.5V_DIFFERENTIAL_HSTL_CLASS_II	16 mA	18	20	21	—	—	—	—	—	—
LVDS	—	11	13	16	11	13	15	11	13	15
RSDS	—	11	13	16	11	13	15	11	13	15
MINI_LVDS	—	11	13	16	11	13	15	11	13	15
SIMPLE_RSDS	—	15	19	23	15	19	23	15	19	23
1.2V_HSTL	—	130	132	133	—	—	—	—	—	—
1.2V_DIFFERENTIAL_HSTL	—	130	132	133	—	—	—	—	—	—
PCI	—	—	—	—	99	120	142	99	120	142
PCI-X	—	—	—	—	99	121	143	99	121	143
LVTTL	OCT_25_OHMS	13	14	14	21	27	33	21	27	33
LVCMOS	OCT_25_OHMS	13	14	14	21	27	33	21	27	33
2.5V	OCT_50_OHMS	346	369	392	324	326	327	324	326	327
1.8V	OCT_50_OHMS	198	203	209	202	203	204	202	203	204

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 4 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
SSTL_2_CLASS_I	OCT_50 _OHMS	67	69	70	25	42	60	25	42	60
SSTL_18_CLASS_I	OCT_50 _OHMS	30	33	36	47	49	51	47	49	51

High Speed I/O Timing Specifications

The timing analysis for LVDS, mini-LVDS, and RSDS is different compared to other I/O standards because the data communication is source-synchronous.

You should also consider board skew, cable skew, and clock jitter in your calculation. This section provides details on the timing parameters for high-speed I/O standards in Cyclone II devices.

Table 5–47 defines the parameters of the timing diagram shown in Figure 5–3.

Table 5–47. High-Speed I/O Timing Definitions (Part 1 of 2)

Parameter	Symbol	Description
High-speed clock	f_{HSCKLK}	High-speed receiver and transmitter input and output clock frequency.
Duty cycle	t_{DUTY}	Duty cycle on high-speed transmitter output clock.
High-speed I/O data rate	HSIODR	High-speed receiver and transmitter input and output data rate.
Time unit interval	TUI	TUI = 1/HSIODR.
Channel-to-channel skew	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement. TCCS = TUI – SW – (2 × RSKM)

Table 5–47. High-Speed I/O Timing Definitions (Part 2 of 2)

Parameter	Symbol	Description
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. Sampling window is the sum of the setup time, hold time, and jitter. The window of t_{SU} + t_H is expected to be centered in the sampling window. SW = TUI – TCCS – (2 × RSKM)
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2
Input jitter (peak to peak)	—	Peak-to-peak input jitter on high-speed PLLs.
Output jitter (peak to peak)	—	Peak-to-peak output jitter on high-speed PLLs.
Signal rise time	t_{RISE}	Low-to-high transmission time.
Signal fall time	t_{FALL}	High-to-low transmission time.
Lock time	t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Figure 5–3. High-Speed I/O Timing Diagram

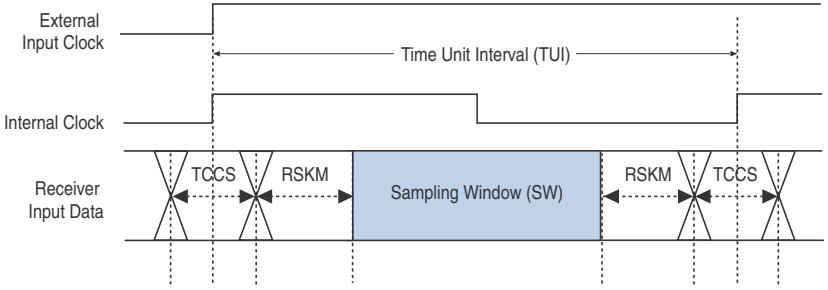
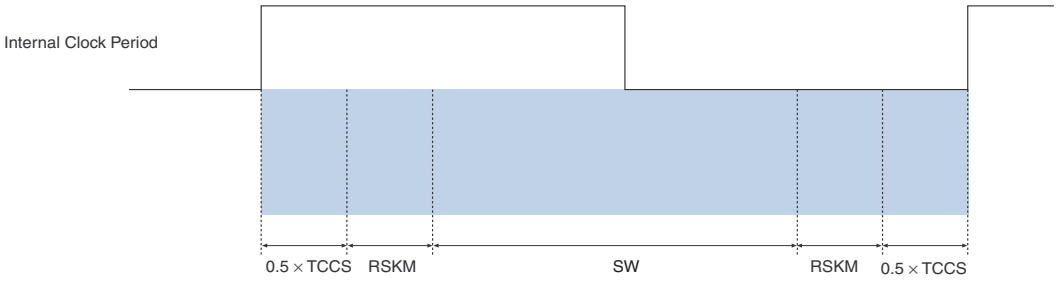


Figure 5–4 shows the high-speed I/O timing budget.

Figure 5–4. High-Speed I/O Timing Budget *Note (1)*



Note to Figure 5–4:
(1) The equation for the high-speed I/O timing budget is: period = TCCS + RSKM + SW + RSKM.

Table 5–48 shows the RSDS timing budget for Cyclone II devices at 311 Mbps. RSDS is supported for transmitting from Cyclone II devices. Cyclone II devices cannot receive RSDS data because the devices are intended for applications where they will be driving display drivers. Cyclone II devices support a maximum RSDS data rate of 311 Mbps using DDIO registers. Cyclone II devices support RSDS only in the commercial temperature range.

Table 5–48. RSDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max (1)	Min	Typ	Max (1)	Min	Typ	Max (1)	
f_{HSCLK} (input clock frequency)	×10	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×8	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×7	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×4	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×2	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×1	10	—	311	10	—	311	10	—	311	MHz
Device operation in Mbps	×10	100	—	311	100	—	311	100	—	311	Mbps
	×8	80	—	311	80	—	311	80	—	311	Mbps
	×7	70	—	311	70	—	311	70	—	311	Mbps
	×4	40	—	311	40	—	311	40	—	311	Mbps
	×2	20	—	311	20	—	311	20	—	311	Mbps
	×1	10	—	311	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%

Table 5–48. RSDS Transmitter Timing Specification (Part 2 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max *(1)*	Min	Typ	Max *(1)*	Min	Typ	Max *(1)*	
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	20–80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	80–20%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	—	—		100	—		100	—	—	100	µs

Note to Table 5–48:

(1) These specifications are for a three-resistor RSDS implementation. For single-resistor RSDS in ×10 through ×2 modes, the maximum data rate is 170 Mbps and the corresponding maximum input clock frequency is 85 MHz. For single-resistor RSDS in ×1 mode, the maximum data rate is 170 Mbps, and the maximum input clock frequency is 170 MHz. For more information about the different RSDS implementations, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the Cyclone II Device Handbook.

In order to determine the transmitter timing requirements, RSDS receiver timing requirements on the other end of the link must be taken into consideration. RSDS receiver timing parameters are typically defined as t_{SU} and t_H requirements. Therefore, the transmitter timing parameter specifications are t_{CO} (minimum) and t_{CO} (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for RSDS are shown in Figure 5–5.

Figure 5–5. RSDS Transmitter Clock to Data Relationship

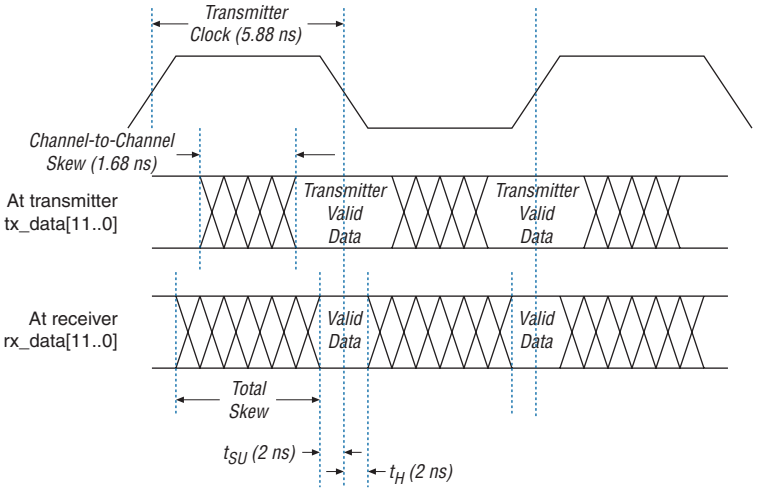


Table 5–49 shows the mini-LVDS transmitter timing budget for Cyclone II devices at 311 Mbps. Cyclone II devices cannot receive mini-LVDS data because the devices are intended for applications where they will be driving display drivers. A maximum mini-LVDS data rate of 311 Mbps is supported for Cyclone II devices using DDIO registers. Cyclone II devices support mini-LVDS only in the commercial temperature range.

Table 5–49. Mini-LVDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×8	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×7	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×4	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×2	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×1	10	—	311	10	—	311	10	—	311	MHz

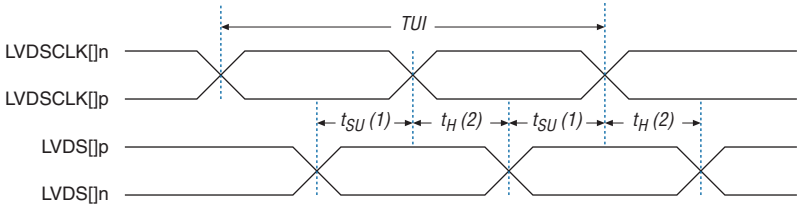
Table 5–49. Mini-LVDS Transmitter Timing Specification (Part 2 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Device operation in Mbps	×10	100	—	311	100	—	311	100	—	311	Mbps
	×8	80	—	311	80	—	311	80	—	311	Mbps
	×7	70	—	311	70	—	311	70	—	311	Mbps
	×4	40	—	311	40	—	311	40	—	311	Mbps
	×2	20	—	311	20	—	311	20	—	311	Mbps
	×1	10	—	311	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	20–80%	—	—	500	—	—	500	—	—	500	ps
t_{FALL}	80–20%	—	—	500	—	—	500	—	—	500	ps
t_{LOCK}		—	—	100	—	—	100	—	—	100	µs

In order to determine the transmitter timing requirements, mini-LVDS receiver timing requirements on the other end of the link must be taken into consideration. The mini-LVDS receiver timing parameters are typically defined as t_{SU} and t_H requirements. Therefore, the transmitter timing parameter specifications are t_{CO} (minimum) and t_{CO} (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for mini-LVDS are shown in Figure 5–6.

Figure 5–6. mini-LVDS Transmitter AC Timing Specification



Notes to Figure 5–6:
(1) The data setup time, t_{SU}, is 0.225 × TUI.
(2) The data hold time, t_H, is 0.225 × TUI.

Tables 5–50 and 5–51 show the LVDS timing budget for Cyclone II devices. Cyclone II devices support LVDS receivers at data rates up to 805 Mbps, and LVDS transmitters at data rates up to 640 Mbps.

Table 5–50. LVDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Unit
		Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	
f_{HSCLK} (input clock frequency)	×10	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×8	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×7	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×4	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×2	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×1	10	—	402.5	402.5	10	—	402.5	402.5	10	—	402.5 (8)	402.5 (8)	MHz
HSIODR	×10	100	—	640	640	100	—	550	640	100	—	311 (5)	550 (7)	Mbps
	×8	80	—	640	640	80	—	550	640	80	—	311 (5)	550 (7)	Mbps
	×7	70	—	640	640	70	—	550	640	70	—	311 (5)	550 (7)	Mbps
	×4	40	—	640	640	40	—	550	640	40	—	311 (5)	550 (7)	Mbps
	×2	20	—	640	640	20	—	550	640	20	—	311 (5)	550 (7)	Mbps
	×1	10	—	402.5	402.5	10	—	402.5	402.5	10	—	402.5 (9)	402.5 (9)	Mbps
t_{DUTY}	—	45	—	55	—	45	—	55	—	45	—	55	—	%
	—	—	—	—	160	—	—	—	312.5	—	—	—	363.6	ps
TCCS (3)	—	—	—	200		—	—	200		—	—	200		ps
Output jitter (peak to peak)	—	—	—	500		—	—	500		—	—	550 (10)		ps
t_{RISE}	20–80%	150	200	250		150	200	250		150	200	250 (11)		ps

Table 5–50. LVDS Transmitter Timing Specification (Part 2 of 2)

Symbol	Conditions	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Unit
		Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	
t_{FALL}	80–20%	150	200	250		150	200	250		150	200	250 (11)		ps
t_{LOCK}	—	—	—	100		—	—	100		—	—	100 (12)		µs

Notes to Table 5–50:

(1) The maximum data rate that complies with duty cycle distortion of 45–55%.

(2) The maximum data rate when taking duty cycle in absolute ps into consideration that may not comply with 45–55% duty cycle distortion. If the downstream receiver can handle duty cycle distortion beyond the 45–55% range, you may use the higher data rate values from this column. You can calculate the duty cycle distortion as a percentage using the absolute ps value. For example, for a data rate of 640 Mbps (UI = 1562.5 ps) and a t_{DUTY} of 250 ps, the duty cycle distortion is ± t_{DUTY} / (UI*2) *100% = ± 250 ps / (1562.5 *2) * 100% = ± 8%, which gives you a duty cycle distortion of 42–58%.

(3) The TCCS specification applies to the entire bank of LVDS, as long as the SERDES logic is placed within the LAB adjacent to the output pins.

(4) For extended temperature devices, the maximum input clock frequency for ×10 through ×2 modes is 137.5 MHz.

(5) For extended temperature devices, the maximum data rate for ×10 through ×2 modes is 275 Mbps.

(6) For extended temperature devices, the maximum input clock frequency for ×10 through ×2 modes is 200 MHz.

(7) For extended temperature devices, the maximum data rate for ×10 through ×2 modes is 400 Mbps.

(8) For extended temperature devices, the maximum input clock frequency for ×1 mode is 340 MHz.

(9) For extended temperature devices, the maximum data rate for ×1 mode is 340 Mbps.

(10) For extended temperature devices, the maximum output jitter (peak to peak) is 600 ps.

(11) For extended temperature devices, the maximum t_{RISE} and t_{FALL} are 300 ps.

(12) For extended temperature devices, the maximum lock time is 500 us.

Table 5–51. LVDS Receiver Timing Specification

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×8	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×7	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×4	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×2	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×1	10	—	402.5	10	—	402.5	10	—	402.5 *(3)*	MHz
HSIODR	×10	100	—	805	100	—	640	100	—	640 *(2)*	Mbps
	×8	80	—	805	80	—	640	80	—	640 *(2)*	Mbps
	×7	70	—	805	70	—	640	70	—	640 *(2)*	Mbps
	×4	40	—	805	40	—	640	40	—	640 *(2)*	Mbps
	×2	20	—	805	20	—	640	20	—	640 *(2)*	Mbps
	×1	10	—	402.5	10	—	402.5	10	—	402.5 *(4)*	Mbps
SW	—	—	—	300	—	—	400	—	—	400	ps
Input jitter tolerance	—	—	—	500	—	—	500	—	—	550	ps
t_{LOCK}	—	—	—	100	—	—	100	—	—	100 *(5)*	ps

Notes to Table 5–51:
(1) For extended temperature devices, the maximum input clock frequency for x10 through x2 modes is 275 MHz.
(2) For extended temperature devices, the maximum data rate for x10 through x2 modes is 550 Mbps.
(3) For extended temperature devices, the maximum input clock frequency for x1 mode is 340 MHz.
(4) For extended temperature devices, the maximum data rate for x1 mode is 340 Mbps.
(5) For extended temperature devices, the maximum lock time is 500 us.

External Memory Interface Specifications

Table 5–52 shows the DQS bus clock skew adder specifications.

Table 5–52. DQS Bus Clock Skew Adder Specifications

Mode	DQS Clock Skew Adder	Unit
×9	155	ps
×18	190	ps

Note to Table 5–52:
(1) This skew specification is the absolute maximum and minimum skew. For example, skew on a ×9 DQ group is 155 ps or ±77.5 ps.

JTAG Timing Specifications

Figure 5–7 shows the timing requirements for the JTAG signals.

Figure 5–7. Cyclone II JTAG Waveform

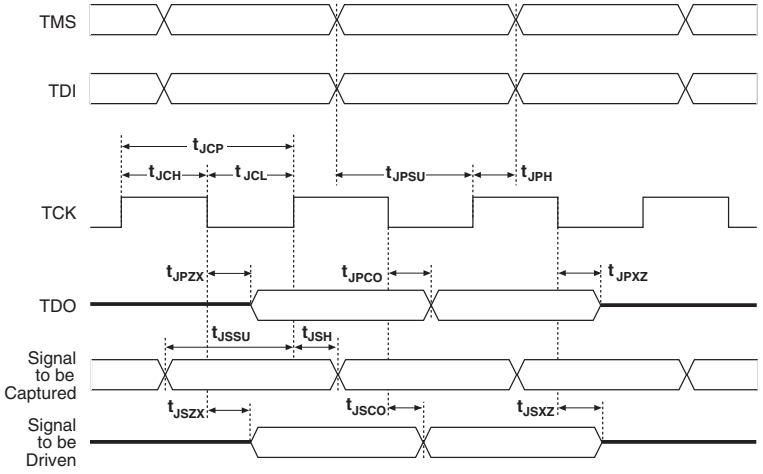


Table 5–53 shows the JTAG timing parameters and values for Cyclone II devices.

Table 5–53. Cyclone II JTAG Timing Parameters and Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns
t_{JPSU}	JTAG port setup time *(2)*	5	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(2)*	—	13	ns
t_{JPZX}	JTAG port high impedance to valid output *(2)*	—	13	ns
t_{JPXZ}	JTAG port valid output to high impedance *(2)*	—	13	ns
t_{JSSU}	Capture register setup time *(2)*	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 5–53:

(1) This information is preliminary.

(2) This specification is shown for 3.3-V LVTTL/LVCMOS and 2.5-V LVTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the JTAG port and capture register clock setup time is 3 ns and port clock to output time is 15 ns.

Cyclone II devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Cyclone II devices are in the 18th position or after they will fail configuration. This does not affect the SignalTap® II logic analyzer.

For more information on JTAG, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices* chapter in the *Cyclone II Handbook*.

PLL Timing Specifications

Table 5–54 describes the Cyclone II PLL specifications when operating in the commercial junction temperature range (0° to 85° C), the industrial junction temperature range (–40° to 100° C), the automotive junction temperature range (–40° to 125° C), and the extended temperature range (–40° to 125° C). Follow the PLL specifications for –8 speed grade devices when operating in the industrial, automotive, or extended temperature range.

Table 5–54. PLL Specifications *Note (1)* ***(Part 1 of 2)***

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–6 speed grade)	10	—	*(4)*	MHz
	Input clock frequency (–7 speed grade)	10	—	*(4)*	MHz
	Input clock frequency (–8 speed grade)	10	—	*(4)*	MHz
f_{INPFD}	PFD input frequency (–6 speed grade)	10	—	402.5	MHz
	PFD input frequency (–7 speed grade)	10	—	402.5	MHz
	PFD input frequency (–8 speed grade)	10	—	402.5	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$ *(5)*	Input clock period jitter	—	200	—	ps
f_{OUT_EXT} (external clock output)	PLL output frequency (–6 speed grade)	10	—	*(4)*	MHz
	PLL output frequency (–7 speed grade)	10	—	*(4)*	MHz
	PLL output frequency (–8 speed grade)	10	—	*(4)*	MHz
f_{OUT} (to global clock)	PLL output frequency (–6 speed grade)	10	—	500	MHz
	PLL output frequency (–7 speed grade)	10	—	450	MHz
	PLL output frequency (–8 speed grade)	10	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	—	55	%
t_{JITTER} (p-p) *(2)*	Period jitter for external clock output f_{OUT_EXT} > 100 MHz	—	—	300	ps
	f_{OUT_EXT} ≤100 MHz	—	—	30	mUI
t_{LOCK}	Time required to lock from end of device configuration	—	—	100 *(6)*	µs
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±60	ps

Table 5–54. PLL Specifications Note (1) (Part 2 of 2)

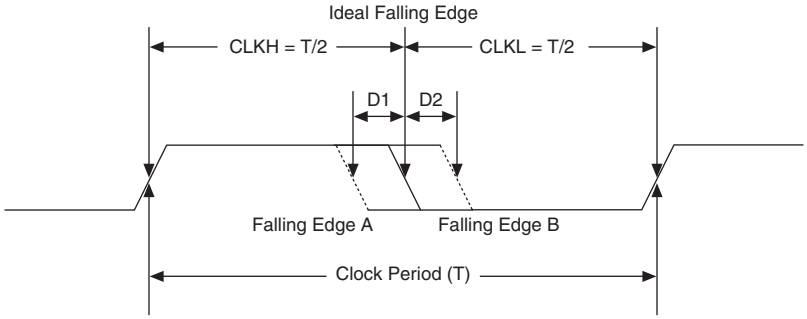
Symbol	Parameter	Min	Typ	Max	Unit
f_{VCO} (3)	PLL internal VCO operating range	300	—	1,000	MHz
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns

Notes to Table 5–54:
(1) These numbers are preliminary and pending silicon characterization.
(2) The t_{JITTER} specification for the PLL[4..1]_OUT pins are dependent on the I/O pins in its VCCIO bank, how many of them are switching outputs, how much they toggle, and whether or not they use programmable current strength.
(3) If the VCO post-scale counter = 2, a 300- to 500-MHz internal VCO frequency is available.
(4) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
(5) Cyclone II PLLs can track a spread-spectrum input clock that has an input jitter within ±200 ps.
(6) For extended temperature devices, the maximum lock time is 500 us.

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 5–8. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (Figure 5–8). The maximum DCD for a clock is the larger value of D1 and D2.

Figure 5–8. Duty Cycle Distortion



DCD expressed in absolution derivation, for example, D1 or D2 in Figure 5–8, is clock-period independent. DCD can also be expressed as a percentage, and the percentage number is clock-period dependent. DCD as a percentage is defined as:

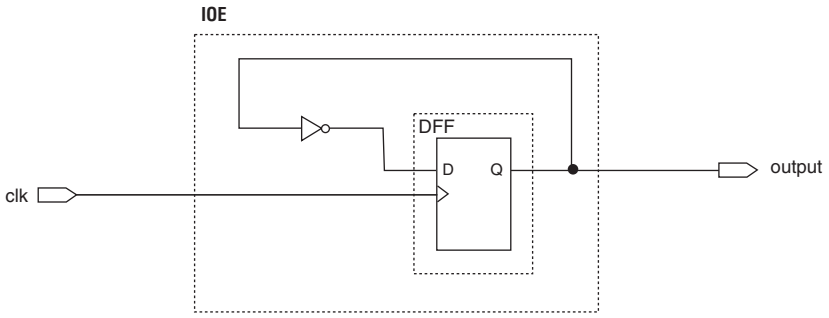
(T/2 – D1) / T (the low percentage boundary)

(T/2 + D2) / T (the high percentage boundary)

DCD Measurement Techniques

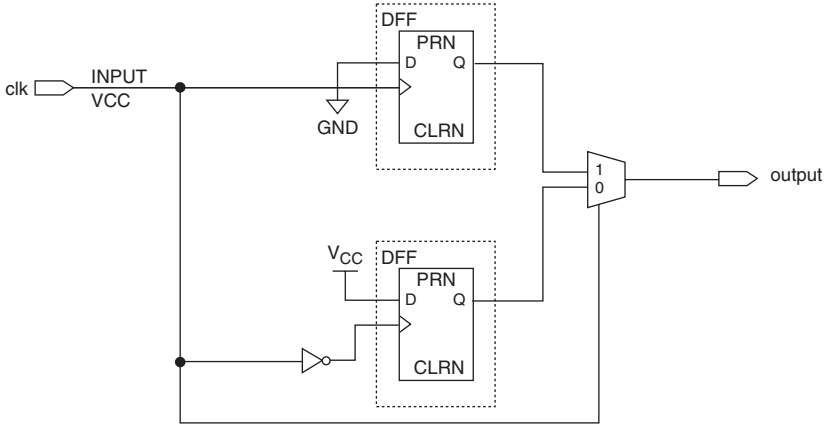
DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions (Figure 5–9). Therefore, any DCD present on the input clock signal, or caused by the clock input buffer, or different input I/O standard, does not transfer to the output signal.

Figure 5–9. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs



However, when the output is a double data rate input/output (DDIO) signal, both edges of the input clock signal (positive and negative) trigger output transitions (Figure 5–10). Therefore, any distortion on the input clock and the input clock buffer affect the output DCD.

Figure 5–10. DCD Measurement Technique for DDIO (Double-Data Rate) Outputs



When an FPGA PLL generates the internal clock, the PLL output clocks the IOE block. As the PLL only monitors the positive edge of the reference clock input and internally re-creates the output clock signal, any DCD present on the reference clock is filtered out. Therefore, the DCD for a DDIO output with PLL in the clock path is better than the DCD for a DDIO output without PLL in the clock path.

Tables 5–55 through 5–58 give the maximum DCD in absolution derivation for different I/O standards on Cyclone II devices. Examples are also provided that show how to calculate DCD as a percentage.

Table 5–55. Maximum DCD for Single Data Outputs (SDR) on Row I/O Pins Notes (1), (2) (Part 1 of 2)

Row I/O Output Standard	C6	C7	C8	Unit
LVCMOS	165	230	230	ps
LVTTL	195	255	255	ps
2.5-V	120	120	135	ps
1.8-V	115	115	175	ps
1.5-V	130	130	135	ps
SSTL-2 Class I	60	90	90	ps
SSTL-2 Class II	65	75	75	ps
SSTL-18 Class I	90	165	165	ps
HSTL-15 Class I	145	145	205	ps
HSTL-18 Class I	85	155	155	ps

Table 5–55. Maximum DCD for Single Data Outputs (SDR) on Row I/O Pins *Notes (1), (2)* *(Part 2 of 2)*

Row I/O Output Standard	C6	C7	C8	Unit
Differential SSTL-2 Class I	60	90	90	ps
Differential SSTL-2 Class II	65	75	75	ps
Differential SSTL-18 Class I	90	165	165	ps
Differential HSTL-18 Class I	85	155	155	ps
Differential HSTL-15 Class I	145	145	205	ps
LVDS	60	60	60	ps
Simple RSDS	60	60	60	ps
Mini LVDS	60	60	60	ps
PCI	195	255	255	ps
PCI-X	195	255	255	ps

Notes to Table 5–55:
(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.
(2) Numbers are applicable for commercial, industrial, and automotive devices.

Here is an example for calculating the DCD as a percentage for an SDR output on a row I/O on a –6 device:

If the SDR output I/O standard is SSTL-2 Class II, the maximum DCD is 65 ps (refer to Table 5–55). If the clock frequency is 167 MHz, the clock period T is:

$$T = 1/f = 1 / 167\ \text{MHz} = 6\ \text{ns} = 6000\ \text{ps}$$

To calculate the DCD as a percentage:

$(T/2 - DCD) / T = (6000\ \text{ps}/2 - 65\ \text{ps}) / 6000\ \text{ps} = 48.91\%$ (for low boundary)

$(T/2 + DCD) / T = (6000\ \text{ps}/2 + 65\ \text{ps}) / 6000\text{ps} = 51.08\%$ (for high boundary

Table 5–56. Maximum DCD for SDR Output on Column I/O *Notes (1), (2)* *(Part 1 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
LVCMOS	195	285	285	ps
LVTTL	210	305	305	ps

Table 5–56. Maximum DCD for SDR Output on Column I/O Notes (1), (2) *(Part 2 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
2.5-V	140	140	155	ps
1.8-V	115	115	165	ps
1.5-V	745	745	770	ps
SSTL-2 Class I	60	60	75	ps
SSTL-2 Class II	60	60	80	ps
SSTL-18 Class I	60	130	130	ps
SSTL-18 Class II	60	135	135	ps
HSTL-18 Class I	60	115	115	ps
HSTL-18 Class II	75	75	100	ps
HSTL-15 Class I	150	150	150	ps
HSTL-15 Class II	135	135	155	ps
Differential SSTL-2 Class I	60	60	75	ps
Differential SSTL-2 Class II	60	60	80	ps
Differential SSTL-18 Class I	60	130	130	ps
Differential SSTL-18 Class II	60	135	135	ps
Differential HSTL-18 Class I	60	115	115	ps
Differential HSTL-18 Class II	75	75	100	ps
Differential HSTL-15 Class I	150	150	150	ps
Differential HSTL-15 Class II	135	135	155	ps
LVDS	60	60	60	ps
Simple RSDS	60	70	70	ps
Mini-LVDS	60	60	60	ps

Notes to Table 5–56:

(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

(2) Numbers are applicable for commercial, industrial, and automotive devices.

Table 5–57. Maximum for DDIO Output on Row Pins with PLL in the Clock Path Notes (1), (2) *(Part 1 of 2)*

Row Pins with PLL in the Clock Path	C6	C7	C8	Unit
LVCMOS	270	310	310	ps
LVTTL	285	305	335	ps
2.5-V	180	180	220	ps
1.8-V	165	175	205	ps

Table 5–57. Maximum for DDIO Output on Row Pins with PLL in the Clock Path Notes (1), (2) (Part 2 of 2)

Row Pins with PLL in the Clock Path	C6	C7	C8	Unit
1.5-V	280	280	280	ps
SSTL-2 Class I	150	190	230	ps
SSTL-2 Class II	155	200	230	ps
SSTL-18 Class I	180	240	260	ps
HSTL-18 Class I	180	235	235	ps
HSTL-15 Class I	205	220	220	ps
Differential SSTL-2 Class I	150	190	230	ps
Differential SSTL-2 Class II	155	200	230	ps
Differential SSTL-18 Class I	180	240	260	ps
Differential HSTL-18 Class I	180	235	235	ps
Differential HSTL-15 Class I	205	220	220	ps
LVDS	95	110	120	ps
Simple RSDS	100	155	155	ps
Mini LVDS	95	110	120	ps
PCI	285	305	335	ps
PCI-X	285	305	335	ps

Notes to Table 5–57:

(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

(2) Numbers are applicable for commercial, industrial, and automotive devices.

For DDIO outputs, you can calculate actual half period from the following equation:

Actual half period = ideal half period – maximum DCD

For example, if the DDR output I/O standard is SSTL-2 Class II, the maximum DCD for a –5 device is 155 ps (refer to Table 5–57). If the clock frequency is 167 MHz, the half-clock period T/2 is:

T/2 = 1/(2* f)= 1 /(2*167 MHz) = 3 ns = 3000 ps

The actual half period is then = 3000 ps – 155 ps = 2845 ps

Table 5–58. Maximum DCD for DDIO Output on Column I/O Pins with PLL in the Clock Path *Notes (1), (2)*

Column I/O Pins in the Clock Path	C6	C7	C8	Unit
LVCMOS	285	400	445	ps
LVTTL	305	405	460	ps
2.5-V	175	195	285	ps
1.8-V	190	205	260	ps
1.5-V	605	645	645	ps
SSTL-2 Class I	125	210	245	ps
SSTL-2 Class II	195	195	195	ps
SSTL-18 Class I	130	240	245	ps
SSTL-18 Class II	135	270	330	ps
HSTL-18 Class I	135	240	240	ps
HSTL-18 Class II	165	240	285	ps
HSTL-15 Class I	220	335	335	ps
HSTL-15 Class II	190	210	375	ps
Differential SSTL-2 Class I	125	210	245	ps
Differential SSTL-2 Class II	195	195	195	ps
Differential SSTL-18 Class I	130	240	245	ps
Differential SSTL-18 Class II	132	270	330	ps
Differential HSTL-18 Class I	135	240	240	ps
Differential HSTL-18 Class II	165	240	285	ps
Differential HSTL-15 Class I	220	335	335	ps
Differential HSTL-15 Class II	190	210	375	ps
LVDS	110	120	125	ps
Simple RSDS	125	125	275	ps
Mini-LVDS	110	120	125	ps

Notes to Table 5–58:

(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

(2) Numbers are applicable for commercial, industrial, and automotive devices.

Referenced Documents

This chapter references the following documents:

- *Cyclone II Architecture* chapter in *Cyclone II Device Handbook*
- *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices* chapter in the *Cyclone II Handbook*
- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Early Power Estimator User Guide*
- *PowerPlay Power Analysis* chapters in volume 3 of the *Quartus II Handbook*

Document Revision History

Table 5–59 shows the revision history for this document.

Table 5–59. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
February 2008 v4.0	• Updated the following tables with I/O timing numbers for automotive-grade devices: Tables 5–2, 5–12, 5–13, 5–15, 5–16, 5–17, 5–18, 5–19, 5–21, 5–22, 5–23, 5–25, 5–26, 5–27, 5–28, 5–36, 5–37, 5–40, 5–41, 5–42, 5–43, 5–55, 5–56, 5–57, and 5–58. • Added "Referenced Documents".	Added I/O timing numbers for automotive-grade devices.
April 2007 v3.2	• Updated Table 5–3.	Updated R_{CONF} typical and maximum values in Table 5–3.

February 2007 v3.1	• Added document revision history. • Added V_{CCA} minimum and maximum limitations in Table 5–1. • Updated *Note (1)* in Table 5–2. • Updated the maximum V_{CC} rise time for Cyclone II "A" devices in Table 5–2. • Updated R_{CONF} information in Table 5–3. • Changed V_I to I_i in Table 5–3. • Updated LVPECL clock inputs in *Note (6)* to Table 5–8. • Updated *Note (1)* to Table 5–12. • Updated C_{VREF} capacitance description in Table 5–13. • Updated "Timing Specifications" section. • Updated Table 5–45. • Added Table 5–46 with information on toggle rate derating factors. • Corrected calculation of the period based on a 640 Mbps data rate as 1562.5 ps in *Note (2)* to Table 5–50. • Updated "PLL Timing Specifications" section. • Updated V_{CO} range of 300–500 MHz in *Note (3)* to Table 5–54. • Updated chapter with extended temperature information.	—
December 2005 v2.2	Updated PLL Timing Specifications	—
November 2005 v2.1	Updated technical content throughout.	—
July 2005 v2.0	Updated technical content throughout.	—
November 2004 v1.1	Updated the "Differential I/O Standards" section. Updated Table 5–54.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—