7. I/O Multiplexing and Considerations

7.1. Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G, H or I. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0..31) in the PORT must be written to '1'. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

This table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 7-1. PORT Function Multiplexing

Pin			I/O pin	Supply	A	B(1)(2)						C	D	E	F	G	H	I
SAML21E	SAML21G	SAML21J			EIC/RSTC	REF	ADC	AC	PTC	DAC	OPAMP	SERCOM (1)(2)	SERCOM-ALT	TC/TCC (3)	TCC	COM	AC/GCLK/SUPC	CCL
1	1	1	PA00	VSWOUT	EXTINT[0]/ EXTWAKE[0]								SERCOM1/ PAD[0]	TCC2/ WO[0]				
2	2	2	PA01	VSWOUT	EXTINT[1]/ EXTWAKE[1]								SERCOM1/ PAD[1]	TCC2/ WO[1]				
3	3	3	PA02 (5)	VDDANA	EXTINT[2]/ EXTWAKE[2]		AIN[0]		Y[0]	VOUT[0]	OA_NEG[0]							
4	4	4	PA03	VDDANA	EXTINT[3]/ EXTWAKE[3]	VREFA	AIN[1]		Y[1]									
		5	PB04	VDDANA	EXTINT[4]		AIN[12]		Y[10]									
		6	PB05	VDDANA	EXTINT[5]		AIN[13]		Y[11]		OA_NEG[1]							
		9	PB06	VDDANA	EXTINT[6]		AIN[14]		Y[12]		OA_NEG[2]							CCL2 IN[0]
		10	PB07	VDDANA	EXTINT[7]		AIN[15]		Y[13]									CCL2 IN[1]
	7	11	PB08 (5)	VDDANA	EXTINT[8]		AIN[2]				OA_OUT[1]		SERCOM4/ PAD[0]	TC0/ WO[0]				CCL2 IN[2]
	8	12	PB09	VDDANA	EXTINT[9]		AIN[3]		Y[15]		OA_POS[1]		SERCOM4/ PAD[1]	TC0/ WO[1]				CCL2 OUT
5	9	13	PA04 (5)	VDDANA	EXTINT[4]/ EXTWAKE[4]	VREFB	AIN[4]	AIN[0]			OA_OUT[2]		SERCOM0/ PAD[0]	TCC0/ WO[0]				CCL0 IN[0]
6	10	14	PA05 (5)	VDDANA	EXTINT[5]/ EXTWAKE[5]		AIN[5]	AIN[1]		VOUT[1]	OA_POS[2]		SERCOM0/ PAD[1]	TCC0/ WO[1]				CCL0 IN[1]
7	11	15	PA06	VDDANA	EXTINT[6]/ EXTWAKE[6]		AIN[6]	AIN[2]	Y[4]		OA_POS[0]		SERCOM0/ PAD[2]	TCC1/ WO[0]				CCL0 IN[2]
8	12	16	PA07 (5)	VDDANA	EXTINT[7]/ EXTWAKE[7]		AIN[7]	AIN[3]			OA_OUT[0]		SERCOM0/ PAD[3]	TCC1/ WO[1]				CCL0 OUT
11	13	17	PA08 (5)	VDDIO(6)	NMI		AIN[16]		X[0] Y[6]			SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TCC0/ WO[0]	TCC1/ WO[2]			CCL1 IN[0]
12	14	18	PA09	VDDIO(6)	EXTINT[9]		AIN[17]		X[1] Y[7]			SERCOM0/ PAD[1]	SERCOM2/ PAD[1]	TCC0/ WO[1]	TCC1/ WO[3]			CCL1 IN[1]
13	15	19	PA10	VDDIO(6)	EXTINT[10]		AIN[18]		X[2] Y[8]			SERCOM0/ PAD[2]	SERCOM2/ PAD[2]	TCC1/ WO[0]	TCC0/ WO[2]		GCLK_IO[4]	CCL1 IN[2]
14	16	20	PA11	VDDIO(6)	EXTINT[11]		AIN[19]		X[3] Y[9]			SERCOM0/ PAD[3]	SERCOM2/ PAD[3]	TCC1/ WO[1]	TCC0/ WO[3]		GCLK_IO[5]	CCL1 OUT
	19	23	PB10	VDDIO	EXTINT[10]				Y[2]				SERCOM4/ PAD[2]	TC1/ WO[0]	TCC0/ WO[4]		GCLK_IO[4]	CCL1 IN[2]
	20	24	PB11	VDDIO	EXTINT[11]				Y[3]				SERCOM4/ PAD[3]	TC1/ WO[1]	TCC0/ WO[5]		GCLK_IO[5]	CCL1 OUT
		25	PB12	VDDIO	EXTINT[12]				X[12] Y[5]			SERCOM4/ PAD[0		TC0/ WO[0]	TCC0/ WO[6]		GCLK_IO[6]	
		26	PB13	VDDIO	EXTINT[13]				X[13] Y[14]			SERCOM4/ PAD[1]		TC0/ WO[1]	TCC0/ WO[7]		GCLK_IO[7]	

Pin			I/O pin	Supply	A	B[1][2]						C	D	E	F	G	H	I
SAML21E	SAML21G	SAML21J			EIC/RSTC	REF	ADC	AC	PTC	DAC	OPAMP	SERCOM [1][2]	SERCOM-ALT	TC/TCC [3]	TCC	COM	AC/GCLK/SUPC	CCL
		27	PB14	VDDIO	EXTINT[14]				X[14]			SERCOM4/PAD[2]		TC1/WO[0]			GCLK_IO[0]	CCL3 IN[0]
		28	PB15	VDDIO	EXTINT[15]				X[15]			SERCOM4/PAD[3]		TC1/WO[1]			GCLK_IO[1]	CCL3 IN[1]
	21	29	PA12	VDDIO	EXTINT[12]							SERCOM2/PAD[0]	SERCOM4/PAD[0]	TCC2/WO[0]	TCC0/WO[6]		AC/CMP[0]	
	22	30	PA13	VDDIO	EXTINT[13]							SERCOM2/PAD[1]	SERCOM4/PAD[1]	TCC2/WO[1]	TCC0/WO[7]		AC/CMP[1]	
15	23	31	PA14	VDDIO[6]	EXTINT[14]							SERCOM2/PAD[2]	SERCOM4/PAD[2]	TC4/WO[0]	TCC0/WO[4]		GCLK_IO[0]	
16	24	32	PA15	VDDIO[6]	EXTINT[15]							SERCOM2/PAD[3]	SERCOM4/PAD[3]	TC4/WO[1]	TCC0/WO[5]		GCLK_IO[1]	
17	25	35	PA16	VDDIO[6]	EXTINT[0]				X[4]			SERCOM1/PAD[0]	SERCOM3/PAD[0]	TCC2/WO[0]	TCC0/WO[6]		GCLK_IO[2]	CCL0 IN[0]
18	26	36	PA17	VDDIO[6]	EXTINT[1]				X[5]			SERCOM1/PAD[1]	SERCOM3/PAD[1]	TCC2/WO[1]	TCC0/WO[7]		GCLK_IO[3]	CCL0 IN[1]
19	27	37	PA18	VDDIO[6]	EXTINT[2]				X[6]			SERCOM1/PAD[2]	SERCOM3/PAD[2]	TC4/WO[0]	TCC0/WO[2]		AC/CMP[0]	CCL0 IN[2]
20	28	38	PA19	VDDIO[6]	EXTINT[3]				X[7]			SERCOM1/PAD[3]	SERCOM3/PAD[3]	TC4/WO[1]	TCC0/WO[3]		AC/CMP[1]	CCL0 OUT
		39	PB16	VDDIO	EXTINT[0]							SERCOM5/PAD[0]		TC2/WO[0]	TCC0/WO[4]		GCLK_IO[2]	CCL3 IN[2]
		40	PB17	VDDIO	EXTINT[1]							SERCOM5/PAD[1]		TC2/WO[1]	TCC0/WO[5]		GCLK_IO[3]	CCL3 OUT
	29	41	PA20	VDDIO	EXTINT[4]				X[8]			SERCOM5/PAD[2]	SERCOM3/PAD[2]	TC3/WO[0]	TCC0/WO[6]		GCLK_IO[4]	
	30	42	PA21	VDDIO	EXTINT[5]				X[9]			SERCOM5/PAD[3]	SERCOM3/PAD[3]	TC3/WO[1]	TCC0/WO[7]		GCLK_IO[5]	
21	31	43	PA22	VDDIO[6]	EXTINT[6]				X[10]			SERCOM3/PAD[0]	SERCOM5/PAD[0]	TC0/WO[0]	TCC0/WO[4]		GCLK_IO[6]	CCL2 IN[0]
22	32	44	PA23	VDDIO[6]	EXTINT[7]				X[11]			SERCOM3/PAD[1]	SERCOM5/PAD[1]	TC0/WO[1]	TCC0/WO[5]	USB/SOF 1kHz	GCLK_IO[7]	CCL2 IN[1]
23	33	45	PA24	VDDIO[6]	EXTINT[12]							SERCOM3/PAD[2]	SERCOM5/PAD[2]	TC1/WO[0]	TCC1/WO[2]	USB/DM		CCL2 IN[2]
24	34	46	PA25	VDDIO[6]	EXTINT[13]							SERCOM3/PAD[3]	SERCOM5/PAD[3]	TC1/WO[1]	TCC1/WO[3]	USB/DP		CCL2 OUT
	37	49	PB22	VDDIN	EXTINT[6]								SERCOM5/PAD[2]	TC3/WO[0]			GCLK_IO[0]	CCL0 IN[0]
	38	50	PB23	VDDIN	EXTINT[7]								SERCOM5/PAD[3]	TC3/WO[1]			GCLK_IO[1]	CCL0 OUT
25	39	51	PA27	VDDIN	EXTINT[15]												GCLK_IO[0]	
31	45	57	PA30	VDDIN	EXTINT[10]								SERCOM1/PAD[2]	TCC1/WO[0]		CORTEX_M0P/SWCLK	GCLK_IO[0]	CCL1 IN[0]
32	46	58	PA31	VDDIN	EXTINT[11]								SERCOM1/PAD[3]	TCC1/WO[1]		SWDIO [4]		CCL1 OUT
		59	PB30	VDDIN	EXTINT[14]								SERCOM5/PAD[0]	TCC0/WO[0]	TCC1/WO[2]			
		60	PB31	VDDIN	EXTINT[15]								SERCOM5/PAD[1]	TCC0/WO[1]	TCC1/WO[3]			
		61	PB00	VSWOUT	EXTINT[0]		AIN[8]						SERCOM5/PAD[2]	TC3/WO[0]			SUPC/PSOK	CCL0 IN[1]
		62	PB01	VSWOUT	EXTINT[1]		AIN[9]						SERCOM5/PAD[3]	TC3/WO[1]			SUPC/OUT[0]	CCL0 IN[2]
	47	63	PB02	VSWOUT	EXTINT[2]		AIN[10]						SERCOM5/PAD[0]	TC2/WO[0]			SUPC/OUT[1]	CCL0 OUT
	48	64	PB03	VSWOUT	EXTINT[3]		AIN[11]						SERCOM5/PAD[1]	TC2/WO[1]			SUPC/VBAT	

Note:

1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.