## 0.1 NAND Gate

A two-input NAND circuit is constructed on the bread board using the CD4007 gate array.

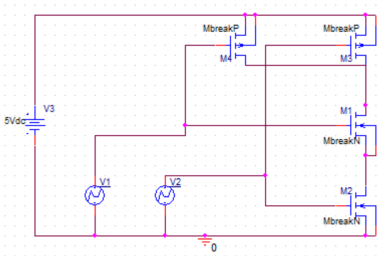


Figure 1: Layout of Two-input NAND Gate

The two-input NAND gate has following logic chart (or truth table) where $x$ and $y$ are inputs and $S$ is the output and 0 corresponds to low and 1 corresponds to high. The output voltage is taken at the drain node of the NMOS M1 in Figure 1.

Table 1: Logic Chart of Two-input NAND Gate

| x | y | S |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The behavior of the NAND gate circuit is not tested using the oscilloscope due to complications in its construction on the bread board. However, the behavior of the circuit is expected to be consistent with Figure 1 where 0 and 1 correspond to low and high output voltages, respectively. The following SPICE simulation shows the expected behavior of the NAND gate circuit.

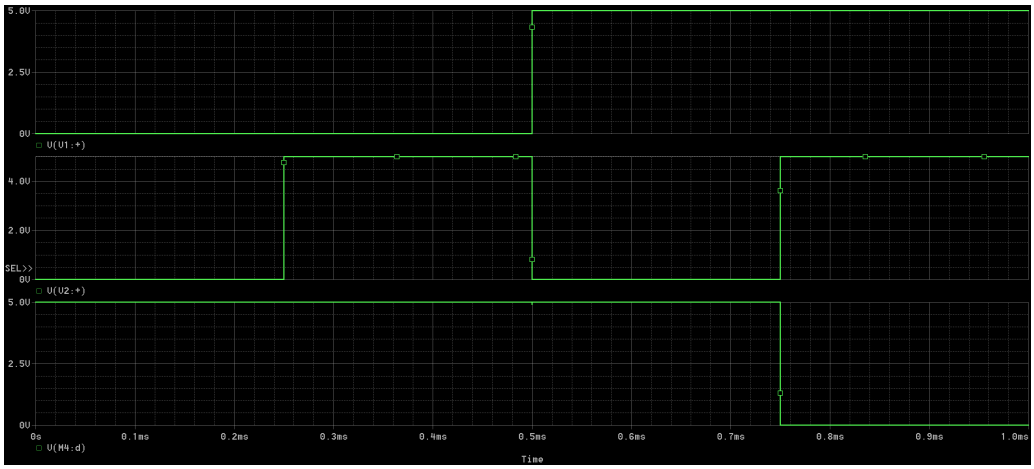


Figure 2: Simulated NAND Circuit Behavior

The top plot shows $V_1$, which is a input square wave $(0 - 5\text{V})$ with a 1kHz frequency. The middle plot shows $V_2$, which is a input square wave $(0 - 5\text{V})$ with a 2kHz frequency. Lastly, the bottom plot shows the output waveform of the two-input NAND circuit. Figure 2 effectively shows that the behavior of the circuit does match the truth table in Figure 1.

## 0.2 NOR Gate

The CD4007 gate array was used to make a two-input NOR gate.

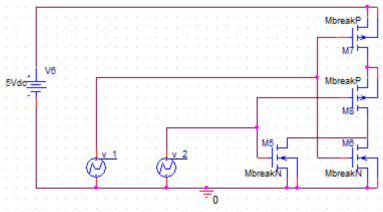


Figure 3: The two-input NOR gate circuit.

The two-input NOR gate operates such that the output will be high only when both inputs are low. Otherwise, the output will be low. It can be shown from the circuit above that $V_1$ and $V_2$ serve as the inputs and $V_{out}$ is taken across the drain of $M8$ to the ground.

| x | y | S |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Table 2: Logic of the two-input NOR gate.

The analysis of this circuit shows that the behavior of the two-input NOR gate is consistent with our logic table and our expectations. The figure below shows the results of the NOR gate simulation.

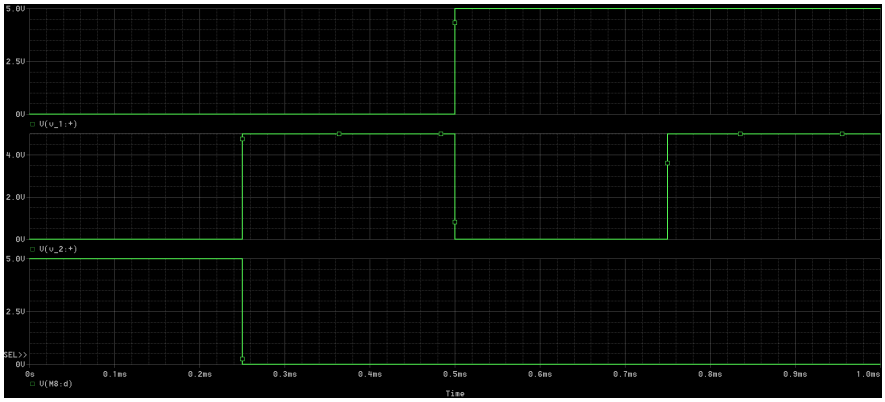


Figure 4: Simulation output of the NOR gate.

Using $V_1$ and $V_2$ as the inputs, we see that the output, $M8$, of our NOR gate will only be high when both inputs are low. This proves that our expectations for the NOR logic and circuit structure are correct; however, this is still a simulation. Due to some complications with the CD4007 and breadboard, the results are only available from a SPICE simulation.