Lab 6: Introduction to Digital Circuits - CMOS Inverter

EECS 170LB

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1 Introduction

The voltage transfer characteristic and propagation delays of a CMOS inverter are analyzed. The CMOS inverter is then designed using a layout editor so position and dimension specific parameters can be accurately approximated. After analyzing the properties of an integrated circuit MOSFET in the layout editor, CMOS inverters of different dimensions are analyzed. The effects of transistor widths on propagation delays and voltage transfer characteristics are approximated.

2 Procedure and Results

2.1 CMOS Inverter Circuit

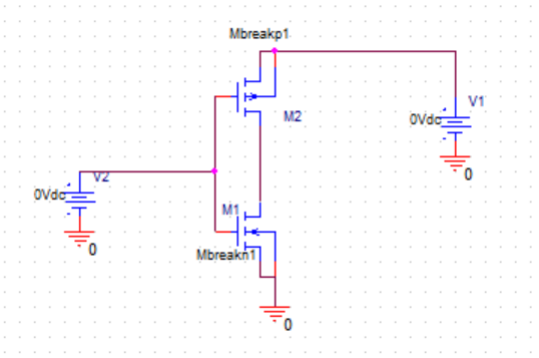

Figure 1: CMOS Inverter Circuit

A DC sweep simulation is run to determine the voltage transfer characteristic for the CMOS inverter circuit in figure (1).

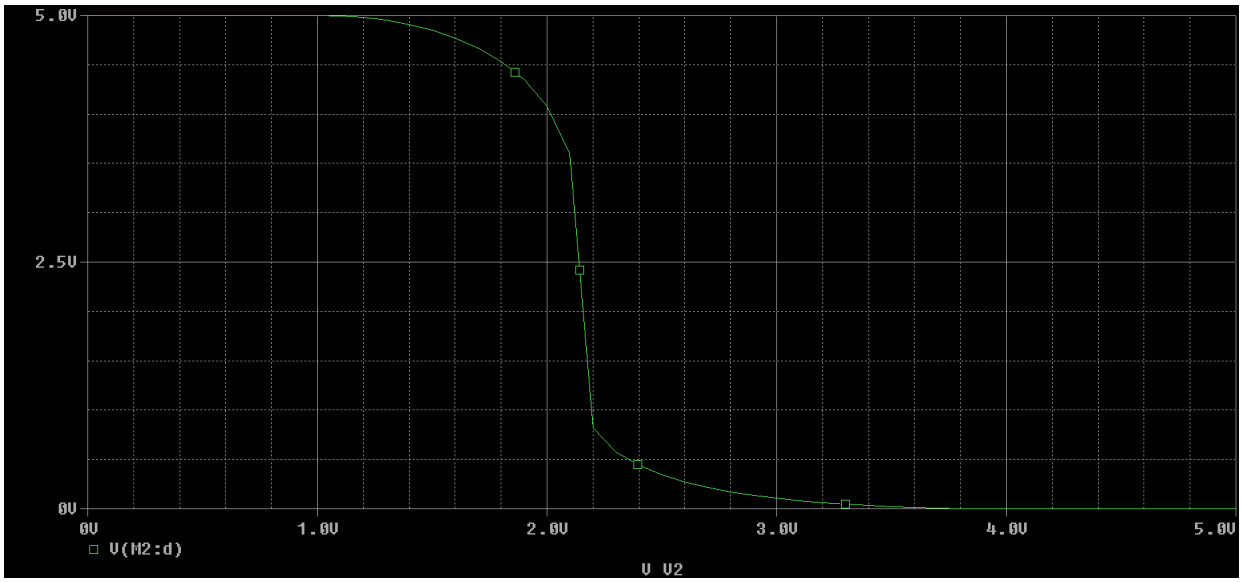

Figure 2: Figure (1) Circuit Voltage Transfer Characteristic

At low input gate voltages, "low" meaning "close to ground", V_{GS} for the NMOS on the bottom drops below its threshold voltage. Therefore, no current flows through the NMOS transistor. However, V_{SG} for the PMOS on the top exceeds its threshold voltage. As a result, the PMOS transistor is on and sets the output voltage to the supply voltage. If a load capacitance is connected to the output of the inverter, it is charged to the supply voltage, in this case 5V.

At high input gate voltages, "high" meaning "close to supply", V_{GS} for the NMOS exceeds its threshold voltage, and the output voltage node is grounded. However, the PMOS is turned off since the input gate voltage is close to its source voltage. Because the output voltage is high when the input voltage is low and the output voltage is low when the input voltage is high, the circuit essentially "inverts" the input, hence the name "inverter". Assuming the output voltage is a continuous function of the input voltage, the CMOS inverter gradually moves from supply to ground as the input gate voltage is increased.

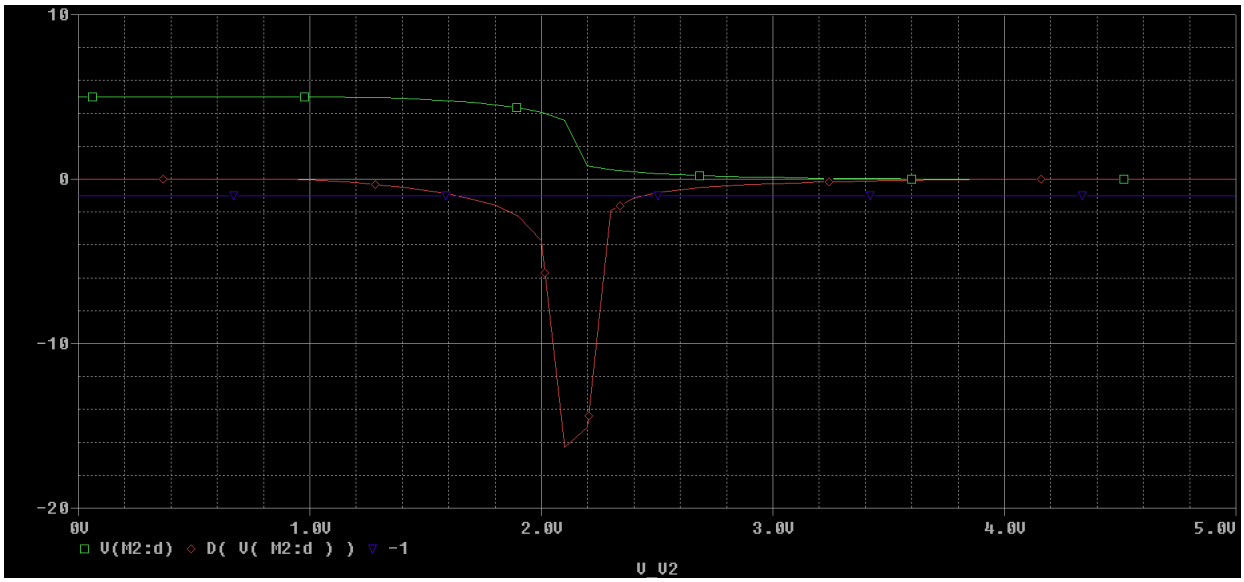

Figure 3: CMOS Inverter Noise Margin Measurement

The green curve is the voltage transfer characteristic. The red curve is $\frac{dV_{out}}{dV_{in}}$. The blue line is simply the value -1. The x-coordinate of the first point of intersection of the red and blue lines is V_{IL}. The x-coordinate of the second intersection is V_{IH}.

The noise margins NM_L and NM_H for the CMOS inverter can be acquired from analyzing its voltage transfer characteristic (VTC). Let V_{IL} be the point at which the slope of the VTC curve is -1 when the NMOS is turned off. V_{IL} is the highest value of input gate voltage such that the output can be correctly interpreted as a "1", or high voltage level. Past that point, the circuit no longer operates as an inverter and begins to act more as a voltage amplifier. Similarly, let V_{IH} be the point at which the slope is -1 when the PMOS is turned off. V_{IH} is the minimum gate input voltage such that the output is correctly interpreted as a "0". V_{OH} is the inverter's output voltage when the input voltage is grounded. V_{OL} is the output when the input is set to supply. The noise margins are then defined by the following equations:

$$NM_L = V_{IL} - V_{OL} \tag{1}$$

$$NM_H = V_{OH} - V_{OL} \tag{2}$$

Regarding equations (1) and (2), NM_L and NM_H are the largest voltage levels of noise that can be introduced to the inverter's output before its logic level is incorrect. V_{OL} and V_{OH} are clearly 0V and 5V from the VTC curve. V_{IH} and V_{IL} can be determined by analyzing the points at which the slope of the VTC is -1. This is what figure (3) depicts. So, $V_{IL} = 1.6340$V, and

$V_{IH} = 2.4438$V. Therefore, the noise margins are given by $NM_L = 1.6340$V and $NM_H = 2.5562$V.

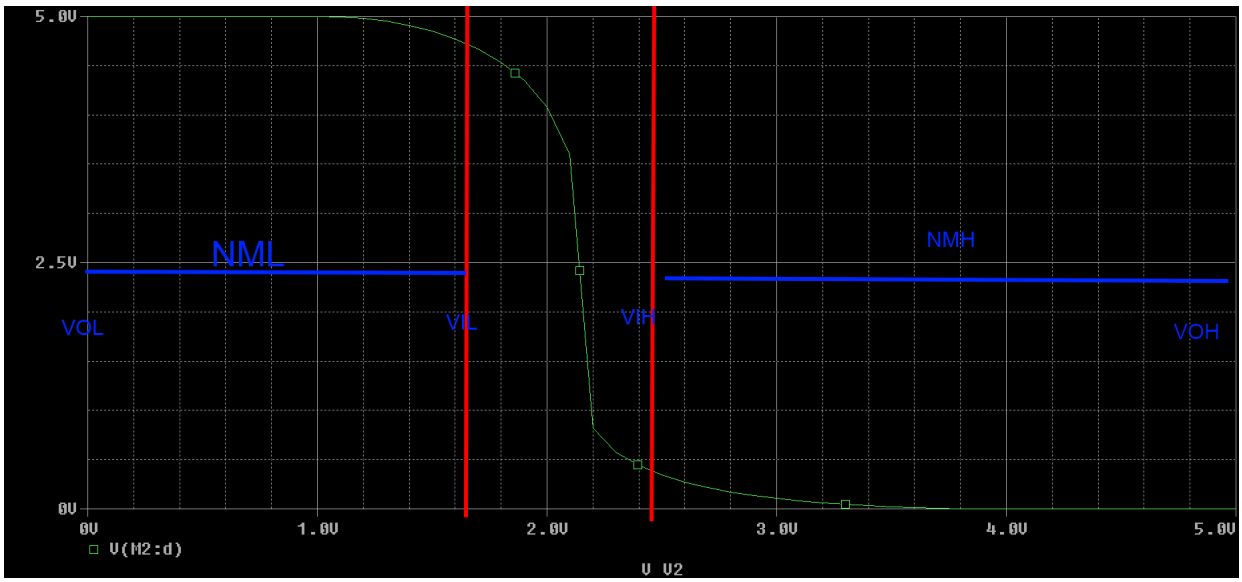

Figure 4: Depiction of Noise Margins on Voltage Transfer Characteristic

The CMOS inverter, unlike other inverters like common-source amplifiers, is designed for optimal noise margins. For other inverters, V_{OH} and V_{OL} do not fully reach supply and ground respectively. In the case of a common-source amplifier, when the input voltage is close to supply, the transistor operates in the triode mode. Therefore, the circuit operates like a voltage divider, and the output voltage does not fully reach ground. As a result, a lower noise voltage is required to flip an output "0" to the amplifier state or even a "1". However, in a CMOS inverter, one of the transistors is in cutoff when the output is a "1" or a "0". Therefore, the open circuit fully consumes the supply voltage, meaning the output voltage hits either supply or ground. Thus, it takes a higher noise voltage to cause the inverter's output to be incorrect.

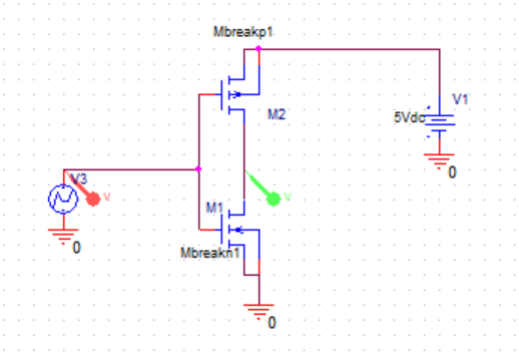

Figure 5: CMOS Inverter with Square-Wave Input

The circuit in figure (5) is used to observe the inverter's transient behavior.

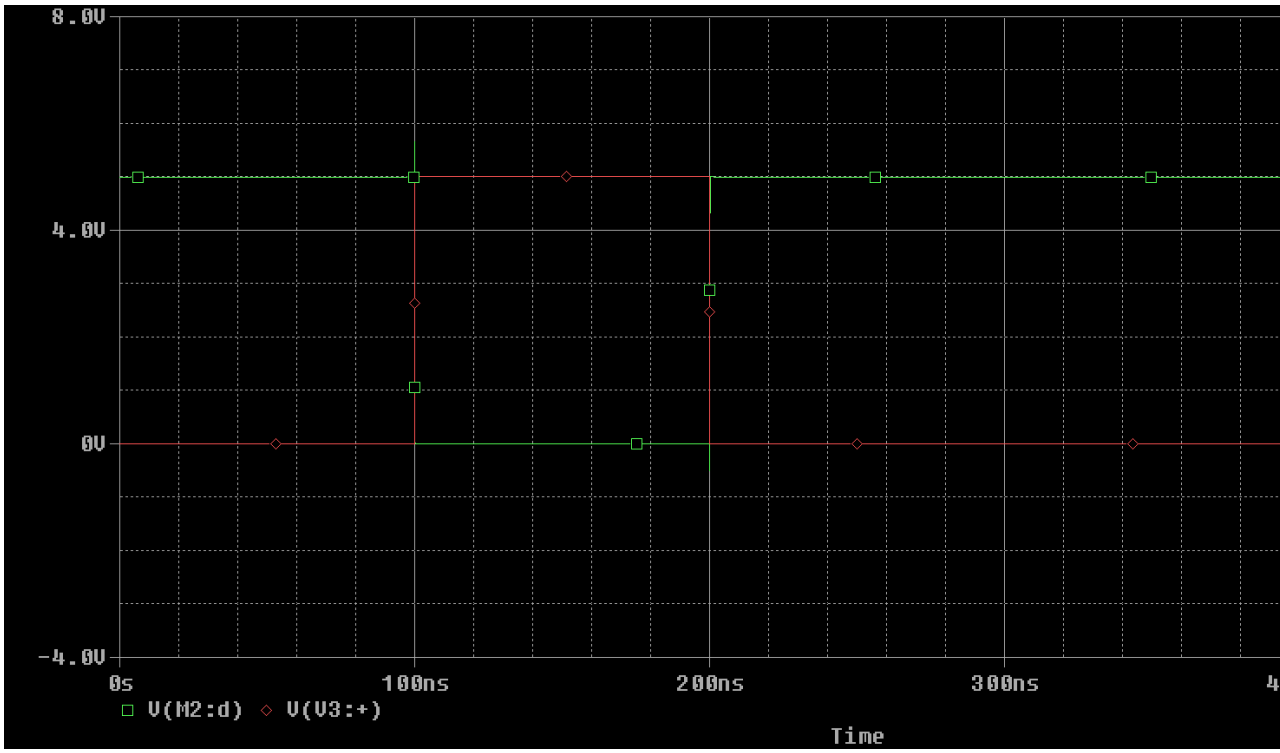

Figure 6: Transient Analysis of the Circuit in Figure (5)

The green curve is the output voltage, and the red curve is the input voltage.

The propagation delay can be ascertained from the transient response in figure (6). t_{PLH} is defined as the time it takes for the inverter's output to

transition from half the supply voltage to the supply voltage. t_{PHL} is the time it takes the inverter to transition from the supply voltage to half the supply voltage. The propagation delay is therefore defined by the following equation:

$$t_p = \frac{t_{PHL} + t_{PLH}}{2} \tag{3}$$

Because $t_{PHL} = 81$ps and $t_{PLH} = 103$ps, the propagation delay $t_p = 92$ps.

2.2 CMOS Inverter Layout

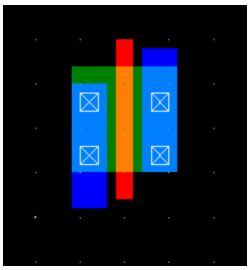

Figure 7: NMOS Layout

Figure (7) shows an NMOS transistor's layout. Figure (8) depicts the I_{DS} versus V_{DS} curve of the level 1 NMOS model.

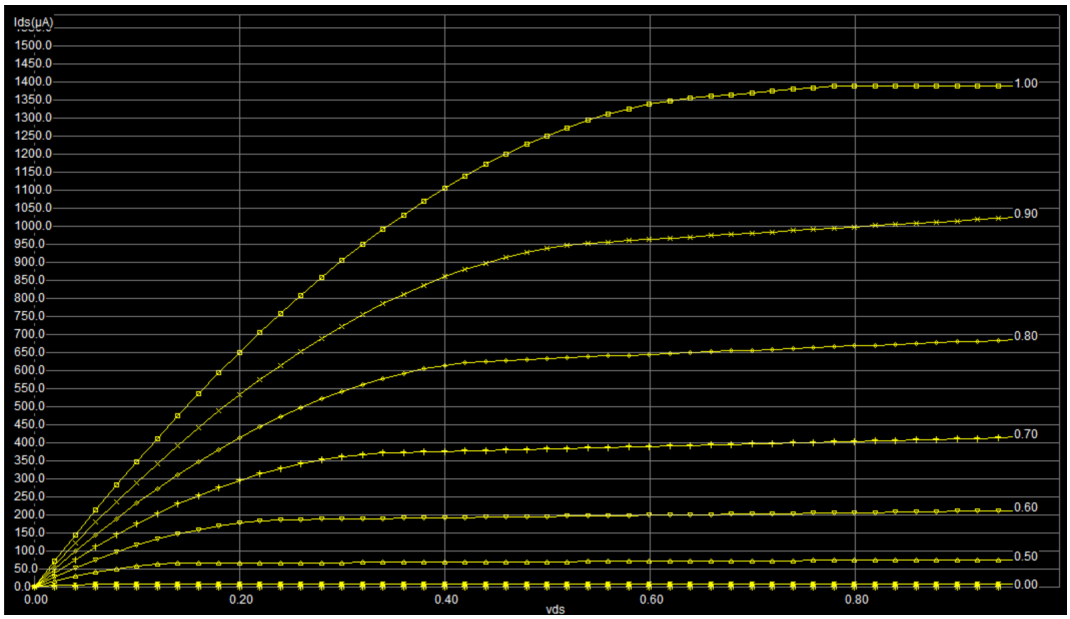

Figure 8: Level 1 NMOS Model

The L1 NMOS model is a standard transistor model that accounts for some channel length modulation effects (very slight slope in the saturation graph). When $V_{DS} = V_{GS} - V_T$, the current tapers off, and the MOSFET enters the saturation region.

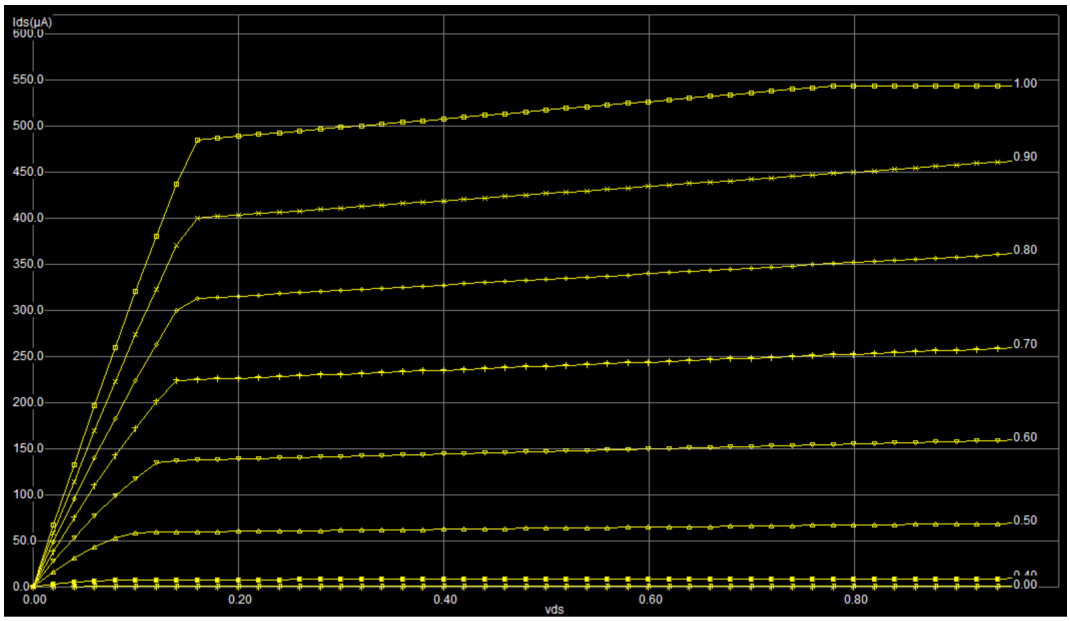

Figure 9: Level 3 NMOS Model

L3 is an improvement that accounts for effects that cause the transistor to enter saturation at lower voltages. This may be a short-channel effect in integrated circuits. If the channel is sufficiently short, the depletion regions at the source and drains can extend into the channel. As a result, the transistor may enter saturation at lower voltages since the depletion regions extend into the channel at higher drain voltages in saturation. This is the cause of channel length modulation.

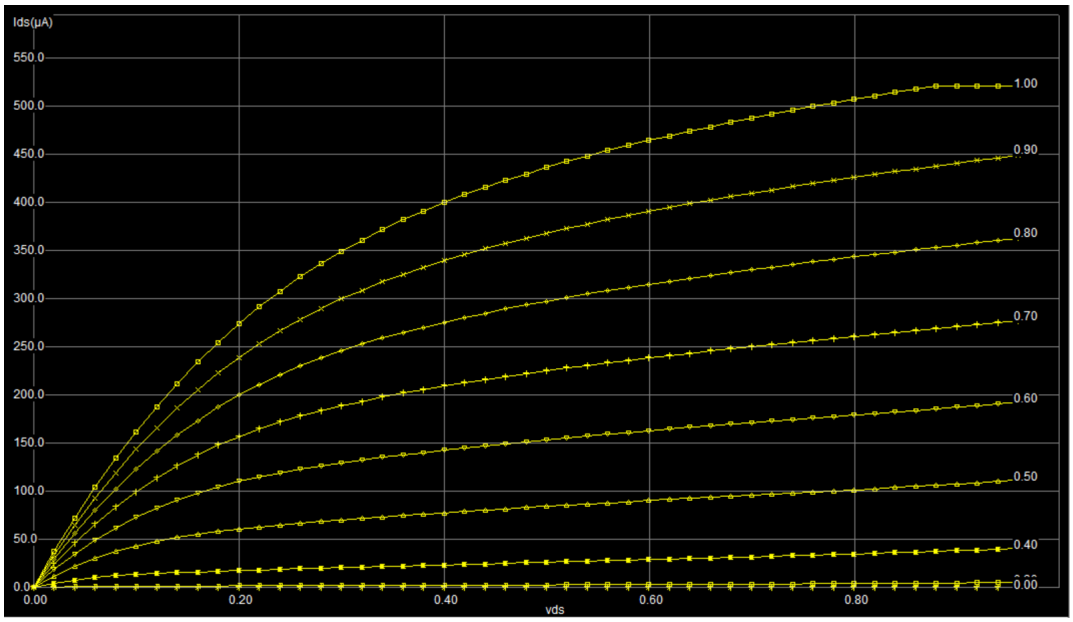

Figure 10: BSIM4 NMOS Model

The BSIM4 model accounts for channel length modulation, which explains why the current increases linearly with V_{DS} in saturation. However, it is much more complicated in nature than the other two models in terms of its level of sophistication. Level 3's triode region is quite linear. However, the model typically considered in lab uses polynomial growth that depends on at least V_{DS}^2 and possibly V_{DS}^3 with channel-length modulation. The channel-length modulation effect in BSIM4 is a bit more pronounced than it is typically in the models used in the course. From these plots, level 1 seems to be the closest to the currently used transistor model. However, the i_D vs V_{GS} plots give a clearer view.

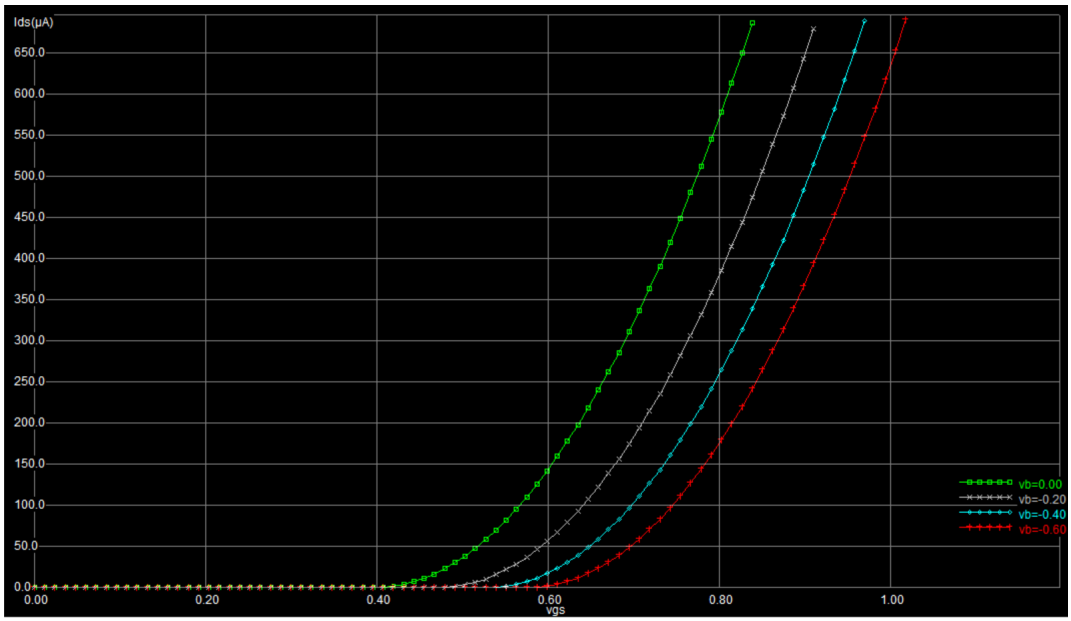

Figure 11: Level 1 i_D versus V_{GS}

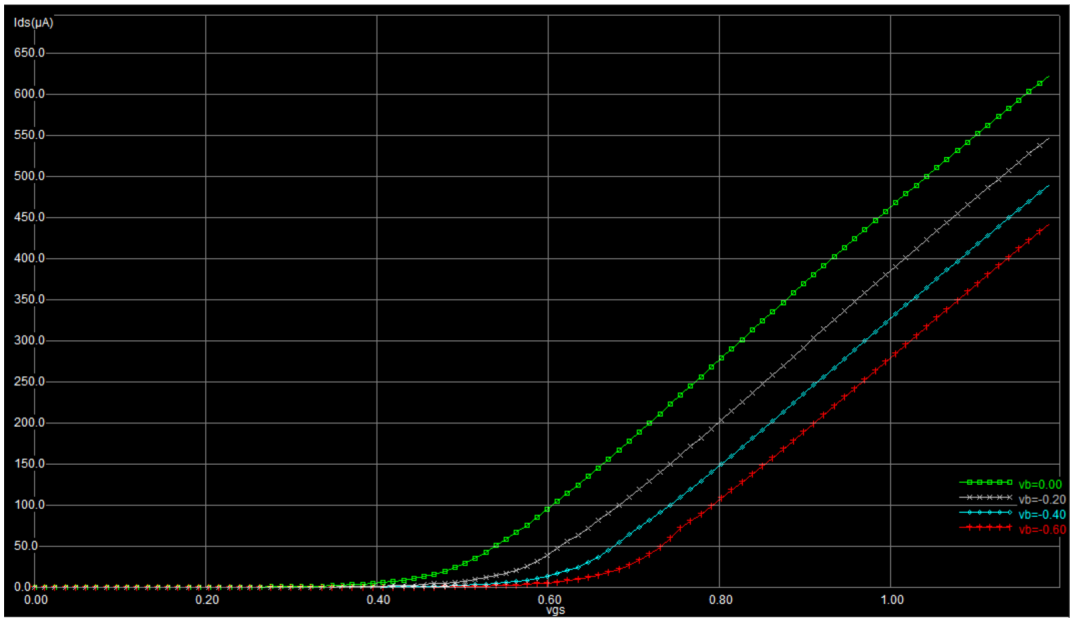

Figure 12: Level 3 i_D versus V_{GS}

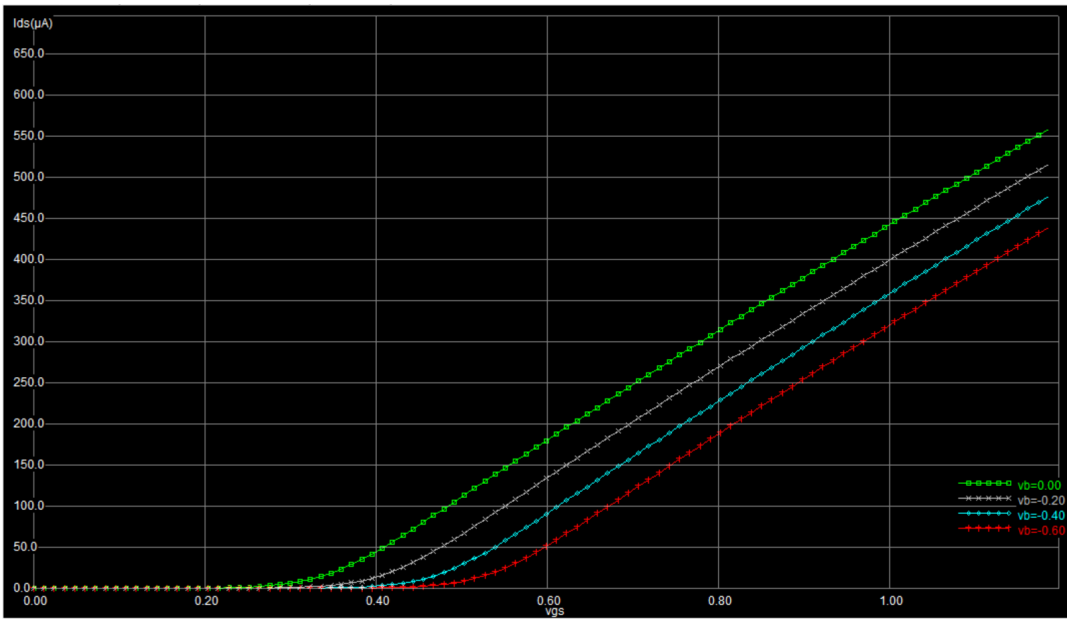

Figure 13: BSIM4 i_D versus V_{GS}

The level 1 model follows the quadratic relationship expected for the plot, whereas the other plots are more linear. Therefore, the level 1 MOSFET model is closest to the one typically used in the course.

The body effect in a MOSFET occurs when the body is not grounded. Typically, the NMOS body is set to the lowest voltage in the circuit. However, if the body's voltage is decreased, it becomes harder to attract electrons to the body because the voltage is lower. Therefore, the threshold voltage increases as the body voltage is decreased because it now requires a higher gate voltage to attract the electrons to form the channel. This is evident from the transistor models.

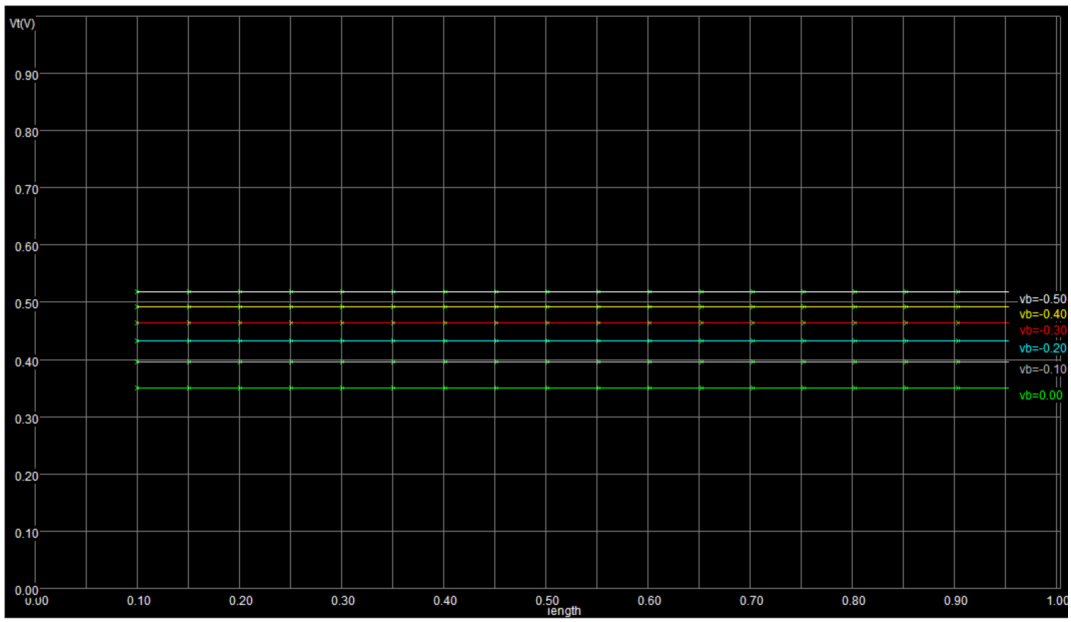

Figure 14: L1 NMOS Body Effect

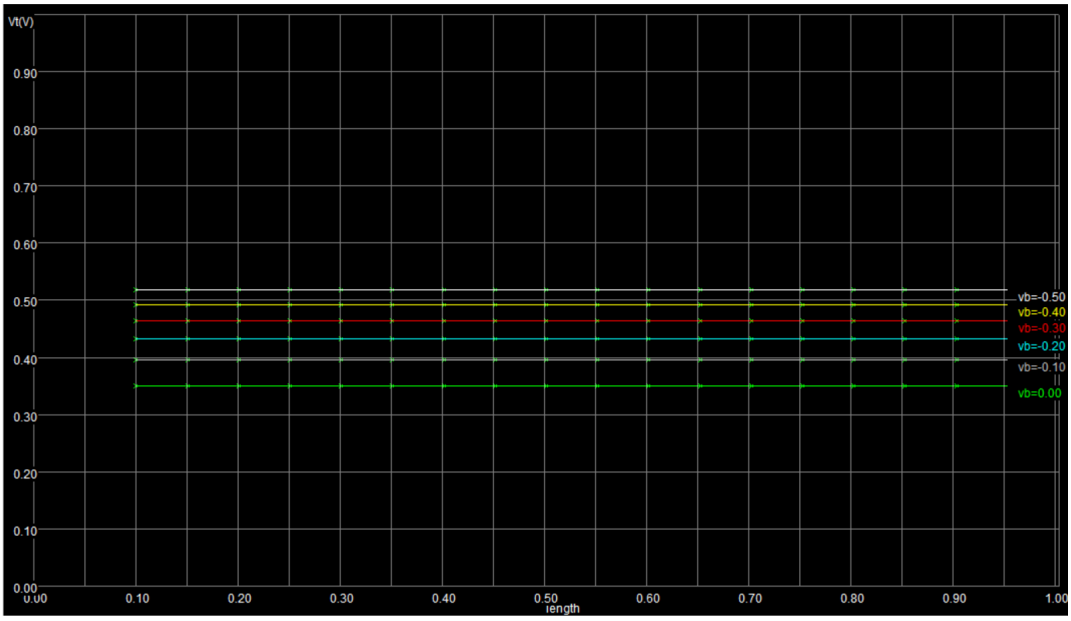

Figure 15: L3 NMOS Body Effect

The body effect observed in figures (14) and (15) is essentially the same. Decreasing the body voltage increases the threshold voltage. If the threshold voltage increases, the overdrive voltage drops, and the current therefore decreases. So, decreasing the body voltage decreases the current. In neither of these models does the body effect depend on the channel length.

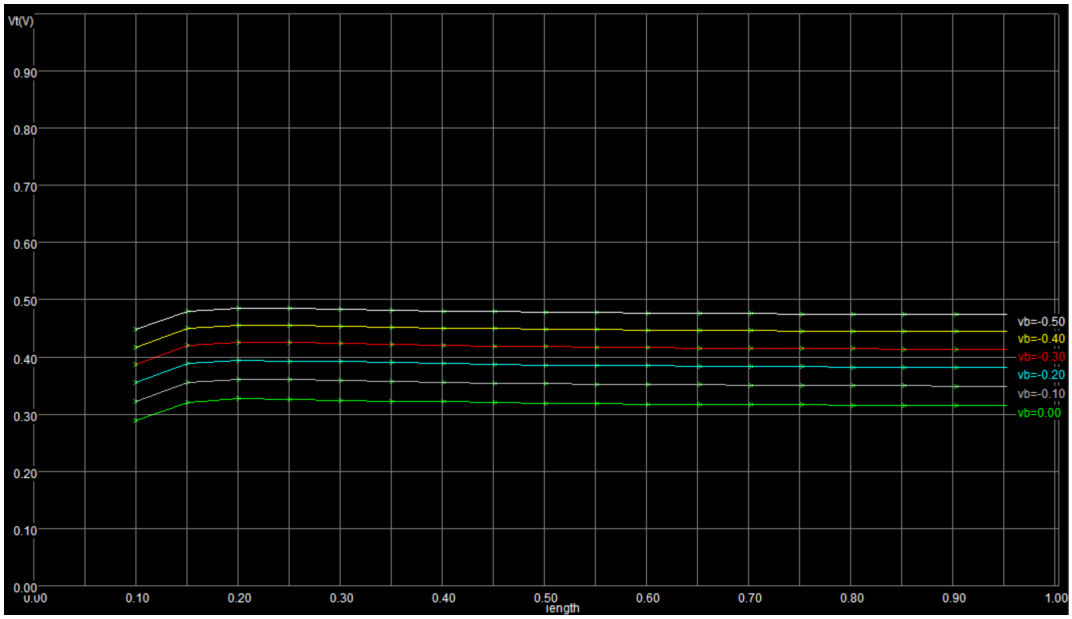

Figure 16: BSIM4 NMOS Body Effect

The BSIM4 model accounts for effects that occur in submicron processes when the channel length becomes very short. The threshold voltage drops when the channel length is very short. This might be because the depletion layers from the source and the drain help facilitate the motion of charges in the channel, meaning fewer charges and therefore a lower gate voltage is required to sustain an adequate current. The SPICE model typically used in lab does not seem to contain information on such short-channel effects, but does contain information about junction capacitances with the body, meaning that it probably accounts for some body effects. Again, level 1 seems closest to the SPICE model provided, whereas level 3 and especially BSIM4 are much more sophisticated.

If the oxide layer thickness is increased, the MOS capacitor's capacitance is decreased. Thus, for the same applied gate voltage, less charge accumulates in the channel. Therefore, ceteris paribus, the current should decrease if the oxide layer thickness is increased.

The MOSFET model used in the course is somewhat accurate and captures some nonidealities in a true integrated circuit MOSFET, such as channel-length

modulation. However, at deeper submicron processes, other short-channel effects come to play. These affect threshold voltages as well as the current. So, the MOSFET model can possibly be used for larger transistor processes, but more sophisticated models such as Level 3 or even BSIM4 are required for a modern integrated circuit design.

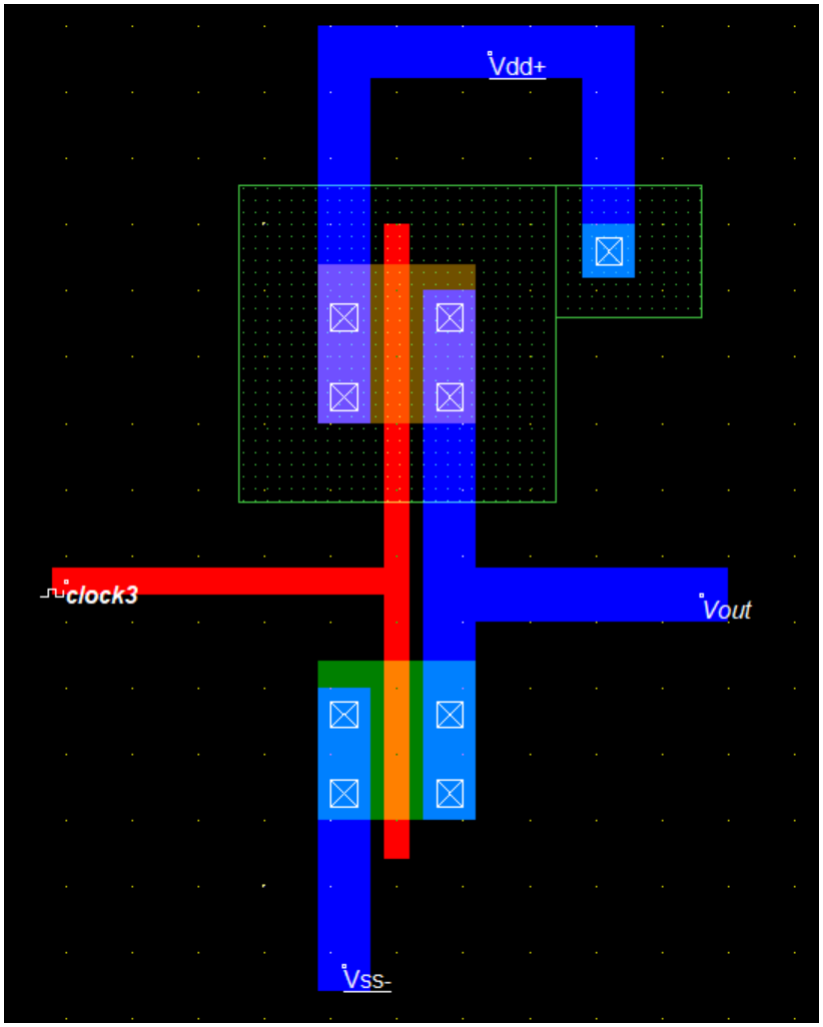

Figure 17: Layout of CMOS Inverter - 0.6µm Width for NMOS and PMOS

The CMOS inverter can be implemented in a true integrated circuit process, depicted in figure (17). The design depicted passes the design rule check.

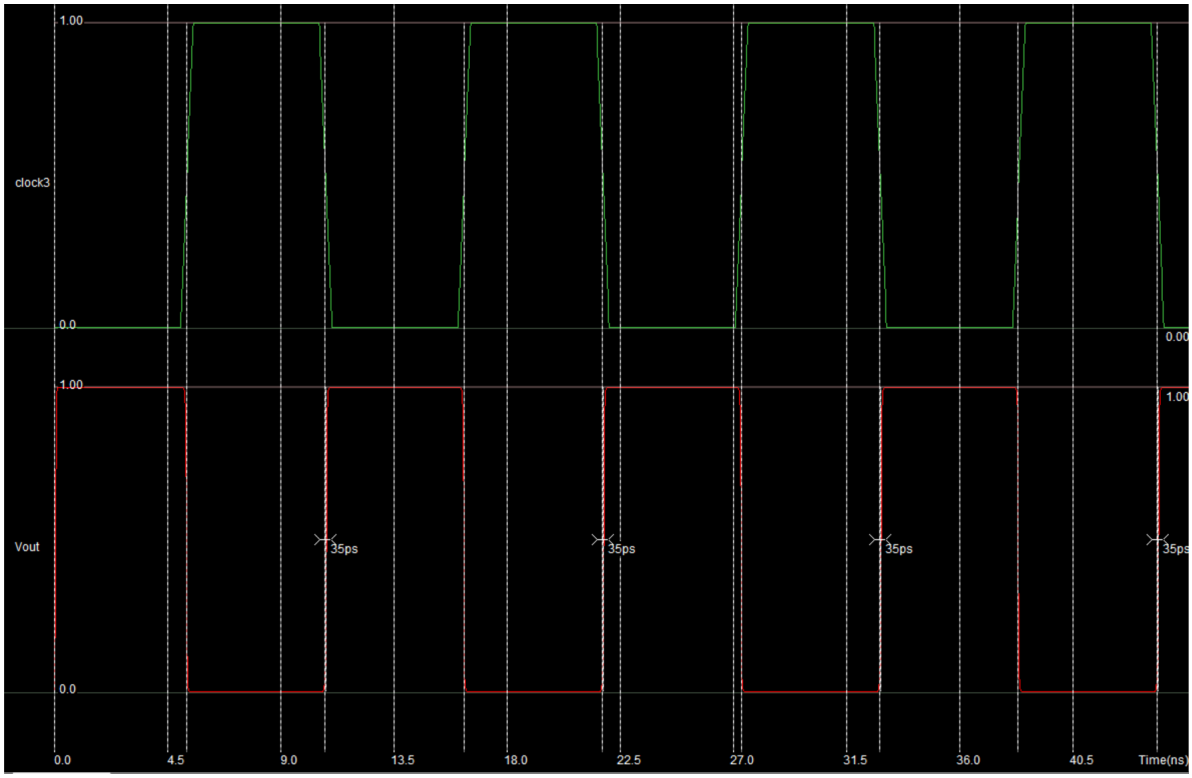

Figure 18: CMOS Inverter Layout Transient Response - 0.6µm Width for NMOS and PMOS

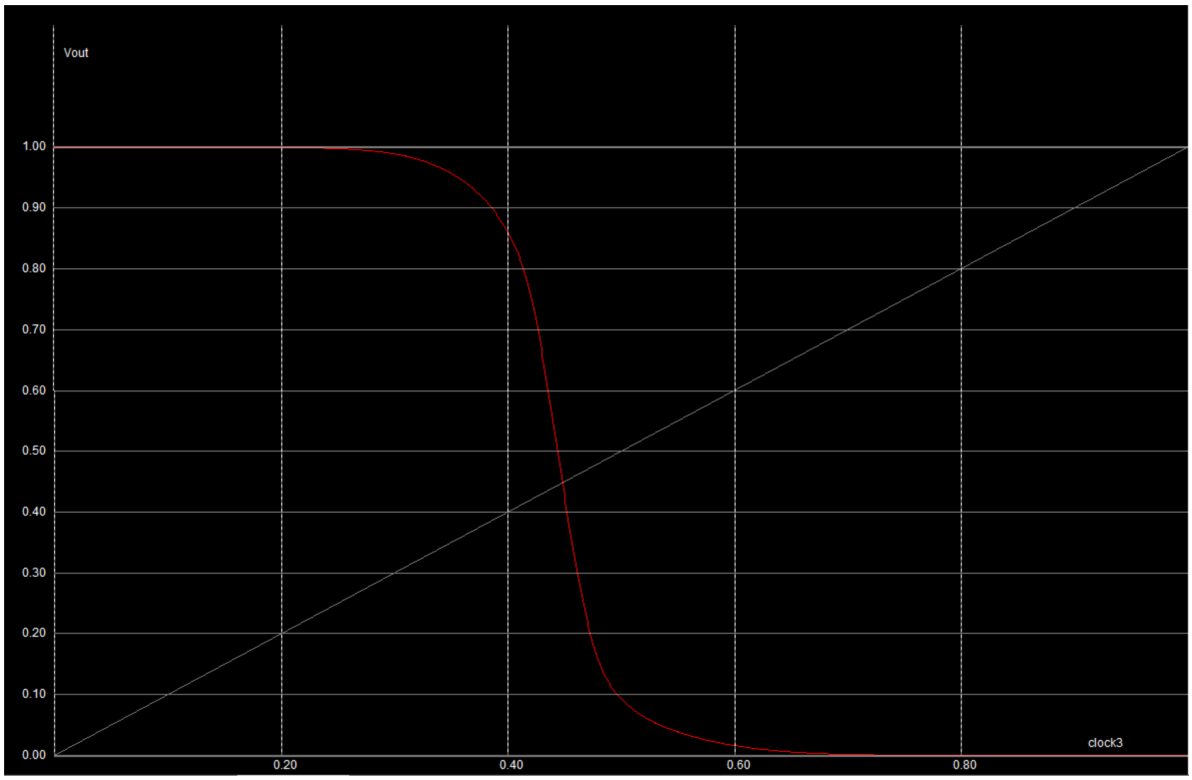

Figure 19: CMOS Inverter Layout Voltage Transfer Characteristic (VTC) - 0.6µm Width for NMOS and PMOS

Figure (18) presents the transient response of the inverter. Figure (19) depicts the voltage transfer characteristic. The nature of the results is similar to those presented in SPICE simulations earlier. Two inverters are then cascaded to observe the loading effects and changes in propagation delay.

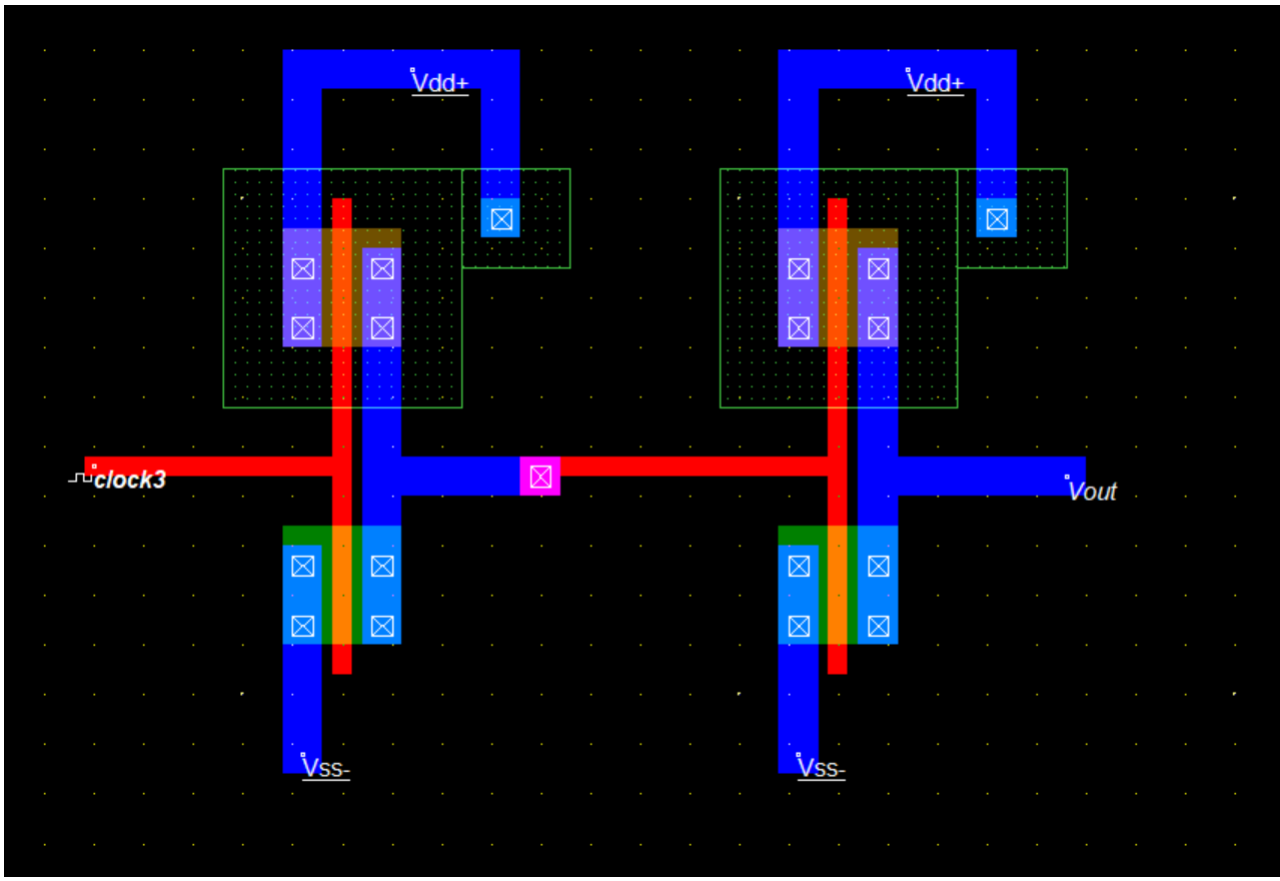

Figure 20: Cascaded Inverter Layout - 0.6µm Width for NMOS and PMOS

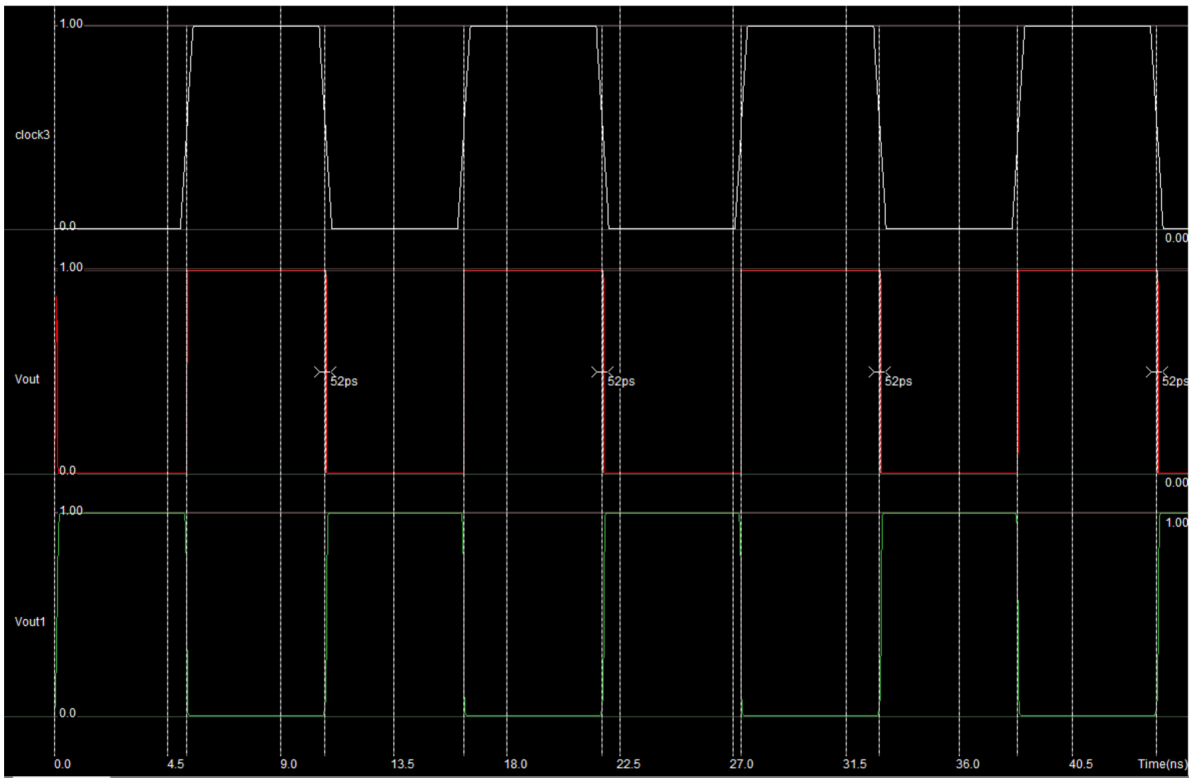

Figure 21: Cascaded Inverter Transient - 0.6µm Width for NMOS and PMOS

The results below are obtained when the NMOS width is kept the same, but the PMOS width is increased to 1.5µm.

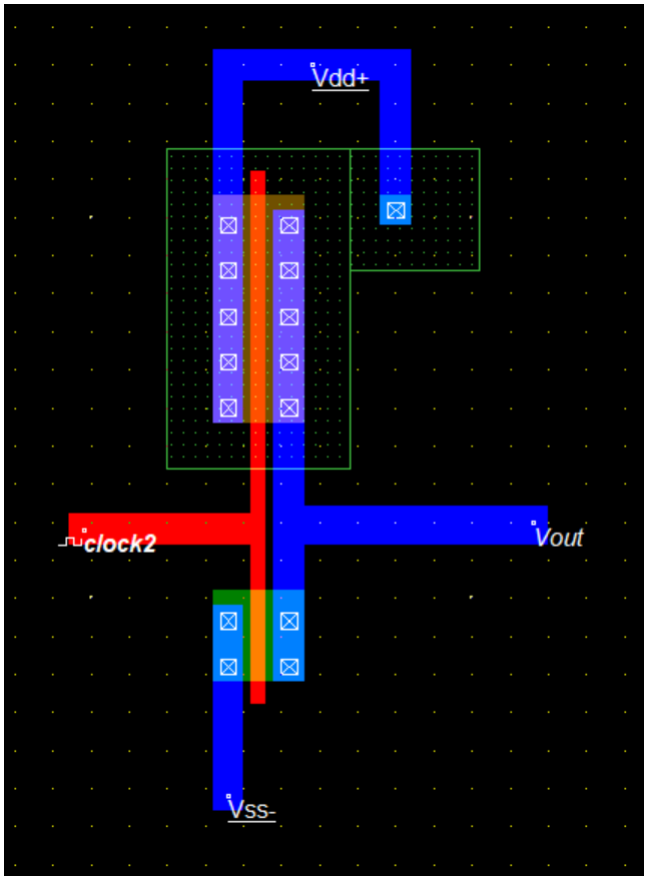

Figure 22: Layout of CMOS Inverter - 0.6µm Width for NMOS, 1.5 µm Width for PMOS

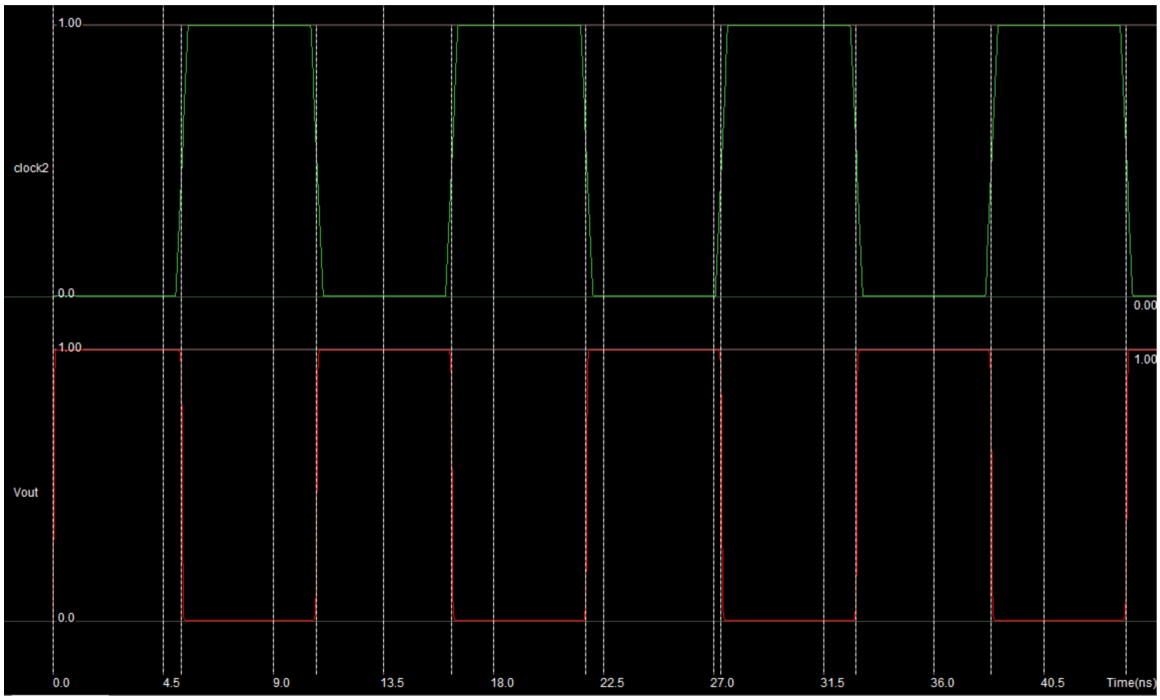

Figure 23: CMOS Inverter Layout Transient Response - 0.6µm Width for NMOS, 1.5 µm Width for PMOS

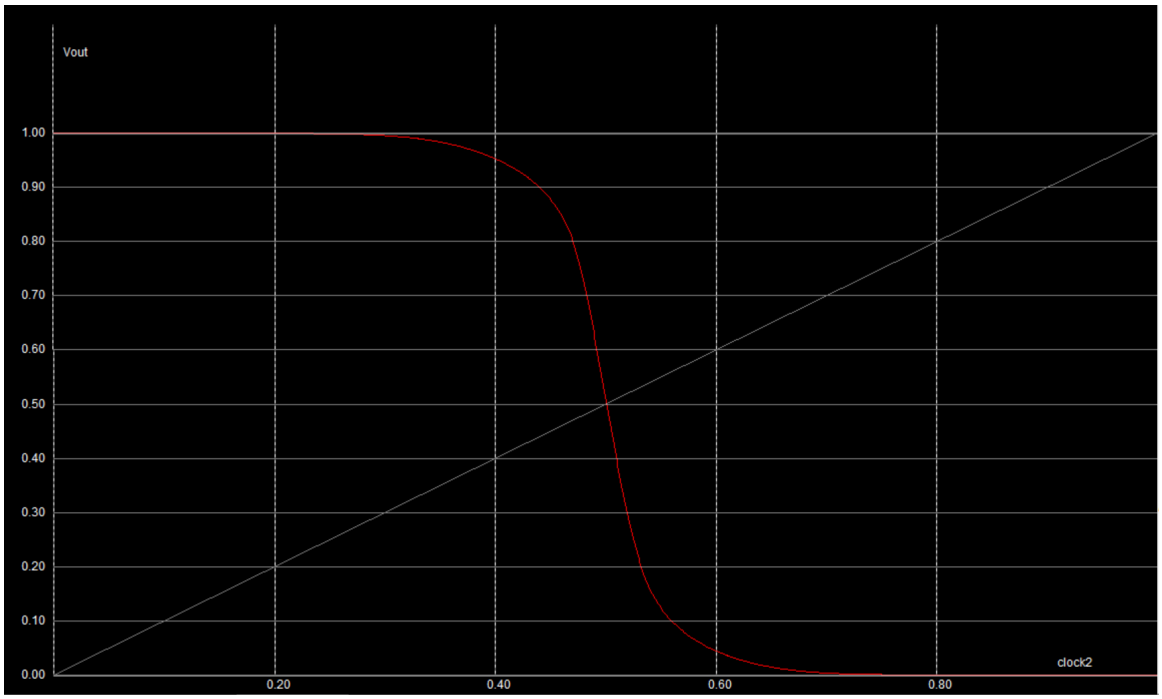

Figure 24: CMOS Inverter Layout Voltage Transfer Characteristic (VTC) - 0.6µm Width for NMOS, 1.5 µm Width for PMOS

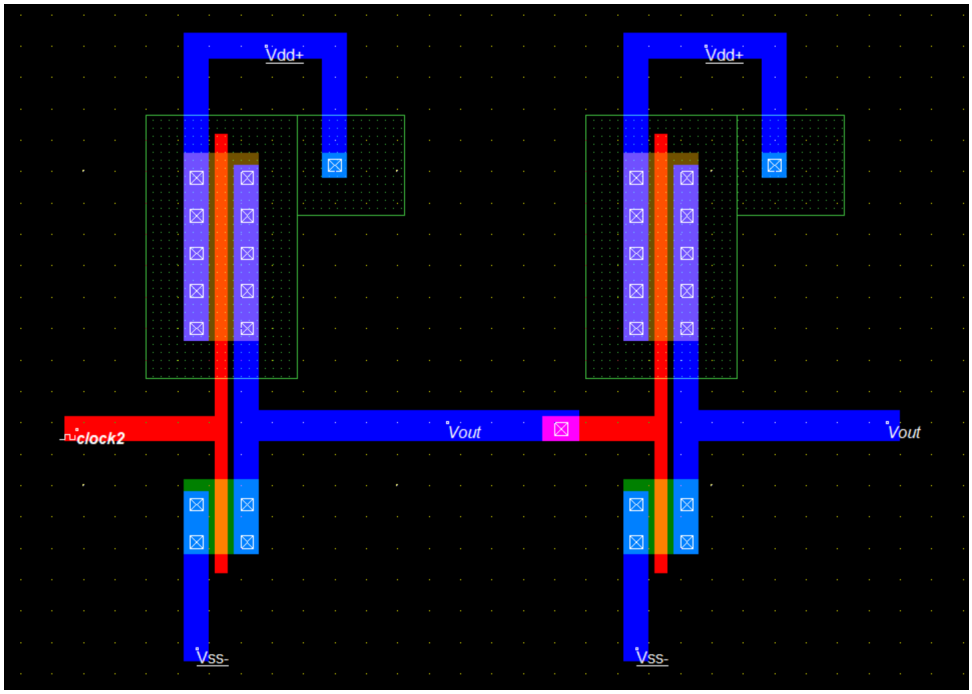

Figure 25: Cascaded Inverter Layout - 0.6µm Width for NMOS, 1.5 µm Width for PMOS

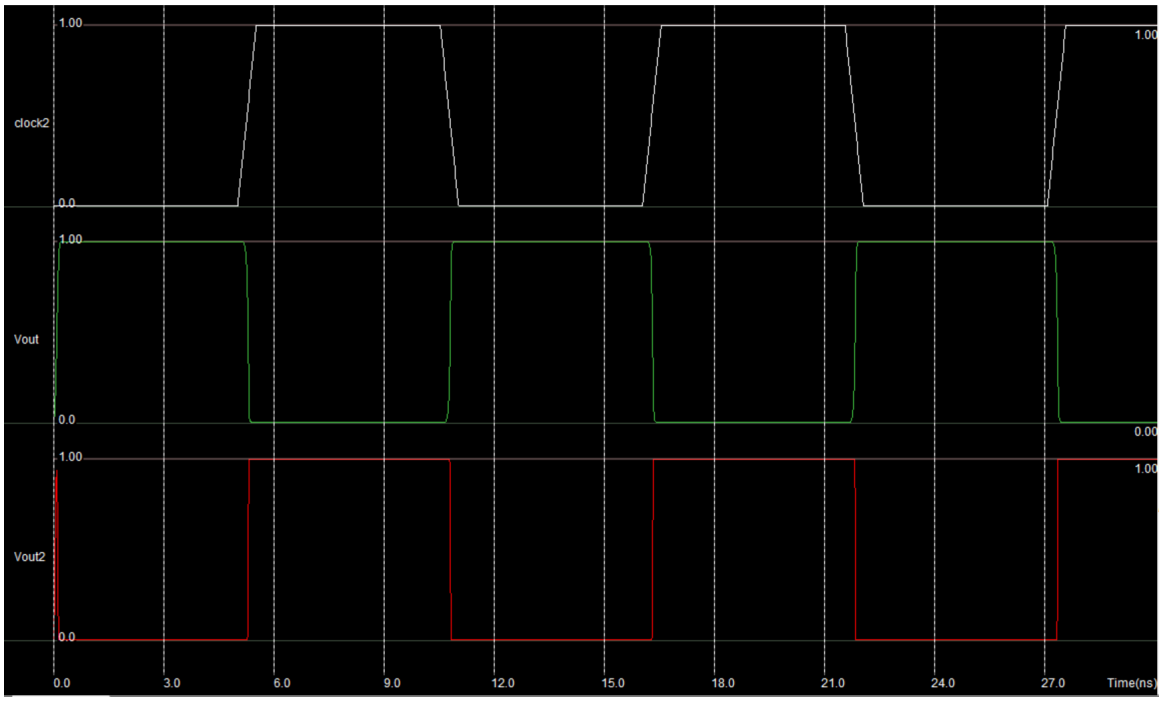

Figure 26: Cascaded Inverter Transient - 0.6µm Width for NMOS, 1.5 µm Width for PMOS

The widths of the NMOS and PMOS are then increased to 1.2µm and 3.0µm respectively.

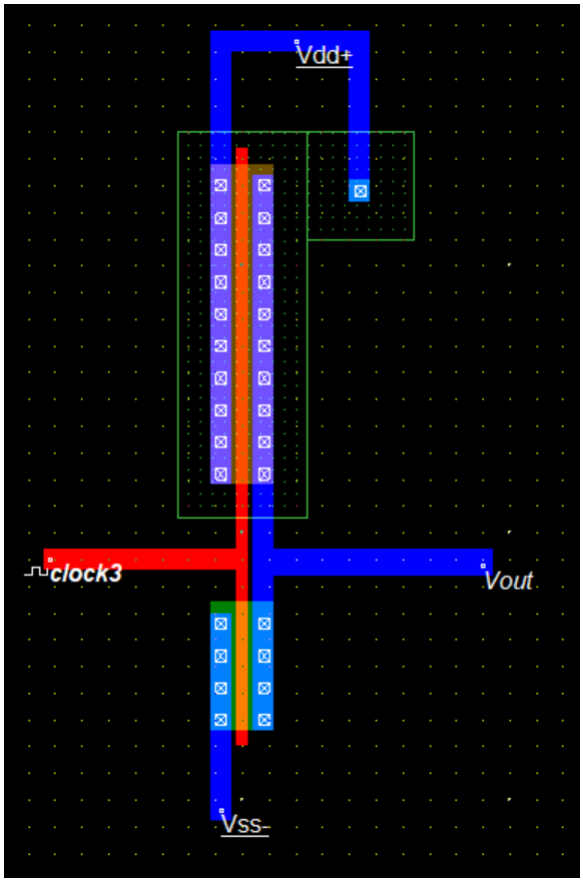

Figure 27: Layout of CMOS Inverter - 1.2µm Width for NMOS, 3.0 µm Width for PMOS

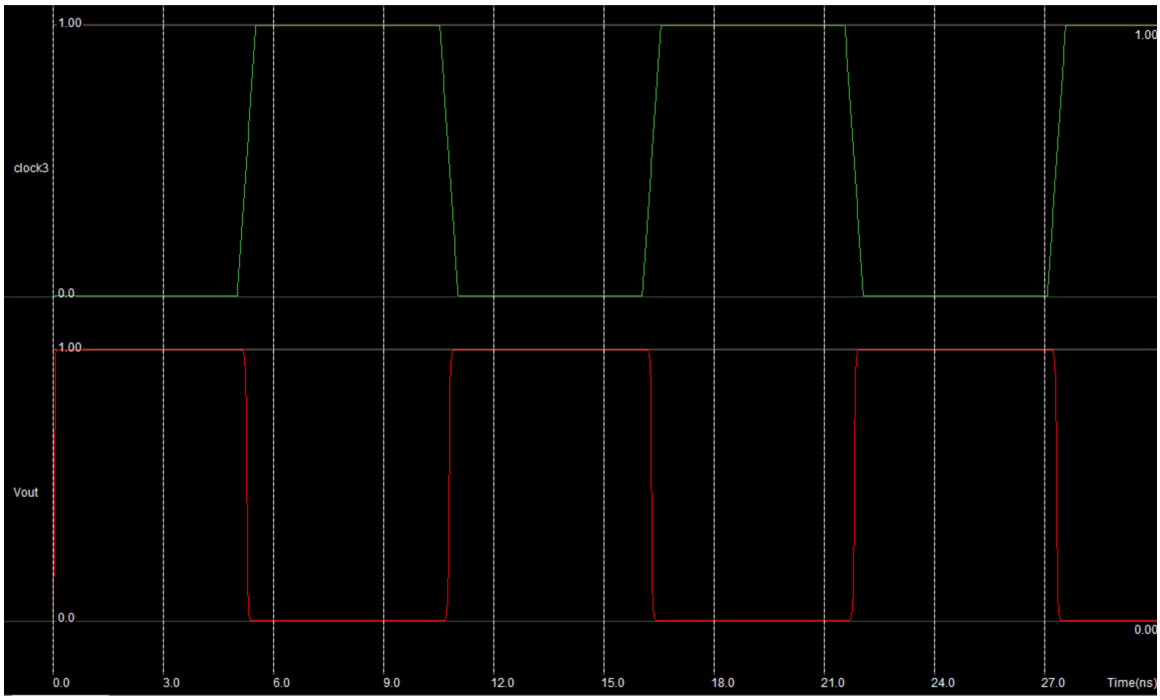

Figure 28: CMOS Inverter Layout Transient Response - 1.2µm Width for NMOS, 3.0 µm Width for PMOS

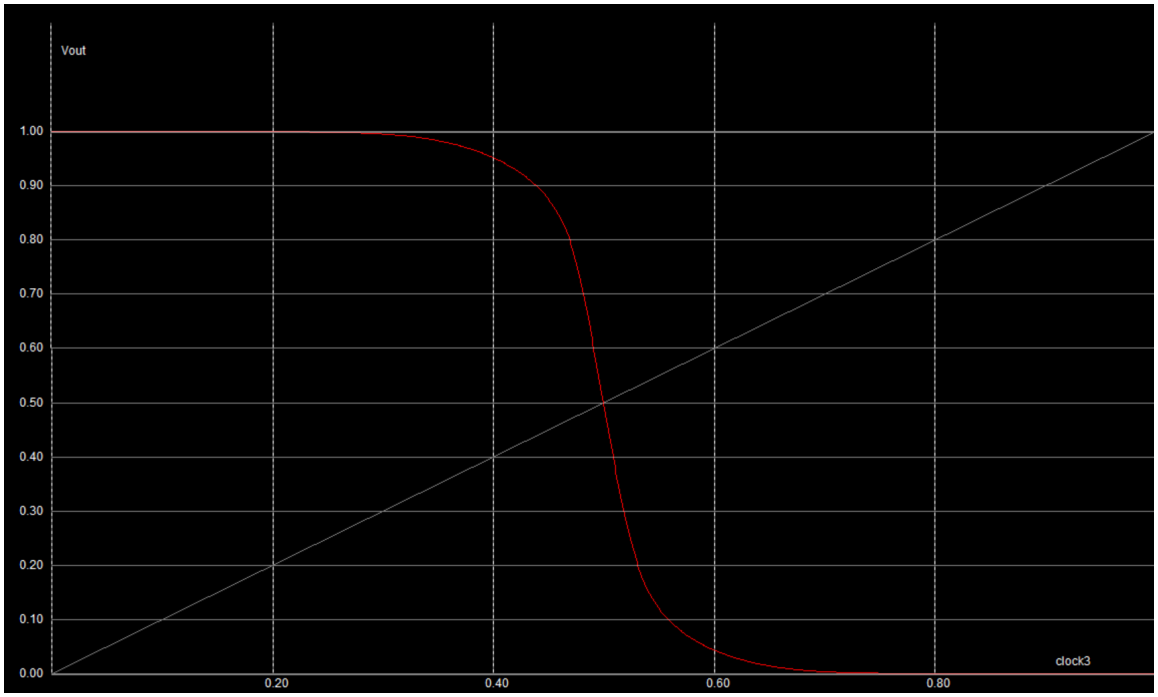

Figure 29: CMOS Inverter Layout Voltage Transfer Characteristic (VTC) - 1.2µm Width for NMOS, 3.0 µm Width for PMOS

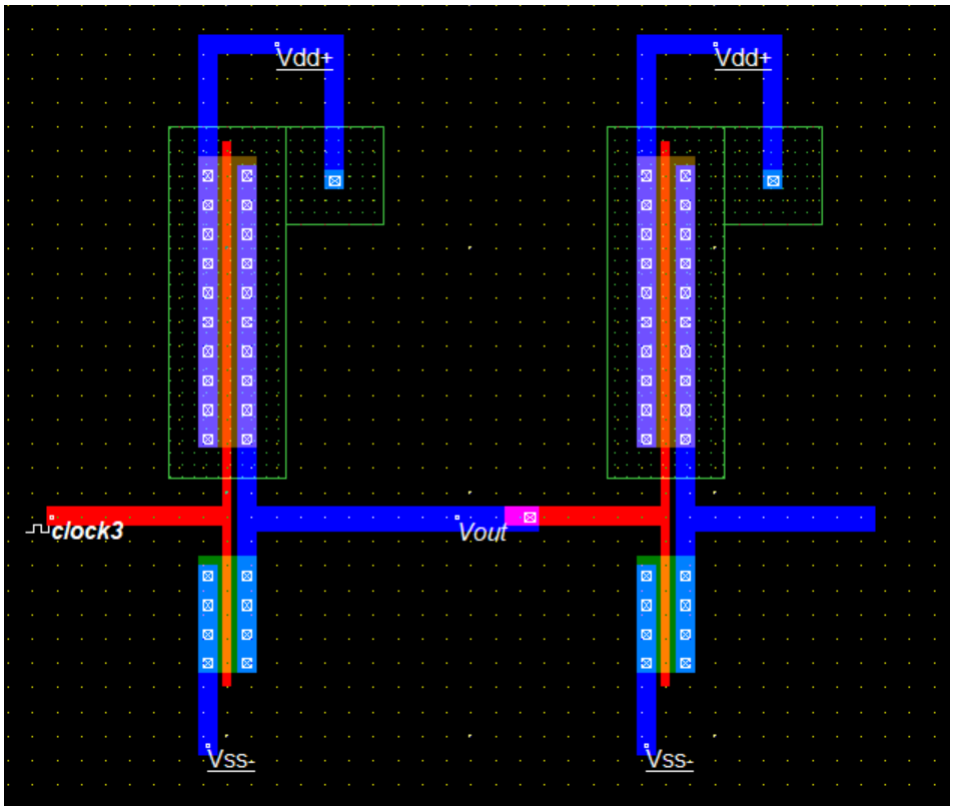

Figure 30: Cascaded Inverter Layout - 1.2µm Width for NMOS, 3.0 µm Width for PMOS

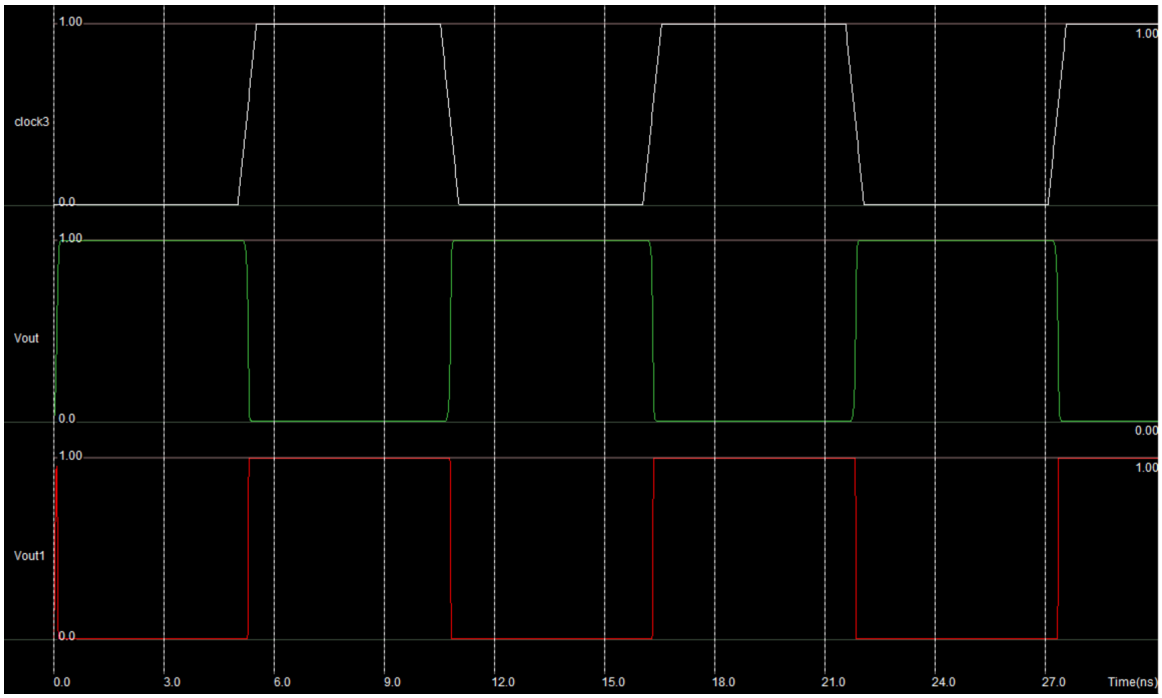

Figure 31: Cascaded Inverter Transient - 1.2µm Width for NMOS, 3.0 µm Width for PMOS

The propagation delays, t_{PHL}, t_{PLH}, and $t_P = \frac{t_{PHL}+t_{PLH}}{2}$, for the single inverter simulations are reported in table (1). t_P is calculated from t_{PHL} and t_{PLH}. t_{PHL} and t_{PLH} are taken directly from the simulation itself.

Table 1: Single Inverter Delays

Layout	tPLH [ps]	tPHL [ps]	tp [ps]
0.6um NMOS - 0.6um PMOS	35	21	28
0.6um NMOS - 1.5um PMOS	6	7	6.5
1.2um NMOS - 3.0um PMOS	6	5	5.5

The delays for the first inverter in the cascaded inverter simulation are reported in table (2).

Table 2: Cascaded Inverter Delays - First Inverter

Layout	tPLH [ps]	tPHL [ps]	tP [ps]
0.6um NMOS - 0.6um PMOS	52	6	29
0.6um NMOS - 1.5um PMOS	23	23	23
1.2um NMOS - 3.0um PMOS	22	22	22

The second inverter delays are taken with respect to the input of the first inverter. It is quite difficult to ascertain accurate delays for the second inverter relative to the first inverter's output from the simulation tool. t_{PLH} for the first simulation reported by the tool seems dubious due to the fact that it is only a mere 2ps, but the results demonstrate general trends. The values are reported in table (3).

Table 3: Cascaded Inverter Delays - Second Inverter

Layout	tPLH [ps]	tPHL [ps]	tP [ps
0.6um NMOS - 0.6um PMOS	2	53	27.5
0.6um NMOS - 1.5um PMOS	23	27	25
1.2um NMOS - 3.0um PMOS	25	25	25

For the single inverter simulation, the delay drops considerably as the widths of the transistors are increased. The results taper off as widths are increased. There are various inherent delays in components due to parasitic inductances and capacitances of the wires and physical limitations on speed. So, a certain amount of delay must always exist. Increasing widths should then become less effective as the widths become very large. By "delay", the amount of time it would take to charge a load capacitance connected at the output, such as the MOS capacitors of the next stage of transistors as well as parasitic capacitances, is implied. So, if the transistors are able to drive more current to the load capacitance, then the load charges more quickly, and the delay drops. So, the reason the delay drops is because increasing the width of the transistor allows more charge per unit time to flow, causing larger currents to more quickly charge a load. For the cascaded inverters, the first inverter's delay decreases, but not as much as it does in the single inverter delay measurements. When only one inverter is present, the voltage can quickly form at the output port after the gate voltage is set. It is limited only by some of the material properties of the transistors in the inverter. However, when an inverter is connected at the load, not only must the output current be generated, which takes time due to the formation of the channel, but the capacitances of the MOSFETs in the next inverter stage and the parasitic capacitances must be charged with that current. So, it takes a little bit longer for the voltage to form, which is why the delay is longer. The delay of the second inverter in the cascade from the input to the first inverter is generally not much longer, maybe by only a few picoseconds, than the delay of the first inverter. Once the voltage has formed at the input of the second inverter, it reduces to the case with a single inverter. So, by the same reasons as above, the voltage at the output should form more quickly than if it were a loaded inverter in an intermediary stage of two cascaded inverters.

When the PMOS inverter's width is made so that its transconductance parameter is balanced with the NMOS, the VTC shifts to the right. When the input to the inverter is low, the PMOS is enabled. PMOS transistors have holes as their charge carrier, and thus their mobility is lower than that of electrons

in the NMOS. So, in the 0.6µm for both NMOS and PMOS test, both have the same dimensions, and the NMOS's transconductance parameter is dominant. If the PMOS's transcondunctance parameter is relatively smaller, then the current it produces is relatively smaller. If the voltage is increased, the NMOS transistor begins to turn on and enter saturation. So, a current starts to flow through both transistors. However, the PMOS cannot support as large of a current. If the PMOS and NMOS are seen as resistors in this state, the PMOS would have a much larger equivalent resistance, and thus the NMOS would take up a smaller voltage drop, meaning V_{out} is smaller. So, V_{out} drops more quickly as V_{in} is increased because the PMOS quickly consumes a much larger voltage drop. When the transistor sizes are changed from 0.6µm for the PMOS and NMOS to 0.6µm for the NMOS and 1.5µm for the PMOS, the transistors are now more balanced, meaning their transconductance parameters are closer in magnitude. If this is the case, the currents that each can supply are comparable. If the voltage divider analogy is revisited, the "resistances" – in a sense – of each transistor are closer in magnitude than in the previous case. So, as V_{in} is increased, the NMOS transistor can sustain a higher voltage drop for longer than when the PMOS's "equivalent resistance" far outweighed the NMOS's. So, the VTC shifts to the right when the transistors become balanced as opposed to the previous unbalanced case. It should be noted that modeling either of these components as a resistor is not entirely accurate since their voltages are not linearly related to their currents, but the voltage divider analogy can be used to understand why the VTC shifts when the transistors move from NMOS having the dominant parameter to balanced parameters.

3 Conclusion

3.1 CMOS Inverter Circuit

The CMOS inverter is an inverter architecture that is optimized for noise and power consumption. This is because of the fact that inverter's output fully reaches supply and ground in either case. Propagation delays acquired are on the order of about 100ps.

3.2 CMOS Inverter Layout

Level 1, the simplest of all of the MOSFET models, is closest to the SPICE model typically used for simulations. Increasing the widths of transistors tends to increase the operating speed of the inverter. When the inverter is loaded, its propagation delay is seen to increase. In the 1.2µm NMOS - 3.0µm PMOS and 0.6µm NMOS - 1.5µm PMOS tests, the voltage transfer characteristic is shifted to the right from the 0.6µm NMOS and PMOS test. This is because the transistors are more balanced in that their transconductance parameters are closer. When the widths are equal, because the mobility of the carrier holes in the PMOS is much lower, the PMOS's transconductance parameter is much

lower, causing the transistors to be unbalanced and for the voltage transfer characteristic to not be as centered.