Experiment 8

MOS Transistors as Switches and Amplifiers

EECS 170A - Lab Bench #1

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1 Procedure

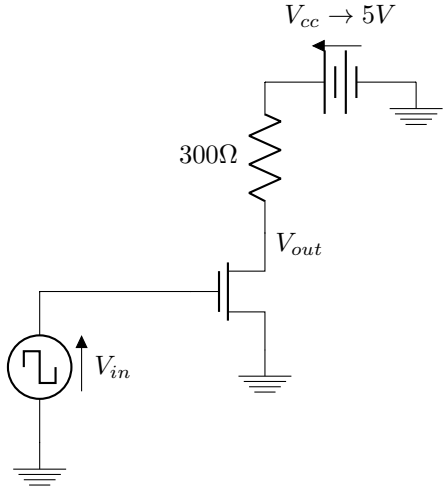
The objective of this lab is to build an inverter with MOSFETs (metal oxide semiconductor field effect transistors) and demonstrate its use as a switch and an amplifier. For the first circuit, the switching behavior of a MOSFET is observed. A circuit with multiple components is built and a voltage pulse is given to the transistor to observe the output voltage signal. The input pulse signal is increased so the time delay, rise time, and fall time are measured. Next, the amplification properties of the MOSFET are demonstrated. An input signal at 10kHz frequency is applied, and the input and output voltage signals are observed. The input voltage is increased until the output voltage starts to clamp. The gain is then measured. The upper cutoff frequency is measured along with voltage gain at this frequency. Lastly, the cutoff frequency is tested while observing the output after setting the function generator to square wave input.

2 Results and Analysis

2.1 Inverting Characteristics of the MOSFET

The MOSFET inverter circuit is shown below:

Figure 1: MOSFET Inverter Circuit



Consider the case when V_{in} is low (close to ground). The MOSFET's gate is set to the ground voltage, the source and the gate are at the same voltage. Typically, the bulk and source are connected to the same node. Thus, if the source is grounded, the bulk is as well. Because the bulk and gate are grounded, the channel does not form because no excess electrons are attracted to the area

under the gate. So, the channel cannot conduct carriers to the drain. Thus, no current flows through the MOSFET.

This operation mode is known as the cutoff region. Each MOSFET has what is known as a threshold voltage V_{Th}. A MOSFET is said to be in the cutoff region and thus abide by this physical description when the following condition holds:

$$V_{GS} \leq V_{Th} \tag{1}$$

When the gate voltage does not exceed the source voltage by an amount greater than the threshold voltage V_{Th}, the MOSFET cannot conduct a current.

Because no current flows through the MOSFET in the cutoff region, no current flows through the resistor connected to its drain terminal. By Ohm's Law, the voltage drop over the resistor is 0V. Since the MOSFET and the resistor are in series and the resistor consumes no voltage, the MOSFET must consume a voltage equivalent to the supply voltage V_{cc}. Therefore, the output voltage V_{out} is high when the input voltage V_{in} is low.

When V_{in} is high, the gate voltage is higher than the grounded source voltage. Because the gate voltage is high, the gate is now at a higher voltage than the grounded bulk. Thus, excess electrons are attracted from the bulk to the area just beneath the gate oxide. These excess electrons increase the conductivity of this area, producing a conductive channel.

Assume the MOSFET is in saturation mode. A MOSFET is said to be in saturation mode when the following condition holds:

$$V_{GS} - V_{Th} < V_{DS} \rightarrow V_{GD} < V_{Th} \tag{2}$$

In saturation mode, current can flow through the MOSFET. However, increasing V_G causes the drain current I_D to level off. Because $V_{GD} < V_{Th}$, the depletion region between the bulk and the drain limits current flow. When V_G is increased, more conduction electrons are attracted to the channel, but they are also impeded with a stronger electric field when entering the drain. Therefore, increasing V_G in this state does not increase the drain current I_D.

Because electrons can flow through the MOSFET, a current through the MOSFET I_D is produced. Because current can flow through the MOSFET, the resistor can now consume voltage. This means that the MOSFET receives a smaller fraction of the voltage. Thus, the output voltage V_{out} is low when the input voltage is V_{in} is high. Clearly, this circuit demonstrates inverting characteristics, which is why it is called an "inverter".

However, this inverter is not ideal. It takes time for the MOSFET channel to form when the gate voltage is high. When the gate voltage drops back to ground, it takes time for the excess electrons to recombine and diffuse back into the bulk. Thus, a rise time, fall time, and delays can be measured for the output waveform.

In the experiment, the circuit is configured so that the MOSFET enters the saturation region when the input is high and the cutoff region when the input

is low. The input and output waveforms are displayed below, where the yellow waveform is the input and the green waveform is the output.

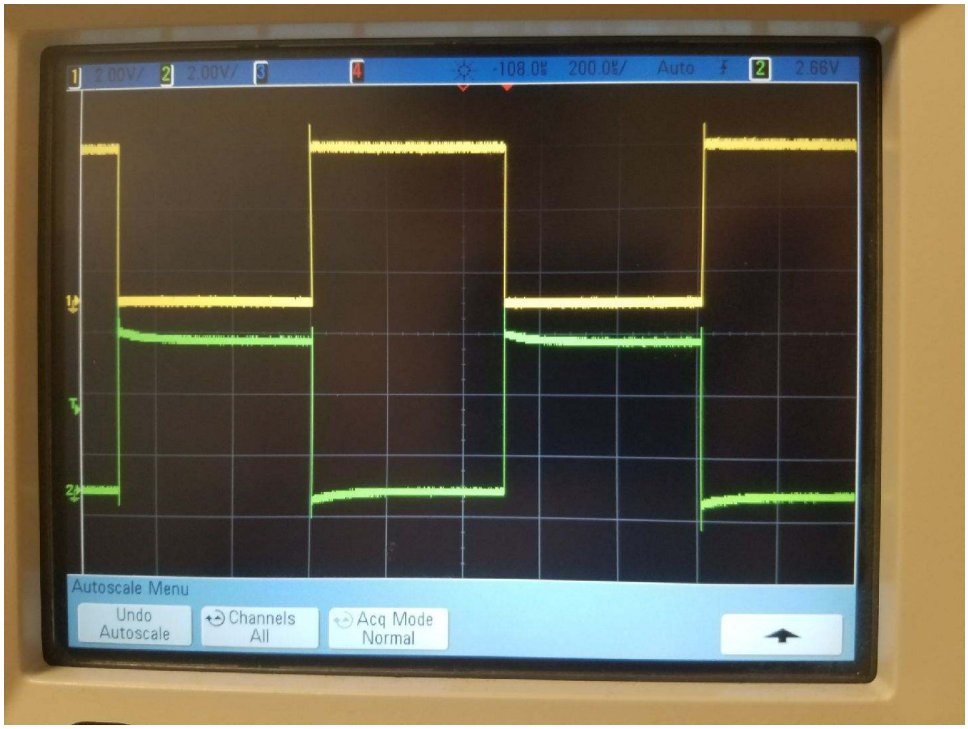


Figure 2: Inverter Input and Output Voltage

V_{in} is a square pulse with an amplitude of 5V and a 50% duty cycle. When the input is high, the output is low. Here, V_{GS} is simply V_{in}. V_{DS} is V_{out}. In experiment 6, the threshold voltage V_{Th} is determined to be about 2V. So, using equation (2), $V_{GS} - V_{Th} = 5 - 2 = 3 < 5 = V_{DS}$, the transistor is in saturation when the input is high. When the input is low, using equation (1), $V_{GS} = 0 < 2 = V_{Th}$. So, the transistor is in the cutoff region when the input is low.

The rise time is measured by acquiring the time it takes for the output voltage to transition from 10% to 90% of its maximum value. It is determined to be about 24ns.

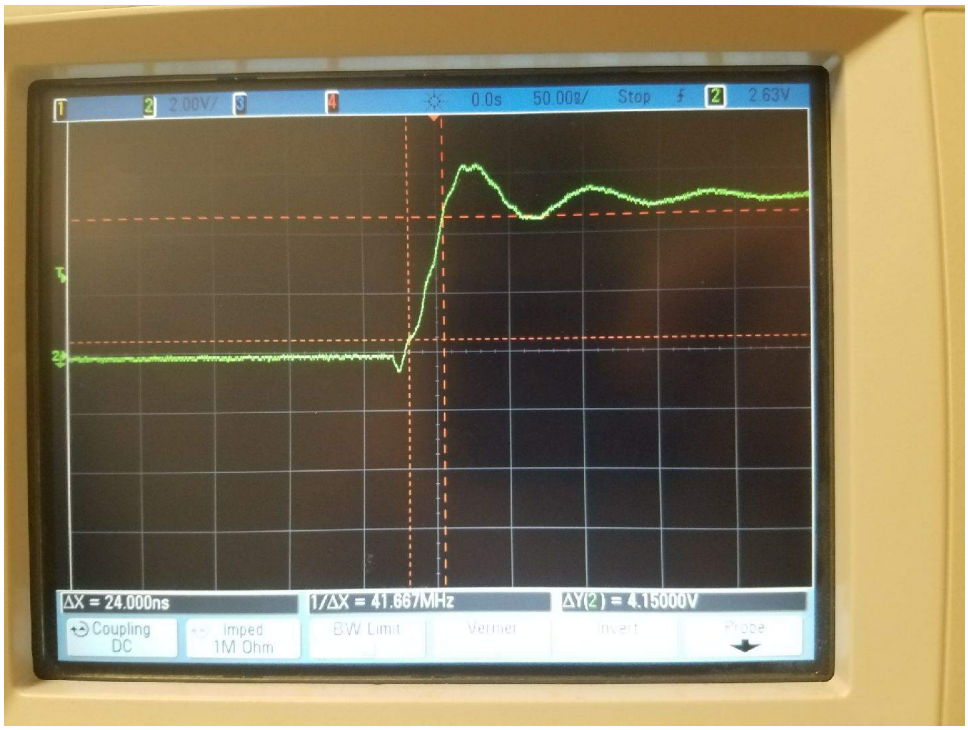


Figure 3: Inverter Rise Time Measurement

The fall time is found by measuring the time it takes for the output voltage to drop from 90% to 10% of the peak value. It is found to be 14.4ns.

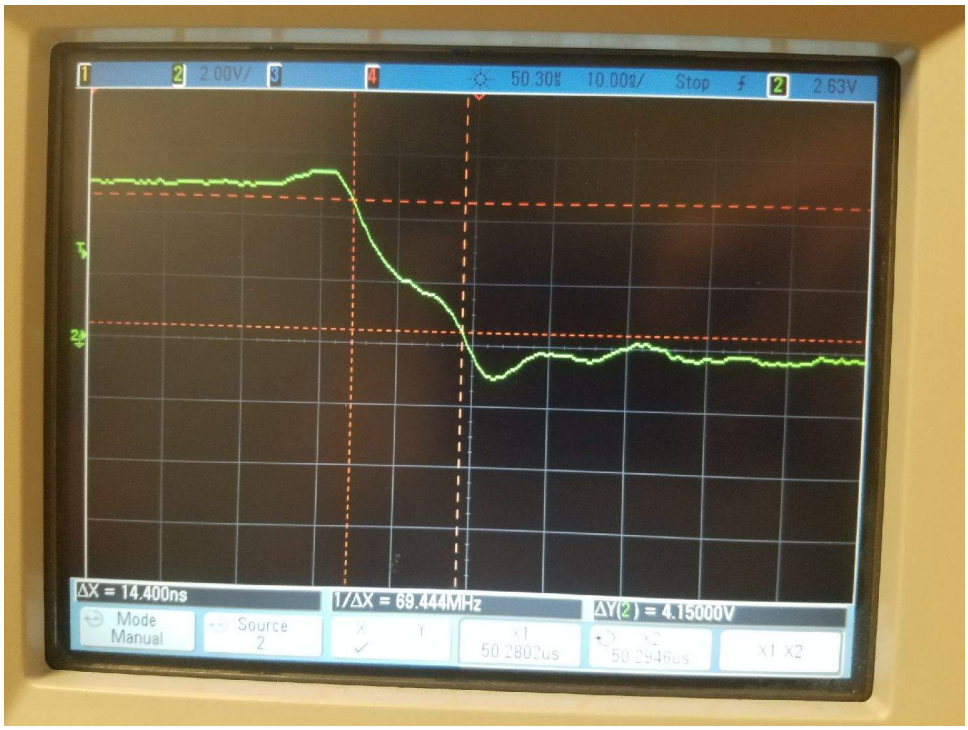


Figure 4: Inverter Fall Time Measurement

Next, the delay between the input and output when the transistor transitions from cutoff to saturation is measured. This is the same as the delay from the rising edge of the input to the falling edge of the output. The delay is measured from the 50% point on the input to the 50% point on the output.

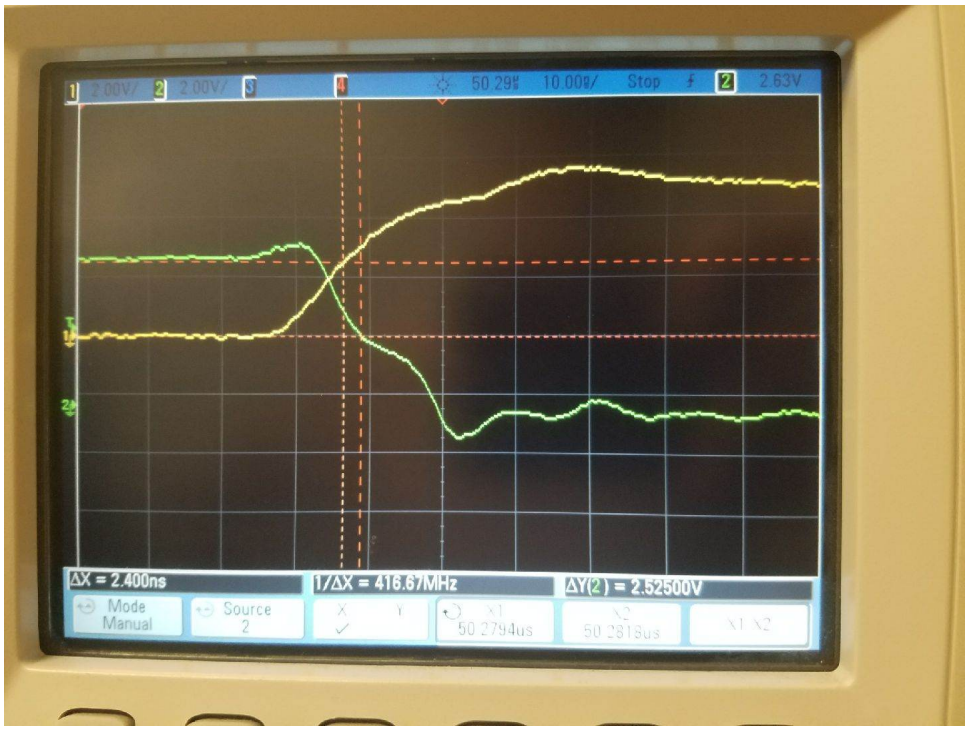


Figure 5: Inverter Delay Measurement

This delay is measured to be 2.4ns. In the same manner, the delay from saturation to cutoff is measured to be 10.4ns.

Table 1: Inverter Times

	Time [ns]
Delay time (cutoff to saturation)	2.4
Delay time (saturation to cutoff)	10.4
Rise time	24
Fall time	14.4

The delays and rise/fall times limit the MOSFET's frequency performance. At a high frequency, say 3GHz, the period is very short, about 0.33ns. When the MOSFET transitions from cutoff to saturation, the response is delayed by 2.4ns, more than an order of magnitude longer than a half-period. Thus, at this frequency, the MOSFET could not transition from state to state since it would not have enough time to transition before the input voltage changes back to its original value. This issue is also not limited to switching applications. MOSFET-based amplifiers are also limited in their amplification abilities at high frequencies.

2.2 Amplifying Characteristics of the MOSFET

The inverter circuit constructed in Figure 1 is also called a common-source amplifier and the amplification characteristics of the circuit is explored in this experiment by analyzing its frequency response.

For this portion of the experiment the MOSFET must always be operating in saturation mode, meaning the condition in Equation 2 must be satisfied. Because a sinusoidal wave is used as the input signal, a DC offset must be applied so that $V_{GD} < V_{Th} = 2\text{V}$ for the entire amplitude range of the sinusoidal input.

The amplifier's input signal is chosen to have 200mVpp with a 2.5Vdc offset and a frequency of 10kHz because at this setting it is observed that the entire amplitude range of the input just lies within the saturation region. Clipping is observed in the output signal when the amplitude of the input signal is increased to 250mVpp. This occurs because a portion of the positive cycle of the input signal now lies outside the saturation region and crosses over to the triode region.

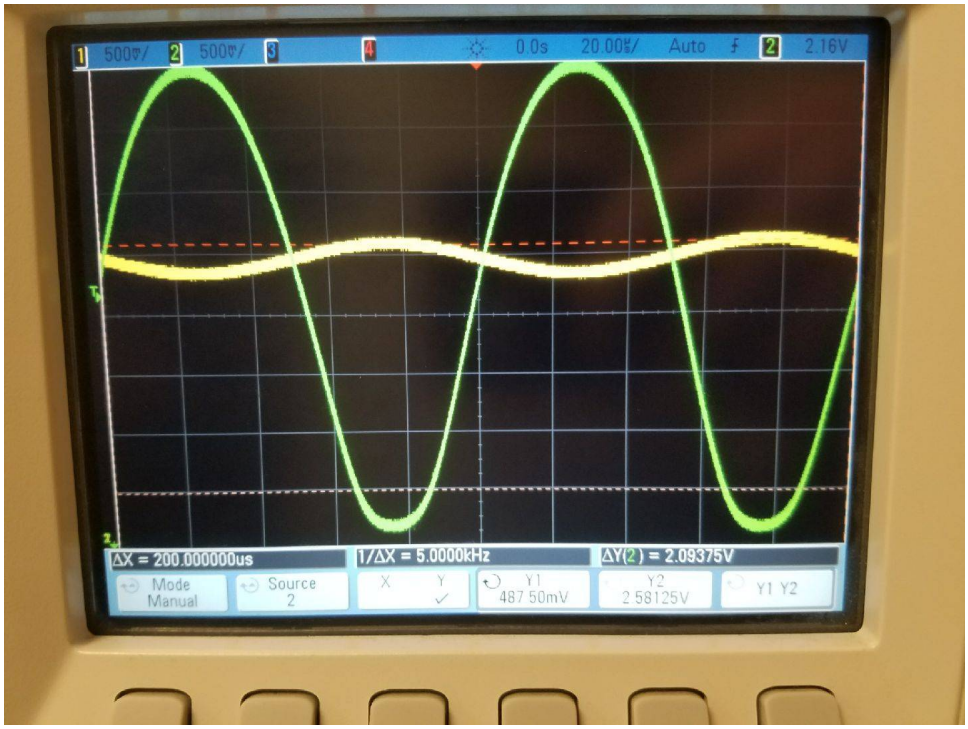


Figure 6: Common-Source Amplifier 10kHz Distortions

Like the common-base amplifier observed in the previous experiment, the common-source amplifier is also a non-ideal amplifier due to capacitive effects. Consider the physical structure of the MOSFET, more specifically the nMOS:

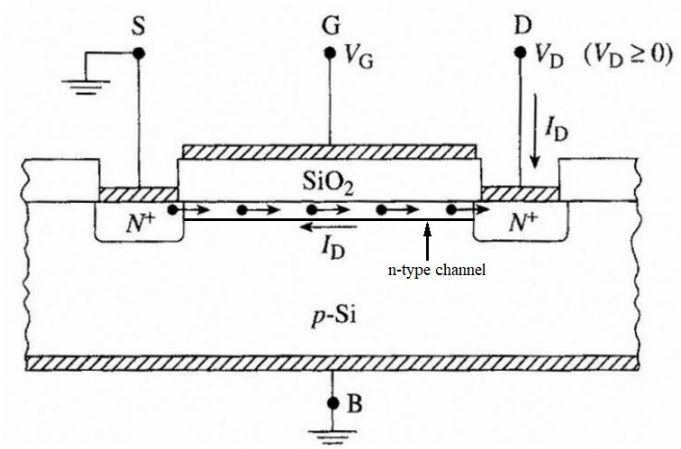
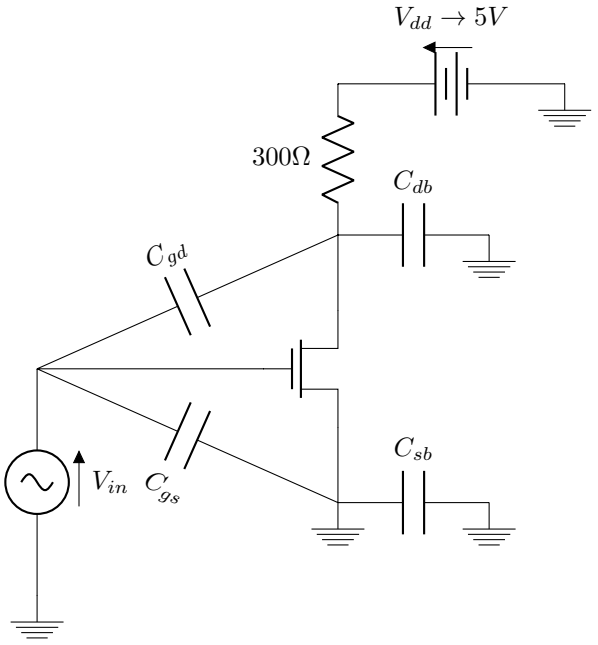


Figure 7: Physical Structure of MOSFET

There is capacitance between the gate to source (C_{gs}) and gate to drain (C_{gd}) due to two reasons: the overlap of the metal gate electrode and the wells of n+ semiconductor material at the source and drain, and the close proximity of the metal gate electrode and the induced n-type channel. There is also junction capacitance between the n+ drain to p-type substrate body (C_{db}) and n+ source to p-type substrate body (C_{sb}) [1]. The equivalent circuit is given in the following model:

Figure 8: MOSFET High Frequency Small Signal Model



At low frequencies, the capacitors in the circuit above are essentially open circuits and thus the amplifier exhibits ideal behavior and maximum gain. However, when the frequency of the input is sufficiently high, the capacitors begin to short the path from the drain to ground, effectively decreasing the amplitude of the output voltage. Increasing the frequency of the input signal will drop the amplitude of the output signal further until $V_{out} = 0$V. This also causes the gain in dB of the amplifier to drop as gain is given by $20log(\frac{V_{out}}{V_{in}})$.

At 10kHz, the input voltage value of 200mVpp corresponds to an output voltage value of 3.3Vpp. $\frac{V_{out}}{V_{in}}$ at 10kHz is calculated to be 16.5 and a gain in dB of 24.3dB. This gain value corresponds with the maximum gain because parasitic capacitances are still regarded as open circuits. The parasitic capacitances will then decrease the gain of the amplifier at high frequencies and a cutoff frequency, f_c, can be found when the gain in dB is a value that is 3dB less than the maximum value or when the $\frac{V_{out}}{V_{in}}$ ratio is less than the maximum value by a factor of $\sqrt{2}$. The cutoff should then occur when $\frac{V_{out}}{V_{in}} = \frac{16.5}{\sqrt{2}} = 11.7$ which corresponds to a gain in dB of 21.3dB. Using the condition above, f_c is observed to be approximately 3.6MHz.

Table 2: Common-Source Amplifier Frequency Response

Frequency [kHz]	V_{out}/V_{in} [unitless]	Gain [dB]
10	16.5	24.3
3600	11.7	21.3

A square wave with frequency of $f_c = 3.6$MHz is then set as the input signal to observe distortions in the output waveform. Two duty cycles for the square input are used for the observation: 20% and 50%. The two duty cycles give the following waveforms:

Figure 9: Common-Source Amplifier Square Wave Response 20% Duty Cycle

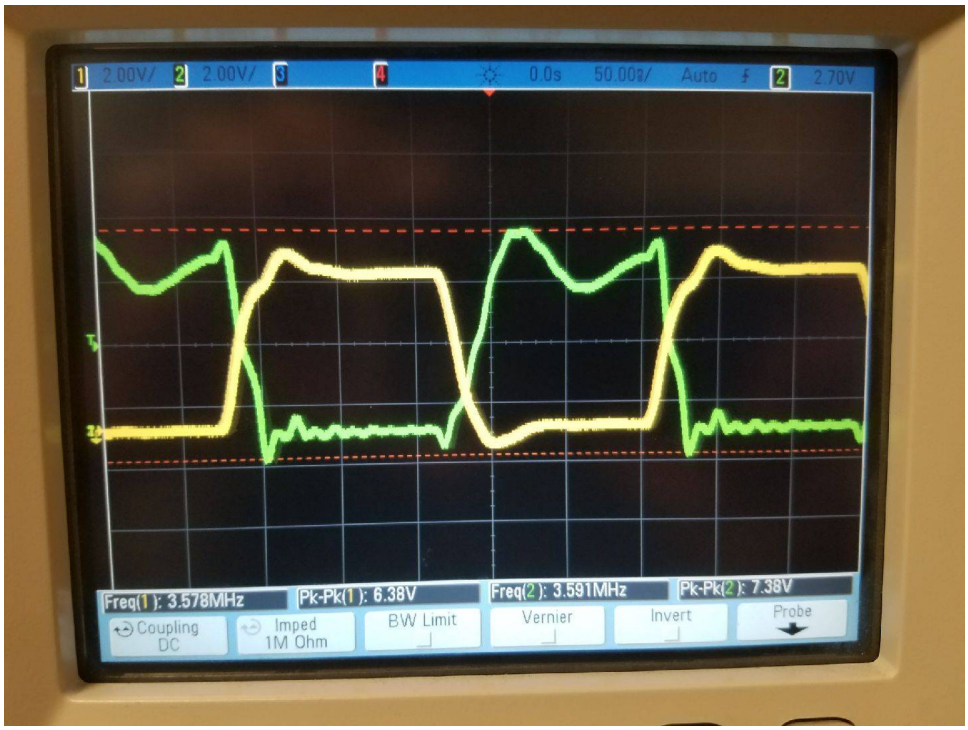


Figure 10: Common-Source Amplifier Square Wave Response 50% Duty Cycle

For both the 20% and 50% duty cycle square inputs, the input and output signals have very noticeable distortions due to second-order effects. However, if the distortion is ignored, the output signal still resembles an inversion of the input signal. This is because at 3.6MHz, the period of the wave is 278ns which is still significantly higher than the delay times, rise time, and fall time found in the inverter experiment. This means that for both duty cycles, the output voltage still has sufficient time to fully develop.

3 Discussion

3.1 Inverting Characteristics of the MOSFET

The MOSFET exhibits the inverting capabilities predicted by theory. It also switches at a much faster rate than the bipolar-junction transistor (BJT). An equivalent BJT circuit would have rise and fall times as well as delays in the µs range, whereas the MOSFET's are in the ns range. Moreover, the MOSFET operates in saturation when the input is high and cutoff when the input is low, a desired characteristic of the circuit. Given the measured data, it is clear that the output voltage V_{out} takes longer to transition from low to high than it does to

transition from high to low. Furthermore, the MOSFET is unable to operate at high frequencies, such as 3GHz, inasmuch as it is limited by its state transition delays.

3.2 Amplifying Characteristics of the MOSFET

The common-source amplifier which utilizes the MOSFET has a significantly higher cutoff frequency than the common-emitter amplifier which utilizes the BJT. The common-emitter amplifier would have its cutoff frequency around the order of magnitude of 100kHz while the common-source amplifier is found to have its cutoff frequency in the MHz range. However, noticeable second-order distortion is observed in input and output signals that approach or exceed the cutoff frequency. This distortion however, is not due to delay times as it is observed that inversion and amplification still occurs at an adequately fast pace around the cutoff frequency. For the common-emitter amplifier, second-order effects are not seen near the cutoff frequency, but switching time is too slow for voltages to fully develop. As a result, the advantages and disadvantages of the MOSFET and BJT are made more clear.

4 References

1. http://aries.ucsd.edu/NAJMABADI/CLASS/ECE102/12-F/NOTES/ECE102_F12-LecSet-8.pdf