Lab 7

EECS 170LB

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1 Introduction

The CD4007 gate array is used to construct an inverter, NAND gate, and NOR gate circuit. The behavior of the three CMOS circuits are analyzed for further understanding of CMOS logic and design.

2 CMOS Inverter

The CMOS inverter is configured using a CD4007 IC. A 1kHz ramp going from 0V to 5V is applied to the inverter's input.

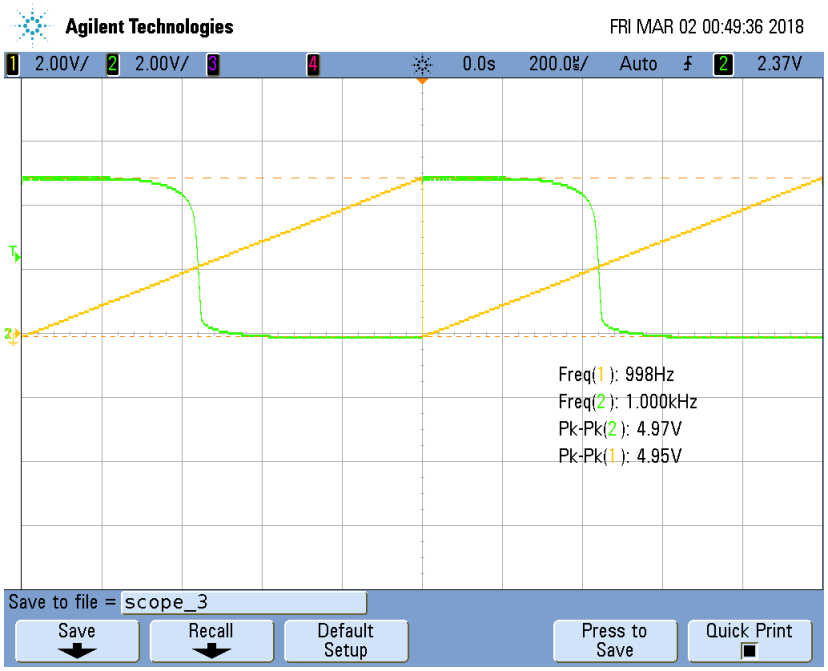

Figure 1: V_{out} and V_{in}

V_{out} versus time is in green. V_{in} versus time is in yellow.

When the input voltage is low, the PMOS is turned on, pulling up V_{out} to supply. So, the output is high when the input is low. When the input voltage is high, the NMOS is turned on, pulling down V_{out} to ground. Thus, the circuit acts as an inverter, explaining why the output transitions as it does. The ramp function resets every period, which is why the output does the same.

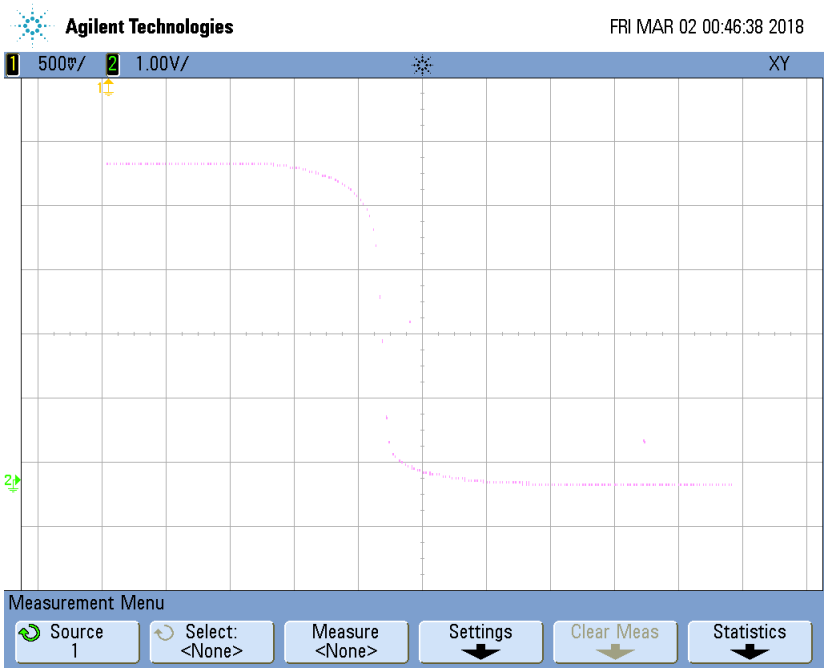

Figure 2: Voltage Transfer Characteristic of CMOS Inverter - V_{out} versus V_{in}

V_{in} is a ramp function, meaning its range is simply from ground to supply. So, when V_{out} is plotted against V_{in}, the value of V_{out} can be observed at every possible value at and between the high and low values. Thus, the inverting voltage transfer characteristic of the CMOS inverter is observed in this plot. The physics of why the inverter works in this manner is explained above.

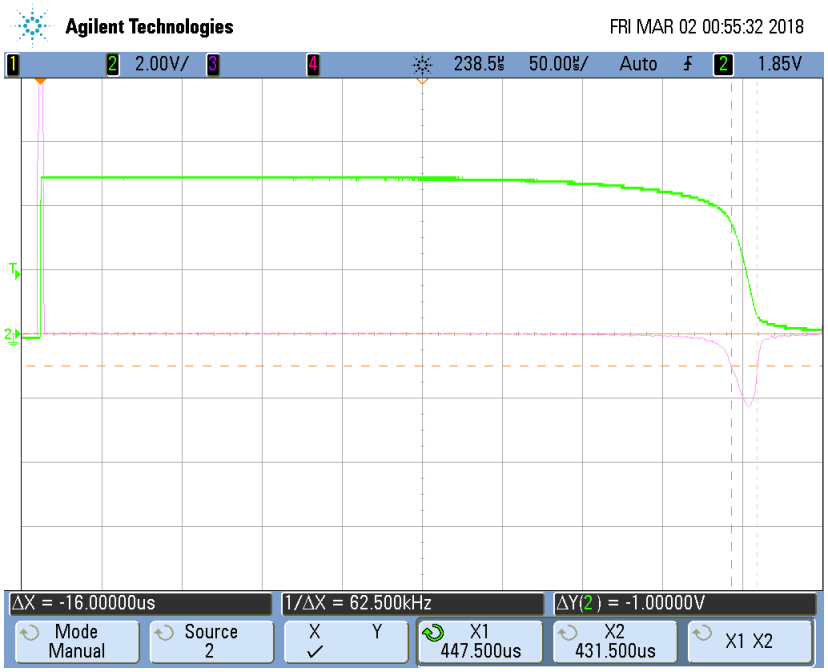

Figure 3: V_{IL} and V_{IH} Measurement

The green curve is V_{out} versus time. The purple curve is $\frac{dV_{out}}{dV_{in}}$ versus time.

V_{IL} and V_{IH} are defined as the two points along the voltage transfer characteristic at which $\frac{dV_{out}}{dV_{in}} = -1$. The points at which $\frac{dV_{out}}{dV_{in}}$ attains a value of -1 is where the V_{IL} and V_{IH} times are determined.

Table 1: V_{IL} and V_{IH} Times

Voltage Name	Time [us]
Vih	447.8
Vil	431

Table (1) lists the times at which V_{IL} and V_{IH} are the values of V_{in} relative to the start of the ramp function's period based on the measurements in table (3). With time as the independent variable and V_{in} as the dependent variable, the starting point of the ramp function's period is the point (0µs,0V) and the ending point is (1000µs,5V). This is because the period of the ramp function is given by the reciprocal of its frequency, 1kHz, and its maximum attainable value is the supply voltage, 5V. Therefore, the following equation describes V_{in} as a function of time within one period:

$$V_{in} = (0.005[\frac{V}{\mu s}])t \ , \ 0[\mu s] < t < 1000[\mu s] \tag{1}$$

Using equation (1) and the times from table (1), V_{IL} and V_{IH} can be computed. The results are presented in table (2).

Table 2: Values Used for Noise Margin Calculations

Voltage Name	Voltage [V]
Voh	4.875
Vol	0
Vil	2.155
Vih	2.239

The noise margins of a CMOS inverter are defined by:

$$NM_L = V_{IL} - V_{OL} \tag{2}$$

$$NM_H = V_{OH} - V_{IH} \tag{3}$$

The values for the noise margins of this CMOS inverter are given in table (3).

Table 3: Noise Margins

Noise Margin	Voltage [V]
NML	2.155
NMH	2.636

A square wave input with the same frequency and amplitudes is then provided to the CMOS inverter.

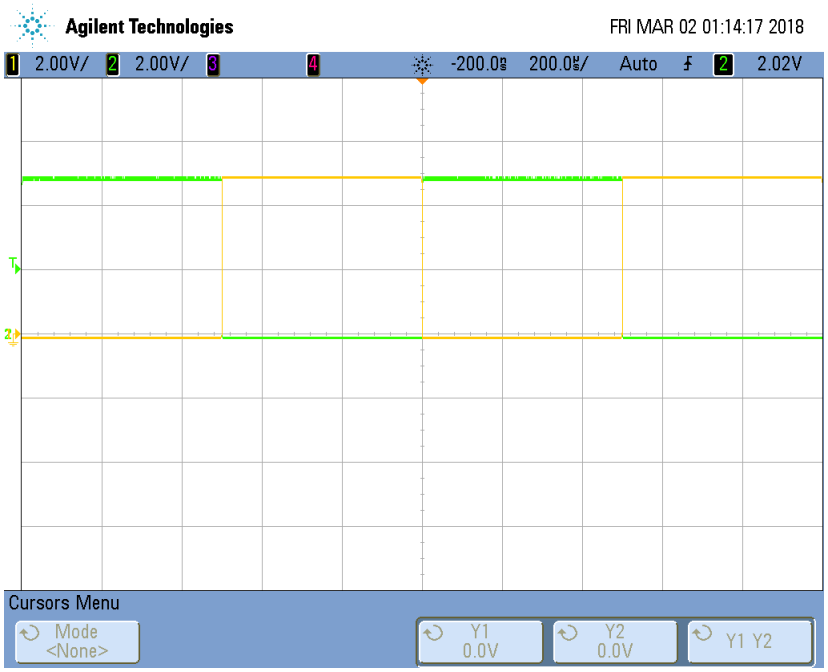

Figure 4: Square Wave Input - Transient

The same color convention as figure (1) is followed.

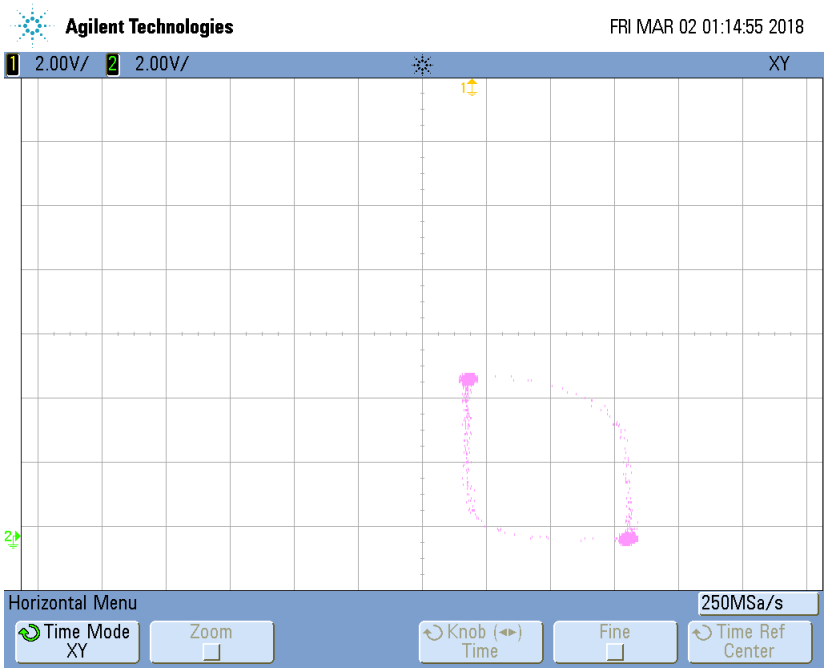

Figure 5: Square Wave Input - Voltage Transfer Characteristic

The two points (V_{out} , V_{in}) at which the output is pulled to supply and ground are very pronounced in figure (5). However, because the square wave transitions so quickly, very few other points between are sampled. As a result, the quality of the voltage transfer characteristic is significantly diminished. A sine wave input is then tested.

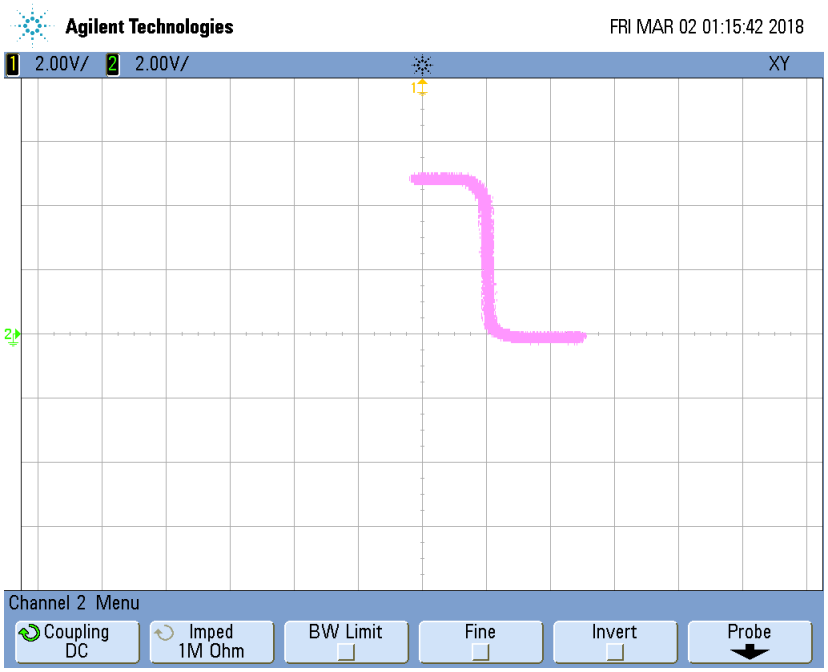

Figure 6: Sine Wave Input - Voltage Transfer Characteristic

In the same period, the sine wave gives much better quality than the ramp function input when determining the voltage transfer characteristic.

3 NAND and NOR Gate

3.1 NAND Gate

A two-input NAND circuit is constructed on the bread board using the CD4007 gate array.

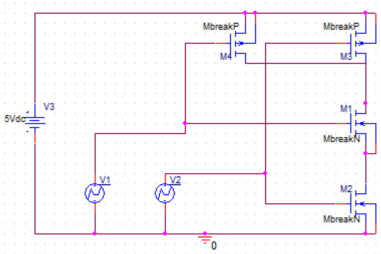

Figure 7: Layout of Two-input NAND Gate

The two-input NAND gate has following logic chart (or truth table) where x and y are inputs and S is the output and 0 corresponds to low and 1 corresponds to high. The output voltage is taken at the drain node of the NMOS M1 in Figure 7.

Table 4: Logic Chart of Two-input NAND Gate

x	y	S
0	0	1
0	1	1
1	0	1
1	1	0

The behavior of the NAND gate circuit is not tested using the oscilloscope due to complications in its construction on the bread board. However, the behavior of the circuit is expected to be consistent with Figure 4 where 0 and 1 correspond to low and high output voltages, respectively. The following SPICE simulation shows the expected behavior of the NAND gate circuit.

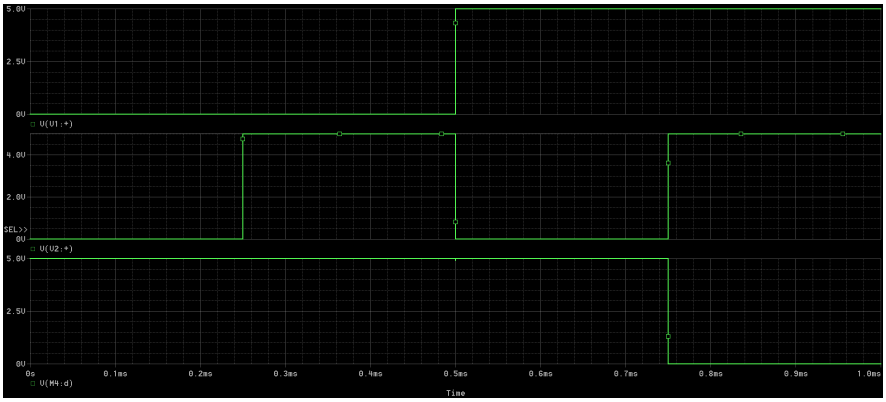

Figure 8: Simulated NAND Circuit Behavior

The top plot shows V_1, which is a input square wave $(0 - 5\text{V})$ with a 1kHz frequency. The middle plot shows V_2, which is a input square wave $(0 - 5\text{V})$ with a 2kHz frequency. Lastly, the bottom plot shows the output waveform of the two-input NAND circuit. Figure 8 effectively shows that the behavior of the circuit does match the truth table in Figure 4.

3.2 NOR Gate

The CD4007 gate array was used to make a two-input NOR gate.

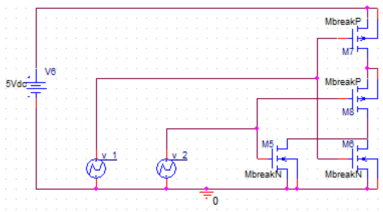

Figure 9: The two-input NOR gate circuit.

The two-input NOR gate operates such that the output will be high only when both inputs are low. Otherwise, the output will be low. It can be shown from the circuit above that V_1 and V_2 serve as the inputs and V_{out} is taken across the drain of $M8$ to the ground.

x	y	S
0	0	1
0	1	0
1	0	0
1	1	0

Table 5: Logic of the two-input NOR gate.

The analysis of this circuit shows that the behavior of the two-input NOR gate is consistent with our logic table and our expectations. The figure below shows the results of the NOR gate simulation.

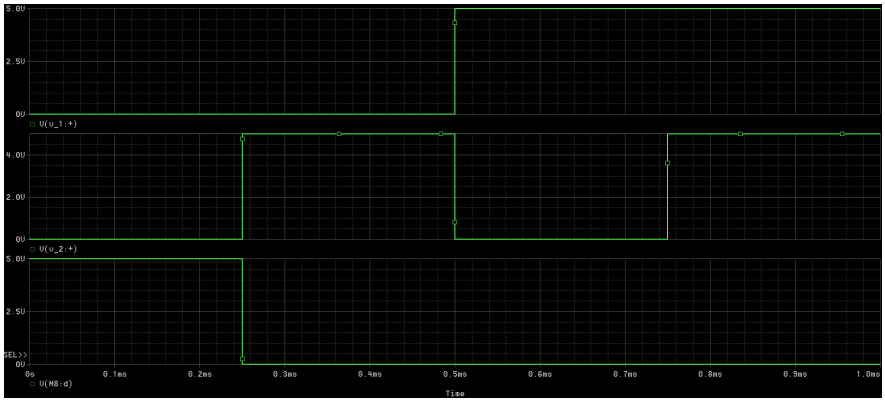

Figure 10: Simulation output of the NOR gate.

Using V_1 and V_2 as the inputs, we see that the output, $M8$, of our NOR gate will only be high when both inputs are low. This proves that our expectations for the NOR logic and circuit structure are correct; however, this is still a

simulation. Due to some complications with the CD4007 and breadboard, the results are only available from a SPICE simulation.

4 Conclusion

4.1 CMOS Inverter

The highest quality voltage transfer characteristic occurs when a sine wave input is applied. It may have to do with the relatively higher density of points in a sine wave since the sine wave is longer than the ramp in one period if unrolled. The noise margins are similar to what is often received in simulation results for well-designed CMOS inverters.

4.2 NAND Gate

The SPICE simulation and the logic chart for the two-input NAND gate effectively show the true behavior of the circuit constructed on the bread board. However, the true behavior of the circuit would also show propagation delay between the input and output waveforms. But propagation delay may be negligible because the circuit is tested using low-frequency $1 - 2$ kHz square waves as inputs.

4.3 NOR Gate

The two-input NOR gate simulation results were consistent with our logic and theory for the circuit. While testing the NOR gate configuration of the CD4007, there would likely be propagation delays and other non-ideal behavior. Given that our frequency is only $1kHz$ these effects may be negligable.