Lab 2: Hands-On Analysis of MOSFET Transistors and Amplifiers

EECS 170LB

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1 Introduction

The i_D versus V_{ds} (V_{sd} for PMOS) curves are determined for the NMOS and PMOS transistor at different values of V_{gs} (V_{sg} for PMOS). The NMOS transistor's behavior is then further examined by acquiring the voltage transfer characteristics of a common-source and common-drain amplifier. Properties of the amplifiers, such as operating regions at different V_{in} values, are observed. A CD4007 MOSFET IC is used for the experiments.

2 Procedure and Results

2.1 NMOS

3 Part 1

3.1 Part A

Using the circuit shown in figure 1, we measured the drain current with $V_{bs} = 0V$, $V_{gs} = 2.5V$, and $0V \leq V_{ds} \leq 5V$.

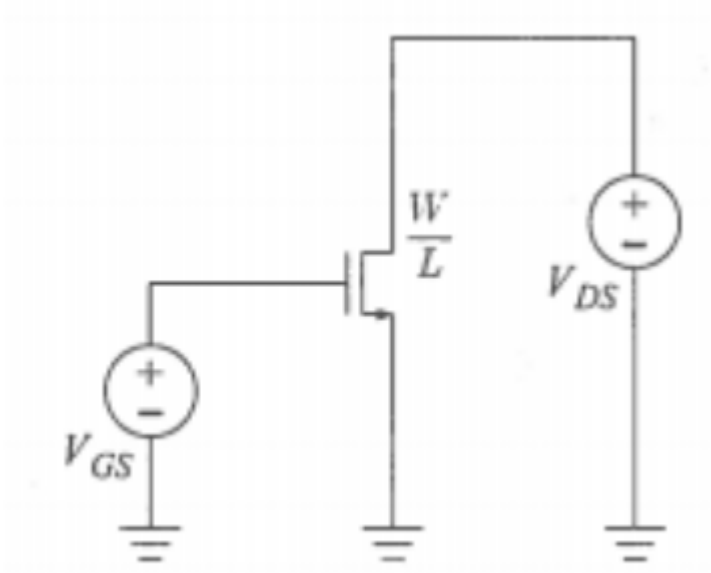


Figure 1 - Varying Vds to Ids with different Vgs

Figure 1: The circuit tested in part 1.

From the data we collected for I_{ds} and V_{ds}, we were able to find that the NMOS entered triode mode at $V_{ov} \approx 0.1V$. As soon as the drain voltage surpassed $V_{ds} = 0.1V$ we saw a dramatic increase in drain current. This increase

began to taper off around $V_{ds} \approx 0.8V$, as the NMOS entered saturation mode. We can approximate the threshold voltage to be $V_{tn} = 1.7V$.

$$V_{tn} = V_{gs} - V_{ds} = 2.5V - 0.8V = 1.7V \tag{1}$$

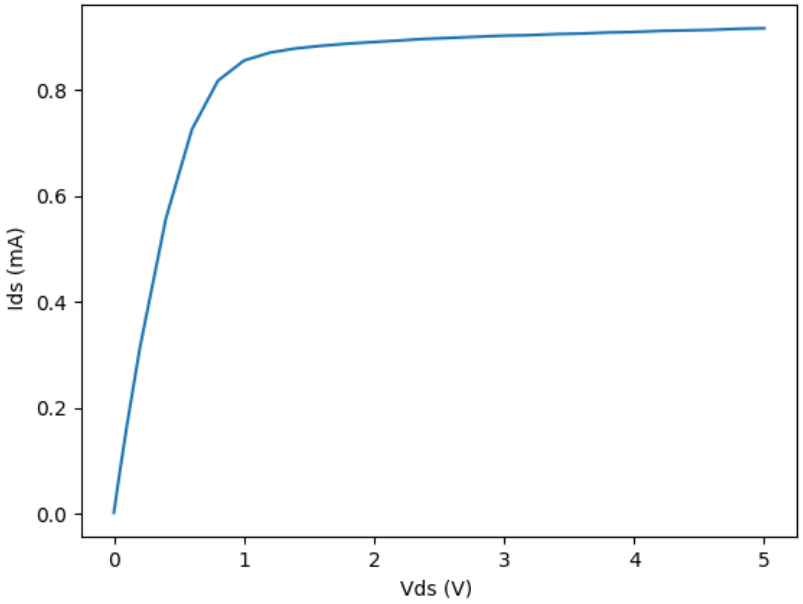


Figure 2: The resulting I_{ds} vs V_{ds} graph for $V_{gs} = 2.5V$.

During testing we noticed capacitive effects when moving from triode down to cutoff. If we were increasing drain voltage from below the point of cutoff to move into triode mode the drain voltage of $V_{ds} = 0.15V$ resulted in $I_{ds} \approx 166\mu A$; however, when moving from saturation or triode mode down into cutoff mode a drain voltage of $V_{ds} = 0.15V$ produced $I_{ds} \approx 310\mu A$. We believe this is due to the capacitive effects of the MOSFET structure.

3.2 Part B

During Part B we used the same parameters from Part A, except the gate voltage was increased to $V_{gs} = 5V$. We can see from the I_{ds} and V_{ds} curve in figure 3 the NMOS is operating in triode mode over the range of $0.8 \leq V_{ds} \leq 3.2V$.

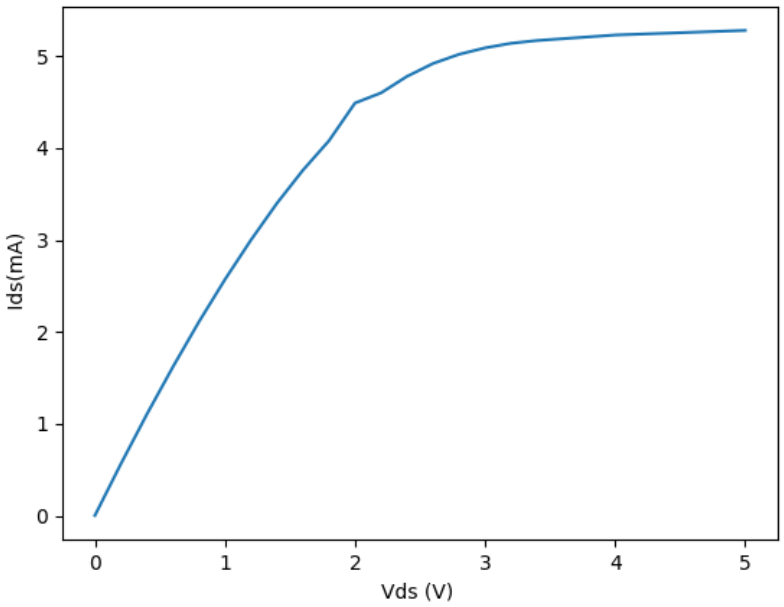


Figure 3: The resulting I_{ds} vs V_{ds} graph for $V_{gs} = 5V$.

We can check our approximation from part A for the threshold voltage of $V_{tn} = 1.7V$.

$$V_{ds} = V_{gs} - V_{tn} = 5V - 1.7V = 3.3V. \tag{2}$$

This result for $V_{ds} = 3.3V$ as the edge of saturation agrees well with the measured data. We can see on the curve the drain current stays fairly constant after approximately $V_{ds} = 3.2V$. After comparing the percentage of change in the drain current and drain voltage, we find that after $V_{ds} = 3.2V$ the change in the drain current stays at less than one percent, despite the change in drain voltage of about five percent. This result proves that our result of $V_{tn} = 1.7V$ is a good approximation for the threshold voltage.

3.3 PMOS

4 PMOS

4.1 Part A

Using the circuit shown in figure 4 we measured I_{sd} as we varied the drain voltage from within the range of $0V \leq V_{sd} \leq 5V$. The value of the gate voltage was

set to $V_{sg} = 2.5V$.

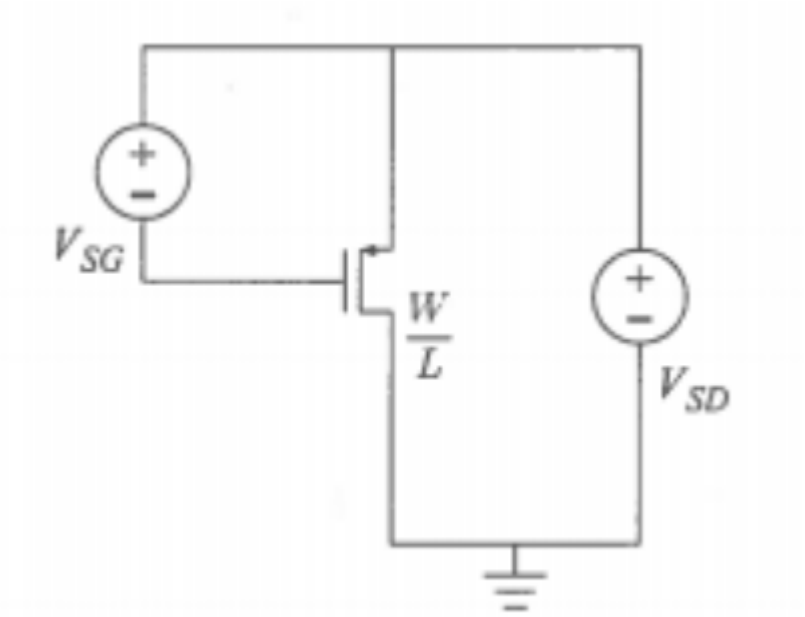


Figure 2 - Varying Vsd to Isd with different Vsg

Figure 4: The PMOS transistor circuit used for our measurements.

We can see from the I_{sd} vs V_{sd} curve in figure 5 that this PMOS transistor is in cutoff until $V_{sd} \approx 1.8V$.

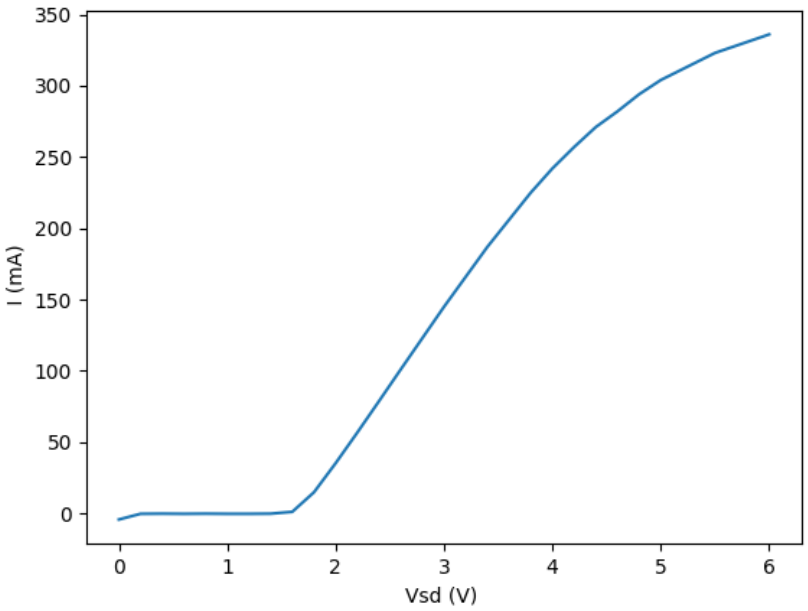


Figure 5: The resulting I_{sd} vs V_{sd} graph for $V_{sg} = 2.5V$

To turn on this transistor the gate voltage must be greater than the source voltage by at least the absolute value of the threshold voltage. This means that at $V_{sd} = 1.8V$, $V_{sg} \geq |V_{tp}|$.

To operate in triode mode the drain voltage must be greater than the gate voltage by at least the absolute value of the threshold voltage. The transistor enters triode mode at $V_{sd} \geq 1.8V$. Given that our data did not show signs of entering saturation mode, we were unable to find the saturation edge.

4.2 Part B

For part B we used the procedures from part A, but changed the gate voltage to $V_{sg} = 5V$.

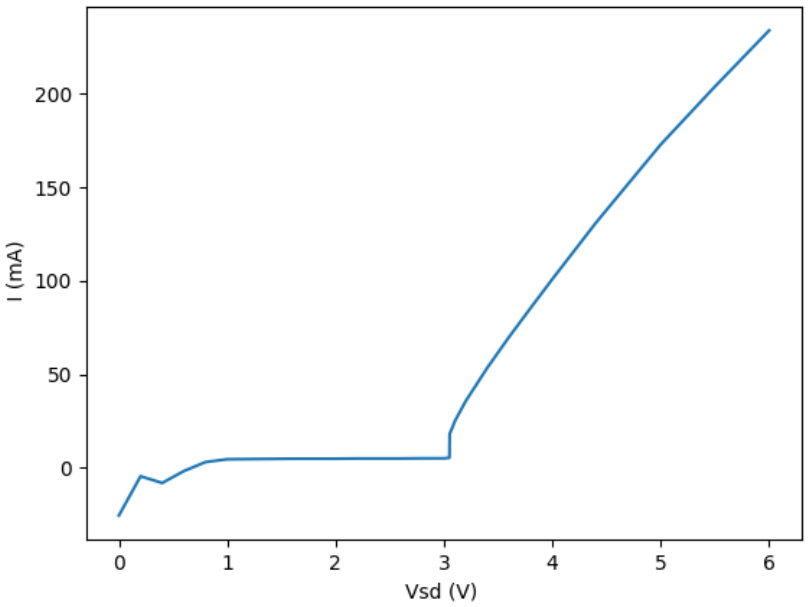


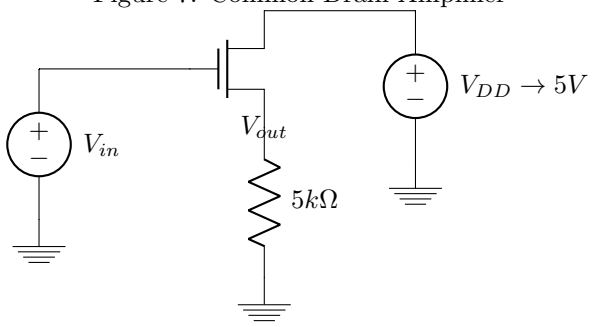
Figure 6: The resulting I_{sd} vs V_{sd} graph for $V_{sg} = 5V$

We see that the transistor operates in cutoff until $V_{sd} = 3.05V$. It then operates in triode mode for the rest of the values we tested up to $V_{sd} = 6V$. Given that our data did not show signs of entering saturation mode, we were unable to find the saturation edge.

4.3 Common Drain Amplifier

4.4 Theory and Procedure

Figure 7: Common-Drain Amplifier



A common-drain amplifier is to be constructed. V_{in} is swept from 0V to 5V. The following is the saturation condition for the NMOS transistor:

$$V_{DS} > V_{GS} - V_T \rightarrow V_D > V_G - V_T \rightarrow V_{in} < 5V + V_T \tag{3}$$

So long as V_{in} stays below 5V and high enough that the MOSFET does not enter the cutoff region, it remains in saturation. So, for small values of V_{in}, the transistor operates in the cutoff region because a current-enabling channel cannot form. Once V_{in} is high enough that the channel can form, the transistor operates in the saturation region due to the high drain voltage "pinching-off" the channel. By design, V_{in} never exceeds 5V. So, the transistor transitions from cutoff to saturation during the DC sweep.

4.5 Results