

1 PMOS

1.1 Part A

Using the circuit shown in figure 1 we measured I_{sd} as we varied the drain voltage from within the range of $0V \leq V_{sd} \leq 5V$. The value of the gate voltage was set to $V_{sg} = 2.5V$.

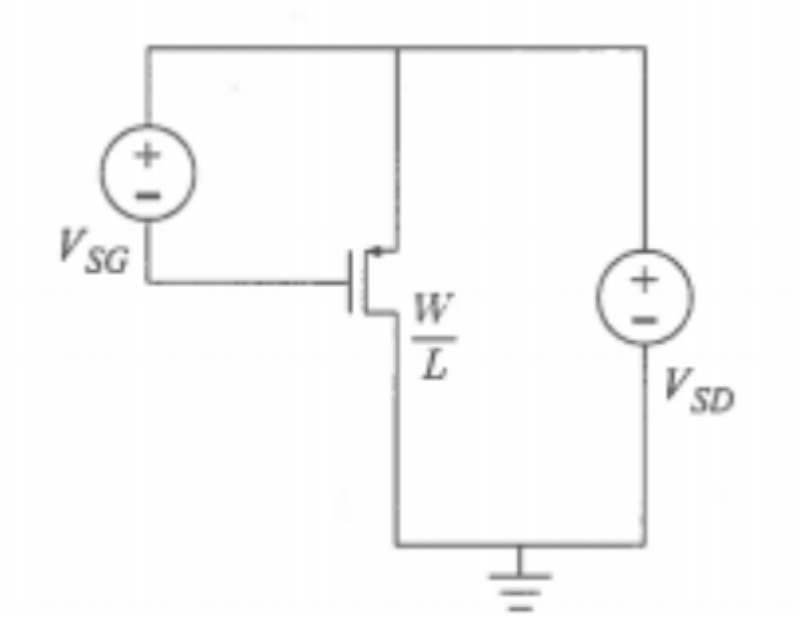


Figure 2 - Varying V_{sd} to I_{sd} with different V_{sg}

Figure 1: The PMOS transistor circuit used for our measurements.

We can see from the I_{sd} vs V_{sd} curve in figure 2 that this PMOS transistor is in cutoff until $V_{sd} \approx 1.8V$.

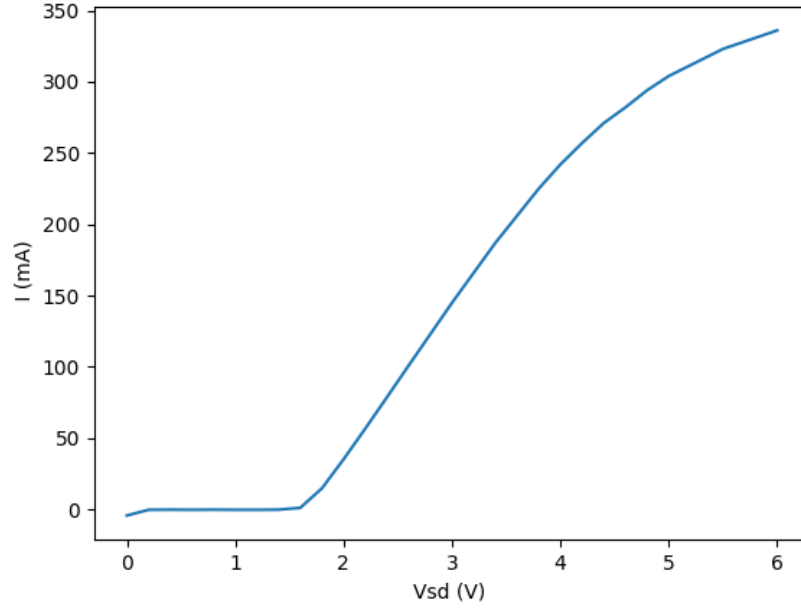


Figure 2: The resulting I_{sd} vs V_{sd} graph for $V_{sg} = 2.5V$

To turn on this transistor the gate voltage must be less than the source voltage by at least the absolute value of the threshold voltage. This means that at $V_{sd} = 1.8V$, $V_{sg} \leq |V_{tp}|$.

To operate in triode mode the drain voltage must be greater than the gate voltage by at least the absolute value of the threshold voltage. The transistor enters triode mode at $V_{sd} \leq 1.8V$. Given that our data did not show signs of entering saturation mode, we were unable to find the saturation edge.

1.2 Part B

For part B we used the procedures from part A, but changed the gate voltage to $V_{sg} = 5V$.

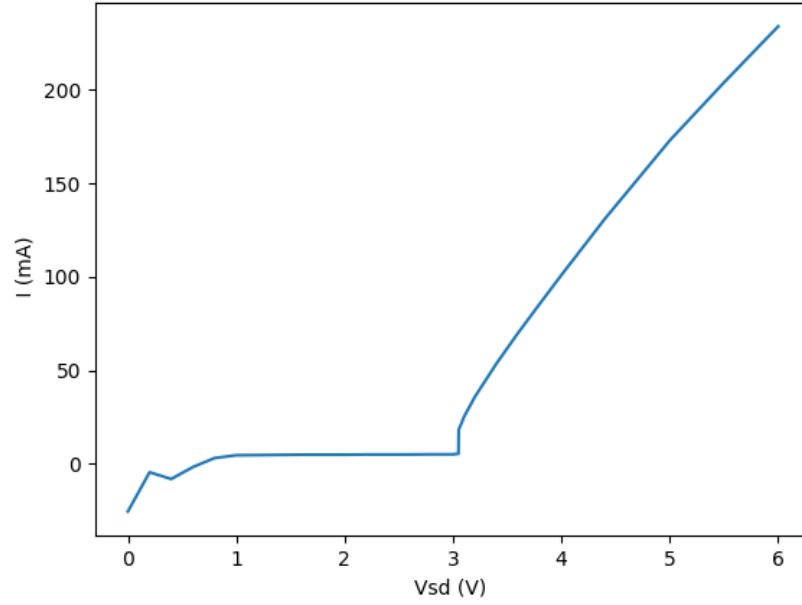


Figure 3: The resulting I_{sd} vs V_{sd} graph for $V_{sg} = 5V$

We see that the transistor operates in cutoff until $V_{sd} = 3.05V$. The difference in V_{sd} from part A has to do with the fixed gate voltage and the variable drain voltage being connected to the same node at the source. It then operates in triode mode for the rest of the values we tested up to $V_{sd} = 6V$. Given that our data did not show signs of entering saturation mode, we were unable to find the saturation edge.