Lab 3: Analysis of MOSFET Transistors and Amplifiers

EECS 170LB

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1 Introduction

The properties of various MOSFET amplifiers are analyzed. First, a common-source amplifier with a simple resistor is simulated. Its behavior when a small signal is applied and at various bias points is then considered. The resistor is then replaced with an NMOS transistor. After this, a CMOS amplifier and a common source amplifier with a complementary load are both simulated.

2 Procedure and Results

2.1 Common Source Amplifier with Passive Load

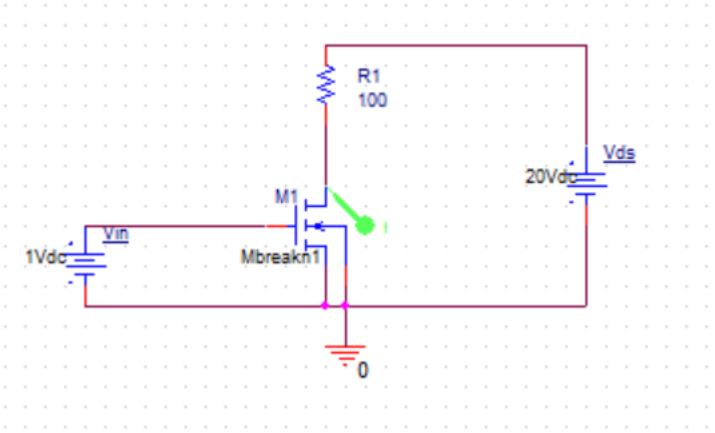

Figure 1: Common Source Amplifier with Passive Load

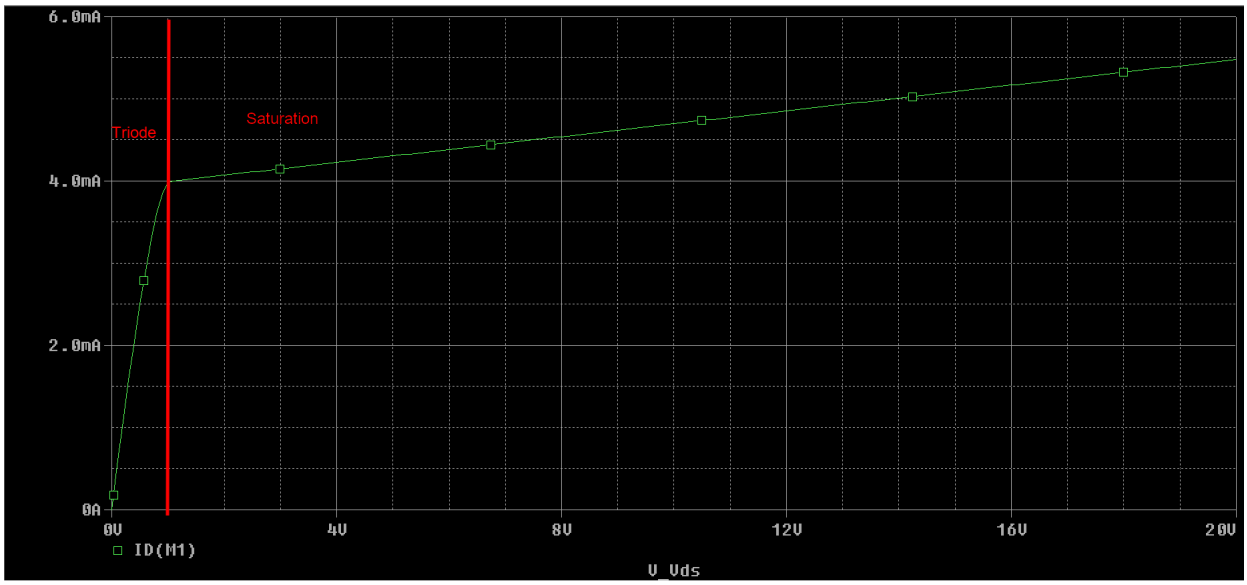

Figure 2: i_D versus V_{DS}

The curve in figure (2) is the expected i_D versus V_{DS} curve of an NMOS transistor with channel length modulation effects. From the diagram, $V_{GS} - V_T$ appears to be 1V since that is where the edge between triode and saturation occurs. The transistor operates in triode for $V_{DS} < V_{GS} - V_T = 1\text{V}$, and it operates in saturation for $V_{DS} > 1\text{V}$.

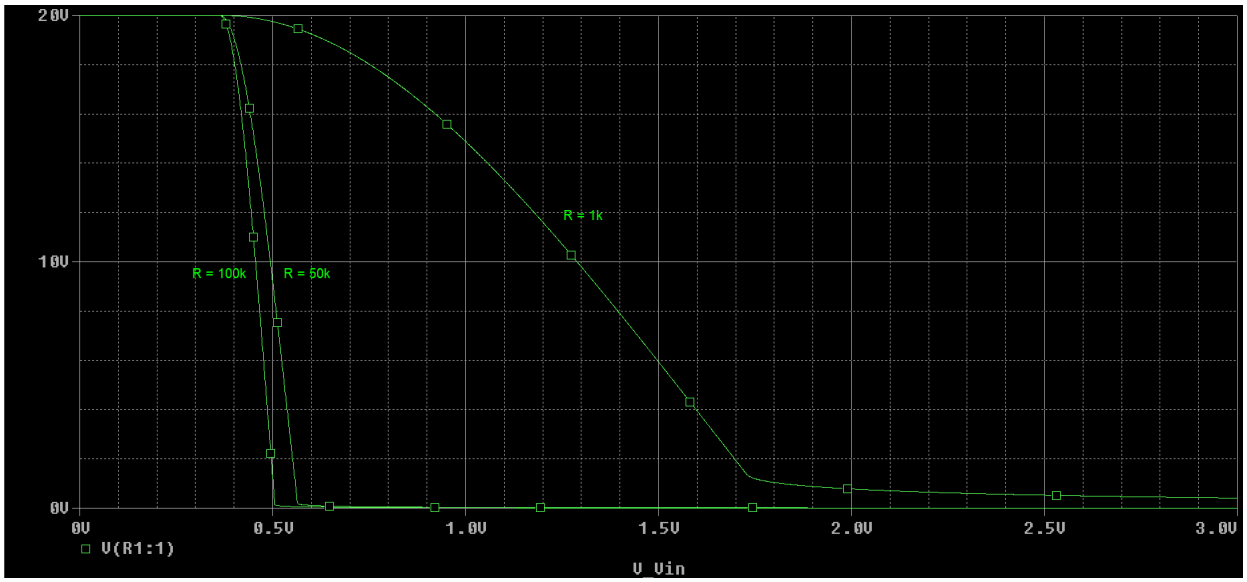

Figure 3: Voltage Transfer Characteristic

For low values of V_{in}, the transistor remains in cutoff. As a result, no voltage drops over the resistor since no current flows. Therefore, $V_{DS} = V_{out}$ is maximized at the supply voltage. As V_{in} is increased, the conductive channel forms and current can flow. However, assuming the current is a continuous function of V_{in}, it starts off at relatively small values, meaning that the voltage drop over the resistor is still small. Thus, the transistor's V_{DS} is still large and far exceeds V_{in}. As V_{in} increases, more current can flow, the resistor eats up more of the supply voltage, and V_{out} rapidly drops. For sufficiently large values of V_{in}, the transistor enters the triode region since V_{DS} becomes comparable in magnitude to V_{in}. At this point, the current no longer follows a linear relationship with V_{in}^2 and instead begins following a linear relationship with V_{in}. As a result, the resistor's voltage does not increase as rapidly and V_{out} therefore does not decrease as rapidly as they do in the saturation region.

Certain applications may call for other properties, but the common source amplifier should act as an inverter or a voltage amplifier. As an inverter, the steepest drop from the supply voltage to ground is desired. This occurs when $R = 100\text{k}\Omega$. As a voltage amplifier, high linearity and high small-signal voltage gain are desired. The linearity of the $R = 100\text{k}\Omega$ and $R = 50\text{k}\Omega$ curves are nearly the same and better than the $R = 1\text{k}\Omega$ curve. Voltage gain is defined as $A_v = \frac{dV_{out}}{dV_{in}}$. Thus, the largest $|A_v|$ occurs when the slope is steepest. The steepest slope occurs when $R = 100\text{k}\Omega$. So, overall, the best choice of resistor value is $R = 100\text{k}\Omega$.

When the common source amplifier is used for its voltage amplification characteristics, a bias current is typically used to tune the amplifier accordingly. The amplifier should operate near the middle of the saturation region. The small-signal gain magnitude is much higher in the saturation region than it is in the triode or cutoff regions. Furthermore, the transistor gets the maximum signal swing at the middle of the saturation region, making it operate over a wider range of input signal amplitudes. However, increasing V_{GS} can increase the amplifier's gain, as is discussed below, but leads to a lower output swing. So, whenever gain is preferred over output swing, the voltage can be increased beyond the bias point in the middle of the saturation region.

2.2 Small-Signal Analysis of Common Source Amplifier

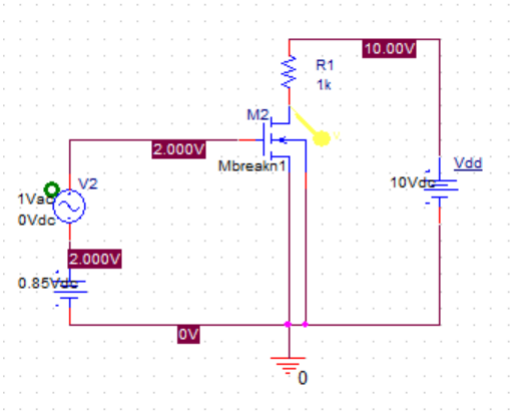

Figure 4: Common Source Amplifier with Sinusoidal Input

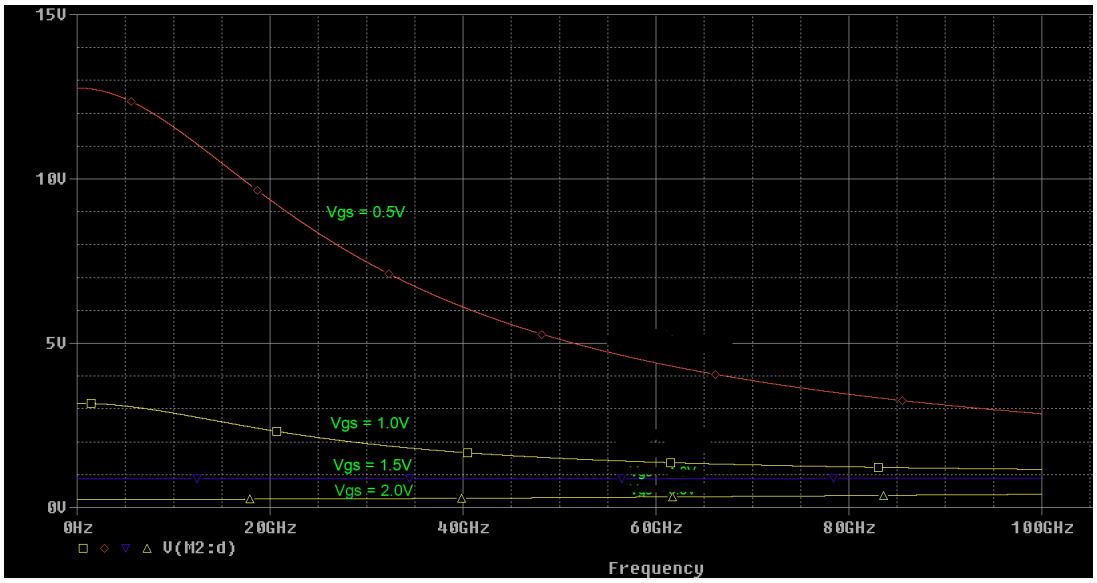

Figure 5: AC Sweep of Common-Source Amplifier

Given the SPICE MOSFET model parameters, the NMOS's transconductance parameter k_n is approximately $19.4\frac{mA}{V^2}$. Its transconductance g_m is given by $k_n V_{ov}$. V_{ov} is simply the bias voltage at the gate minus the threshold voltage V_T. The threshold voltage is set to 0.362984V in the MOSFET model.

Table 1: g_m Values for Different V_{GS} Bias Points

Vgs [V]	gm [mA/V]
0.5	2.7
1.0	12.4
1.5	22.1
2.0	31.8

The transconductance g_m increases with V_{GS} since more charge accumulates in the channel when the gate voltage is higher. Since the MOSFET's channel can support more charge, higher currents can flow for the same applied V_{DS}. The transconductance captures how well voltage applied to the MOSFET is converted to current, so the transconductance should be higher at higher V_{GS} values.

The output resistance is given by $r_o = \frac{1}{\lambda I'_D}$. λ is given as $0.02V^{-1}$ in the SPICE model. I'_D is the saturation current without taking channel-length modulation into account. So, $I'_D = \frac{k_n}{2} V_{ov}^2$. Therefore, the output resistance is given by:

$$r_o = \frac{2}{\lambda k_n (V_{GS} - V_T)^2} \tag{1}$$

Table 2: r_o Values for Different V_{GS} Bias Points

Vgs [V]	ro [kOhm]
0.5	275
1.0	12.7
1.5	4.0
2.0	1.9

It has already been established that higher currents flow when V_{GS} is higher. If this is the case, then if one were to calculate the resistance for a fixed V_{DS} value, higher currents would flow whenever V_{GS} is increased. So, the output resistance drops as V_{GS} is increased since higher currents flow for the same applied voltage.

The open circuit small-signal gain of a common source amplifier is given by $A_{vo} = -g_m R_D$, where R_D is the drain resistance. R_D here is fixed, but g_m increases with V_{GS}. So, the small-signal gain magnitude increases with increasing V_{GS}. If V_{GS} is higher, then g_m is higher, meaning the MOSFET more easily converts a voltage applied at the gate to a current flowing through the MOSFET. So, smaller variations in the gate voltage, lead to larger variations in the drain current. V_{out} is directly related to the drain current because of the resistor in series with the MOSFET. So, smaller variations in the gate voltage lead to larger variations in the output voltage V_{out} when one increases V_{GS}. This is why the gain's magnitude increases with increasing V_{GS}.

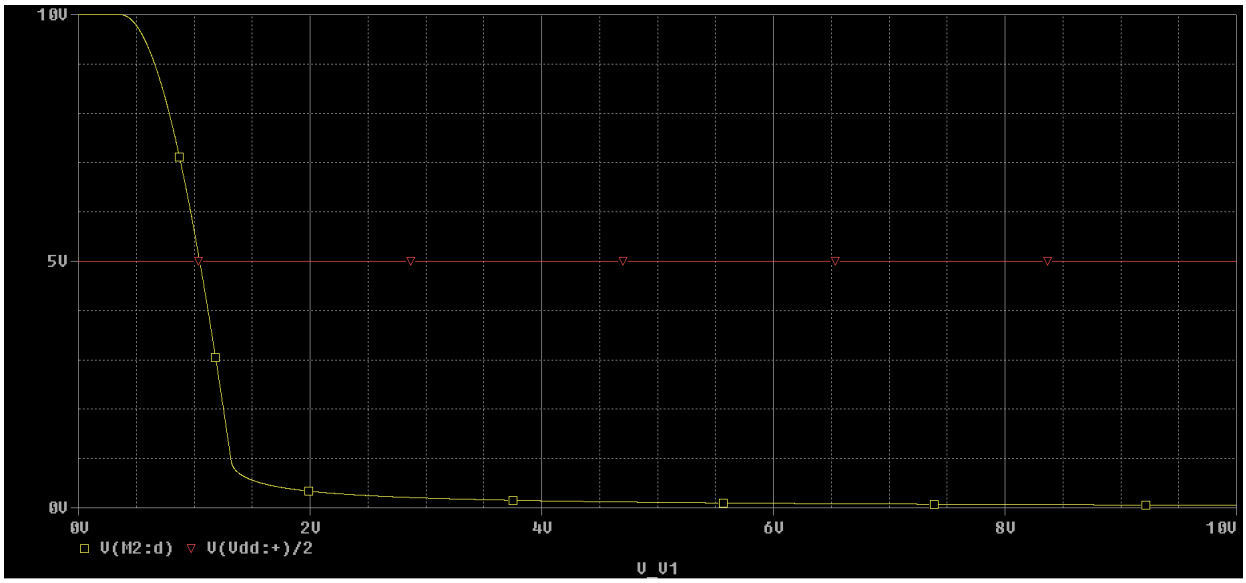

Figure 6: Voltage Transfer Characteristic

If V_{GS} is biased at about 1V, then the output voltage V_{out} is biased at about $\frac{V_{DD}}{2}$, where $V_{DD} = 10$V is the supply voltage. As the input bias voltage at V_{GS} is increased, the output bias voltage at V_{out} decreases because of the inverting nature of the common source amplifier. If the amplifier is biased in the middle of the saturation region, which is where the steep downward slope in figure (6) occurs, then varying the small-signal V_{gs} linearly varies the output voltage V_{out}. This is because the slope, or $\frac{dV_{out}}{dV_{in}}$, is steepest in this region. So, the amplifier is most linear when it is biased here. If it is biased closer to cutoff region at lower voltages or the triode region at higher voltages, varying V_{gs} could produce a clamped waveform at the output, meaning the gain is not constant, and the amplifier is not linear.

2.3 Common Source Amplifier with Active Load

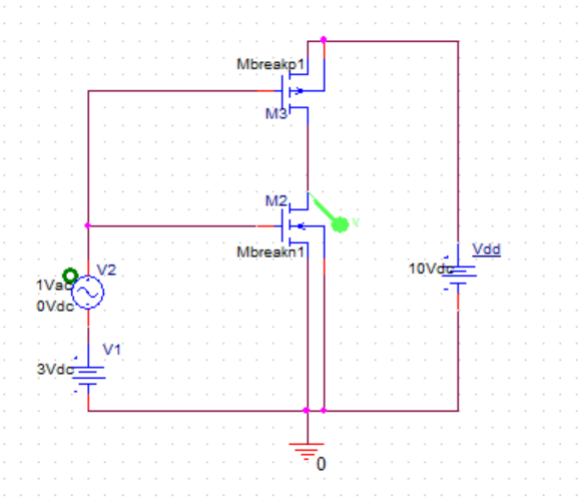

Figure 7: Common-Source Amplifier with Active Load

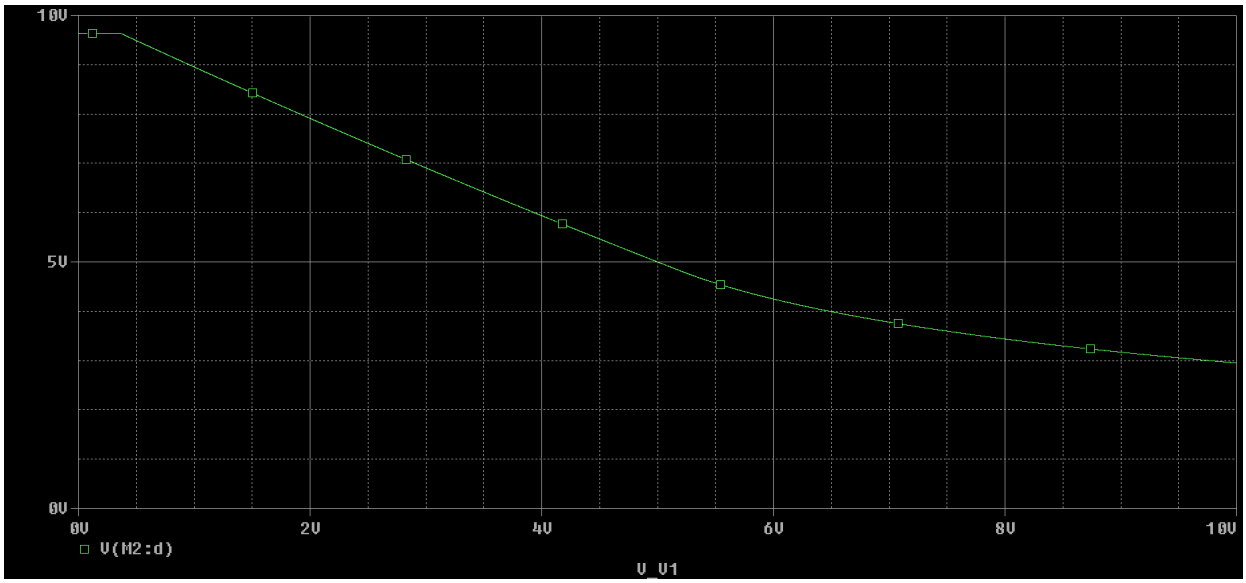

Figure 8: Voltage Transfer Characteristic

When the bias voltage V_{GS} is increased, V_{out}'s bias is decreased. For sufficiently low V_{GS} values, the output is biased at 5V. For sufficiently high V_{GS} values, the output is biased near 0V.

After the bottom transistor exits cutoff, the common-source amplifiers with both passive and active loads exhibit linear behavior until a certain point. How-

ever, now that an NMOS is being used in place of a resistor, the slope is much lower in magnitude. As a result, the gain of this amplifier is much lower than if a true resistor is to be used. Therefore, if the option is available, a true resistor is preferred to an NMOS acting as a resistor.

2.4 CMOS Amplifier

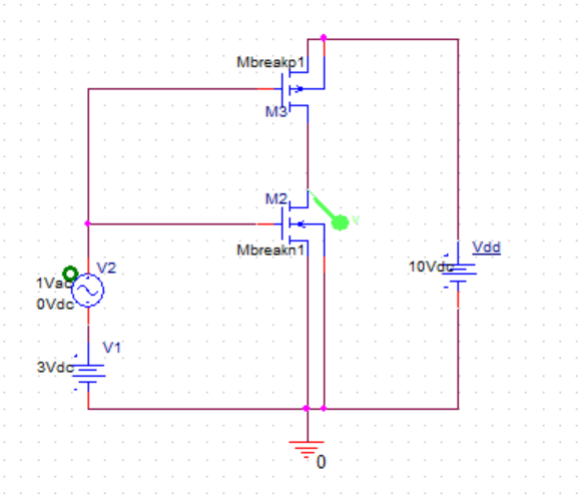

Figure 9: CMOS Amplifier

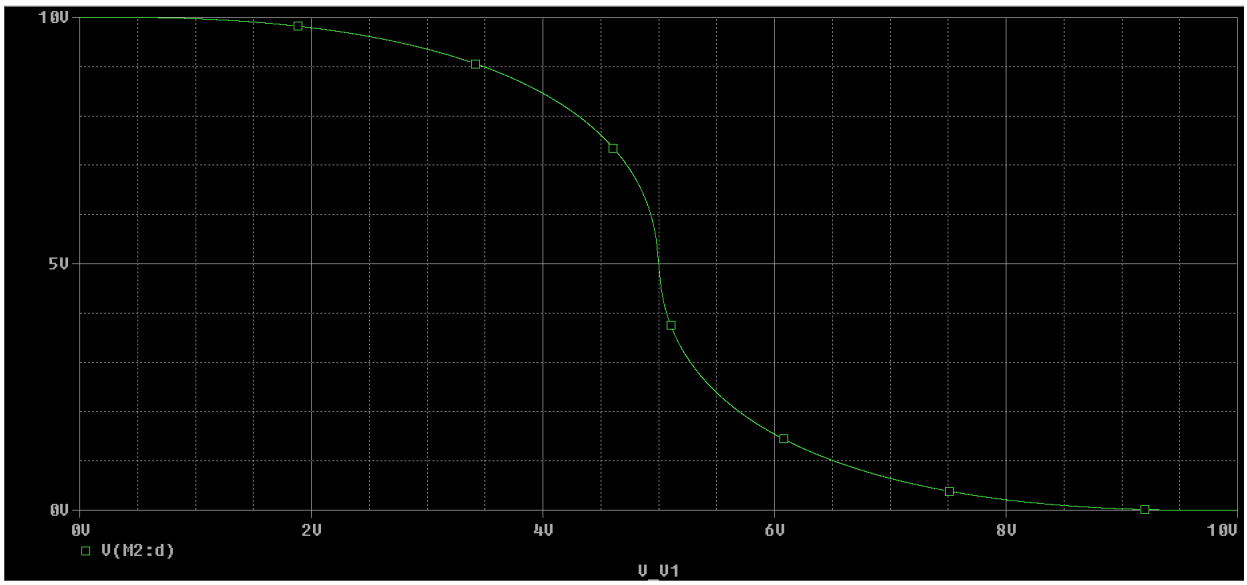

Figure 10: Voltage Transfer Characteristic

The CMOS amplifier has a sharper decrease than when only NMOS transistors are used. However, the descent is not as sharp as when a resistor is used, except possibly at $V_{GS} = 5\text{V}$. Like with the other amplifiers, increasing the input bias voltage decreases the output bias voltage.

2.5 Common Source Amplifier with Complementary Load

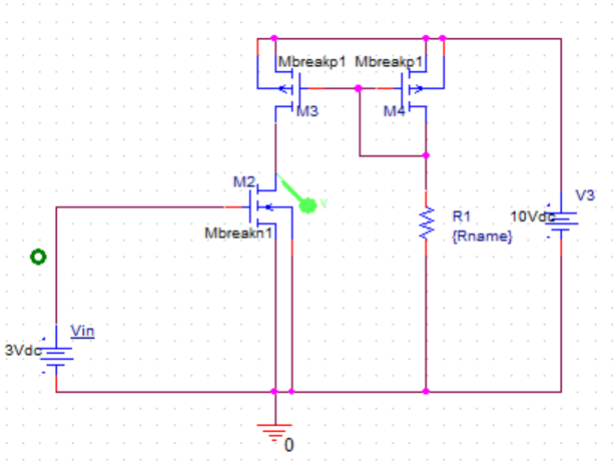

Figure 11: Common Source Amplifier with Complementary Load

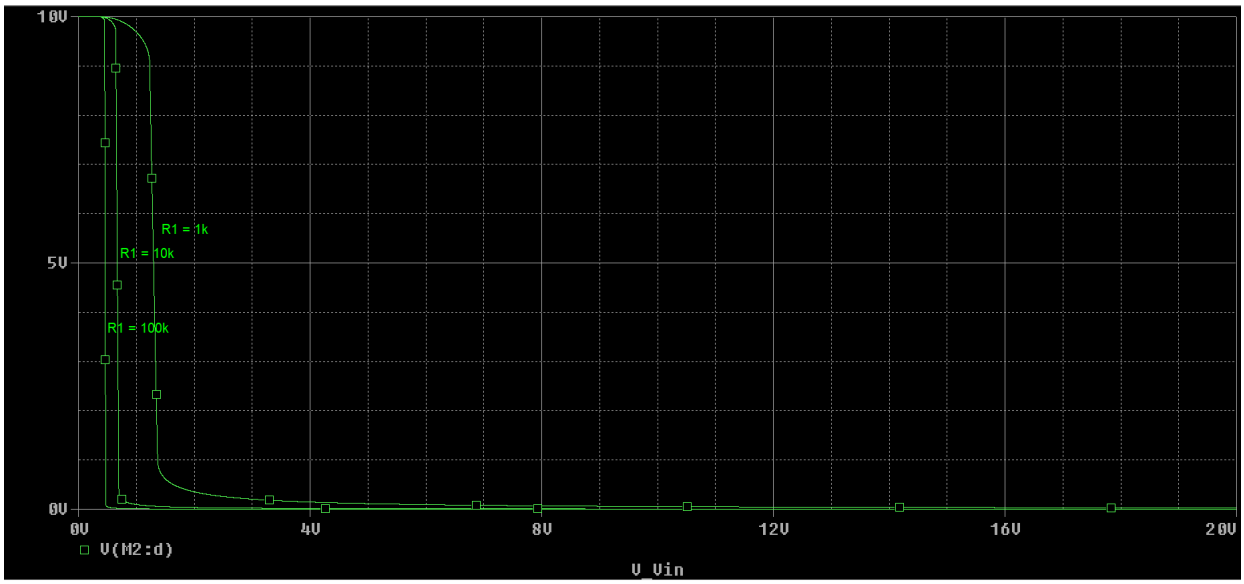

Figure 12: Voltage Transfer Characteristic

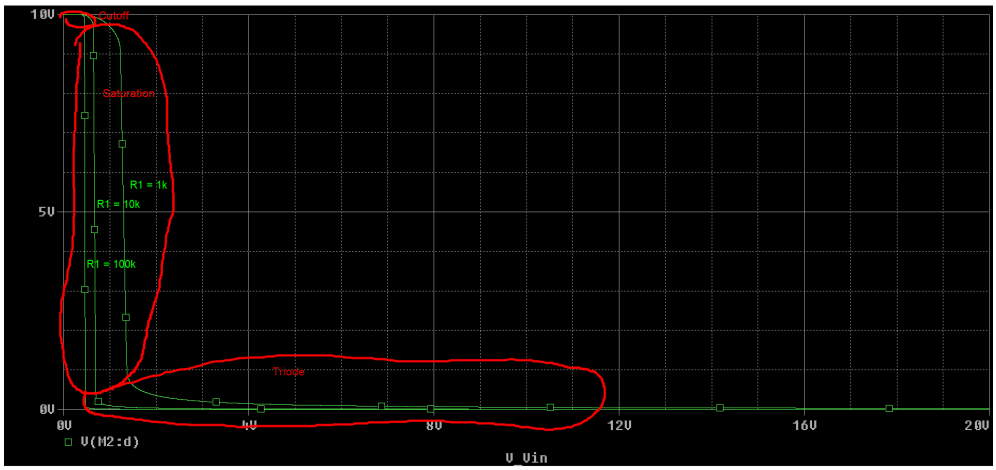

Figure 13: Voltage Transfer Characteristic with Regions of Operation

The gain can be approximated by calculating the slope of the curve in the saturation region given two points. For $R_1 = 1\text{k}\Omega$, the gain is approximately $-58\frac{V}{V}$. For $R_1 = 10\text{k}\Omega$, the gain is approximately $-170\frac{V}{V}$. For $R_1 = 100\text{k}\Omega$, the gain is approximately $-507\frac{V}{V}$.

Table 3: Voltage Gain at Different R_1 Values

R1 [kOhm]	Gain [V/V]
1	-58
10	-170
100	-507

Again, the best resistor value is the one that leads to the steepest descent, or equivalently highest gain, in the saturation region. This occurs when the load is largest. So, $R_1 = 100\text{k}\Omega$ is the best choice for a good voltage amplifier and inverter.

3 Conclusion

For the common source amplifier with a passive load, the largest resistor value leads to the highest gain and good linearity. The amplifier should be biased in the saturation region for best results. As the bias voltage V_{GS} is increased, g_m and gain increase, and r_o decreases. When an active load, namely an NMOS transistor, is used in place of a resistor, the performance is not as good. The CMOS amplifier offers better performance than using two NMOS transistors.

When a complementary load is simulated, again, the largest resistor tends to lead to higher gains and better linearity.