1 PSpice Simulation

The D-Latch circuit was built using an inverting CMOS structure and four NAND gates, using two PMOS and two NMOS transistors each. The circuit is shown in figure 1.

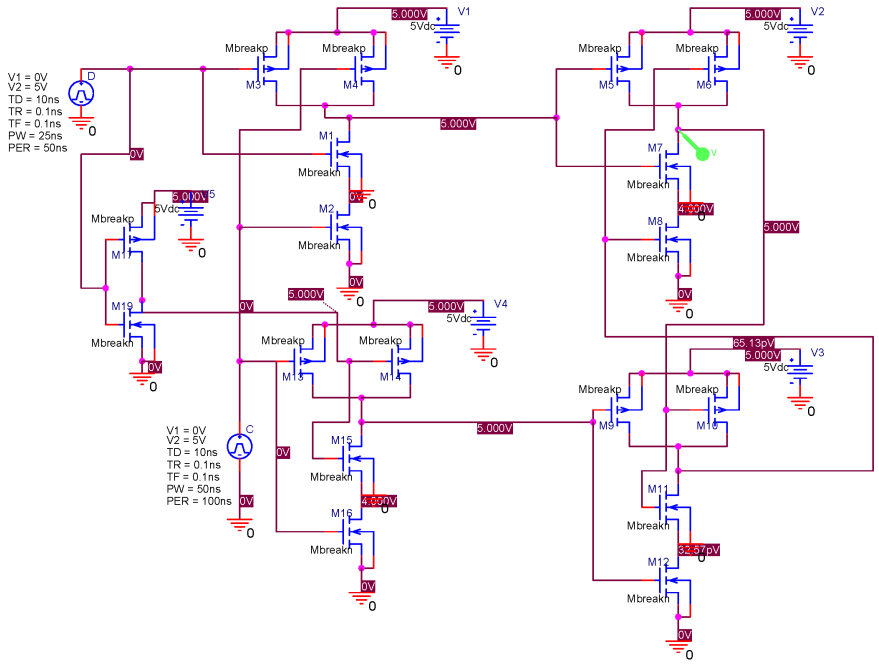

Figure 1: The D-Latch circuit model for PSpice simulation.

Our assumption is that when the control input is high the value of the input, D, will be stored as the output value. This value will change with D; however, when the control input is low the value of the output cannot be changed. For example, if we have D high and C high, the output will be high, but if we then change C to low, then the value of D before the change will be stored as the output value until C is brought high again. The behavior of the D-Latch is shown in the FSM in figure 2.

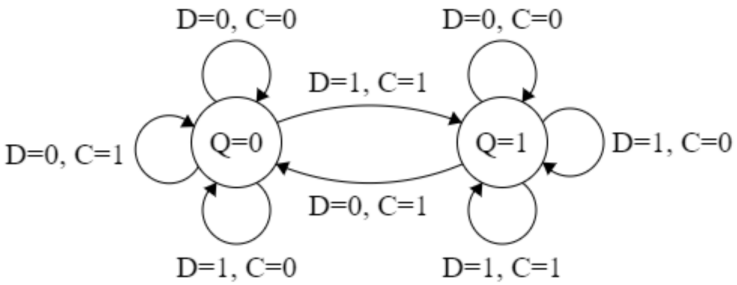

Figure 2: The behavior of a D-Latch.

The results of all the simulations were consistent with the assumed behavior of the D-Latch circuit. In figure 4 it is shown that when the control input is high the value of input D is stored at the output Q, and when the control input is low the value of D is passed to the output Q. For this simulation the input and control input the settings in figure 3 were used. These values were supplied in the lab specification document.

There is a small spike that occurs when D is becoming high while C is becoming low. This is believed to be due to propagation delays that occur while the values are changing; however, these effects quickly die out and the values returns to the expected behavior.

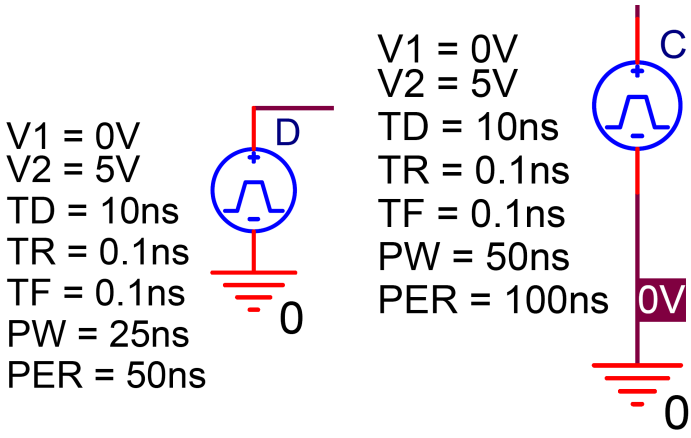

Figure 3: The simulated input (left) and the simulated control input.

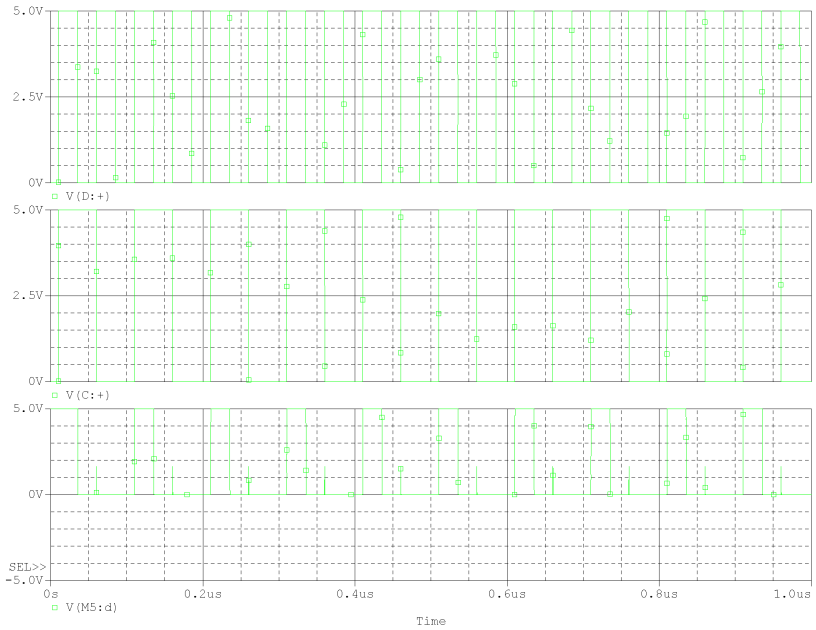

Figure 4: The simulation results of our D-Latch, using inputs from figure 3.