0.0.1 Gain and Frequency Response of Common-Emitter Amplifier

This portion of the experiment demonstrates the amplification behavior of the inverter, also known as a common-emitter amplifier. Its properties are characterized by analyzing its gain and frequency response.
The amplifier's input signal has a 200mVpp amplitude and an 800mVpp offset. When the amplitude is increased to 400mVpp, distortions occur in which the waveform becomes clipped. This is because the output waveform is amplified, but its peak and trough voltages are limited by the supply and ground voltages, respectively.

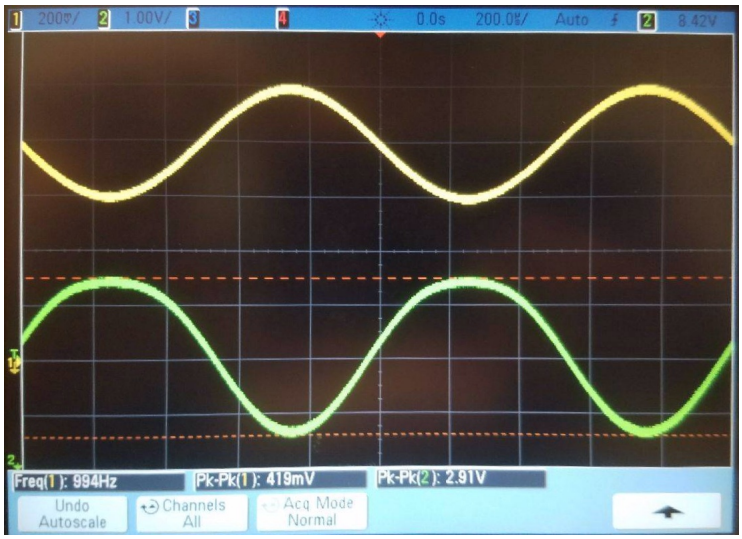
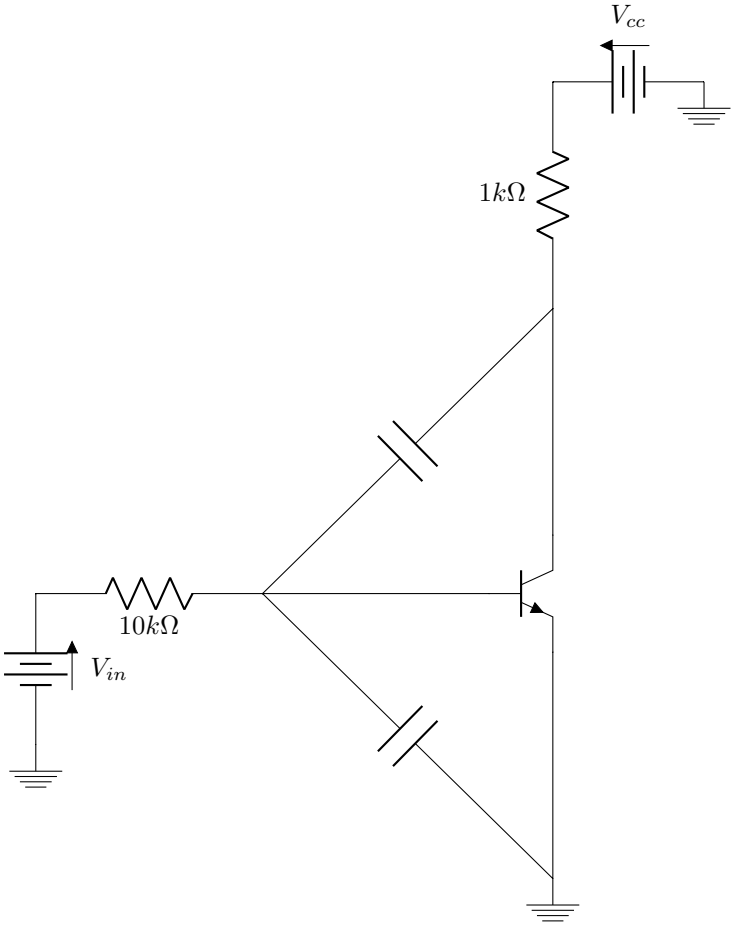


Figure 1: Common-Emitter Amplifier 10kHz Distortions

The amplifier does not have a perfect frequency response due to the structure of the BJT used. The BJT has two pn-junctions, one between the collector and the base and one between the base and the emitter. Due to a variety of effects, the junctions each have an associated capacitance. At DC, current can easily flow through the BJT. Thus, these capacitances are not accurately modeled using a series capacitance since that would simply charge. A better model uses parallel capacitances, like in figure (**??**) below:

Figure 2: High Frequency BJT Model



At low frequencies, the parasitic capacitances acts as broken circuits. Thus, the circuit reduces to an ideal common-emitter amplifier. However, at higher frequencies, signals can short through the parasitic capacitances. Specifically, a short path exists between ground and the collector, making $V_{out} = 0$V. Thus, as frequency increases, the output voltage for a given input voltage, and therefore the gain, should drop. This is because gain is defined as $\frac{V_{out}}{V_{in}}$ [**??**].

At 10kHz, the input voltage is the starting value of 200mVpp, and the output voltage is 1.63Vpp. Thus, the gain is 8.15. Since parasitic capacitances should drop the gain at higher frequencies, a cutoff frequency can be defined. The cutoff frequency f_c is the frequency at which the output voltage is $\frac{1}{\sqrt{2}}$ of the peak output voltage for a given input voltage [**??**]. So, in this case, f_c is the frequency at which the output voltage is $\frac{1.63}{\sqrt{2}}$ Vpp $\approx$ 1.15 Vpp. This can be measured by simply increasing the frequency until an output voltage amplitude

of 1.15 Vpp occurs. Using this method, the cutoff frequency $f_c \approx 150$kHz is obtained. At this point, the gain is approximately 5.75.

Table 1: Common-Emitter Amplifier Frequency Response

Frequency [kHz]	Gain [unitless]
10	8.15
150	5.75

0.0.2 Square Wave Response of Common-Emitter Amplifier

The frequency of the square wave response is set to the cutoff frequency $f_c = 150$kHz. In order to understand the square wave response of a common-emitter amplifier, the 20% duty cycle case is considered first.

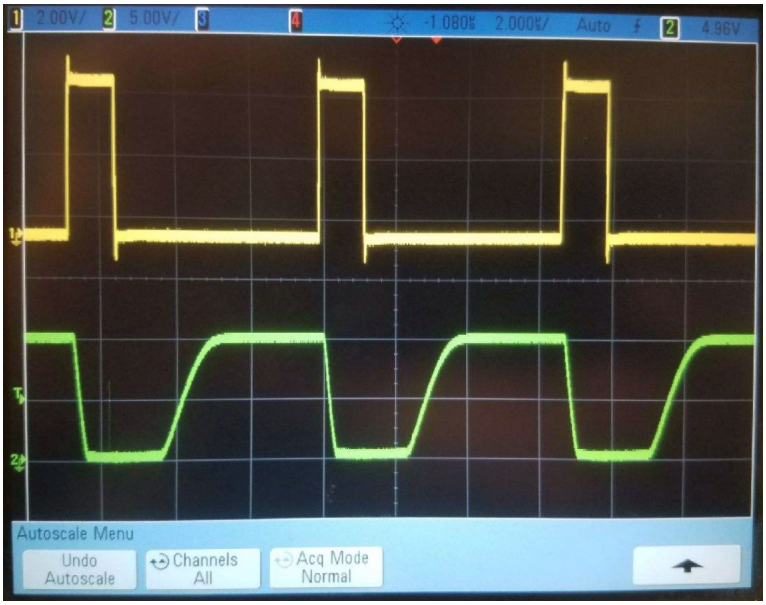


Figure 3: Common-Emitter Amplifier Square Wave Response 20% Duty Cycle

When the square wave pulse is high, the output drops nearly to ground due to the inverting characteristics of the amplifier. When the input drops to ground, the output gradually becomes high for the same reason. There is a brief delay between the falling edge of the input waveform and the rising "edge" of the output waveform. This is because the capacitors in figure (2) need to charge first before the low-pass filter's DC characteristics take over. The charging and discharging of the capacitors represents the formation and destruction of the depletion regions in the BJT.
The reason the output waveform appears to saturate is because the duty cycle

is low enough that the input signal remains low for long enough that a steady state can be established. It saturates at 10V, the supply voltage, because the output voltage cannot exceed supply. The amplifier operates on the principle of using the weaker signal to enable or disable a transistor switch that controls a larger voltage. This larger voltage is the supply voltage, which is why the output cannot exceed supply.
When the duty cycle is increased to 50%, the same physical principles still apply.

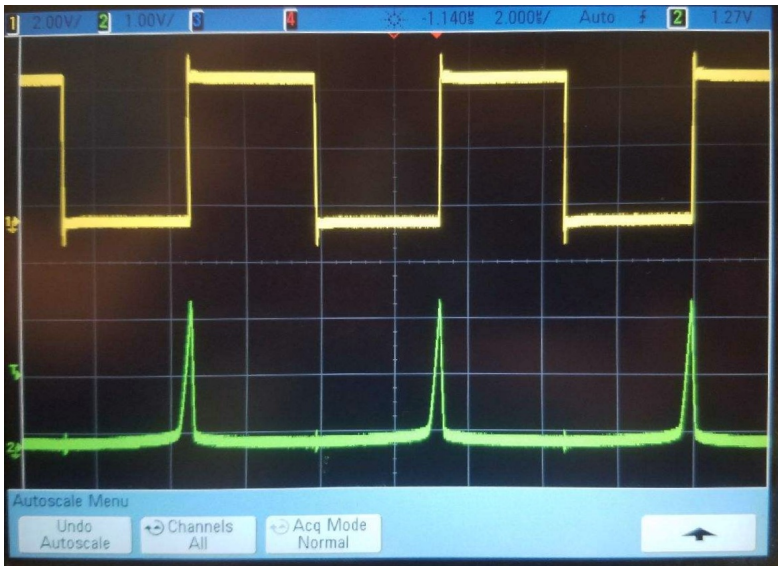


Figure 4: Common-Emitter Amplifier Square Wave Response 50% Duty Cycle

The output waveform waits for a time delay and then begins to develop. However, because the duty cycle is longer, the input signal remains low for a shorter period of time. Thus, the output voltage does not have a sufficient amount of time to fully develop and is cut short when the rising edge of the input occurs.

References

http://www.ittc.ku.edu/~jstiles/412/handouts/5.8\%20BJT\%20Internal\%20Capacitances\%20and\%20high\%20frequency\%20model/section\%205_8\%20BJT\%20Internal\%20Capacitances\%20lecture.pdf
http://alignment.hep.brandeis.edu/Lab/Filter/Filter.html