0.1 CMOS Inverter

The highest quality voltage transfer characteristic occurs when a sine wave input is applied. It may have to do with the relatively higher density of points in a sine wave since the sine wave is longer than the ramp in one period if unrolled. The noise margins are similar to what is often received in simulation results for well-designed CMOS inverters.

0.2 NAND Gate

The SPICE simulation and the logic chart for the two-input NAND gate effectively show the true behavior of the circuit constructed on the bread board. However, the true behavior of the circuit would also show propagation delay between the input and output waveforms. But propagation delay may be negligible because the circuit is tested using low-frequency kHz square waves as inputs.

0.3 NOR Gate

The two-input NOR gate simulation results were consistent with our logic and theory for the circuit. While testing the NOR gate configuration of the CD4007, there would likely be propagation delays and other non-ideal behavior. Given that our frequency is only $1kHz$ these effects may be negligable.