

A CMOS inverter and CMOS logic NAND gate is constructed to be used in the D Latch layout design.

The width and length of the NMOS to be used in the inverter is given to be $0.5\text{ }\mu\text{m}$ and $0.1\text{ }\mu\text{m}$, respectively. The PMOS to be used in the inverter is then designed so that the inverter is matched (steepest slope of the VTC curve occurs when $V_{out} = V_{in} = \frac{V_{DD}}{2}$). The CMOS inverter is matched using a PMOS with a width $W = 1.2\text{ }\mu\text{m}$ and a length $L = 0.1\text{ }\mu\text{m}$. This results in the following layout for the CMOS inverter.

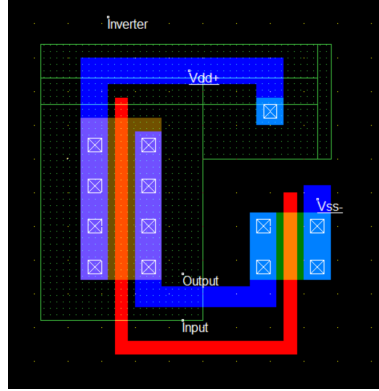


Figure 1: CMOS Inverter Layout

The VTC of the CMOS inverter shown below verifies that it is matched.

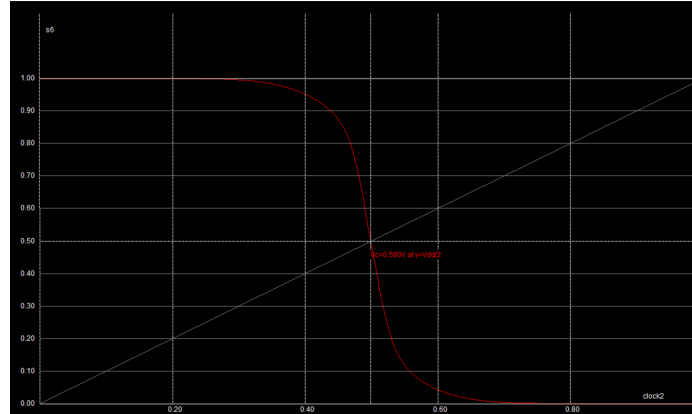


Figure 2: VTC of CMOS Inverter Layout

The logic of the CMOS inverter is verified using a 250 MHz clock input with a rise and fall time of 0.050 ns .

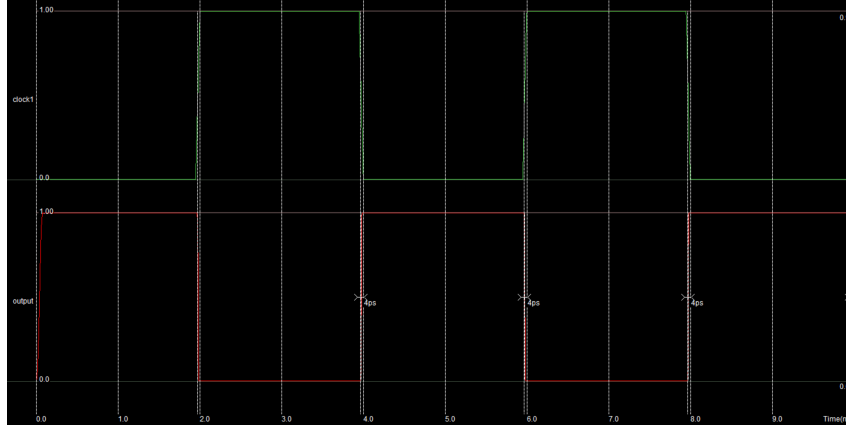


Figure 3: CMOS Inverter Logic Test

Next, a CMOS logic NAND gate is constructed with two PMOS in parallel and two NMOS in series. The NAND gate is designed so that it operates with the same speed of the CMOS inverter. To achieve this design goal, the width of both NMOS are doubled to $W = 1.0 \mu\text{m}$ so that it operates twice as fast to compensate for the speed lost due to having two NMOS connected in series. This results in the following layout for the NAND gate.

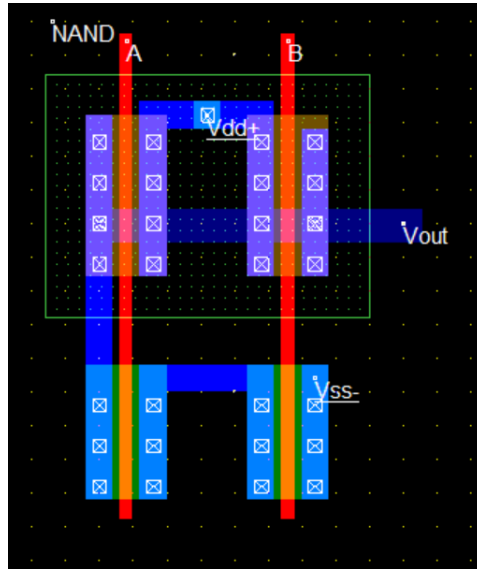


Figure 4: NAND Gate Layout

The logic of the NAND gate verified using a 250 MHz clock input and a 125

MHz clock input with rise and fall times of 0.050 ns.

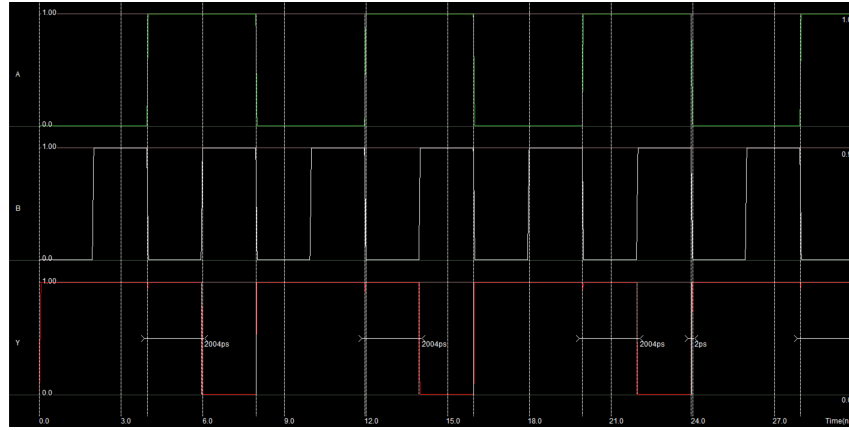


Figure 5: NAND Gate Logic Test

Using the CMOS inverter and NAND gate designed above, the following D Latch layout is constructed.

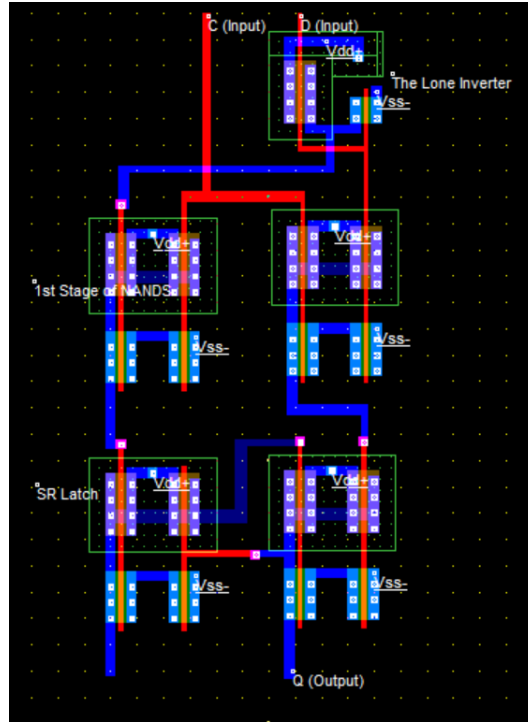


Figure 6: D Latch Layout

The expected behavior of the D Latch can be expressed in the following truth table.

Table 1: Logic Chart of D Latch Circuit

C	D	Q_{prev}	Q
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	1
0	0	1	1
0	1	1	1
1	0	1	0
1	1	1	1

The truth table above translates to the the following finite state machine (FSM).

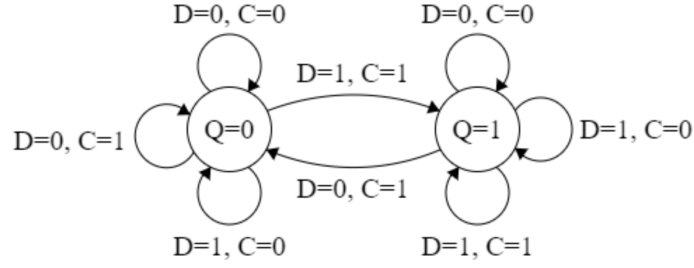


Figure 7: D Latch FSM

The delays for the transitions between Q high and Q low (τ_{PHL}) and vice versa (τ_{PLH}) can be used to determine the maximum operating frequency of the D Latch.

The D Latch is tested with input clock C at 250 MHz, 1 GHz, and 4 GHz with clock D always set to half the frequency of C. Rise and fall times of 0.050 ns and 0.001 ns are tested for each clock frequency.

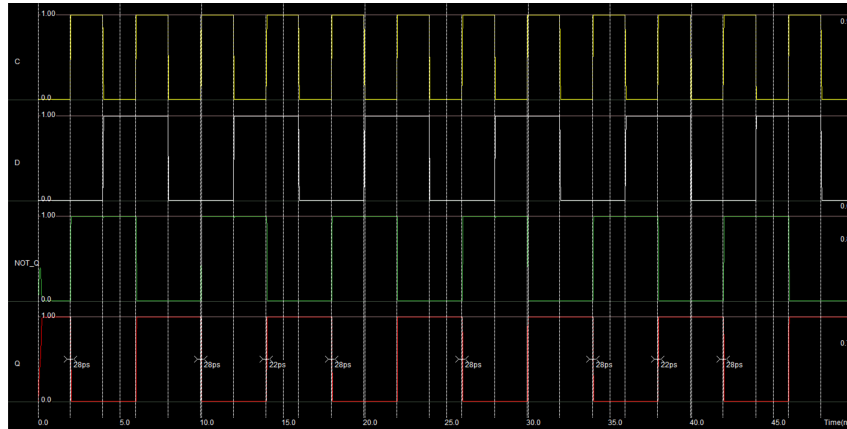


Figure 8: Test Case 1 - $f_C = 250$ MHz, Rise/Fall Time = 0.050 ns

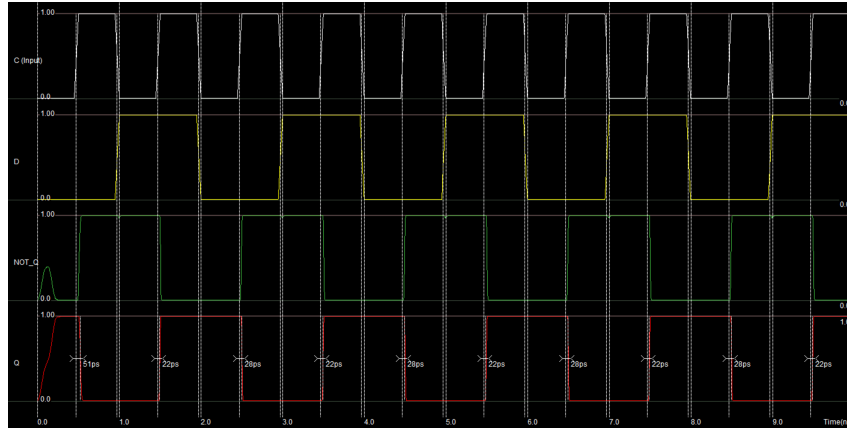


Figure 9: Test Case 2 - $f_C = 1$ GHz, Rise/Fall Time = 0.050 ns

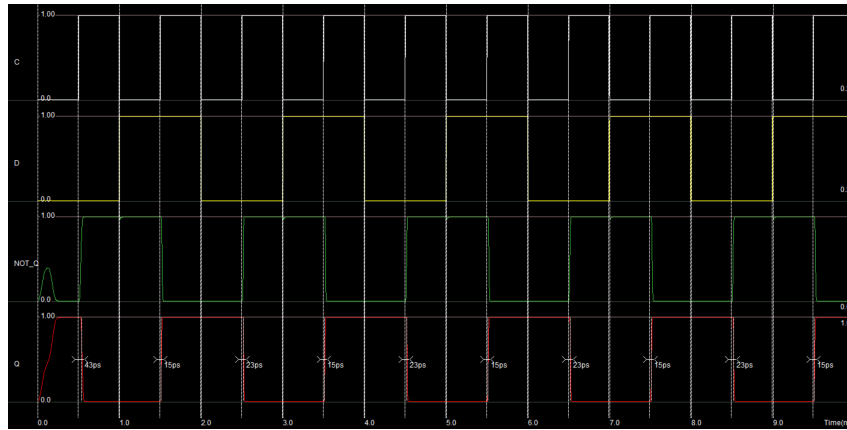


Figure 10: Test Case 3 - $f_C = 1$ GHz, Rise/Fall Time = 0.001 ns

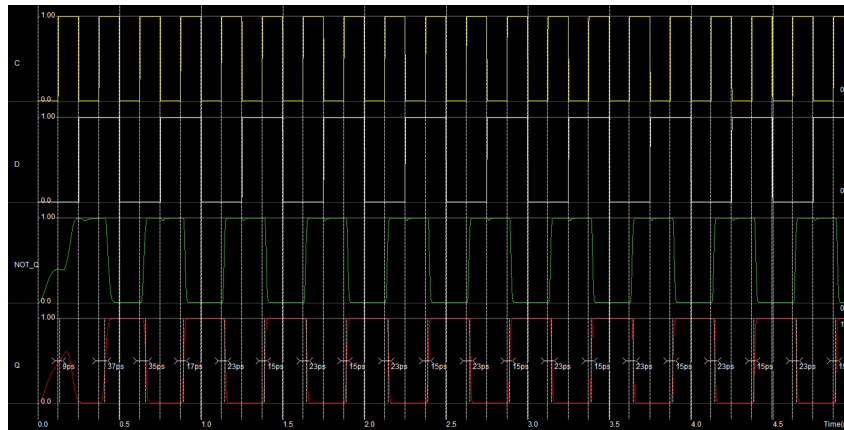
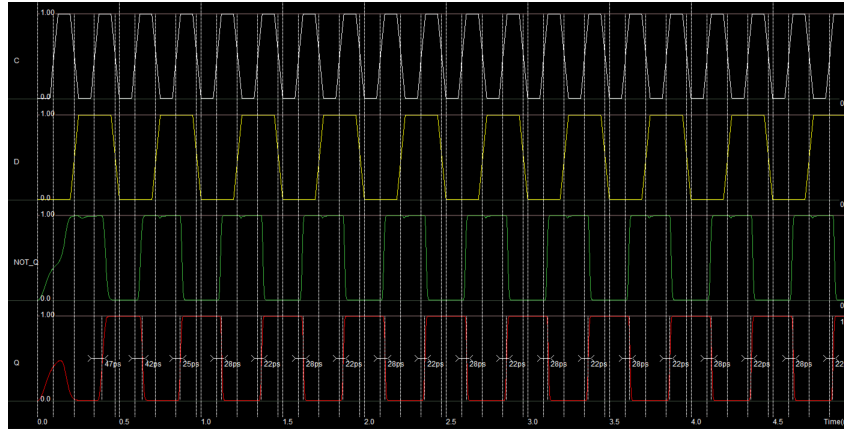


Figure 12: Test Case 5 - $f_C = 4$ GHz, Rise/Fall Time = 0.001 ns

The following delays and average power dissipation values are found.

Table 2: D Latch Layout Test Results

fC [GHz]	fD	Rise/Fall Time [ns]	tPHL of Q [ps]	tPLH of Q [ps]	Average Power [uW]
0.25	0.125	0.050	28	22	4.340
1	0.5	0.050	28	22	16.218
1	0.5	0.001	23	15	14.240
4	2	0.050	28	22	58.177
4	2	0.001	23	15	52.991

It is observed that the delay of the D Latch is only dependent on the rise and fall times of the input clocks. This behavior is expected because the dynamic

portions of the inputs are kept constant, and the length of the static portions of the input should not affect the performance of the circuit as long as they are longer than the delays.

Rise and fall times of the input signals affect the propagation delays. So, in order to discuss critical path delays and other timing metrics, rise and fall times need to be fixed so that those figures are meaningful. Otherwise, one could simply change the rise and fall times of the input signals and argue that certain circuits operate differently from or better than other circuits. So, the standard used herein for measuring propagation delays is when the rise and fall times are smallest at 0.001 ns.

A propagation delay only technically matters when the output transitions from one state to another. When the rise and fall times of the input clocks are 0.001 ns, the output delays are given by $\tau_{PHL} = 23$ ps and $\tau_{PLH} = 15$ ps. The FSM for the latch contains only two transitions whose delays would be measurable, when $C = 1$, $D = 1$, and $Q = 0$ and when $C = 1$, $D = 0$, and $Q = 1$. The former corresponds to τ_{PLH} since Q transitions from 0 to 1 before the state change occurs, and the latter therefore corresponds to τ_{PHL} . The longer of the two delays is $\tau_{PHL} = 23$ ps. This makes sense since the critical path delay should run through the inverter, and the inverter switching states is what causes the output to change.

So, the propagation delay is given by $\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$, which is 19 ps. So, the maximum switching frequency is given by $f_{max} = \frac{1}{2t_p} \approx 26.3\text{GHz}$.

The length of the D Latch layout is 12.650 μm and the width of the layout is 5.850 μm . The total area of the layout is $74\mu\text{m}^2$.

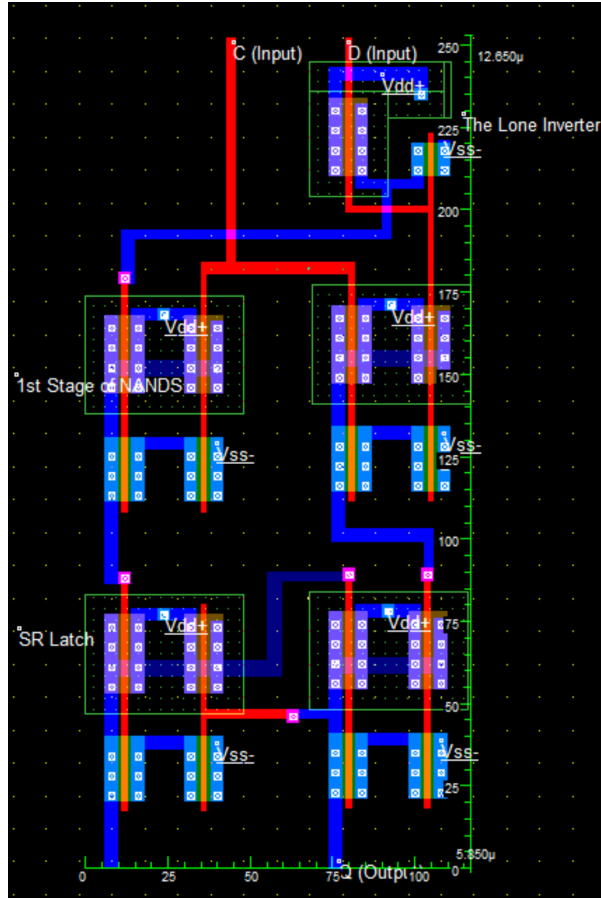


Figure 13: Total Area of D Latch Layout

Operating at 1 GHz, the average power consumption is determined to be 14.240 μ W.

Table 3: Final Layout Characteristics

Maximum Switching Frequency [GHz]	26.3
Power Consumption at 1 GHz [μ W]	14.240
Layout Area [μ m ²]	74

The maximum switching frequency far exceeds the required 1GHz, the power consumption falls well below the required 100W, and the area is considerably smaller than the required 100 m^2 . Therefore, the design satisfies the specification.