A CMOS inverter and CMOS logic NAND gate is constructed to be used in the D Latch layout design.

The width and length of the NMOS to be used in the inverter is given to be 0.5 nm and 0.1 nm, respectively. The PMOS to be used in the inverter is then designed so that the inverter is matched (steepest slope of the VTC curve occurs when $V_{out} = V_{in} = \frac{V_{DD}}{2}$). The CMOS inverter is matched using a PMOS with a width $W = 1.2$ nm and a length $L = 0.1$ nm. This results in the following layout for the CMOS inverter.

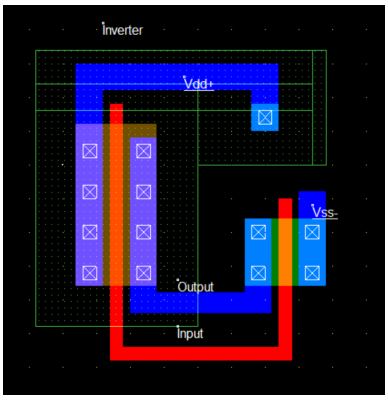

Figure 1: CMOS Inverter Layout

The VTC of the CMOS inverter shown below verifies that it is matched.

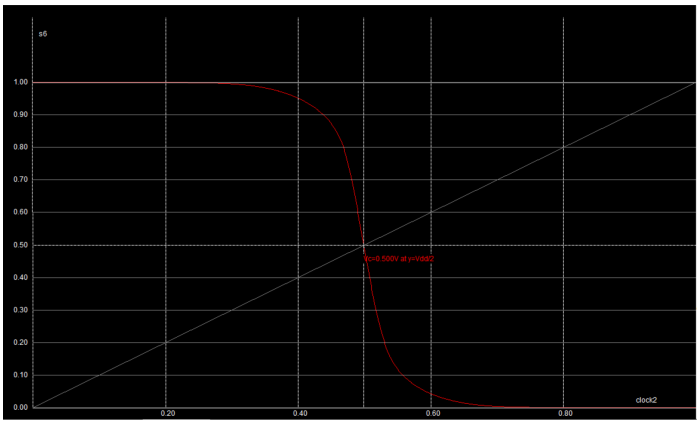

Figure 2: VTC of CMOS Inverter Layout

The logic of the CMOS inverter is verified using a 250 MHz clock input with a rise and fall time of 0.050 ns.

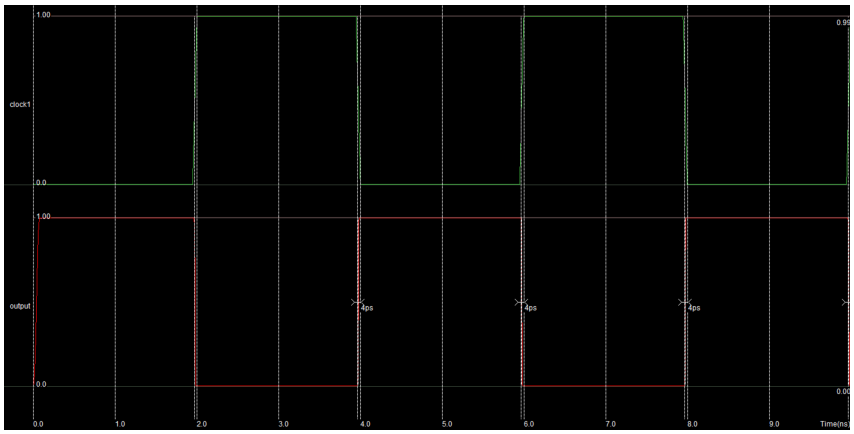

Figure 3: CMOS Inverter Logic Test

Next, a CMOS logic NAND gate is constructed with two PMOS in parallel and two NMOS in series. The NAND gate is designed so that it operates with the same speed of the CMOS inverter. To achieve this design goal, the width of both NMOS are doubled to $W = 1.0$ nm so that it operates twice as fast to compensate for the speed lost due to having two NMOS connected in series. This results in the following layout for the NAND gate.

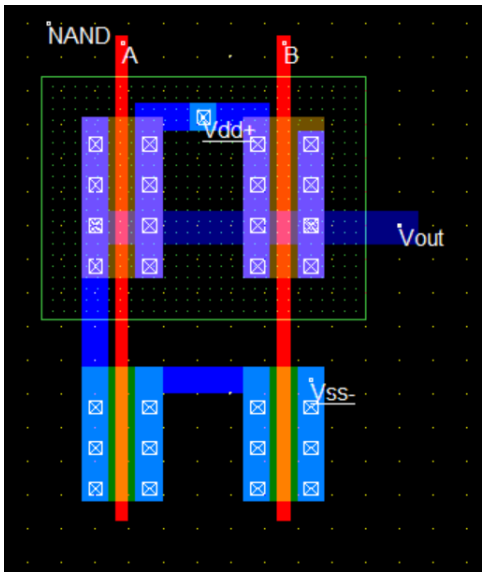

Figure 4: NAND Gate Layout

The logic of the NAND gate verified using a 250 MHz clock input and a 125

MHz clock input with rise and fall times of 0.050 ns.

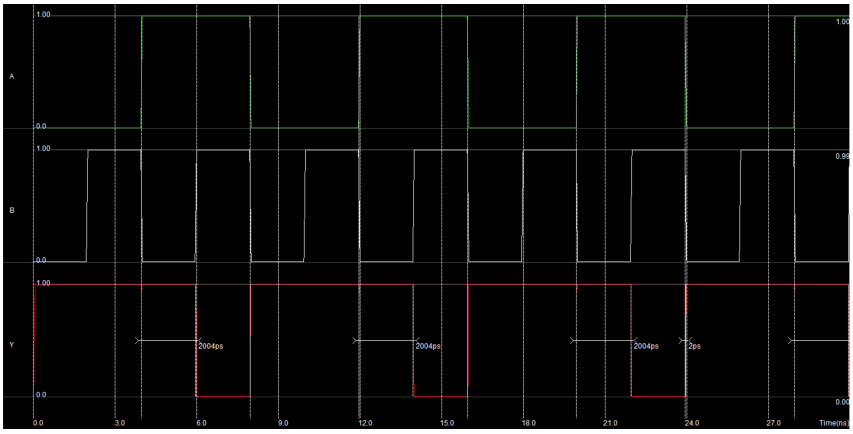

Figure 5: NAND Gate Logic Test

Using the CMOS inverter and NAND gate designed above, the following D Latch layout is constructed.

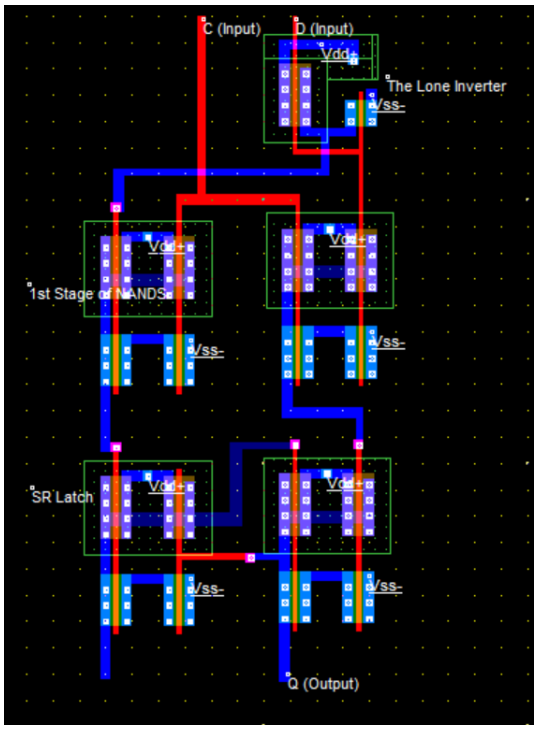

Figure 6: D Latch Layout

The expected behavior of the D Latch can be expressed in the following truth table.

Table 1: Logic Chart of D Latch Circuit

C	D	Q_{prev}	Q
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	1
0	0	1	1
0	1	1	1
1	0	1	0
1	1	1	1

The truth table above translates to the the following finite state machine (FSM).

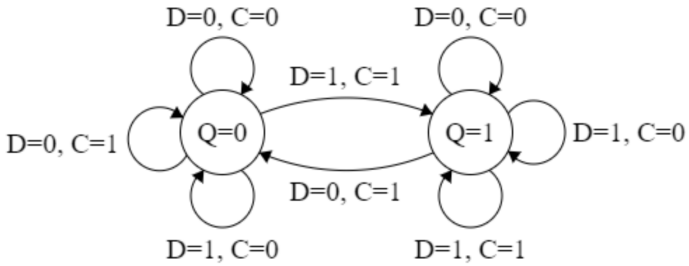

Figure 7: D Latch FSM

The delays for the transitions between Q high and Q low (τ_{PHL}) and vise versa (τ_{PLH}) can be used to determine the maximum operating frequency of the D Latch.

The D Latch is tested with input clock C at 250 MHz, 1 GHz, and 4 GHz with clock D always set to half the frequency of C. Rise and fall times of 0.050 ns and 0.001 ns are tested for each clock frequency.

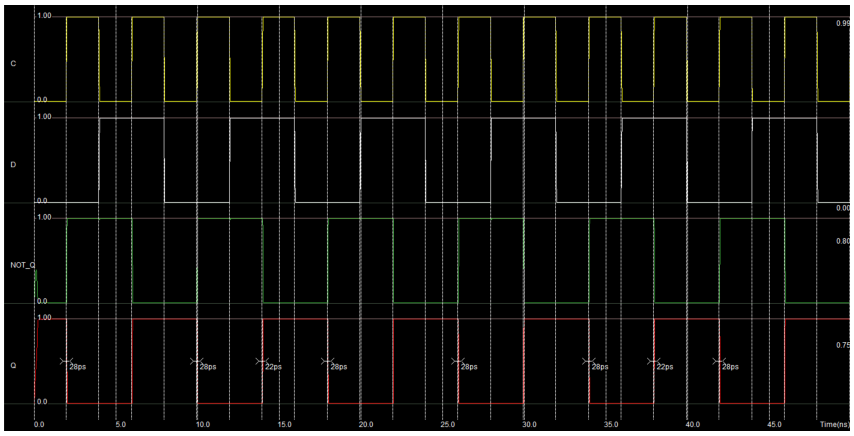

Figure 8: Test Case 1 - $f_C = 250$ MHz, Rise/Fall Time = 0.050 ns

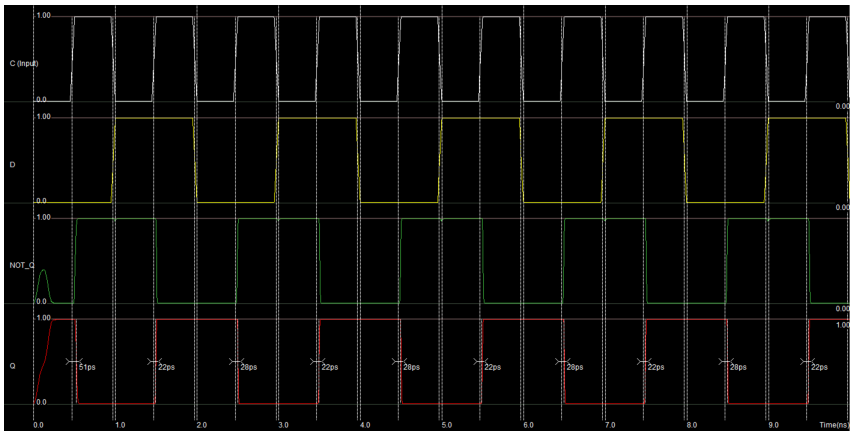

Figure 9: Test Case 2 - $f_C = 1$ GHz, Rise/Fall Time = 0.050 ns

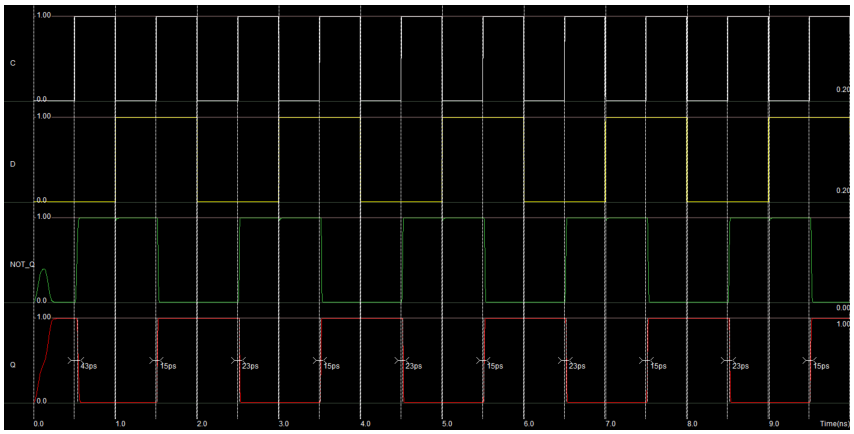

Figure 10: Test Case 3 - $f_C = 1$ GHz, Rise/Fall Time = 0.001 ns

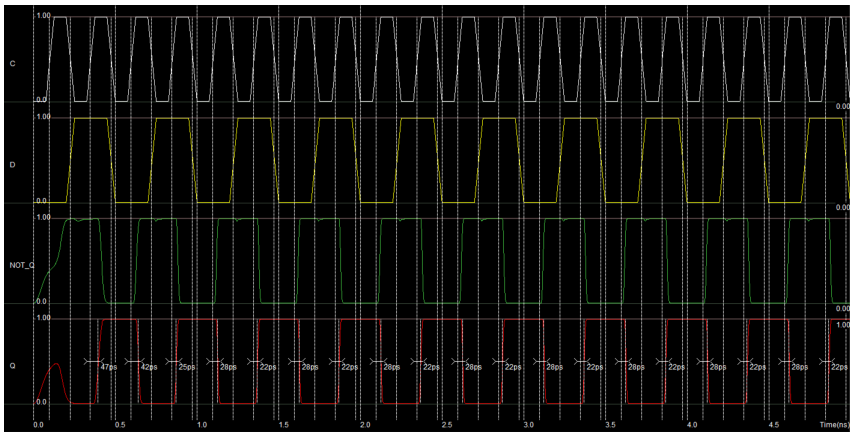

Figure 11: Test Case 4 - $f_C = 4$ GHz, Rise/Fall Time = 0.050 ns

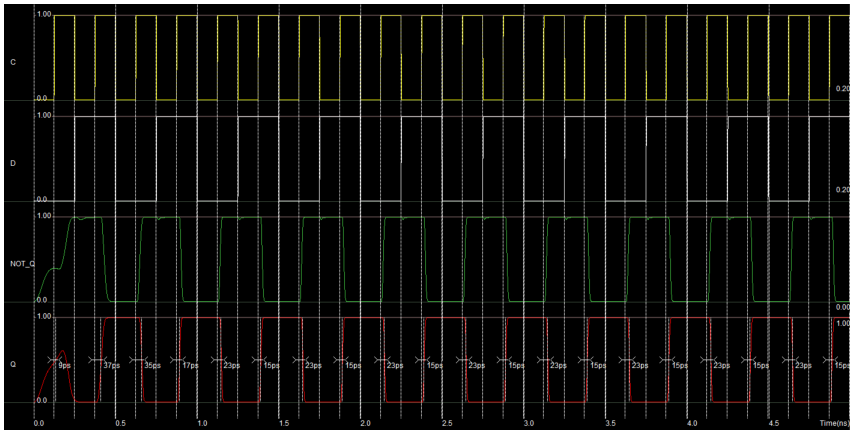

Figure 12: Test Case 5 - $f_C = 4$ GHz, Rise/Fall Time = 0.001 ns

The following delays and average power dissipation values are found.

Table 2: D Latch Layout Test Results

fC [GHz]	fD	Rise/Fall Time [ns]	tPHL of Q [ps]	tPLH of Q [ps]	Average Power [uW]
0.25	0.125	0.050	28	22	4.340
1	0.5	0.050	28	22	16.218
1	0.5	0.001	23	15	14.240
4	2	0.050	28	22	58.177
4	2	0.001	23	15	52.991

It is observed that the delay of the D Latch is only dependent on the rise and fall times of the input clocks. This behavior is expected because the dynamic

portions of the inputs are kept constant and the length of the static portions of the input should not affect the performance of the circuit as long as they are longer than the delays.

The most ideal rise and fall times of the input clocks, 0.001 ns, result in the output delays $\tau_{PHL} = 23$ ps and $\tau_{PLH} = 15$ ps. Taking the longer delay 23 ps, the maximum operating frequency of the D Latch is determined to be 1/23 ps = 43 GHz.

The length of the D Latch layout is 12.650 µm and the width of the layout is 5.850 µm. The total area of the layout is $74\mu m^2$.

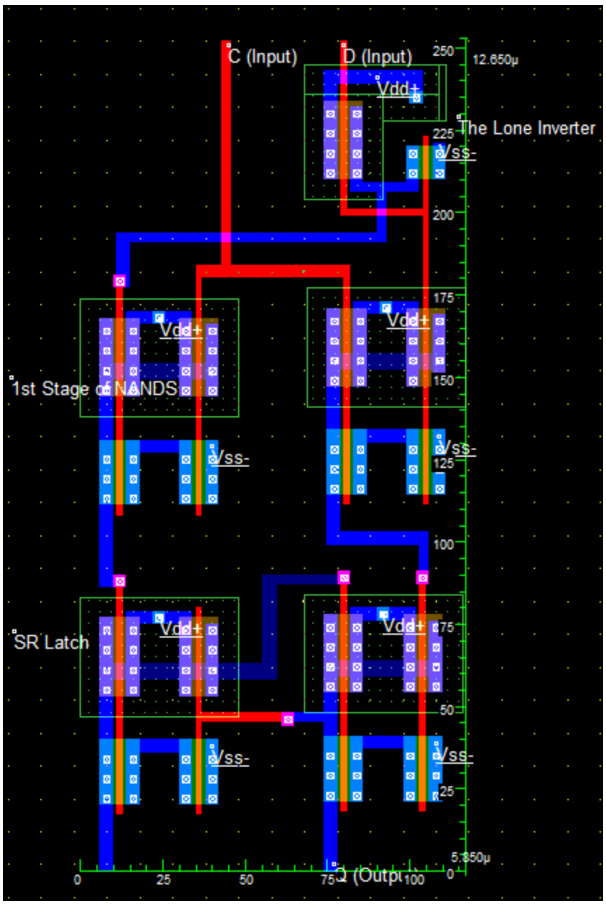

Figure 13: Total Area of D Latch Layout

Operating at 1 GHz, the average power consumption is determined to be 14.240 µW.