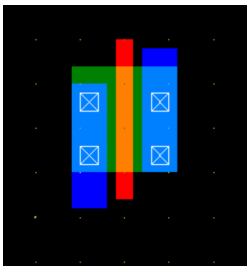

Figure 1: NMOS Layout

Figure (1) shows an NMOS transistor's layout. Figure (2) depicts the I_{DS} versus V_{DS} curve of the level 1 NMOS model.

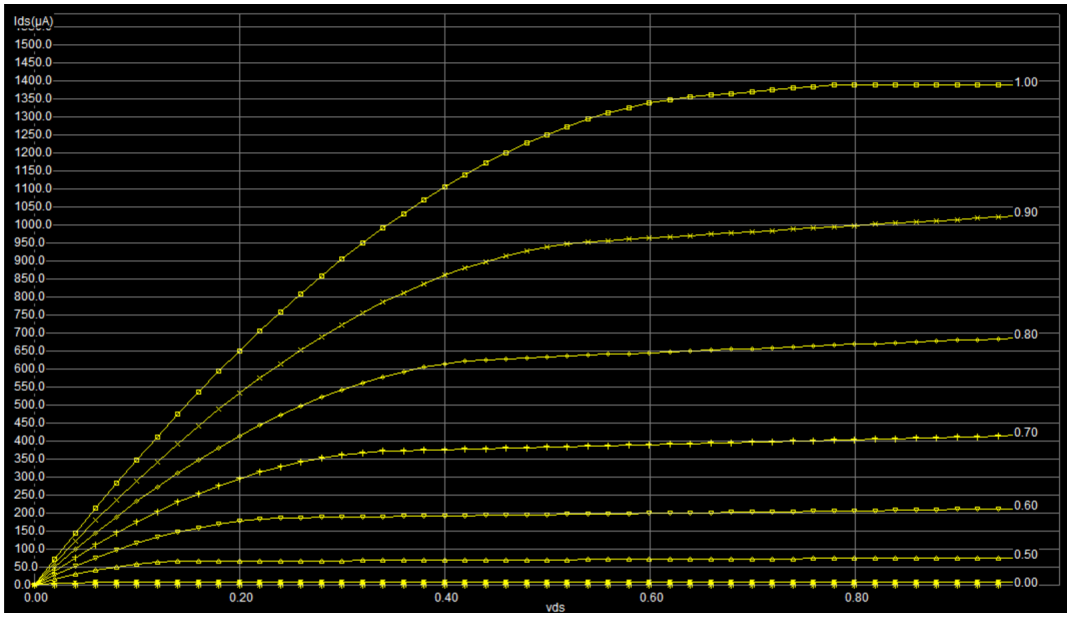

Figure 2: Level 1 NMOS Model

The L1 NMOS model is a standard transistor model that accounts for some channel length modulation effects (very slight slope in the saturation graph). When $V_{DS} = V_{GS} - V_T$, the current tapers off, and the MOSFET enters the saturation region.

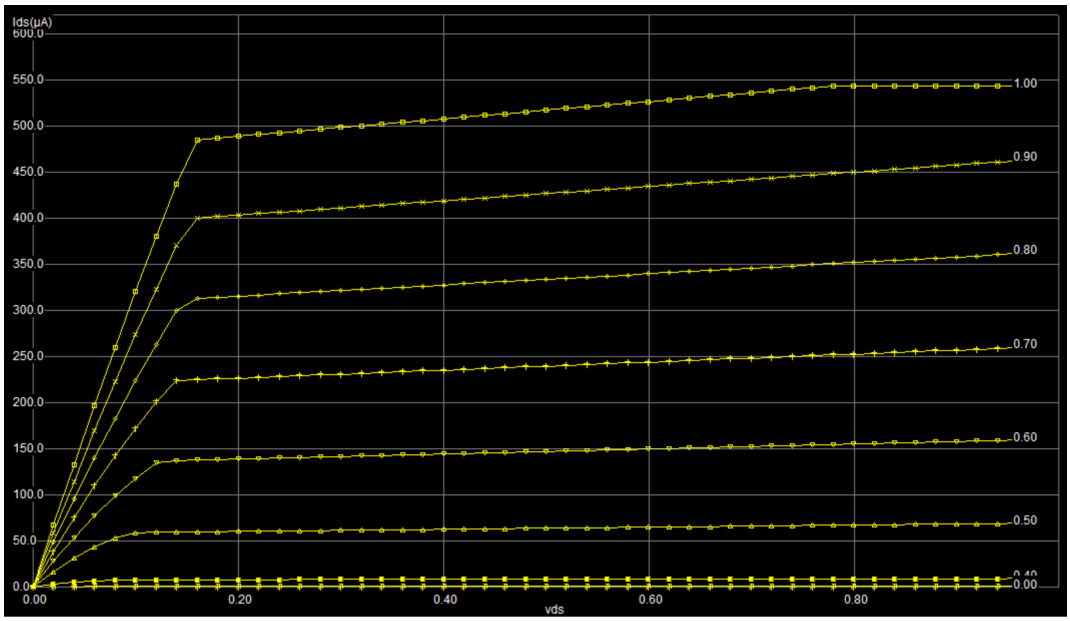

Figure 3: Level 3 NMOS Model

L3 is an improvement that accounts for effects that cause the transistor to enter saturation at lower voltages. This may be a short-channel effect in integrated circuits. If the channel is sufficiently short, the depletion regions at the source and drains can extend into the channel. As a result, the transistor may enter saturation at lower voltages since the depletion regions extend into the channel at higher drain voltages in saturation. This is the cause of channel length modulation.