

Lab 2: Hands-On Analysis of MOSFET  
Transistors and Amplifiers  
EECS 170LB

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## 1 Introduction

The  $i_D$  versus  $V_{ds}$  ( $V_{sd}$  for PMOS) curves are determined for the NMOS and PMOS transistor at different values of  $V_{gs}$  ( $V_{sg}$  for PMOS). The NMOS transistor's behavior is then further examined by acquiring the voltage transfer characteristics of a common-source and common-drain amplifier. Properties of the amplifiers, such as operating regions at different  $V_{in}$  values, are observed. A CD4007 MOSFET IC is used for the experiments.

## 2 Procedure and Results

### 2.1 NMOS

#### 2.1.1 Part A

Using the circuit shown in figure 1, we measured the drain current with  $V_{bs} = 0V$ ,  $V_{gs} = 2.5V$ , and  $0V \leq V_{ds} \leq 5V$ .

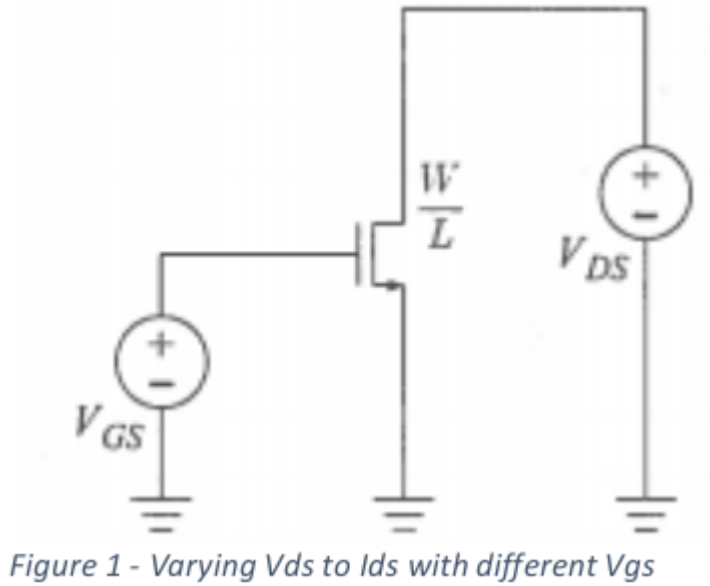


Figure 1: The circuit tested in part 1.

From the data collected for  $I_{ds}$  and  $V_{ds}$ , the NMOS starts in triode mode. A dramatic increase in drain current is observed in this region. This increase begins to taper off around  $V_{ds} \approx 0.8V$ , as the NMOS enters saturation mode. The threshold voltage is approximated to be  $V_{tn} = 1.7V$ .

$$V_{tn} = V_{gs} - V_{ds} = 2.5V - 0.8V = 1.7V \quad (1)$$

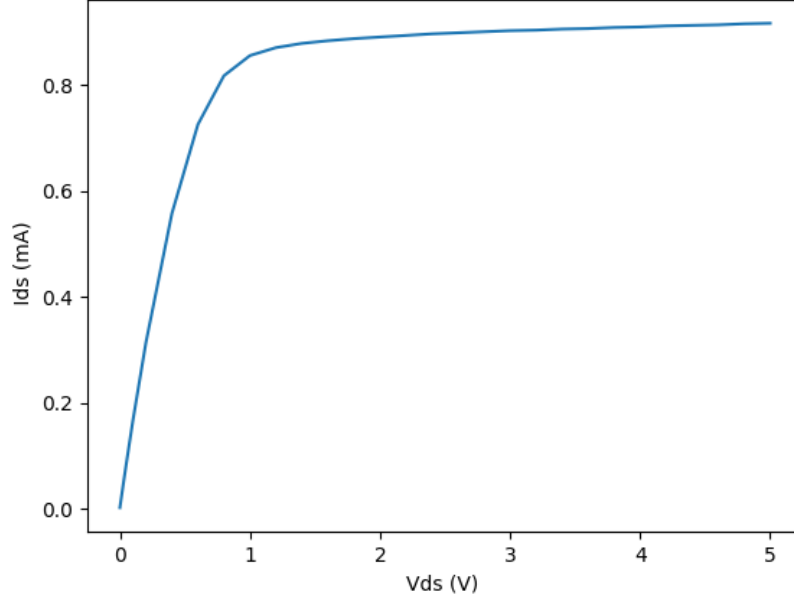


Figure 2: The resulting  $I_{ds}$  vs  $V_{ds}$  graph for  $V_{gs} = 2.5V$ .

During testing, capacitive effects in the triode region are observed. Increasing the drain voltage past  $V_{ds} = 0.15V$  results in  $I_{ds} \approx 166\mu A$ . However, decreasing the drain voltage afterward to  $V_{ds} = 0.15V$  produces  $I_{ds} \approx 310\mu A$ .

### 2.1.2 Part B

The same parameters from part A are used in part B, except the gate voltage is increased to  $V_{gs} = 5V$ . From the  $I_{ds}$  and  $V_{ds}$  curve in figure 3, the NMOS is operating in triode mode for  $V_{ds} \leq 3.2V$  and saturation otherwise.

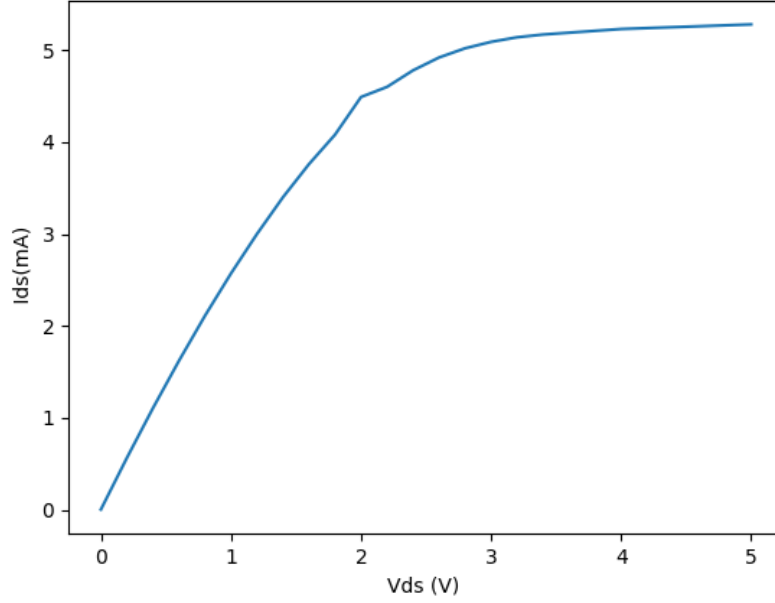


Figure 3: The resulting  $I_{ds}$  vs  $V_{ds}$  graph for  $V_{gs} = 5V$ .

The approximation from part A for the threshold voltage of  $V_{tn} = 1.7V$  can be confirmed.

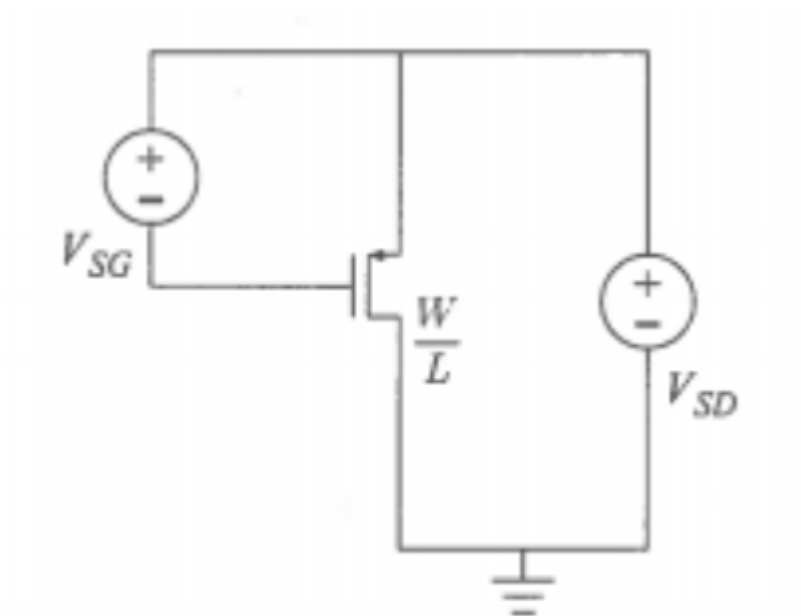
$$V_{ds} = V_{gs} - V_{tn} = 5V - 1.7V = 3.3V. \quad (2)$$

This result for  $V_{ds} = 3.2V$  as the edge of saturation agrees well with the measured data. On the curve, the drain current stays fairly constant after approximately  $V_{ds} = 3.2V$ . After comparing the percentage of change in the drain current and drain voltage, it is determined that after  $V_{ds} = 3.2V$  the change in the drain current stays at less than one percent, despite the change in drain voltage of about five percent. This result proves that the result of  $V_{tn} = 1.7V$  is a good approximation for the threshold voltage.

## 2.2 PMOS

### 2.2.1 Part A

Using the circuit shown in figure 4 we measured  $I_{sd}$  as we varied the drain voltage from within the range of  $0V \leq V_{sd} \leq 5V$ . The value of the gate voltage was set to  $V_{sg} = 2.5V$ .



*Figure 2 - Varying  $V_{sd}$  to  $I_{sd}$  with different  $V_{sg}$*

Figure 4: The PMOS transistor circuit used for our measurements.

We can see from the  $I_{sd}$  vs  $V_{sd}$  curve in figure 5 that this PMOS transistor is in cutoff until  $V_{sd} \approx 1.8V$ .

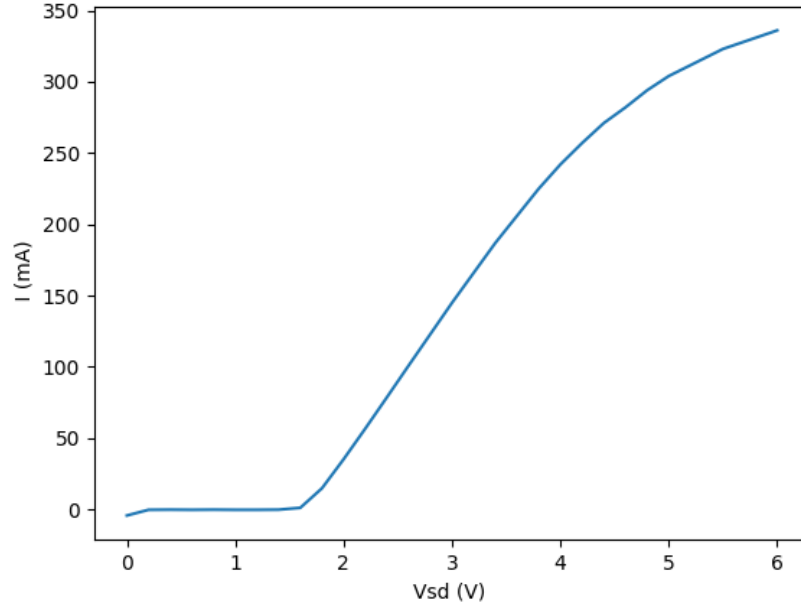


Figure 5: The resulting  $I_{sd}$  vs  $V_{sd}$  graph for  $V_{sg} = 2.5V$

To turn on this transistor the gate voltage must be greater than the source voltage by at least the absolute value of the threshold voltage. This means that at  $V_{sd} = 1.8V$ ,  $V_{sg} \geq |V_{tp}|$ .

To operate in triode mode the drain voltage must be greater than the gate voltage by at least the absolute value of the threshold voltage. The transistor enters triode mode at  $V_{sd} \geq 1.8V$ . Given that our data did not show signs of entering saturation mode, we were unable to find the saturation edge.

### 2.2.2 Part B

For part B we used the procedures from part A, but changed the gate voltage to  $V_{sg} = 5V$ .

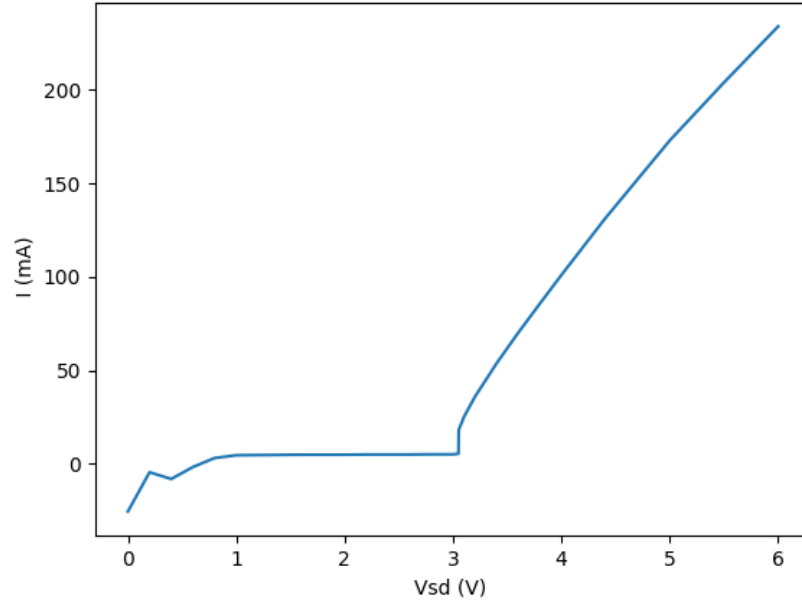
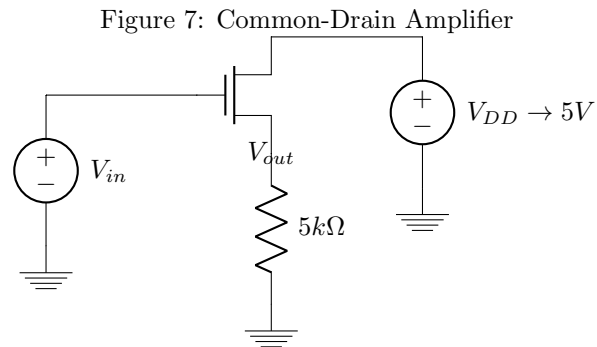


Figure 6: The resulting  $I_{sd}$  vs  $V_{sd}$  graph for  $V_{sg} = 5V$

We see that the transistor operates in cutoff until  $V_{sd} = 3.05V$ . It then operates in triode mode for the rest of the values we tested up to  $V_{sd} = 6V$ . Given that our data did not show signs of entering saturation mode, we were unable to find the saturation edge.

### 2.3 Common Drain Amplifier



A common-drain amplifier is to be constructed.  $V_{in}$  is swept from 0V to 5V. The following is the saturation condition for the NMOS transistor:

$$V_{DS} > V_{GS} - V_T \rightarrow V_D > V_G - V_T \rightarrow V_{in} < 5V + V_T \quad (3)$$

So long as  $V_{in}$  stays below 5V and high enough that the MOSFET does not enter the cutoff region, it remains in saturation. So, for small values of  $V_{in}$ , the transistor operates in the cutoff region because a current-enabling channel cannot form. Once  $V_{in}$  is high enough that the channel can form, the transistor operates in the saturation region due to the high drain voltage "pinching-off" the channel. By design,  $V_{in}$  never exceeds 5V. So, the transistor transitions from cutoff to saturation during the DC sweep.

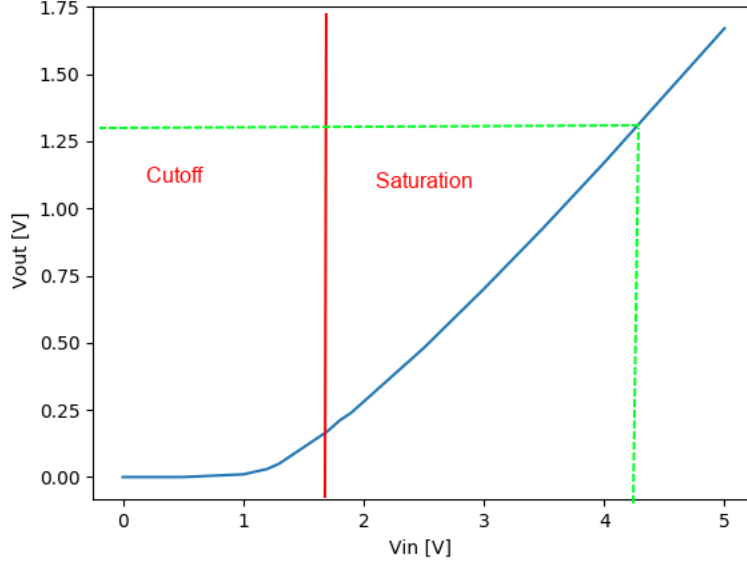


Figure 8: Common Drain Amplifier Voltage Transfer Characteristic

The amplifier should be biased in the middle of the saturation region. Using the characteristics of the NMOS determined earlier, the threshold voltage is taken to be  $V_T = 1.7V$ . Suppose the transistor exits the cutoff region for some  $V_{in} > V_T$ . Then, no current flows through the resistor. Therefore, the source voltage becomes 0V, meaning that  $V_{GS} = V_{in} > V_T$ . This is a contradiction. Thus, transistor cannot begin to exit cutoff at a voltage above  $V_T$ .

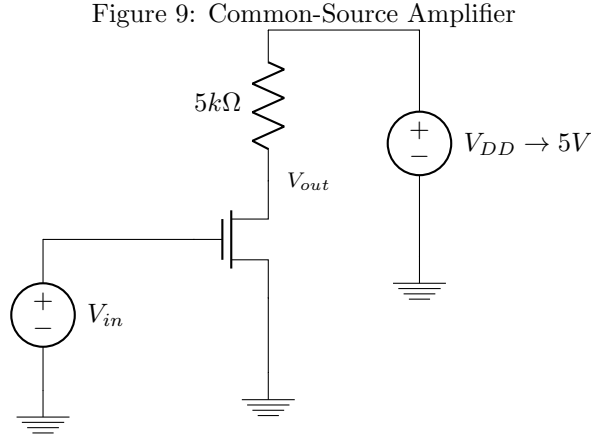
For a voltage  $V_{in} < V_T$ , assume the transistor is not in cutoff. Then, current flows through the resistor. Therefore, the source voltage is above ground, meaning that  $V_{GS} = V_{in} - V_S < V_T$ . This is a contradiction. So, the transistor



exits cutoff mode when  $V_{in} = V_T = 1.7V$ . The current begins to rise from 0mA before this point. However,  $V_T = 1.7V$  is used when calculating the edge between saturation and triode. For the sake of consistency,  $V_T = 1.7V$  is used for the edge between cutoff and saturation.

The transistor exits saturation when  $V_{in} = 5V + V_T = 5V + 1.7V = 6.7V$ . So, the midpoint of the saturation region occurs when  $V_{in} = \frac{1.7V + 6.7V}{2} = 4.2V$ , which corresponds to a bias current of  $\frac{V_{out}}{5k\Omega} \approx \frac{1.3V}{5k\Omega} = 0.26mA$ .

## 2.4 Common Source Amplifier



The common-source amplifier pictured above is then constructed.  $V_{in}$  is again swept from 0V to 5V. In the common-source arrangement, the NMOS transistor has the following condition for saturation:

$$V_{DS} > V_{GS} - V_T \rightarrow V_{out} = 5V - I_D R > V_{in} - V_T \rightarrow V_{in} < 5V - I_D R + V_T \quad (4)$$

In the common-source arrangement,  $V_{in}$  is equivalent to  $V_{GS}$ . So, when  $V_{in}$  is less than the threshold voltage, the transistor operates in the cutoff region and no current is passed through the transistor and consequently, the resistor. Because the transistor effectively acts as an open circuit,  $V_{out}$  is equivalent to  $V_{DD}$  for the entirety of the cutoff region. When  $V_{in}$  begins to overtake the threshold voltage, the transistor immediately operates in the saturation region. This is because small values of  $V_{GS}$  yield small  $I_D$  and thus, the condition in equation (4) is met. As  $V_{in}$  gets larger,  $I_D$  will also increase and  $V_{out}$  will decrease as a result. When  $V_{in}$  becomes sufficiently large,  $I_D$  will be large enough to violate the saturation condition and the transistor will then operate in triode mode. In triode region,  $V_{out}$  is expected to be very small because of the large  $I_D$ .

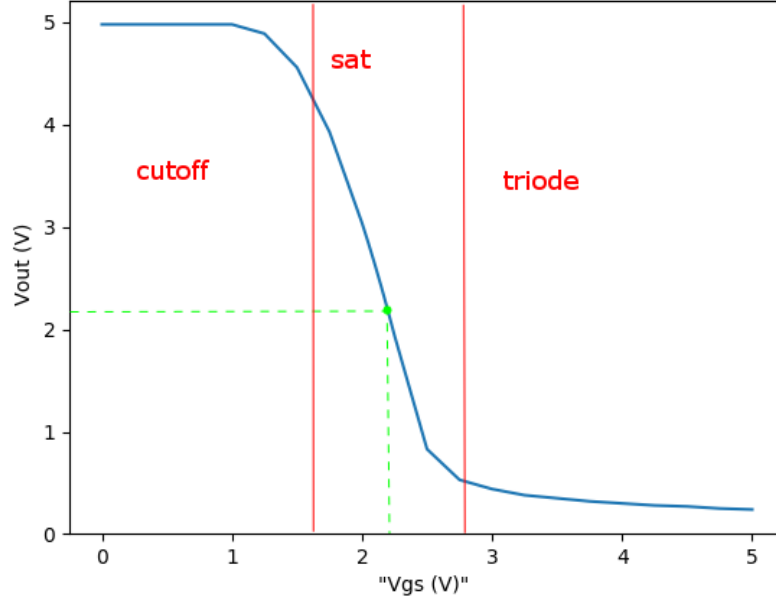


Figure 10: Common Source Amplifier Voltage Transfer Characteristic

The threshold voltage  $V_T$  is again taken to be 1.7V. So, the NMOS transistor operates in the cutoff region when  $V_{in} < 1.7V$  and  $V_{out} = 5V$  for the majority of this range. When  $V_{in} > 1.7V$ , the transistor enters saturation mode and  $V_O$  sharply decreases.

Then, the bias point occurs when the following condition is met:

$$V_{DS} = V_{DD} - I_D R \rightarrow V_{in} = 5V - I_D R = V_{out} \quad (5)$$

Following the condition above, the bias point occurs at  $V_{in} = V_{out} \approx 2.2V$  according to results shown in Figure (10). This voltage corresponds to the bias current  $I_D = \frac{V_{out}}{5k\Omega} \approx \frac{2.2V}{5k\Omega} = 0.44mA$ . The transistor enters triode mode when  $V_{in}$  exceeds  $5V - I_D R + V_T$ , which is beyond the bias point. With the assumption that the bias point occurs at the midpoint between the saturation and triode boundaries,  $V_{in}$  at triode region can be approximated to be  $2.2V + (2.2V - 1.7V) \approx 2.7V$ .

## 3 Conclusion

### 3.1 NMOS and PMOS

The resulting measurements from the NMOS transistor experiments agreed well with theory, and we were able to see how the transistor moved through all the modes of operation. The data clearly showed the transistor's cutoff voltage and threshold voltage. We noticed the effect of the NMOS's capacitance when moving from triode mode to cutoff. The accumulated charge was enough to keep the channel open so that the drain current was twice as large as when the accumulated charge was not present.

The PMOS transistor clearly displayed operation in cutoff and triode mode. We were able to observe a variable cutoff voltage, because the source voltage is not grounded. We noticed that we were able to change the cutoff voltage by varying the gate voltage.

### 3.2 Common Drain Amplifier

The common drain amplifier essentially follows the trend of the input voltage at the gate,  $V_{in}$ . It starts in the cutoff region since the input voltage is too low to form the channel. However, as the input is increased, the current flows, and an output voltage develops over the resistor. The voltage over the resistor is directly related to the current flowing through the transistor, which is directly related to voltage  $V_{in}$  applied at the gate. Since the output voltage is taken between the resistor and ground, the output voltage  $V_{out}$  is directly related to the input voltage  $V_{in}$ , which explains why they follow the same trend. It transitions from cutoff to saturation to triode, but does not reach triode in the range of voltages considered. The proper bias point occurs in the middle of the saturation region, for  $V_{in} \approx 4.2V$ , since the slope is steepest. Moreover, biasing the amplifier in the saturation region leads to high linearity in the output of the amplifier.

### 3.3 Common Source Amplifier

The common source amplifier exhibited the behavior of a logical inverter with low input voltage yielding high output voltage and high input voltage yielding low output voltage. At  $V_{in}$  lower than threshold, the transistor operates in cutoff, and  $V_{out}$  is therefore at its highest value. When  $V_{in}$  exceeds threshold, current begins to flow which causes a voltage drop across the resistor, thus decreasing  $V_{out}$ . The current continues to increase as  $V_{in}$  increases, resulting in larger voltage drops across the resistor which further decreases  $V_{out}$ . Eventually, the transistor hits triode mode and current levels off. The bias point, like the common drain amplifier, occurs in the middle of the saturation region and corresponds to the steepest slope in the curve.