Figure 1: Diode-Connected NMOS Circuit

Two operation modes are possible for the circuit in figure (1). In the first case, consider $V_{GS} < V_T$. At this point, the transistor is in cutoff mode, and no current flows. For the second case, $V_{GS} > V_T$. Since $V_G = V_D$ and $V_{GS} > V_{GS} - V_T$, $V_{DS} > V_{GS} - V_T$. This satisfies the condition for saturation. So, the transistor is either in cutoff or in saturation. So, the transistor's drain current is given by:

$$i_D = \begin{cases} \frac{k_n}{2}(V_{GS} - V_T)^2 & V_{GS} > V_T \\ 0 & V_{GS} < V_T \end{cases} \tag{1}$$

This current behavior mimics that of a pn-junction diode, but with a current that varies quadratically instead of exponentially with the applied voltage V_{GS}. The transistor, like a diode, requires a certain voltage in order to "turn-on", specifically V_T. Once this voltage is exceeded, the transistor is activated and immediately enters the saturation region. From this, increasing V_{GS} leads to quadratically larger drain currents, just like how increasing the applied voltage leads to exponentially growing diode currents.

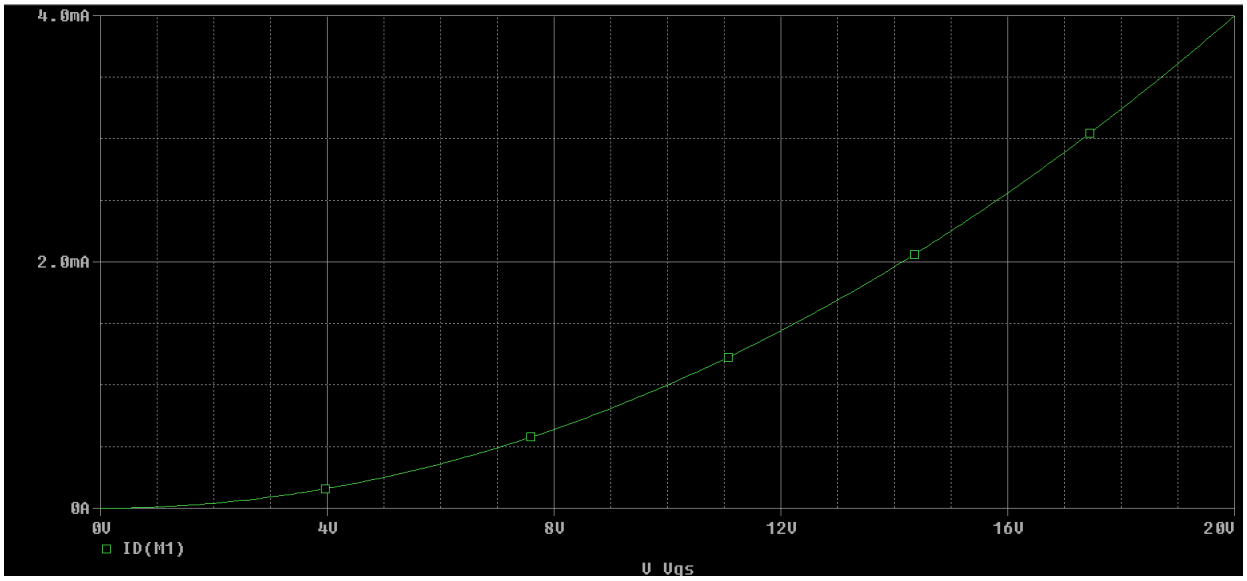

Figure 2: DC Sweep of Circuit in Figure (1)