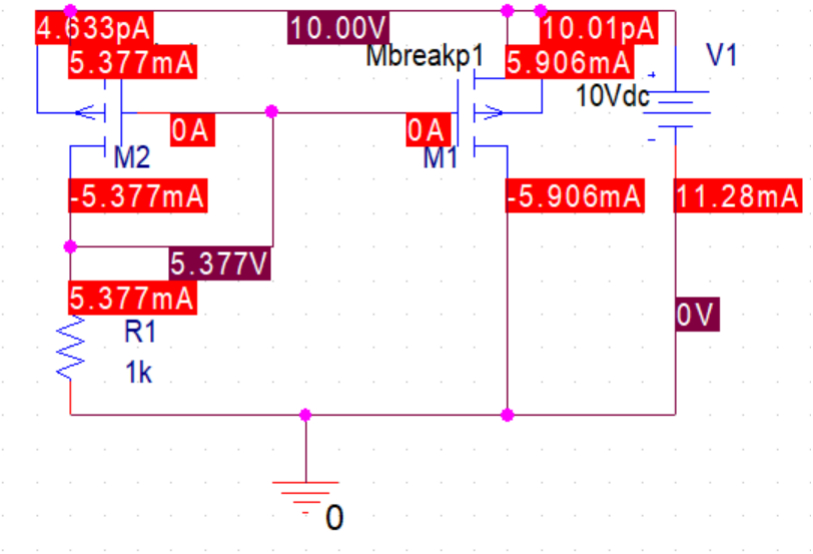

Figure 1: PMOS Current Mirror Bias Simulation

A current mirror takes an input current i_{in} and produces an output current i_{out} such that $i_{in} \approx i_{out}$. However, looking at figure (1), which current, whether it is the current through M_2 or M_1, is i_{in} or i_{out} is ambiguous. In order to determine which is truly the input current, a known current must be supplied through one transistor.

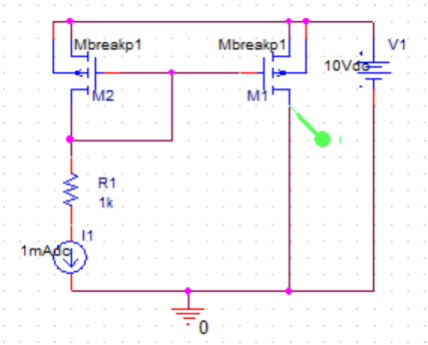

Figure 2: Known Current Supplied to M_2

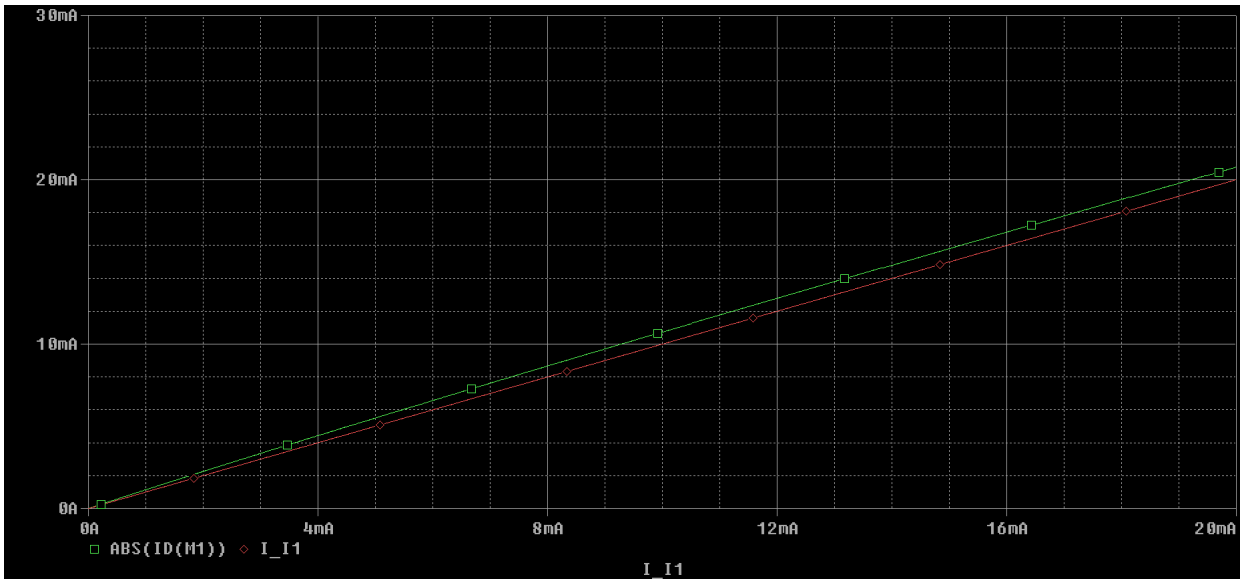

Figure 3: i_{M2} versus i_{M1}

The green line is i_{M1}, and the red line is i_{M2}. They are plotted against the known current i_{M2}.

Across a range of current, $i_{M1} \approx i_{M2}$ when i_{M2} is the known current. Suppose that i_{M1} is fixed instead.

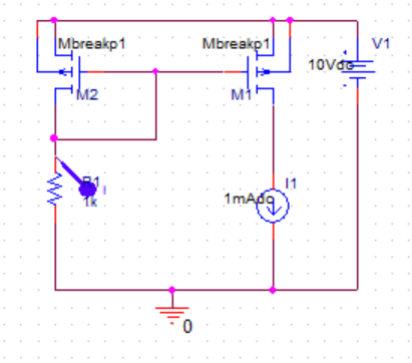

Figure 4: Known Current Supplied to M_1

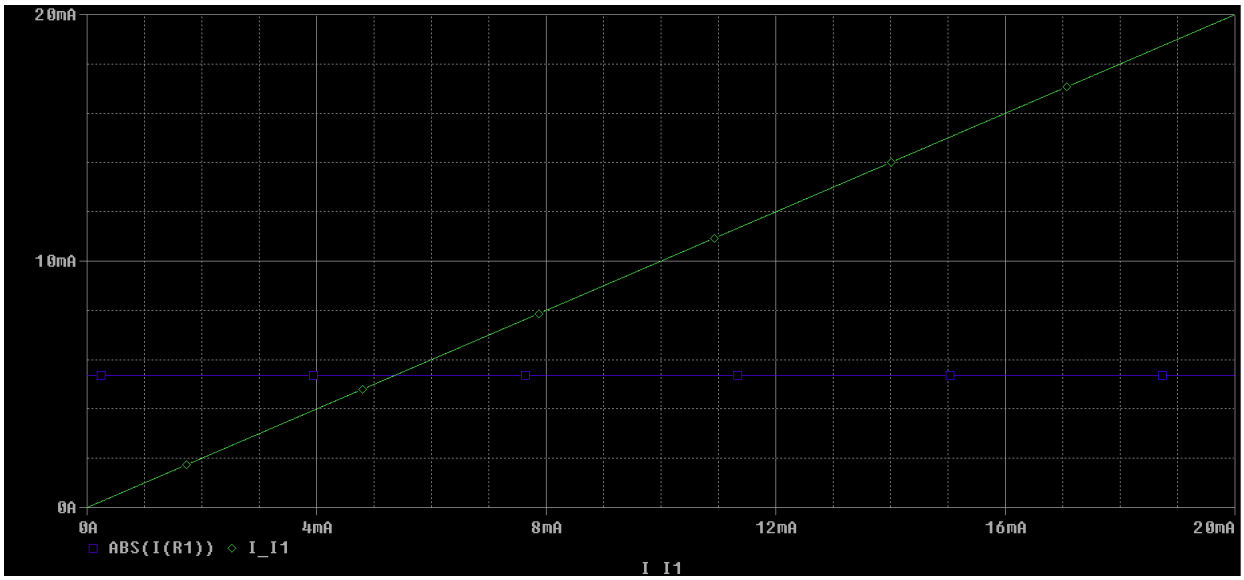

Figure 5: i_{M1} versus i_{M2}

The green line is i_{M1}, and the blue line is i_{M2}. They are plotted against the known current i_{M1}.

Here, i_{M2} remains constant, regardless of the value of i_{M1}. Therefore, setting the value of i_{M2} determines the value of i_{M1}, but setting the value of i_{M1} has no effect on the value of i_{M2}. So, the current through the transistor M_2 is the input current being mirrored (5.377mA), and the current through the transistor M_1 is the output current that mirrors i_{M2}.

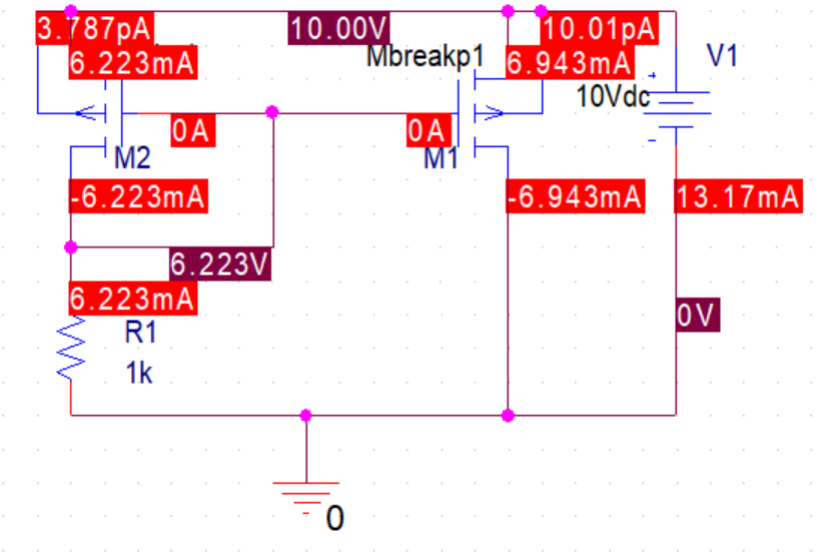

Figure 6: Doubling the Width of the MOSFETs

Suppose the width of each transistor, M_1 and M_2, is doubled. More current flows through each transistor. Widening transistors allows more charge to flow through a given channel in a fixed time interval. So, 6.223mA is the new current value being mirrored.

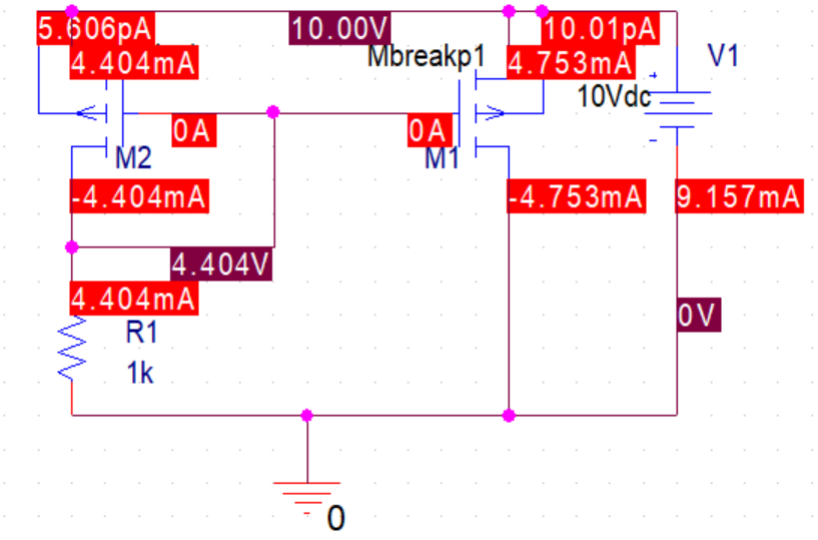

Figure 7: Halving the Width of the MOSFETs

If the width of each transistor is now halved, fewer charges are able to flow through a channel per unit time. So, less current flows through each transistor. 4.404mA is the new current value being mirrored.

Table (1) presents the mirrored current values at different $\frac{W}{L}$ ratios. Clearly, increasing $\frac{W}{L}$ for the transistors increases the mirrored current values because of the mechanics described above, namely that wider channels allow more charges to flow per unit time, leading to more current ceteris paribus.

Table 1: i_{in} at Various $\frac{W}{L}$ Values

Width-to-Length Ratio [unitless]	Mirrored Current [mA]
5	4.404
10	5.377
20	6.223