opcode	sel_pc	sel_dest	reg_rdv	reg_rds	sel_op	sel_ad	sel_int	opcode	sum_mem	sel_mem	sel_data	mem_wr	sel_wb	reg_wrv	reg_wrs	Instrucción
0000	0	0	0	0	0	0	0	0000	0	0	0	0	0	0	0	nop
0001	0	0	1	0	0	0	0	0001	0	0	0	0	1	1	0	sum_vec
0010	0	0	1	0	0	0	0	0010	0	0	0	0	1	1	0	res_vec
0011	0	1	1	0	0	0	0	0011	0	1	1	0	0	1	0	load_vec
0100	0	1	1	0	0	0	0	0100	0	1	1	1	0	0	0	store_vec
0101	0	0	1	1	0	0	1	0101	0	0	0	0	1	0	0	xor_sca
0110	0	0	1	1	1	0	1	0110	0	0	0	0	1	0	0	sl_sca
0111	0	0	1	1	1	0	1	0111	0	0	0	0	1	0	0	sr_sca
1000	0	0	1	1	1	0	1	1000	0	0	0	0	1	0	0	slc_sca
1001	0	0	1	1	1	0	1	1001	0	0	0	0	1	0	0	src_sca
1010	0	0	1	1	0	0	1	1010	0	0	0	0	1	0	0	sum_sca
1011	0	0	1	1	0	0	1	1011	0	0	0	0	1	0	0	res_sca
1100	0	1	0	0	0	0	0	1100	0	0	0	0	1	0	1	mov
1101	0	0	0	1	0	1	0	1101	0	0	0	0	1	1	0	vfs
1110	0	1	1	0	0	0	0	1110	0	0	1	0	0	1	0	lpc
1111	1	1	1	0	0	0	0	1111	1	0	1	1	0	0	0	spc
	Etapa_IF	**Etapa_ID**			**Etapa_EXE**				**Etapa_MEM**				**Etapa_WB**			

1 write