Jeff Bulick
Professor Haller
ECE 121
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BJT Amplifier CE » CC

Circuit Schematic

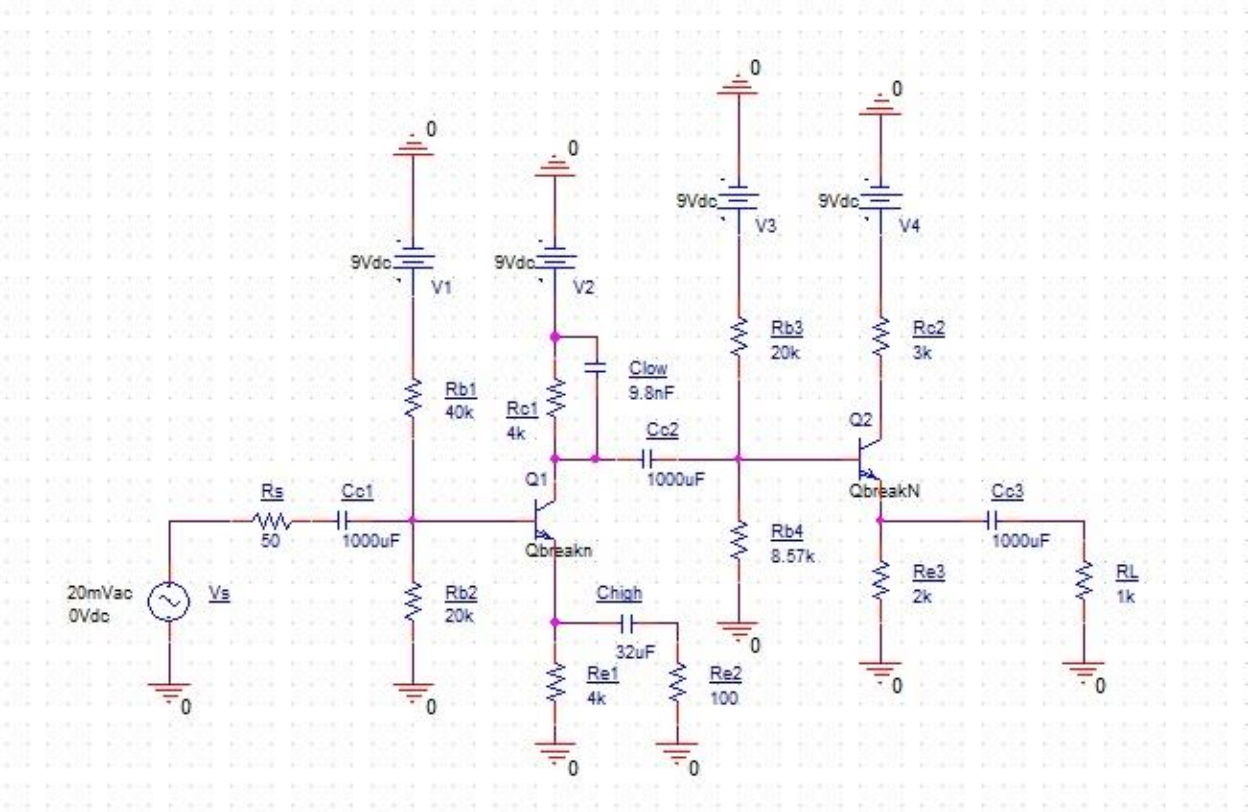

Figure 1

Design Operation:

1. 9V Battery Operation
2. Rin = 6.93k Ohms
3. Rout = 50 Ohms
4. Midband Voltage Gain = 15 V/V (23.5dB)
5. Upper 3dB frequency cutoff = 7kHz
6. Lower 3dB frequency cutoff = 50Hz
7. Bias stable for Beta ranging (50-200)

In order to meet design specifications for our BJT amplifier, we concatenated a self-biasing common emitter to a self-biasing common collector. The design specifications requested a mid-band voltage gain of at least 10V/V. This is where the common emitter comes into play. However, the output resistance of a common emitter is high so we concatenated a common collector to bring down the output resistance to meet spec of less than 500 Ohms. The coupling capacitors were chosen to be large in order to block the DC biasing from interfering with other parts of the circuit while allowing the AC signal to pass through and become amplified. Figure 1 is our final circuit schematic after making numerous changes to meet specifications.

Design Equations and Analysis

- Note: Please refer to Figure 1 for naming of variables used to derive equations

The design was first DC biased using the DC model to make sure that both transistors were operating in the active region. Each transistor was modeled separately because of the coupling capacitors creating an open circuit for the DC model. The equations used:

$$\beta I_b = I_c$$

$$I_e = \alpha I_c$$

$$(1+\beta) I_b = I_e$$

$$I_e = I_b + I_c$$

The self-biasing was achieved for Q1 using a Thevenin with 2 resistors in parallel. The same equations were applied for Q2 by changing the correlating variables. The equations for such are:

Thevenin voltage going into the base current: $V_{bb} = 9V * [R_{b2} / (R_{b1} + R_{b2})]$

Thevenin resistance: $R_{bb} = R_{b1} \parallel R_{b2}$

$V_{bb1} = 3V$, $R_{bb1} = 13{,}333$ Ohms

$V_{bb2} = 2.7V$, $R_{bb2} = 6k$ Ohms

After cancelling out Beta for the self-biasing design, $I_c = [V_{bb} – 0.7] / R_{e1}$

Once both transistors were operating in the active region, we worked with the BJT AC small signal models for the AC circuit to find the gain and Ri/Ro. The derived equations are:

Some parallel combinations: $R_{E1} = R_{e1} \parallel R_{e2}$, $R_{E2} = R_{e3} \parallel R_L$

$$r_\pi = \beta / g_m = \beta / (I_c/V_T)$$

$r_{\pi 1} = 4{,}655$ Ohms

$r_{\pi 2} = 2{,}697$ Ohms

$$Ri = Rin1 = Rb1 \parallel Rb2 \parallel [r_{\pi 1} + (1+ \beta_1) R_{E1}] = \mathbf{6.93k\ Ohms}$$

$$Rin2 = Rb3 \parallel Rb4 \parallel [r_{\pi 2} + (1+ \beta_2) R_{E2}] = 5.5k\ Ohms$$

$$\text{Voltage Gain: } Av = Vo/Vs = - [Rc1 \parallel Rin2] / R_{E1} = \mathbf{15V/V\ (23.5dB)}$$

$$Ro = Re3 \parallel \{ [(Rc1 \parallel Rb3 \parallel Rb4) + r_{\pi 2}] / (1+ \beta_2) \} = \mathbf{50\ Ohms}$$

$$Reout = (Rs + Rb1 \parallel Rb2 \parallel [r_{\pi 1} + (1+ \beta_1)Re1])$$

$$2\pi(\mathbf{50Hz}) = 1 / \{ [Reout \parallel Re2] * C_{high} \}$$

$$\mathbf{C_{high} = 32uF}$$

$$2\pi(\mathbf{7kHz}) = 1 / \{ [Rc1 \parallel Rin2] * C_{low} \}$$

$$\mathbf{C_{low} = 9.8nF}$$

Circuit Simulation

Bode Plot

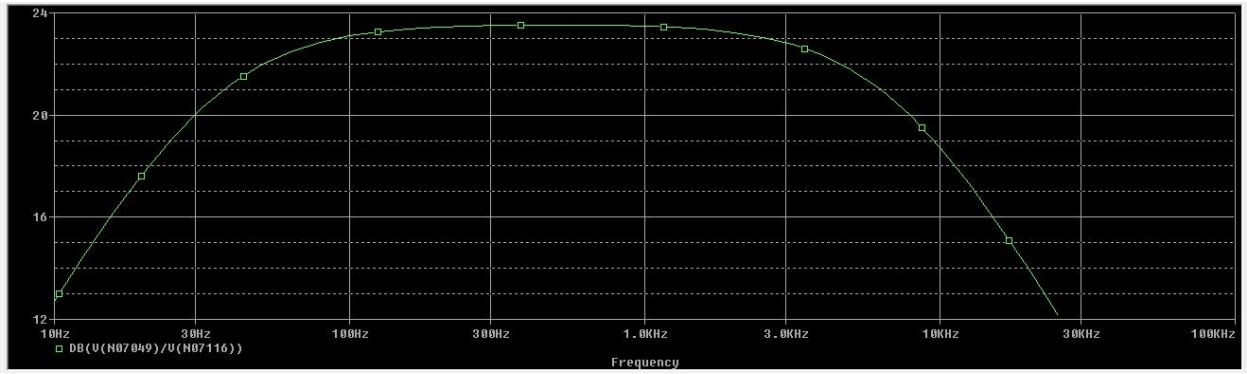

Figure 2

Phase Plot

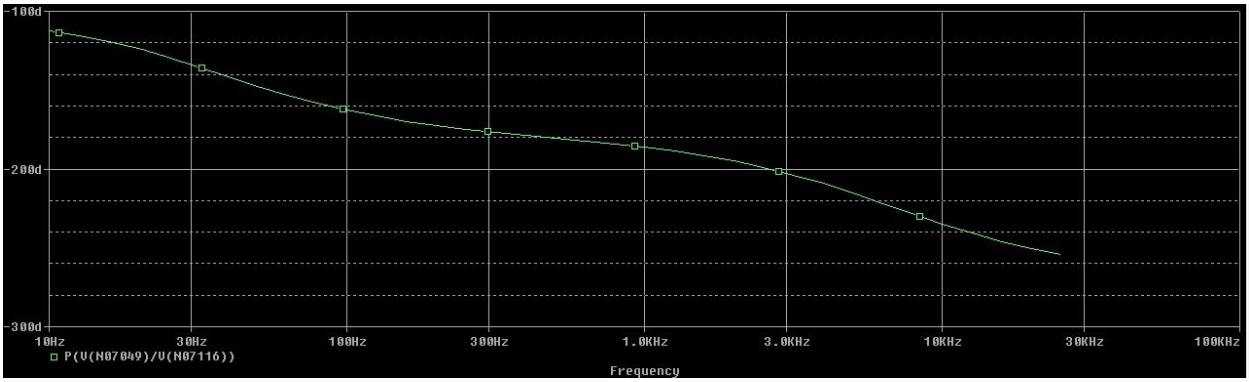

Figure 3

- β = 100

  Av = 23.5 dB
- β = 50

  Av = 23.0 dB
- β = 200

  Av = 23.8 dB

  After changing the properties of the transistor in the PSPICE model, we can conclude that the circuit is Bias stable for all variations of Beta because at most it had a 0.5dB difference.

  We can model the input and output resistance by simulating the AC voltage signal divided by the current in PSPICE.

Input Resistance

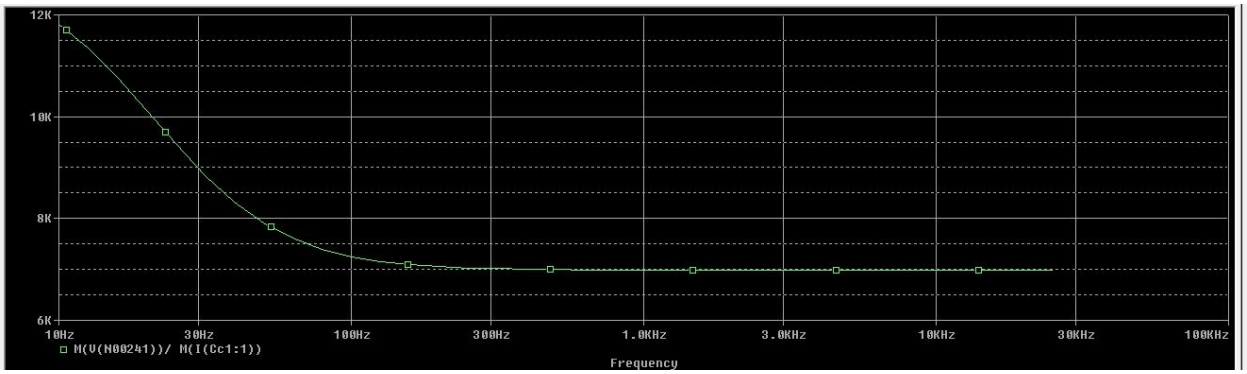

Figure 4

Output Resistance

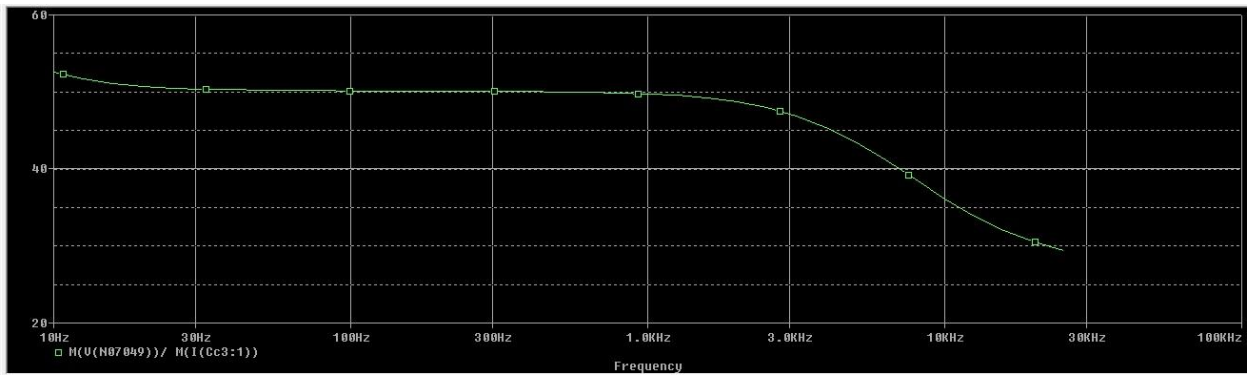

Figure 5

Experimental Results

In order to build the circuit, we were limited to a 50mV P-P AC signal source so we used a voltage divider to get the 20mV signal we require for our testing. The voltage divider used a 3.3k resistor in series with a 3.22k resistor in parallel with Rin of the circuit to get (0.4 * 50mV) = 20mV.

AC input signal

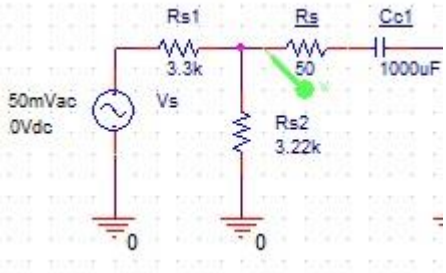

Figure 6

We used 1000uF capacitors for coupling because it was available in lab and will not affect frequency range our circuit is designed for. If the capacitance is too large it will start to distort the signal as the frequency increases. We then calculated the different break frequencies, and found the appropriate capacitors to use in order to achieve them. We then calculated the resistors needed for the correct gain and input/output resistances, and built our circuit on a breadboard. Finally, we tested our circuit in reality, and the results were fairly close to what we were expecting.

Frequency	Input Voltage		Output Voltage		Vo/Vs	Gain(DB)
50		20		120	6	15.56303
80		20		200	10	20
100		20		220	11	20.82785
200		20		270	13.5	22.60668
500		20		320	16	24.0824
1000		20		330	16.5	24.34968
2000		20		320	16	24.0824
5000		20		300	15	23.52183
10000		20		265	13.25	22.44432
20000		20		200	10	20
50000		20		130	6.5	16.25827
100000		20		80	4	12.0412

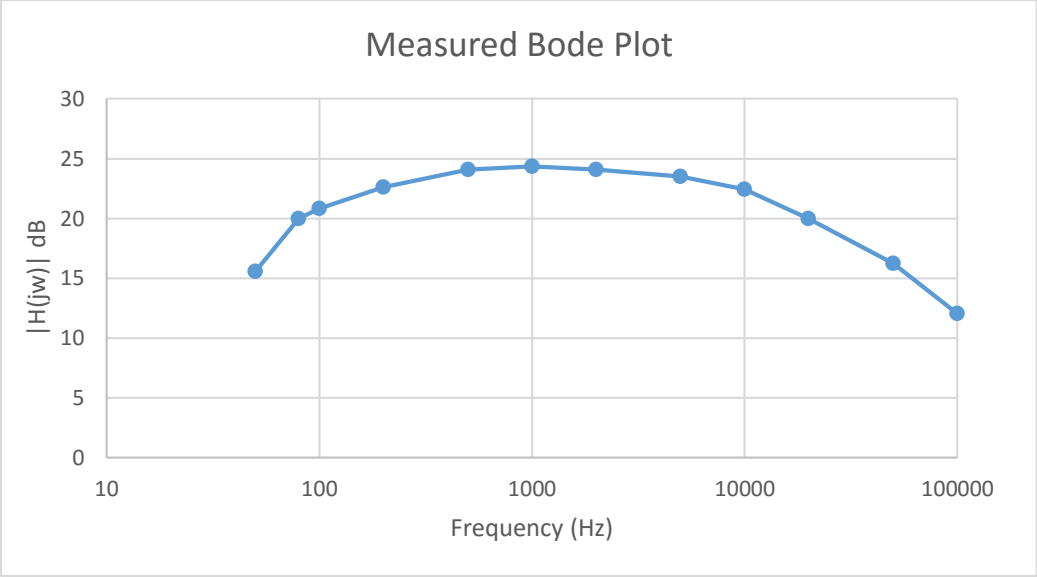

Figure 7

There were slight variations, probably due to a large variety of reasons such as theoretical resistances not being the same as actual ones, as well as capacitances. As you can see in the table below, all of our results were close and still worked within the constraints. Another possible reason for differences is variations in β because not all transistors have the same β, but this did not make a significant difference in reality or our PSPICE model.