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ECE 182 –Section Tuesday
Lab8 – Due November 22nd, 2016

Part 1 Analysis:

What is the conversion time of the ADC0804—that is, what does the data sheet say? What is the time you measured between when you tell it to start converting and it says "I'm done"?

> The conversion time of the ADC0804 given by the data sheet is 100uS. The time we measured for the conversion time is shown in figure 3, and was observed to be around 82uS.

What do the output waveforms of the ADC0804 look like? Describe in detail and provide examples.

> The ADC0804 has eight outputs, labeled D0 to D7, where D0 represent the least significant bit (LSB) and D7 represent the most significant bit (MSB). These eight outputs can be either 5V or 0V, representing digital high and digital low. Each output can be thought of as a bit in a 8 bit binary string, where a high pin is a 1 and a low pin is a 0. This means the ADC has 256 possible configurations of outputs. By mapping this output on a 0 to 5 volt scale, we can calculate an accurate approximation of the input analog voltage, within a certain resolution. When an input of 0V DC was given to the ADC, the output for all pins, D0 to D7 was low (0V). This corresponds with the binary string 00000000, which is 0V when converted and mapped on a 0 to 5 scale (Figure 7). When 2.73V was applied to the input, the output binary string was 10010010, which translates to the decimal number 148. When mapped from 0 to 5, this corresponds with a theoretical 2.87V input, which makes sense when you take into account the resolution and tolerance of the components (Figure 8). When 5V was applied to the input, all the output pins were high, representing the binary string 11111111, which is 5V when converted to decimal and mapped (Figure 9).

Referring to the bits below, discuss the values and weights of each bit. If a converter is known to produce an error 10% higher on one particular bit, which bit should the design engineer configure it to be? Which bit would be most foolish?

MSB _____ _____ _____ _____ _____ _____ LSB

> The bits below represent an 8 bit binary data series. The LSB represents zero or one in the decimal number system. Each following bit working towards the MSB is weighted times two the preceding bit. So the bit to the left of the LSB = 2*1 = 2. The MSB = 2^7 = 128. This byte can represent a total of 256 different combinations (2^7 + 2^6 + … + 2^0). The design engineer should direct the highest error towards the LSB. It would be

the most foolish to have the greatest amount of error on the MSB because the signal would be extremely distorted.

Describe the Nyquist rate and its applications to A/D converters

The Nyquist rate is twice the bandwidth that is the criterion necessary for a sampling rate enough for accurate mathematical representation of a signal. If this criterion is not met, than aliasing occurs which results in distortion of the original signal. Its application to A/D convertors ensures that there is the right amount of sampling to make the Fourier transform 0 for all frequencies greater than half of the sampling frequency.

Part 2 Analysis:

What is the conversion time of the DAC0808? How do you know?

The conversion time of the DAC0808 was measured to be 50uS. This can be found by looking at the difference of time between the input of the initial sine wave to the output of the DAC (132uS, Figure 15) and the conversion time of the ADC (82uS, Figure 3).

What does the output waveform of the DAC0808 look like? Describe in detail and provide examples.

The output of the DAC0808 is a staircase waveform that looks similar to the original sine wave input (Figure 14). The output looks very similar to a sample and hold circuit, however the DAC's input is a digital binary string where the S/H's input is an analog signal. The DAC has 8 inputs, labeled D0, the least significant bit, to D7, the most significant bit. These inputs construct the binary string, and have 256 possible combinations. The VRef+ and VRef- pins are used as the threshold to map this 0-255 digital input to some analog output. In this case, VRef+ was 5V and VRef- was 0V. The DAC takes samples of this digital input and then maps that input from VRef- to VRef+.

The DAC then produces that value as a DC voltage source until the DAC takes a new sample.

Suppose you are given the topology seen below (8 bit converters, with a range from 0-5V) and the system works great. What is the output?

After the A/D converter, the digital representation will be a constant 255 because it is greater than the highest threshold. This bit representation will be passed into the D/A converter and will be a constant DC voltage slightly under 5 volts due to the rails on the integrated circuits.

Now consider the same system knowing a bitter Lafayette student entered the lab and removed the 4th most significant bit (DB4) between the A/D and D/A converter. What should I now expect the final output to be?

Instead of the D/A reading 255 (11111111) it will now read 239 (11101111). This is mapped to the range 0-5V. (239/255)*5V = 4.67V. About **4.7V**DC will be the final output.

Discuss the frequency components before and after the low pass filter for the circuit of Figure 6. Reference screenshots if available

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The fundamental frequency is 1kHz because of the input sine wave. The output of the D/A converter is similar to our staircase waveform. A perfect sine wave only has energy at its fundamental frequency. Square waves and other modulated signals introduce error and energies at harmonic frequencies. The low pass filter is implemented with a break frequency close to after the fundamental frequency to attenuate these harmonics to eliminate distortion. We use a fourth order filter to attenuate at a faster rate and thus produces a clearer representation of the original input signal.

Part 3 and 4 Analysis:

In less than a page (double spaced, Times New Roman 12 pt. font and 1" margins max) describe the signal progression of part 4. Describe the waveforms before and after each component in the flow chart and how each component modulates the signal. Make sure you remember the original input and final output!

The analog input signal is a 5Vpp 1kHz sine wave. This is passed into a sample and hold circuit. The S/H circuit creates a staircase waveform and is used in combination with the decoder to hold the signal long enough to be digitized by the ADC. The ADC also takes in an inverse pulse signal to act as a fully differential ADC to aid in noise reduction. The SH logic input controls the sampling frequency to meet the nyquist criterion. The ADC has 8 outputs that each represent a bit in a binary string. These values correspond to 256 possible combinations. These eight outputs are either 0V or 5V, where 0V represents a 0 in the binary string and 5V represents a 1. The DAC has eight inputs, again labeled from D0 to D7, which again represents a binary string. This binary string value is then mapped by the DAC into voltage values within the range of the DAC's VRef+ and VRef- pins. The DAC output is the staircase waveform. The DAC produces DC voltages equal to the mapped input values until a new sample is read. The distortion is eliminated by passing this signal into our fourth order low pass reconstruction filter that can be seen in figure 16. The theoretical bode plot of this filter is given in figure 17. This filter eliminates harmonic frequencies while retaining the same fundamental frequency in order to produce the best representation of our original 5Vpp 1kHz sine wave analog input. Examining our final output (refer to figure 18) yields a signal that is close to our original signal that we are pleased with. The fundamental frequency is identical. However, we lost some amplitude that can be due to the rails of our IC's and component tolerances producing slightly inaccurate results.

Appendix

Part 1

Output Pulse Train 4022

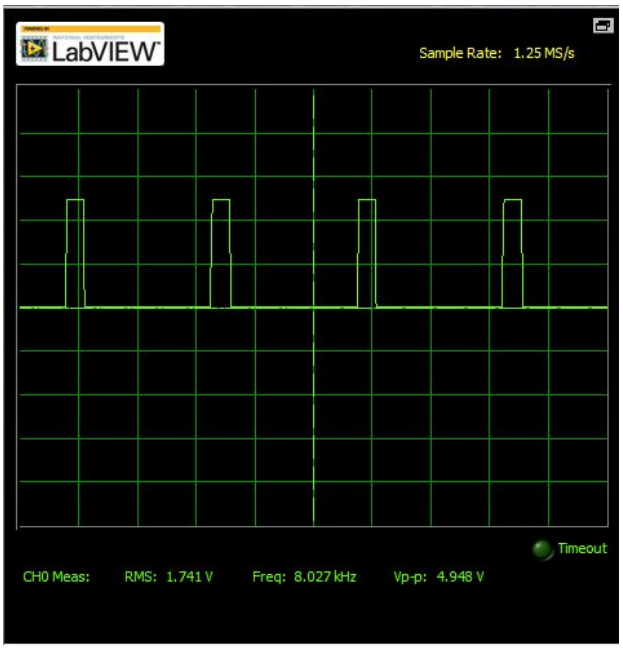

Figure 1

Staircase Waveform Output of SH Circuit LF398

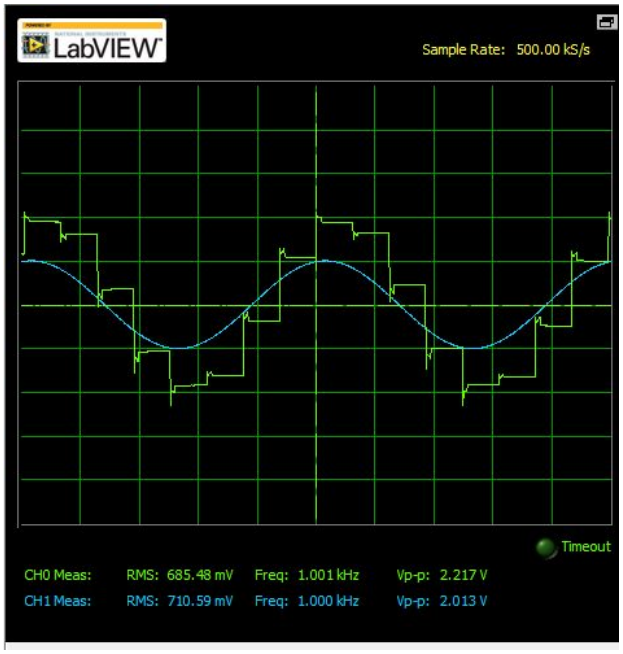

Figure 2

Part 2

Conversion Time ADC0804

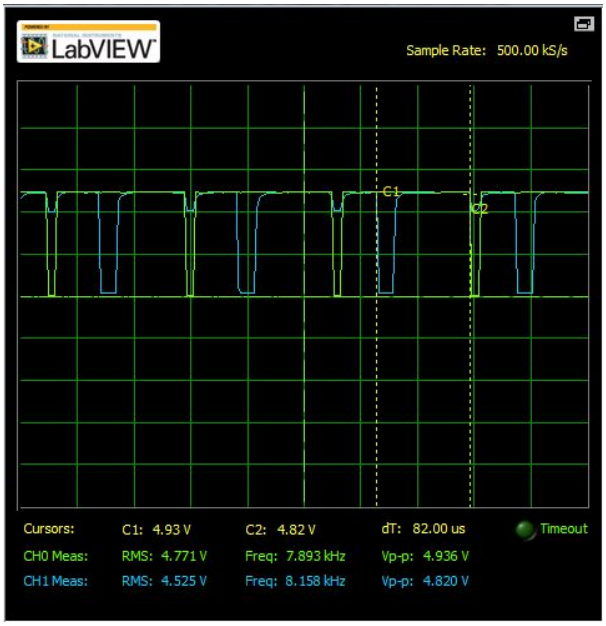

Figure 3

Pin3 Versus Pin5 ADC0804

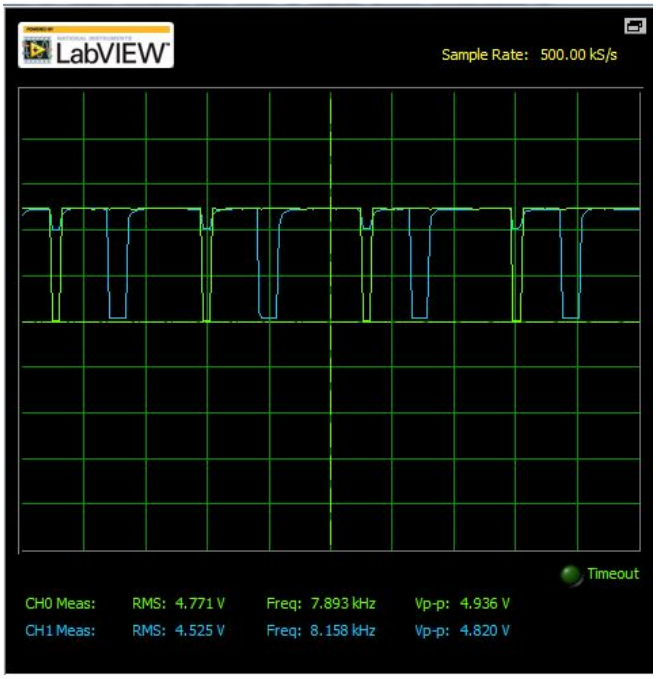

Figure 4

Analog Input A/D Converter SH Input vs MSB Output

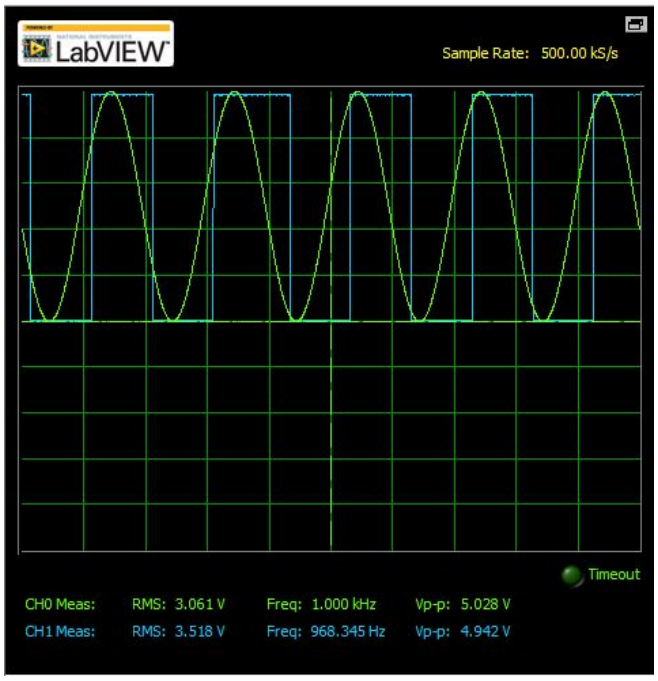

Figure 5

Analog Input A/D Converter SH Input vs LSB Output

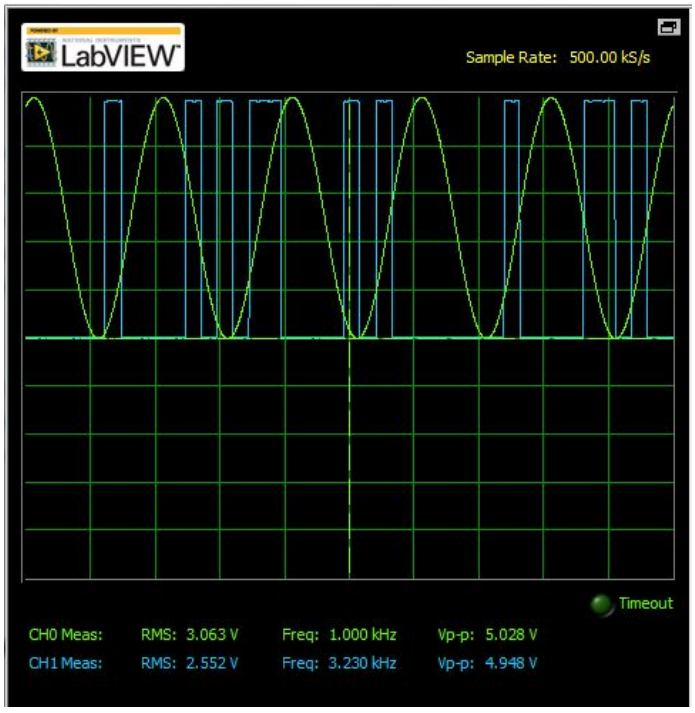

Figure 6

0V Variable DC A/D Converter

Figure 7

2.73V Variable DC A/D Converter

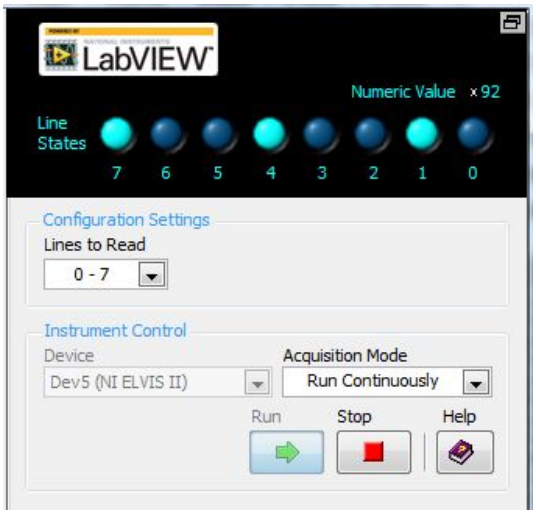

Figure 8

5V Variable DC A/D Converter

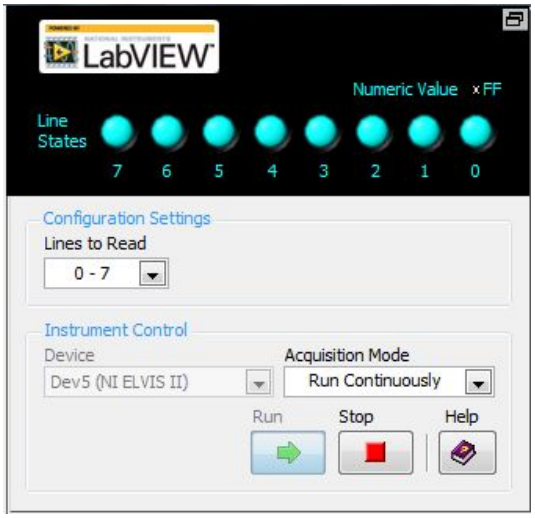

Figure 9

Part 3

D/A All Bits Low

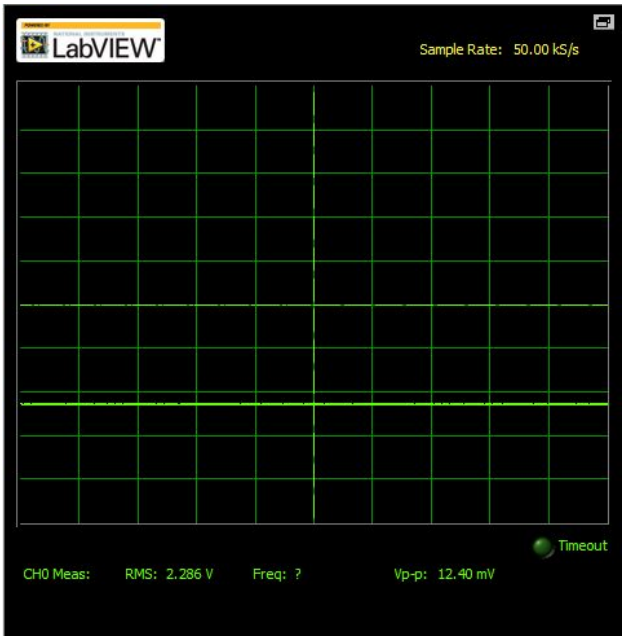

Figure 10

D/A All Bits High

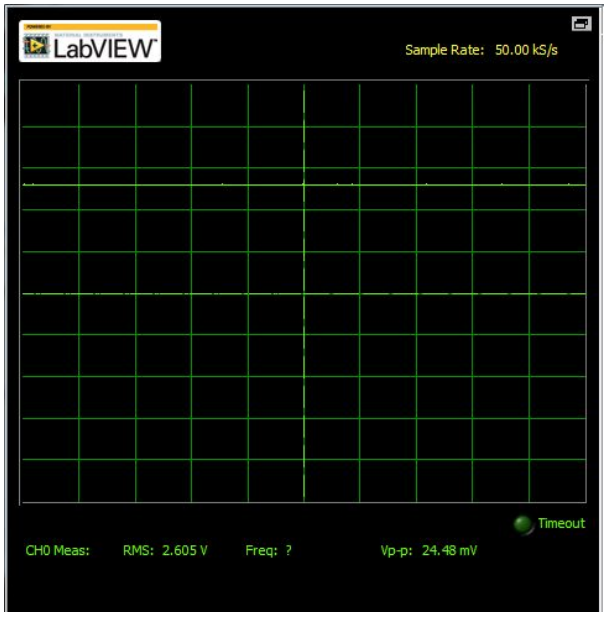

Figure 11

D/A All Bits Low, LSB High

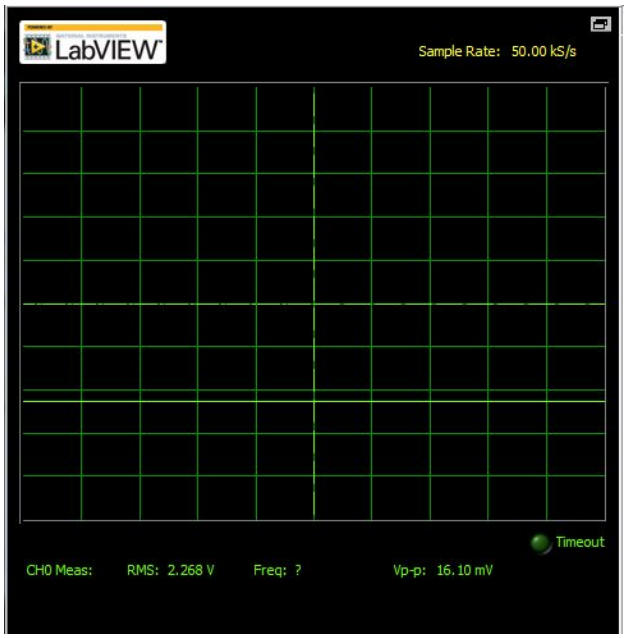

Figure 12

D/A All Bits Low, MSB High

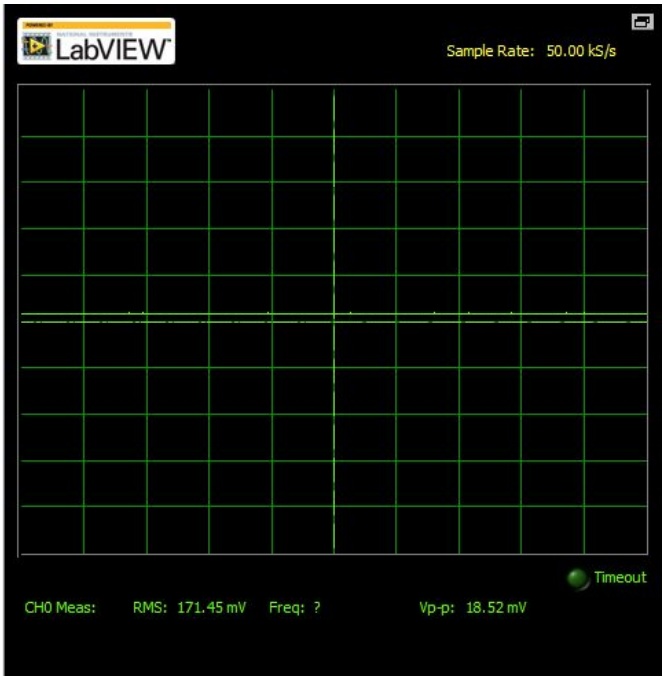

Figure 13

Part 4

D/A Before Reconstruction Circuit

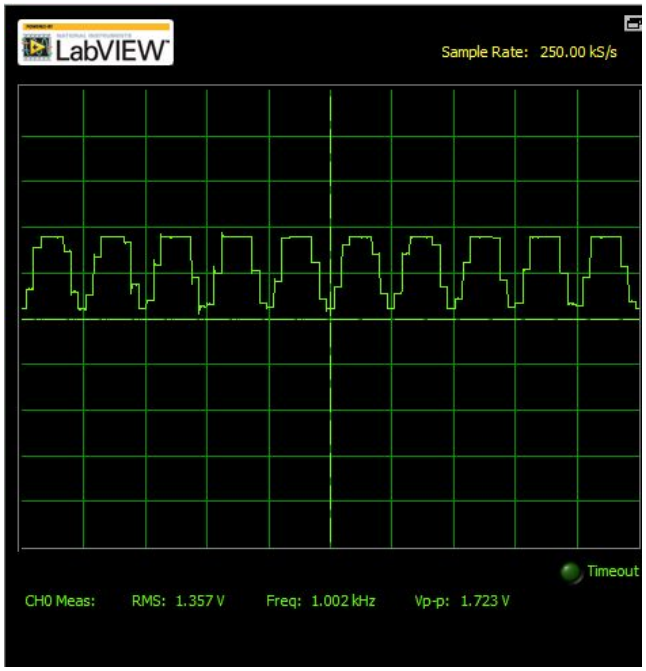

Figure 14

Time From Input Sine to Output DAC

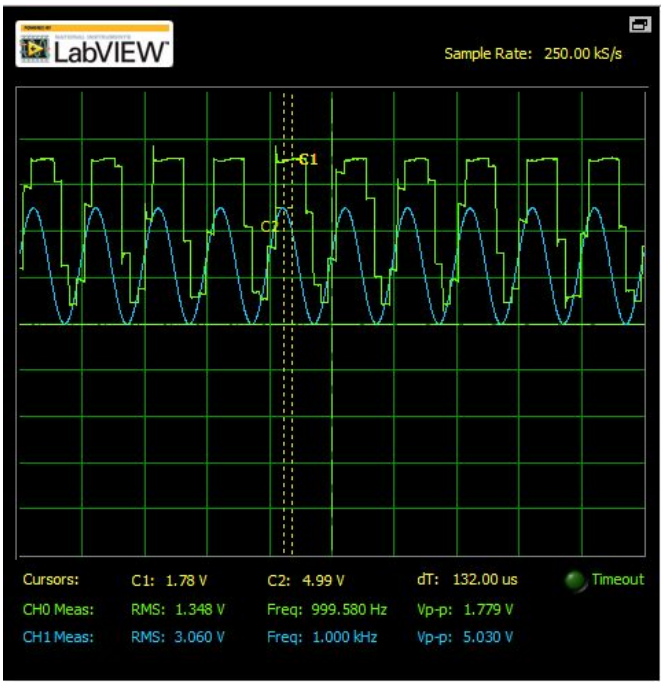

Figure 15

4th Order Reconstruction Filter Design: Extra Credit

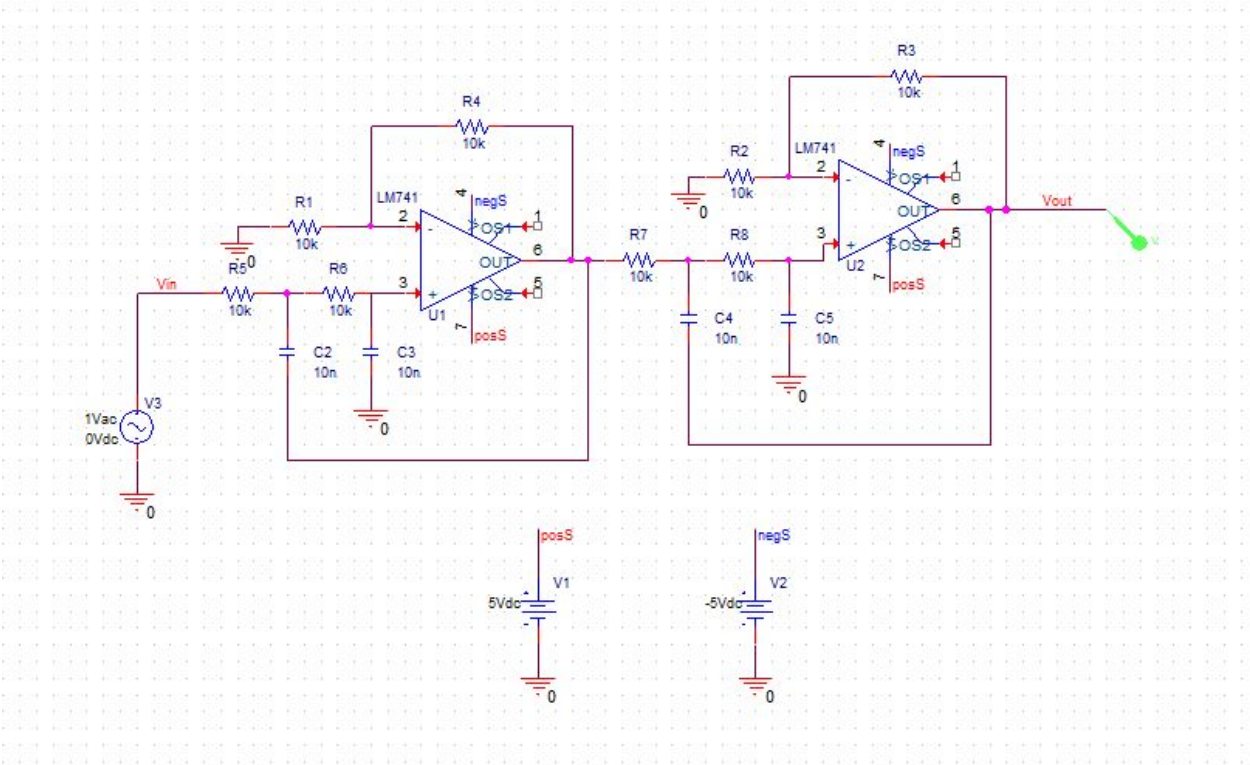

Figure 16

Reconstruction Filter Spectrum

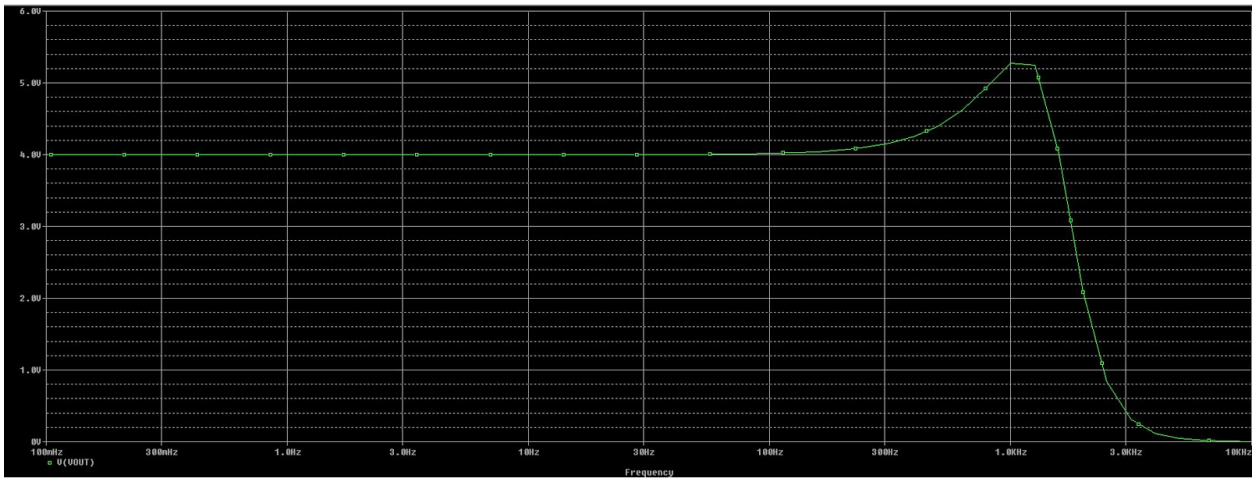

Figure 17

Final Reconstructed Signal

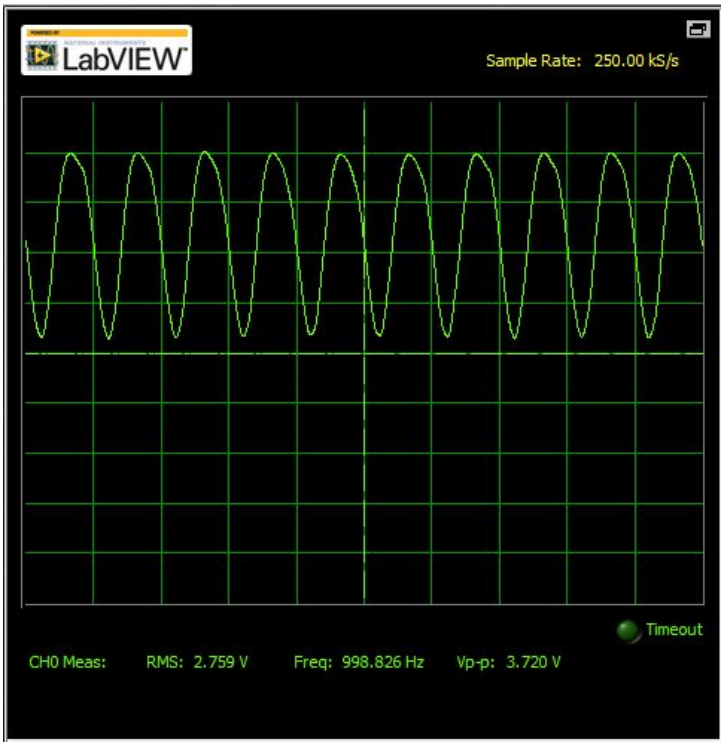

Figure 18