M21024/M21036/M21048

12.5 Gbps Crosspoint Switch Family

Rev V2

Features

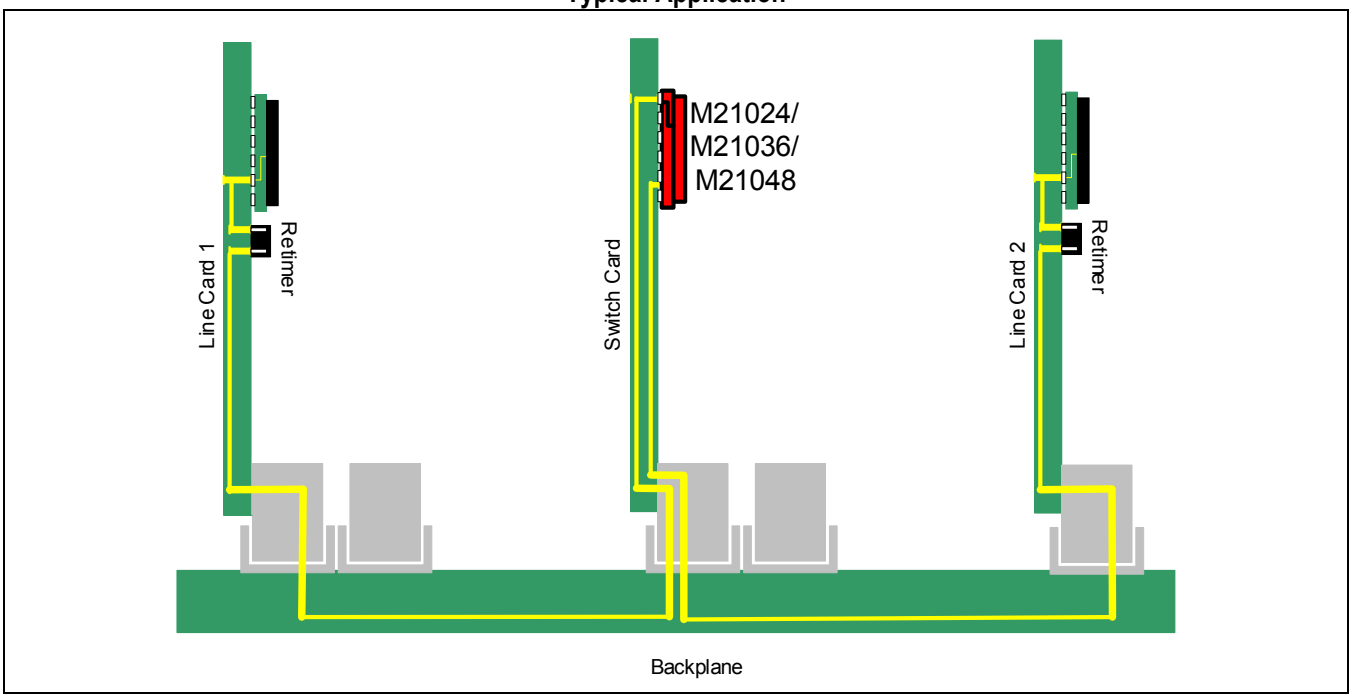
- 24x24 / 36x36 / 48x48 Non-Blocking Crosspoint Switch
- Support any data rates From 100 Mbps to 12.5 Gbps
- Enables channels up to 40" at 12.5 Gbps
- Global or Individual Programmable Input Equalization to compensate up to 24dB of loss at 5.16GHz and 20dB of loss at 6.25GHz
- Global or Individual Programmable Output De-Emphasis up to 10.5 dB
- Integrated Pattern Generator and Checker
- Individual lane LOS (Loss Of Signal) detection and squelch
- Support Out-Of-Band (OOB) signaling

Applications

- Reconfigurable Optical Add-Drop Multiplexor (ROADM) Switch
- Enterprise Circuit Switch
- Multi-rate Line Card Switch
- Serial Digital Video (SDI) Switchers/Routers
- Wireless base-stations
- Redundancy or Protection Switching
- UHDTV/4K Video

The M21024/M21036/M21048 family of devices is made up of fully non-blocking asynchronous crosspoint switches that operate at all data rates from 100 Mbps to 12.5 Gbps. The three products provide superior signal integrity management capabilities through the switch core and at the IO. Each device receiver is equipped with an analog equalizer that is programmable and designed to equalize up to 24 dB of insertion loss at 5.16 GHz for 10GbE applications and up to 20 dB of insertion loss at up to 6.25 GHz for 12.5Gb/s applications. The M21024/ M21036/M21048 switch core is equipped with a sophisticated servo that automatically manages the DC offset in each channel in order to minimize jitter caused by duty cycle distortion. The output stages of the device are equipped with individually programmable drivers that operate with up to 10.5 dB of de-emphasis as well as a wide range of output voltage swing levels. Additionally, the products are equipped with features to assist with channel bring-up and performance monitoring. These features can also be used to configure each input equalizer for fully optimized performance. The M21024/M21036/M21048 can be control with 2-wire (I2C compatible), 4-wire (SPI) or 8-bit parallel bus interfaces for maximum flexibility. It is also possible for the device to automatically load a configuration from an external EEPROM.

Typical Application



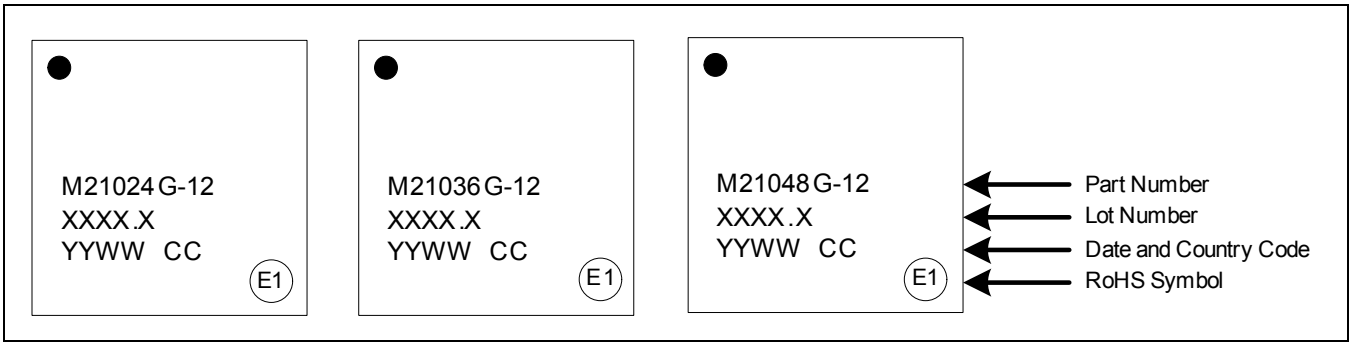
Ordering Information

Part Number	Package	Operating Case Temperature
M21024G-12*	21x21 BGA	-40 °C to +85 °C
M21036G-12*	23x23 BGA	-40 °C to +85 °C
M21048G-12*	27x27 BGA	-40 °C to +85 °C

Revision History

Revision	Level	Date	Description
V2	Release	October 2014	Clarify loss channel support
V1	Release	June 2014	Change data rate support to 12.5 Gbps
H	Release	March 2014	Added input equalizations to features in Front page, Added note 2,3 power consumption specifications in Table 1-3. Added note xINPUTEN, xOUTPUTEN pin description Table 3-1, Table 3-2, Table 3-3. Added note power sequence Section 4.2.2. Added note LOS of Signal Alarm Section 4.4.2. Added note Auxiliary input lane Section 4.4.4. Revised Section 4.5.2 , Output De-emphasis Figure 4-12.
G	Release	October 2013	Updated maximum data rate to 11.88Gbps to support UHDTV, Table 1-4. Added description in Section 4.8.1.
F	Release	June 2012	Updated electrical specifications in Table 1-2, Table 1-3 and Table 1-4. Updated description for the high-speed PRBS generator and checker, Section 4.8. Removed eye monitor information. Added Section 4.4.2.1 and Section 4.4.2.2. Removed Eye Monitor registers in Section 5.0.
E	Advance	January 2012	Corrected pin count in Section 3.3 and Section 3.6. Added packaging description in Section 3.9. Corrrected AT24C048B address mapping table from '60h to 7Fh' to '60h to 8Fh' in Table 4-8.
D	Advance	October 2011	Revised Figure 3-3, updated pin descriptions for the M21036. Revised Table 3-2, updated pin descriptions for the M21036. Revised Figure 3-4, M21036 packaging drawing. The new package does not include the four corner balls.
C	Advance	September 2011	Updated ESD specifications, Table 1-1. Updated Propagation delay and intra-group skew, Table 1-4. Updated Pin descriptions for the M21048 to add groups, Section 3.2. Updated Pin descriptions for the M21024 to add groups, Section 3.8.
B	Advance	June 2011	Refer to revision B of the data sheet.
A	Advance	January 2011	Initial release.

M21024/M21036/M21048 Marking Diagrams



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1.0 Electrical Characteristics

Unless otherwise noted, specifications in this section are valid with DV_{DDO} = 3.3 V, AV_{DDO} = 1.8 V, AV_{DD} = 1.2 V power supplies, 25 °C ambient temperature, 800 mV_{PPD} differential input data swing, default output data swing, PRBS 2^{15}-1 test pattern at 12.5 Gbps, R_{LOAD} = 50 Ω.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Note	Minimum	Maximum	Unit
DV_{DDO}	Digital Output Supply Voltage	1, 3	-0.5	3.6	V
AV_{DDO}	Analog Output Supply Voltage	1, 3	-0.5	2.1	V
AV_{DD}	Analog Core Supply Voltage	1, 3	-0.5	1.5	V
V_{IN}	DC Input Voltage (PCML)	1, 3	V_{SS} – 0.5	AV_{DD} + 0.5	V
$V_{IN, CMOS}$	DC Input Voltage (CMOS)	1, 3	V_{SS} – 0.5	DV_{DDO} + 0.5	V
T_{STORE}	Storage Temperature	1, 3	–65	150	°C
T_{JUNC}	Junction Temperature	1, 3	—	125	°C
$V_{ESD, HBM}$	Electrostatic Discharge Voltage (HBM)	1,2,3	-2000	+2000	V
$V_{ESD, CDM}$	Electrostatic Discharge Voltage (CDM)	1,2,3	-500	+500	V

NOTES:

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage. Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.
2. HBM and CDM per JEDEC Class 2 (JESD22-A114-B).

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DV_{DDO}	Digital Output Supply Voltage	—	1.14	1.2/1.8/2.5/3.3	3.47	V
AV_{DDO}	Analog Output Supply Voltage	—	1.14	1.2/1.8	1.89	V
AV_{DD}	Analog Core Supply Voltage	—	1.14	1.2	1.26	V
T_{CASE}	Case Temperature Range	—	-40	—	85	°C
θ_{JC}	Junction to Case Thermal Resistance	1, 2	—	1	—	°C/W

NOTES:

1. Thermal and heat sink recommendations. Consult your local applications resource.
2. Without heat sink and without airflow.

Table 1-3. Power Consumption Specifications

Symbol	Parameter		Note	Typical	Maximum	Unit
DI_{DDIO}	Digital IO Current Consumption, Maximum peak current using the Parallel interface in Read mode	DV_{DDO} = 3.3 V		18	300	mA
AI_{DDO}	AV_{DDO} Current Consumption per Output Buffer, AC coupled	600 mV_{PPD} Output Swing	2	13	16	mA
		800 mV_{PPD} Output Swing	2	17	21	mA
		1200 mV_{PPD} Output Swing	3	25	31	mA
AI_{DD}	AV_{DD} Current Consumption Switch set to one-to-one configuration	M21048		6	7.8	A
		M21036		4.4	5.9	A
		M21024		3.1	3.9	A
P_{TOTAL}	Total Power Consumption Switch set to one-to-one configuration. All inputs and outputs ON. AV_{DD} = AV_{DDO} = 1.2 V. DV_{DDO} = 3.3 V. 800 mV_{PPD} output swing	M21048		8	11	W
		M21036		5.7	7.9	W
		M21024		4	5.5	W
$P_{TOTAL,STDY}$	Total Power Consumption, Standby mode	M21048/36/24	1	15	—	mW

NOTES:

1. Switch set standby mode. AV_{DD} = AV_{DDO} = 1.2 V
2. For this table AVDDO =1.2V, for 600 and 800mVpp and AVDDO=1.8V for 1200mVppd. 1.8V supports all 3 swing levels (600, 800 and 1200)
3. AV_{DDO} = 1.8 V is required for output swing 1200mVppd, outputs must be AC coupled during normal operation.

Table 1-4. PCML Input/Output Electrical Characteristics (1 of 2)

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DR	NRZ input data rate	1	0.1	—	12.5	Gbps
V_{IN}	Input Range	2,3	250	—	1500	mV_{PPD}
V_{IN_SDI}	Input Range (SDI) V_{IN}	2,4,5	400	—	1500	mV_{PPD}
Vcm_in	Common mode range when inputs are DC coupled V_{ICM}		0.7	—	0.9	V
V_{OUT}	Swing Level 1: Differential swing (p-p)		800	1200	1300	mV_{PPD}
	Swing Level 2: Differential swing (p-p)		500	750	950	mV_{PPD}
	Swing Level 3: Differential swing (p-p)		400	550	700	mV_{PPD}
R_{IN}	Differential Input Termination Resistance	—	80	100	120	Ω
t_{PD}	Propagation Delay (any input to any output)	7	0.25	—	1.0	ns
$t_{SKEW, PN}$	Skew within defined groups of four lanes	7	—	—	100	ps
t_R/t_F	Output Rise/Fall Time (20%-80%)	6,7,8	—	35	50	ps
DCD_{DATA}	Output Duty Cycle Distortion	10	—	20	30	mUI

Table 1-4. PCML Input/Output Electrical Characteristics (2 of 2)

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
t_{DJ}	Output Deterministic Jitter with backplane at 12.5Gbs (20 dB insertion loss at 6.25 GHz)	8,9,12	—	160	315	mUI
	Output Deterministic Jitter point-blank at 12.5Gbs (0 dB insertion loss)	8.9.11	—	60	225	mUI
t_{RJ}	Output Random Jitter RMS with backplane at 12.5GBs (20 dB insertion loss at 6.25 GHz)	8,9,12	—	95	190	mUIpp
	Output Random Jitter RMS point-blank at 12.5Gbs (0 dB insertion loss)	8,9,11	—	11	15	mUI_{RMS}

NOTES:

1. Minimum data rate may be limited by AC coupling capacitor.
2. Inputs should be AC coupled during normal operation. DC coupling is possible.
3. Value specified at the device pins.
4. Measured with 3G-SDI pathological pattern and 40 inches of FR4 trace.
5. Select digital Offset correction loops for video pathological applications.
6. 1.8 V AV_{DDO} is required for output swings greater than 800 mV_{PPD}. Outputs must be AC coupled during normal operation.
7. Value specified using pattern with minimum pulse width of Consecutive Identical Digit (CID) ≥ 10 at 11.88 Gbps data rate; 800 mV_{PPD} DUT input swing.
8. Value specified with load as follows: MACOM M21048/36/24 Evaluation Module (EVM) with 3 ft. coaxial cables into oscilloscope (800 mV_{PPD} DUT output swing).
9. Value as reported by oscilloscope; test system jitter not included.
10. Absolute value specified using 101010 clock-like pattern. Offset correction loops enabled.
11. Value specified at 12.5 Gbps using PRBS 2^15-1 pattern with generator as follows: MACOM M21048/36/24 Evaluation Module with 3 ft. coaxial cables (800 mV_{PPD} DUT input swing. Input equalizer register = 00h).
12. Value specified at 12.5 Gbps using PRBS 2^15-1 pattern with generator as follows: MACOM M21048/36/24 Evaluation Module with -20 dB Insertion Loss at 6.25 GHz (800 mV_{PPD} DUT input swing. Input equalizer register = 1Bh).

Table 1-5. Control/Interface Logic Input/Output Characteristics

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{OH}	Digital Output Logic High	1	0.75 x DV_{DDO}	DV_{DDO}	—	V
V_{OL}	Digital Output Logic Low	2	—	0	0.25 x DV_{DDO}	V
V_{IH}	Digital Input Logic High	1	0.75 x DV_{DDO}	—	DV_{DDO}	V
V_{IL}	Digital Input Logic Low	1	0	—	0.25 x DV_{DDO}	V

NOTES:

1. I_{OH} = -3 mA for DV_{DDO} = 1.2 V. -4 mA for DV_{DDO} >= 1.8 V.
2. I_{OL} = 3 mA for DV_{DDO} = 1.2 V. 4 mA for DV_{DDO} >= 1.8 V.

2.0 Typical Performance Characteristics

Unless otherwise noted, typical performance applies for DV_{DDO} = 3.3 V, AV_{DDO} = 1.2 V, AV_{DD} = 1.2 V, 25 °C ambient temperature, 800 mV_{PPD} differential input/output data swing, PRBS 2^{15} – 1 data pattern at 12.5 Gbps, R_{LOAD} = 50 Ω.

Figure 2-1. Eye Diagram Output @6.25 Gbps , After 30 inches of Backplane (24 dB Insertion Loss at 3.125GHz)

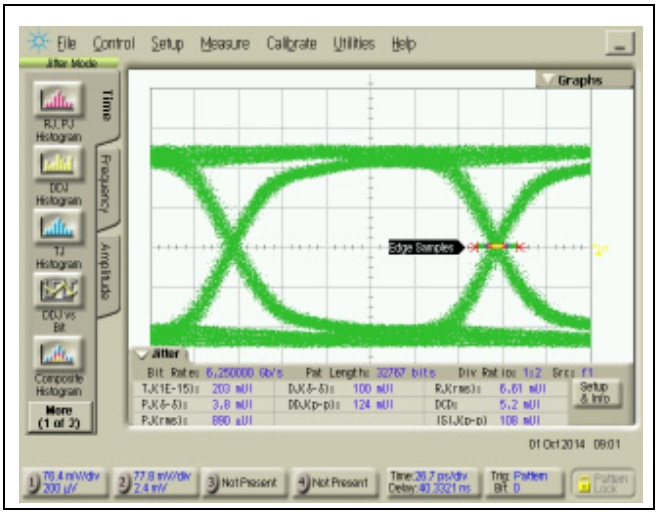


Figure 2-2. Eye Diagram Output@8 Gbps, After 30 inches of Backplane (15.8dB Insertion Loss 4GHz)

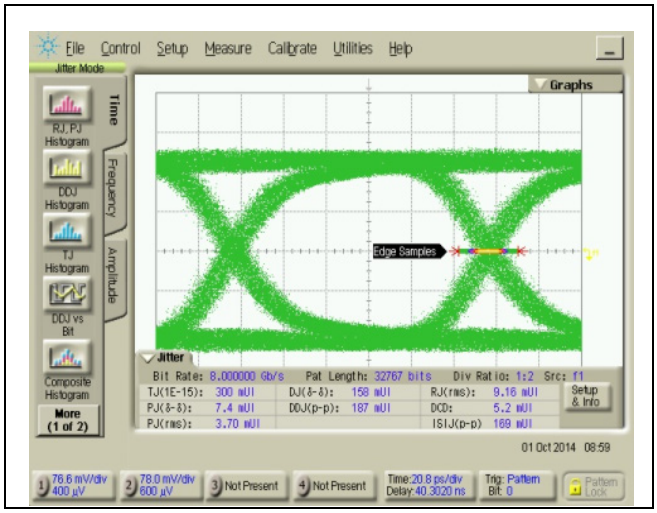


Figure 2-3. Eye Diagram Output @9.9 Gbps, After 30 inches of Backplane (17dB Insertion Loss at 4.95GHz)

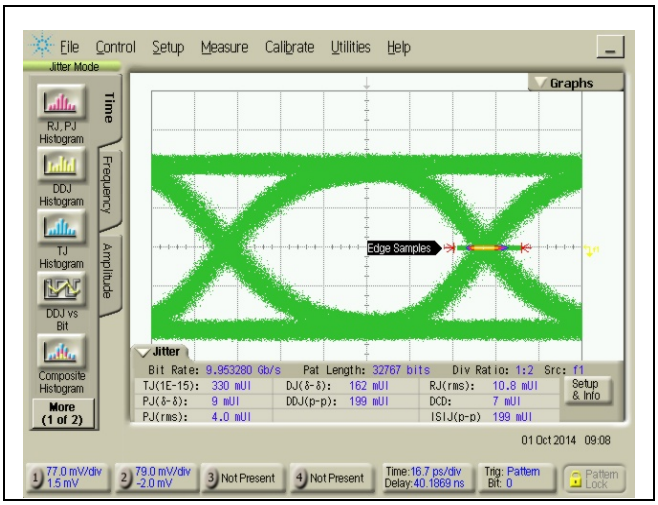


Figure 2-4. Eye Diagram Output @10.3125 Gbps After 30 inches of Backplane (19.5 dB Insertion Loss at 5.156GHz

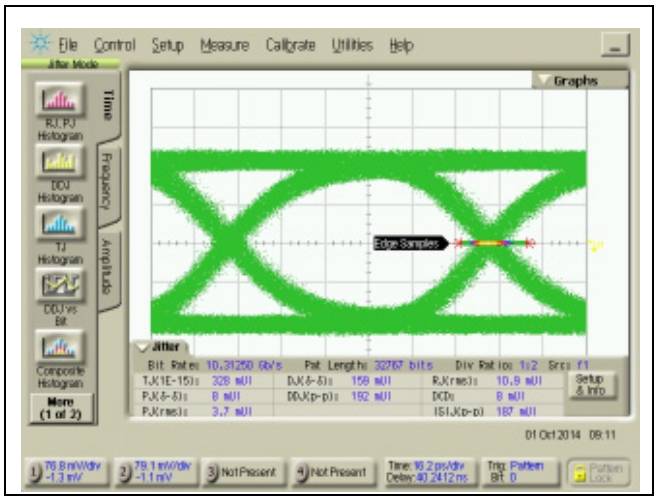


Figure 2-5. Eye Diagram Output@11.88 Gbps After 28 inches of Backplane (21.1dB Insertion Loss at 5.94GHz

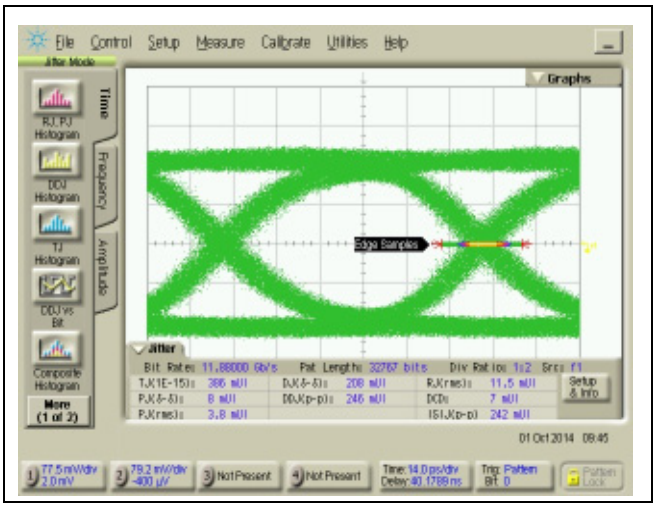


Figure 2-6. Eye Diagram Output@12.5 Gbps , After 28 inches of Backplane (22.2dB Insertion Loss at 6.25GHz

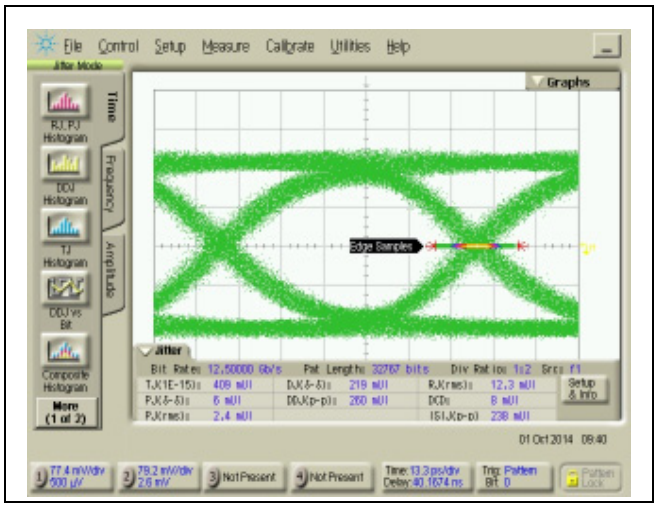


Figure 2-7. M21048 Typical Power Consumption, 1-1 Configuration

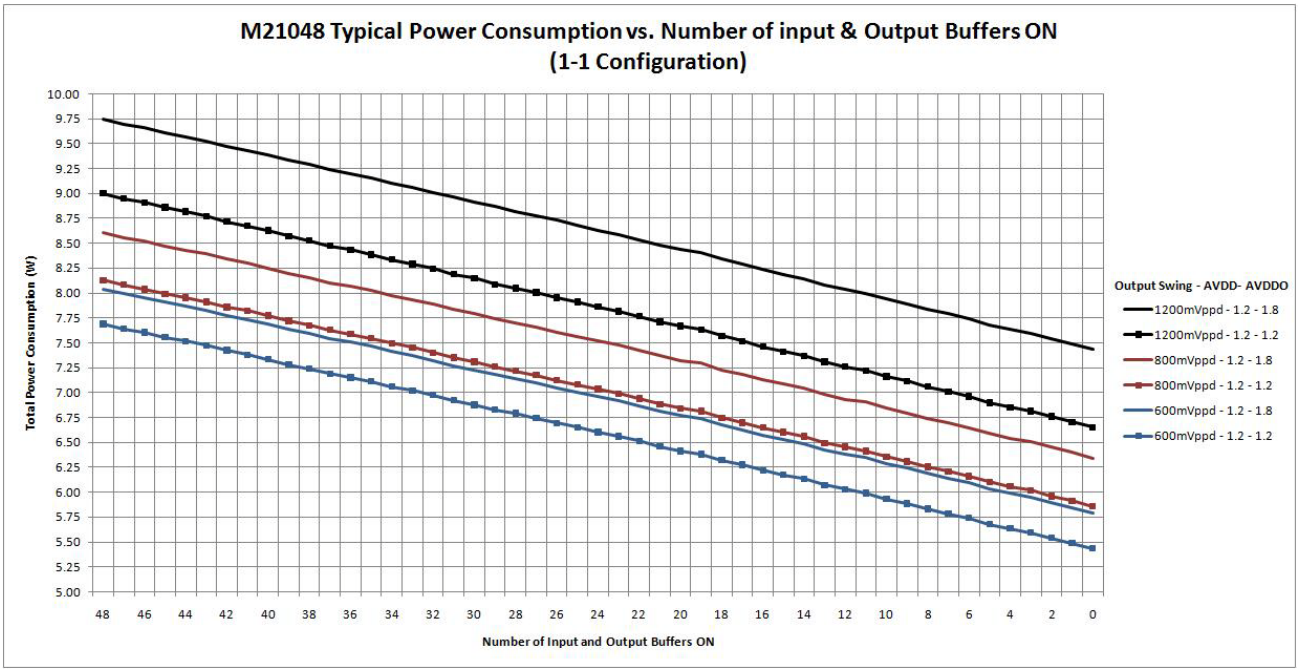


Figure 2-8. M21036 Typical Power Consumption, 1-1 Configuration

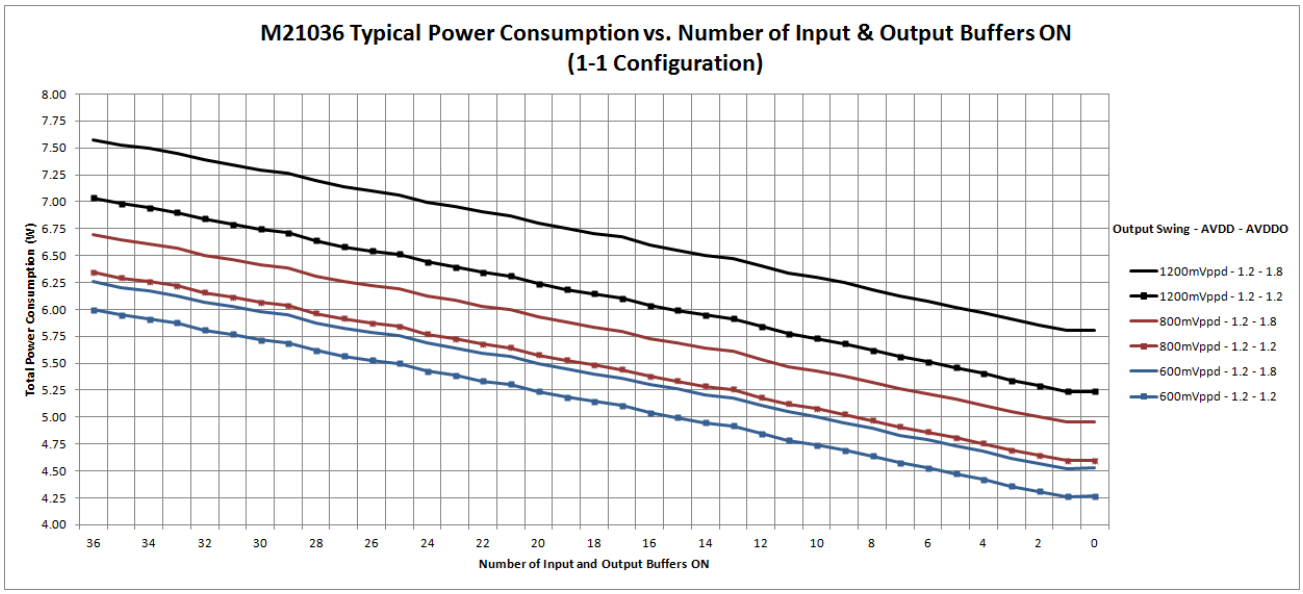
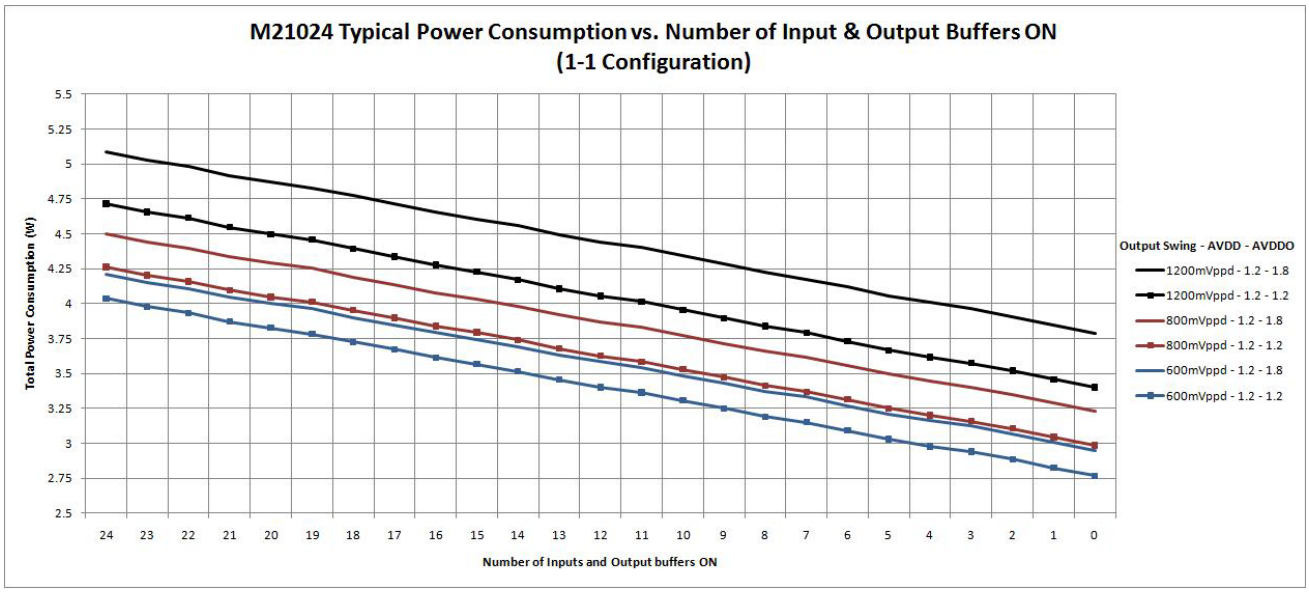


Figure 2-9. M21024 Typical Power Consumption, 1-1 Configuration



3.0 Pinout Diagram, Pin Descriptions, and Package Outline Drawing

3.1 M21048 Pinout

Figure 3-1. M21048 Pinout Diagram (Top View of the Package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A		OUTN_43	OUTP_43	VSS	OUTN_19	OUTP_19	VSS	OUTN_16	OUTP_16	VSS	OUTN_33	OUTP_33	VSS	OUTN_09	OUTP_09	VSS	OUTN_10	OUTP_10	VSS	OUTN_25	OUTP_25	VSS	OUTN_03	OUTP_03	VSS	
B	VSS	VSS	AVDDO	OUTN_41	OUTP_41	AVDDO	OUTN_17	OUTP_17	AVDDO	OUTN_35	OUTP_35	AVDDO	OUTN_11	OUTP_11	AVDDO	OUTN_08	OUTP_08	AVDDO	OUTN_27	OUTP_27	AVDDO	OUTN_01	OUTP_01	AVDDO	VSS	INP_25
C	INP_06	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD	INN_25
D	INN_06	INP_04	VSS	TDI	TRST	AVDDO	OUTN_42	OUTP_42	AVDDO	OUTN_18	OUTP_18	AVDDO	OUTN_32	OUTP_32	AVDDO	OUTN_24	OUTP_24	AVDDO	OUTN_02	OUTP_02	AVDDO	MF4	MF6	VSS	INP_27	VSS
E	VSS	INN_04	VSS	MF11	MSDA	AVDDO	AVDDO	AVDDO	OUTN_40	OUTP_40	AVDDO	OUTN_34	OUTP_34	AVDDO	OUTN_26	OUTP_26	AVDDO	OUTN_00	OUTP_00	AVDDO	AVDDO	MF0	MF2	VSS	INN_27	INP_01
F	INP_28	AVDD	VSS	AVDD	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD	AVDD	VSS	AVDD	INN_01
G	INN_28	INP_30	VSS	INP_07	AVDD	VSS	XOUTPUT EN	XALARM	TMS	TDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	MF9	MF7	MF3	VSS	AVDD	INP_24	VSS	INP_03	VSS
H	VSS	INN_30	VSS	INN_07	INP_05	VSS	XINPUT EN	XOVER TEMP	XRESET	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	MF1	MF5	VSS	INP_26	INN_24	VSS	INN_03	INP_02
J	INP_15	AVDD	VSS	AVDD	INN_05	VSS	CONFIG SEL	XSET	MSCL	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	MF10	MF8	VSS	INN_26	AVDD	VSS	AVDD	INN_02
K	INN_15	INP_13	VSS	INP_29	AVDD	VSS	AVDD	DVDDO	DVDDO	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	AVDD	INP_00	VSS	INP_33	VSS
L	VSS	INN_13	VSS	INN_29	INP_31	VSS	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	INP_32	INN_00	VSS	INN_33	INP_35
M	INP_12	AVDD	VSS	AVDD	INN_31	VSS	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	INN_32	AVDD	VSS	AVDD	INN_35
N	INN_12	INP_14	VSS	INP_37	AVDD	VSS	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	AVDD	INP_34	VSS	INP_09	VSS
P	VSS	INN_14	VSS	INN_37	INP_39	VSS	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	INP_40	INN_34	VSS	INN_09	INP_11
R	INP_36	AVDD	VSS	AVDD	INN_39	VSS	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	INN_40	AVDD	VSS	AVDD	INN_11
T	INN_36	INP_38	VSS	INP_23	AVDD	VSS	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	AVDD	INP_42	VSS	INP_10	VSS
U	VSS	INN_38	VSS	INN_23	INP_45	VSS	NC	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	INP_18	INN_42	VSS	INN_10	INP_08
V	INP_21	AVDD	VSS	AVDD	INN_45	VSS	VSS	CONFIG0	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	INN_AUX	INP_AUX	VSS	INN_18	AVDD	VSS	AVDD	INN_08
W	INN_21	INP_20	VSS	INP_47	AVDD	VSS	VSS	CONFIG1	GRPLN MODE	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	OUTP_ AUX	AVDDO	AVDD	AVDD	VSS	AVDD	INP_16	VSS	INP_41	VSS
Y	VSS	INN_20	VSS	INN_47	AVDD	VSS	M4	EEPROM _SEL	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	OUTN_ AUX	AVDDO	REFN_ PRBS	REFP_ PRBS	NC	AVDD	INN_16	VSS	INN_41	INP_43
AA	INP_22	AVDD	VSS	AVDD	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	AVDD	AVDD	VSS	AVDD	INN_43
AB	INN_22	INP_44	VSS	M2	M0	AVDDO	AVDDO	AVDDO	OUTN_20	OUTP_20	AVDDO	OUTN_46	OUTP_46	AVDDO	OUTN_38	OUTP_38	AVDDO	OUTN_28	OUTP_28	AVDDO	AVDDO	NC	NC	VSS	INP_19	VSS
AC	VSS	INN_44	VSS	M1	M3	AVDDO	OUTN_22	OUTP_22	AVDDO	OUTN_44	OUTP_44	AVDDO	OUTN_36	OUTP_36	AVDDO	OUTN_06	OUTP_06	AVDDO	OUTN_30	OUTP_30	AVDDO	NC	NC	VSS	INN_19	INP_17
AD	INP_46	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD	INN_17
AE	INN_46	VSS	AVDDO	OUTN_21	OUTP_21	AVDDO	OUTN_47	OUTP_47	AVDDO	OUTN_12	OUTP_12	AVDDO	OUTN_15	OUTP_15	AVDDO	OUTN_39	OUTP_39	AVDDO	OUTN_05	OUTP_05	AVDDO	OUTN_29	OUTP_29	AVDDO	VSS	VSS
AF		VSS	OUTN_23	OUTP_23	VSS	OUTN_45	OUTP_45	VSS	OUTN_14	OUTP_14	VSS	OUTN_13	OUTP_13	VSS	OUTN_37	OUTP_37	VSS	OUTN_04	OUTP_04	VSS	OUTN_07	OUTP_07	VSS	OUTN_31	OUTP_31	

3.2 M21048 Pin Description

Table 3-1. M21048 Pin Descriptions (1 of 7)

Pin Name	Pin Number(s)	Type	Description
AV_{DD}	AA2, AA22, AA23, AA25, AA4, AA5, AD2, AD25, C2, C25, F2, F22, F23, F25, F4, F5, G22, G5, J12, J13, J14, J15, J2, J23, J25, J4, K12, K13, K14, K15, K19, K20, K22, K5, K7, L12, L13, L14, L15, L19, L20, L7, L8, M12, M13, M14, M15, M19, M2, M20, M23, M25, M4, M7, M8, N12, N13, N14, N15, N19, N20, N22, N5, N7, N8, P12, P13, P14, P15, P19, P20, P7, P8, R12, R13, R14, R15, R19, R2, R20, R23, R25, R4, R7, R8, T12, T13, T14, T15, T19, T20, T22, T5, T7, T8, U12, U13, U14, U15, U19, U20, U8, V12, V13, V14, V15, V2, V23, V25, V4, W19, W20, W22, W5, Y22, Y5	Power	Analog positive supply
AV_{DDO}	AB11, AB14, AB17, AB20, AB21, AB6, AB7, AB8, AC12, AC15, AC18, AC21, AC6, AC9, AE12, AE15, AE18, AE21, AE24, AE3, AE6, AE9, B12, B15, B18, B21, B24, B3, B6, B9, D12, D15, D18, D21, D6, D9, E11, E14, E17, E20, E21, E6, E7, E8, G11, G12, G13, G14, G15, G16, G17, H10, H11, H12, H13, H14, H15, H16, H17, H18, W10, W11, W12, W13, W14, W15, W16, W18, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y18, Y9	Power	Analog positive supply
DV_{DDO}	K8, K9	Power	Digital positive supply

Table 3-1. M21048 Pin Descriptions (2 of 7)

Pin Name	Pin Number(s)	Type	Description
V_{SS}	A10, A13, A16, A19, A22, A25, A4, A7, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA24, AA3, AA6, AA7, AA8, AA9, AB24, AB26, AB3, AC1, AC24, AC3, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AD24, AD3, AD4, AD5, AD6, AD7, AD8, AD9, AE2, AE25, AE26, AF11, AF14, AF17, AF2, AF20, AF23, AF5, AF8, B1, B2, B25, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C3, C4, C5, C6, C7, C8, C9, D24, D26, D3, E1, E24, E3, F10, F11, F12, F13, F14, F15, F16, F17, F18, F19, F20, F21, F24, F3, F6, F7, F8, F9, G21, G24, G26, G3, G6, H1, H21, H24, H3, H6, J10, J11, J16, J17, J18, J21, J24, J3, J6, K10, K11, K16, K17, K18, K21, K24, K26, K3, K6, L1, L10, L11, L16, L17, L18, L21, L24, L3, L6, L9, M10, M11, M16, M17, M18, M21, M24, M3, M6, M9, N10, N11, N16, N17, N18, N21, N24, N26, N3, N6, N9, P1, P10, P11, P16, P17, P18, P21, P24, P3, P6, P9, R10, R11, R16, R17, R18, R21, R24, R3, R6, R9, T10, T11, T16, T17, T18, T21, T24, T26, T3, T6, T9, U1, U10, U11, U16, U17, U18, U21, U24, U3, U6, U9, V7, V10, V11, V16, V17, V18, V21, V24, V3, V6, V9, W21, W24, W26, W3, W6, W7, Y1, Y24, Y3, Y6	Ground	Ground
CONFIGSEL	J7	CMOS input	Hardware ISC select. (100 kΩ internal pull down) H = ISC2 L = ISC1
EEPROM_SEL	Y8	CMOS input	EEPROM mode select. (100 kΩ internal pull down) H = EEPROM Mode L = Normal Operation
GRPLNMODE	W9	CMOS input	Group/Lane Mode select. (High Z) H = Group Mode L = Lane Mode
xRESET	H9	CMOS input	Reset the entire device. (100 kΩ internal pull-up) H = Normal Operation L = Reset

Table 3-1. M21048 Pin Descriptions (3 of 7)

Pin Name	Pin Number(s)	Type	Description
M4	Y7	CMOS input	Redundancy Mode Enable. (100 kΩ internal pull down) H = Redundancy Mode Enabled L = Redundancy Mode disabled
M3	AC5	CMOS input	Redundancy Mode3 Enable, pin.**M4** must be "High" to able to select this mode. (100 kΩ internal pull down) H = Redundancy Mode3 Enabled L = Redundancy Mode3 disabled
M2	AB4	CMOS input	Redundancy Mode2 Enable, pin.**M4** must be "High" to able to select this mode. (100 kΩ internal pull down) H = Redundancy Mode2 Enabled L = Redundancy Mode2 disabled
M1	AC4	CMOS input	Redundancy Mode1 Enable, pin.**M4** must be "High" to able to select this mode. (100 kΩ internal pull down) H = Redundancy Mode1 Enabled L = Redundancy Mode1 disabled
M0	AB5	CMOS input	Redundancy Mode0 Enable, pin.**M4** must be "High" to able to select this mode. (100 kΩ internal pull down) H = Redundancy Mode0 Enabled L = Redundancy Mode0 disabled
MSCL	J9	CMOS output	EEprom SCL output pin (open drain output, external pull up > 10 kΩ)
MSDA	E5	CMOS input	EEprom SDA input pin (100 kΩ internal pull-up)
TDI	D4	CMOS input	JTAG data input port (100 kΩ internal pull-up)
TDO	G10	CMOS output	JTAG data output port (open drain output, external pull-up)
TMS	G9	CMOS input	JTAG test mode select input port(100 kΩ internal pull-up)
xALARM	G8	CMOS output	LOS alarm. L=alarm assert, H=alarm de-assert (open drain output, external pull-up)
xINPUTEN	H7	CMOS input	Power up inputs. H=power down, L=power up (100 kΩ internal pull-up) **Note**: Hardware configuration will override register configurations
xOUTPUTEN	G7	CMOS input	Power up outputs. H=power down, L=power up (100 kΩ internal pull-up) **Note**: Hardware configuration will override register configurations
xOVERTEMP	H8	CMOS output	Thermal alarm. L=alarm assert, H=alarm de-assert (open drain output, external pull-up)
xSET	J8	CMOS input	Hardware switch state update (update on H to L transition) (100 kΩ internal pull-down)
CONFIG0	V8	CMOS input	Digital interface mode selection (see Section 4.9) (100 kΩ internal pull down)
CONFIG1	W8	CMOS input	Digital interface mode selection (see Section 4.9) (100 kΩ internal pull down)

Table 3-1. M21048 Pin Descriptions (4 of 7)

Pin Name	Pin Number(s)	Type	Description
TRST	D5	CMOS input	Digital interface mode selection (see Section 4.9) (100 kΩ internal pull down)
MF11	E4	CMOS I/O	Multi-function pin for JTAG (100 kΩ internal pull up)
MF10	J19	CMOS input	Multi-function pin for programming interface (high-Z)
MF9	G18	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF8	J20	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF7	G19	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF6	D23	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF5	H20	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF4	D22	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF3	G20	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF2	E23	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF1	H19	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF0	E22	CMOS input	Multi-function pin for programming interface (high-Z)
REFP_PRBS	Y20	PCML input	Positive Reference Clock for PRBS pattern Generator/Checker
REFN_PRBS	Y19	PCML input	Negative Reference Clock for PRBS pattern Generator/Checker Must be properly grounded (as close to the pin as possible)
IN0[P/N]	K23, L23	PCML input	Data input 0; input.Group0 Lane0; true / complement
IN1[P/N]	E26, F26	PCML input	Data input 1; input.Group0 Lane1; true / complement
IN2[P/N]	H26, J26	PCML input	Data input 2; input.Group0 Lane2; true / complement
IN3[P/N]	G25, H25	PCML input	Data input 3; input.Group0 Lane3; true / complement
IN4[P/N]	D2, E2	PCML input	Data input 4; input.Group1 Lane4; true / complement
IN5[P/N]	H5, J5	PCML input	Data input 5; input.Group1 Lane5; true / complement
IN6[P/N]	C1, D1	PCML input	Data input 6; input.Group1 Lane6; true / complement
IN7[P/N]	G4, H4	PCML input	Data input 7; input.Group1 Lane7; true / complement
IN8[P/N]	U26, V26	PCML input	Data input 8; input.Group2 Lane8; true / complement
IN9[P/N]	N25, P25	PCML input	Data input 9; input.Group2 Lane9; true / complement
IN10[P/N]	T25, U25	PCML input	Data input 10; input.Group2 Lane10; true / complement
IN11[P/N]	P26, R26	PCML input	Data input 11; input.Group2 Lane11; true / complement
IN12[P/N]	M1, N1	PCML input	Data input 12; input.Group3 Lane12; true / complement
IN13[P/N]	K2, L2	PCML input	Data input 13; input.Group3 Lane13; true / complement
IN14[P/N]	N2, P2	PCML input	Data input 14; input.Group3 Lane14; true / complement
IN15[P/N]	J1, K1	PCML input	Data input 15; input.Group3 Lane15; true / complement
IN16[P/N]	W23, Y23	PCML input	Data input 16; input.Group4 Lane16; true / complement

Table 3-1. M21048 Pin Descriptions (5 of 7)

Pin Name	Pin Number(s)	Type	Description
IN17[P/N]	AC26, AD26	PCML input	Data input 17; input.Group4 Lane17; true / complement
IN18[P/N]	U22, V22	PCML input	Data input 18; input.Group4 Lane18; true / complement
IN19[P/N]	AB25, AC25	PCML input	Data input 19; input.Group4 Lane19; true / complement
IN20[P/N]	W2, Y2	PCML input	Data input 20; input.Group5 Lane20; true / complement
IN21[P/N]	V1, W1	PCML input	Data input 21; input.Group5 Lane21; true / complement
IN22[P/N]	AA1, AB1	PCML input	Data input 22; input.Group5 Lane22; true / complement
IN23[P/N]	T4, U4	PCML input	Data input 23; input.Group5 Lane23; true / complement
IN24[P/N]	G23, H23	PCML input	Data input 24; input.Group6 Lane24; true / complement
IN25[P/N]	B26, C26	PCML input	Data input 25; input.Group6 Lane25; true / complement
IN26[P/N]	H22, J22	PCML input	Data input 26; input.Group6 Lane26; true / complement
IN27[P/N]	D25, E25	PCML input	Data input 27; input.Group6 Lane27; true / complement
IN28[P/N]	F1, G1	PCML input	Data input 28; input.Group7 Lane28; true / complement
IN29[P/N]	K4, L4	PCML input	Data input 29; input.Group7 Lane29; true / complement
IN30[P/N]	G2, H2	PCML input	Data input 30; input.Group7 Lane30; true / complement
IN31[P/N]	L5, M5	PCML input	Data input 31; input.Group7 Lane31; true / complement
IN32[P/N]	L22, M22	PCML input	Data input 32; input.Group8 Lane32; true / complement
IN33[P/N]	K25, L25	PCML input	Data input 33; input.Group8 Lane33; true / complement
IN34[P/N]	N23, P23	PCML input	Data input 34; input.Group8 Lane34; true / complement
IN35[P/N]	L26, M26	PCML input	Data input 35; input.Group8 Lane35; true / complement
IN36[P/N]	R1, T1	PCML input	Data input 36; input.Group9 Lane36; true / complement
IN37[P/N]	N4, P4	PCML input	Data input 37; input.Group9 Lane37; true / complement
IN38[P/N]	T2, U2	PCML input	Data input 38; input.Group9 Lane38; true / complement
IN39[P/N]	P5, R5	PCML input	Data input 39; input.Group9 Lane39; true / complement
IN40[P/N]	P22, R22	PCML input	Data input 40; input.Group10 Lane40; true / complement
IN41[P/N]	W25, Y25	PCML input	Data input 41; input.Group10 Lane41; true / complement
IN42[P/N]	T23, U23	PCML input	Data input 42; input.Group10 Lane42; true / complement
IN43[P/N]	Y26, AA26	PCML input	Data input 43; input.Group10 Lane43; true / complement
IN44[P/N]	AB2, AC2	PCML input	Data input 44; input.Group11 Lane44; true / complement
IN45[P/N]	U5, V5	PCML input	Data input 45; input.Group11 Lane45; true / complement
IN46[P/N]	AD1, AE1	PCML input	Data input 46; input.Group11 Lane46; true / complement
IN47[P/N]	W4, Y4	PCML input	Data input 47; input.Group11 Lane47; true / complement
INAUX[P/N]	V20, V19	PCML input	Data input AUX; true / complement
OUT0[P/N]	E19, E18	PCML output	Data output 0; output.Group0 Lane0; true / complement

Table 3-1. M21048 Pin Descriptions (6 of 7)

Pin Name	Pin Number(s)	Type	Description
OUT1[P/N]	B23, B22	PCML output	Data output 1; output.Group0 Lane1; true / complement
OUT2[P/N]	D20, D19	PCML output	Data output 2; output.Group0 Lane2; true / complement
OUT3[P/N]	A24, A23	PCML output	Data output 3; output.Group0 Lane3; true / complement
OUT4[P/N]	AF19, AF18	PCML output	Data output 4; output.Group1 Lane4; true / complement
OUT5[P/N]	AE20, AE19	PCML output	Data output 5; output.Group1 Lane5; true / complement
OUT6[P/N]	AC17, AC16	PCML output	Data output 6; output.Group1 Lane6; true / complement
OUT7[P/N]	AF22, AF21	PCML output	Data output 7; output.Group1 Lane7; true / complement
OUT8[P/N]	B17, B16	PCML output	Data output 8; output.Group2 Lane8; true / complement
OUT9[P/N]	A15, A14	PCML output	Data output 9; output.Group2 Lane9; true / complement
OUT10[P/N]	A18, A17	PCML output	Data output 10; output.Group2 Lane10; true / complement
OUT11[P/N]	B14, B13	PCML output	Data output 11; output.Group2 Lane11; true / complement
OUT12[P/N]	AE11, AE10	PCML output	Data output 12; output.Group3 Lane12; true / complement
OUT13[P/N]	AF13, AF12	PCML output	Data output 13; output.Group3 Lane13; true / complement
OUT14[P/N]	AF10, AF9	PCML output	Data output 14; output.Group3 Lane14; true / complement
OUT15[P/N]	AE14, AE13	PCML output	Data output 15; output.Group3 Lane15; true / complement
OUT16[P/N]	A9, A8	PCML output	Data output 16; output.Group4 Lane16; true / complement
OUT17[P/N]	B8, B7	PCML output	Data output 17; output.Group4 Lane17; true / complement
OUT18[P/N]	D11, D10	PCML output	Data output 18; output.Group4 Lane18; true / complement
OUT19[P/N]	A6, A5	PCML output	Data output 19; output.Group4 Lane19; true / complement
OUT20[P/N]	AB10, AB9	PCML output	Data output 20; output.Group5 Lane20; true / complement
OUT21[P/N]	AE5, AE4	PCML output	Data output 21; output.Group5 Lane21; true / complement
OUT22[P/N]	AC8, AC7	PCML output	Data output 22; output.Group5 Lane22; true / complement
OUT23[P/N]	AF4, AF3	PCML output	Data output 23; output.Group5 Lane23; true / complement
OUT24[P/N]	D17, D16	PCML output	Data output 24; output.Group6 Lane24; true / complement
OUT25[P/N]	A21, A20	PCML output	Data output 25; output.Group6 Lane25; true / complement
OUT26[P/N]	E16, E15	PCML output	Data output 26; output.Group6 Lane26; true / complement
OUT27[P/N]	B20, B19	PCML output	Data output 27; output.Group6 Lane27; true / complement
OUT28[P/N]	AB19, AB18	PCML output	Data output 28; output.Group7 Lane28; true / complement
OUT29[P/N]	AE23, AE22	PCML output	Data output 29; output.Group7 Lane29; true / complement
OUT30[P/N]	AC20, AC19	PCML output	Data output 30; output.Group7 Lane30; true / complement
OUT31[P/N]	AF25, AF24	PCML output	Data output 31; output.Group7 Lane31; true / complement
OUT32[P/N]	D14, D13	PCML output	Data output 32; output.Group8 Lane32; true / complement
OUT33[P/N]	A12, A11	PCML output	Data output 33; output.Group8 Lane33; true / complement

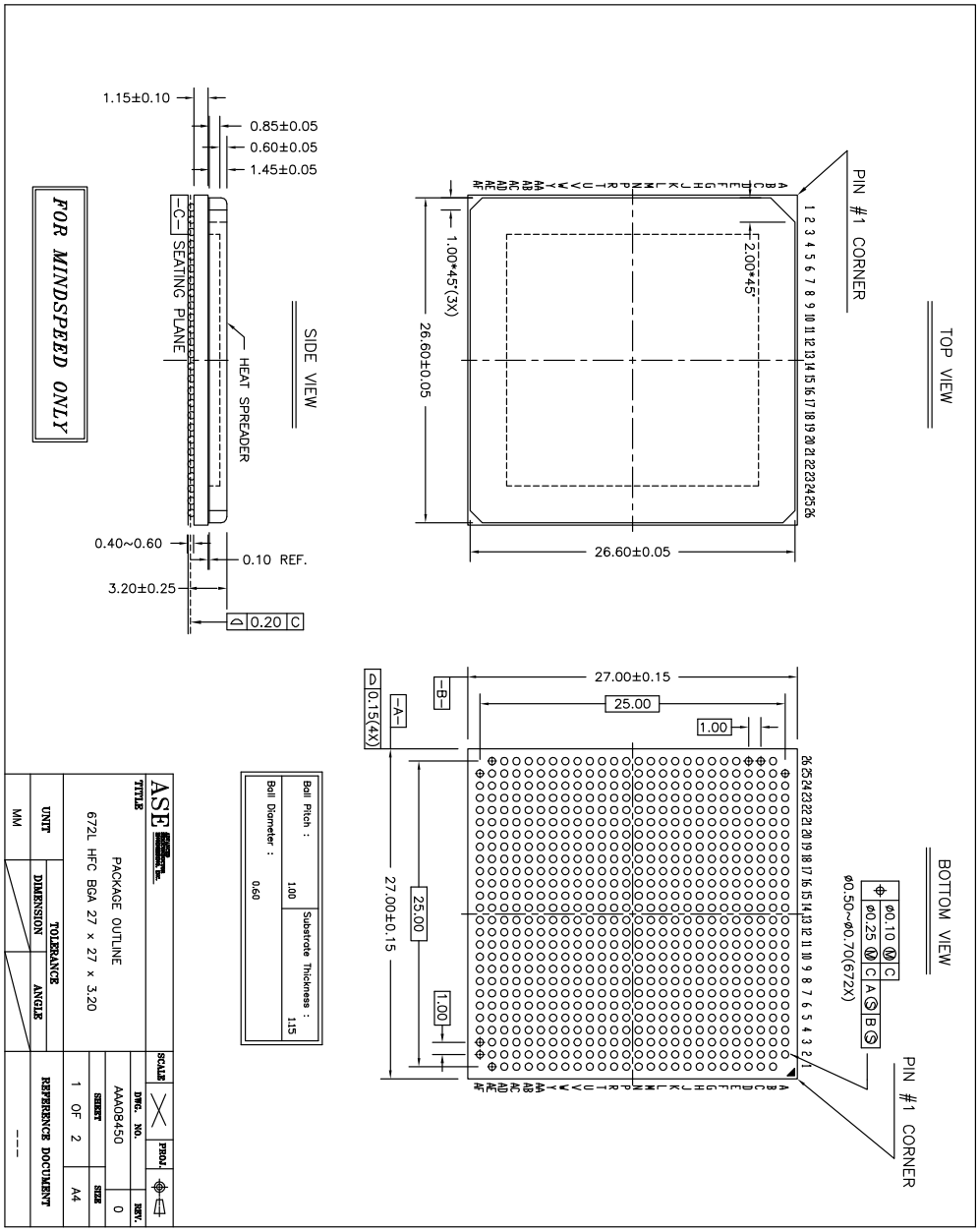
Table 3-1. M21048 Pin Descriptions (7 of 7)

Pin Name	Pin Number(s)	Type	Description
OUT34[P/N]	E13, E12	PCML output	Data output 34; output.Group8 Lane34; true / complement
OUT35[P/N]	B11, B10	PCML output	Data output 35; output.Group8 Lane35; true / complement
OUT36[P/N]	AC14, AC13	PCML output	Data output 36; output.Group9 Lane36; true / complement
OUT37[P/N]	AF16, AF15	PCML output	Data output 37; output.Group9 Lane37; true / complement
OUT38[P/N]	AB16, AB15	PCML output	Data output 38; output.Group9 Lane38; true / complement
OUT39[P/N]	AE17, AE16	PCML output	Data output 39; output.Group9 Lane39; true / complement
OUT40[P/N]	E10, E9	PCML output	Data output 40; output.Group10 Lane40; true / complement
OUT41[P/N]	B5, B4	PCML output	Data output 41; output.Group10 Lane41; true / complement
OUT42[P/N]	D8, D7	PCML output	Data output 42; output.Group10 Lane42; true / complement
OUT43[P/N]	A3, A2	PCML output	Data output 43; output.Group10 Lane43; true / complement
OUT44[P/N]	AC11, AC10	PCML output	Data output 44; output.Group11 Lane44; true / complement
OUT45[P/N]	AF7, AF6	PCML output	Data output 45; output.Group11 Lane45; true / complement
OUT46[P/N]	AB13, AB12	PCML output	Data output 46; output.Group11 Lane46; true / complement
OUT47[P/N]	AE8, AE7	PCML output	Data output 47; output.Group11 Lane47; true / complement
OUTAUX[P/N]	W17, Y17	PCML output	Data output AUX; true / complement
N/C	AA21, AB22, AB23, AC22, AC23, U7, Y21	N/A	Do not connect

3.3 M21048 Package Information

The M21048 is packaged in a 27 mm footprint, 672-pin Ball Grid Array (BGA) and complies with the temperatures and profiles outlined in the JEDEC standard IPC/JEDEC J-STD-020.

Figure 3-2. M21048 Packaging Drawing



3.4 M21036 Pinout

Figure 3-3. M21036 Pinout Diagram (Top View of the Package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A		VSS	OUTN_40	OUTP_40	VSS	OUTN_16	OUTP_16	VSS	OUTN_32	OUTP_32	VSS	OUTN_08	OUTP_08	VSS	OUTN_24	OUTP_24	VSS	OUTN_00	OUTP_00	VSS	MF4		A
B	VSS	VSS	AVDDO	AVDDO	OUTN_18	OUTP_18	AVDDO	OUTN_17	OUTP_17	AVDDO	OUTN_10	OUTP_10	AVDDO	OUTN_03	OUTP_03	AVDDO	OUTN_02	OUTP_02	AVDDO	VSS	MF0	VSS	B
C	VSS	MSDA	MF11	XRESET	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MF6	AVDD	VSS	C
D	INP_05	AVDD	XOVERTEMP	TDI	AVDDO	OUTN_43	OUTP_43	AVDDO	OUTN_35	OUTP_35	AVDDO	OUTN_09	OUTP_09	AVDDO	OUTN_01	OUTP_01	AVDDO	MF1	MF3	VSS	AVDD	INN_24	D
E	INN_05	INP_07	VSS	TDO	TRST	AVDDO	OUTN_19	OUTP_19	AVDDO	OUTN_11	OUTP_11	AVDDO	OUTN_27	OUTP_27	AVDDO	AVDDO	AVDDO	MF9	MF5	VSS	INN_00	INP_24	E
F	VSS	INN_07	VSS	AVDD	MSCL	XALARM	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	MF2	MF7	AVDD	AVDD	VSS	INP_00	VSS	F
G	INP_31	AVDD	VSS	INP_04	AVDD	CONFIGSEL	TMS	XINPUTEN	XOUTPUTEN	AVDD	AVDD	AVDD	AVDD	VSS	VSS	MF10	MF8	AVDD	INN_27	VSS	AVDD	INN_02	G
H	INN_31	INP_06	VSS	INN_04	AVDD	AVDD	XSET	DVDDO	DVDDO	DVDDO	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	INP_27	VSS	INN_01	INP_02	H
J	VSS	INN_06	VSS	AVDD	INP_28	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	INN_03	AVDD	VSS	INP_01	VSS	J
K	INP_13	AVDD	VSS	INP_12	INN_28	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	INP_03	INN_35	VSS	AVDD	INN_32	K
L	INN_13	INP_15	VSS	INN_12	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	INP_35	VSS	INN_08	INP_32	L
M	VSS	INN_15	VSS	AVDD	INP_14	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	INN_09	AVDD	VSS	INP_08	VSS	M
N	INP_39	AVDD	VSS	INP_36	INN_14	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	INP_09	INN_11	VSS	AVDD	INN_10	N
P	INN_39	INP_20	VSS	INN_36	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	INP_11	VSS	INN_43	INP_10	P
R	VSS	INN_20	VSS	AVDD	INP_22	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	INN_17	AVDD	VSS	INP_43	VSS	R
T	INP_21	AVDD	VSS	INP_44	INN_22	AVDD	VSS	CONFIG0	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	OUTP_AUX	AVDD	INP_17	INN_19	VSS	AVDD	INN_40	T
U	INN_21	INP_23	VSS	INN_44	AVDD	CONFIG1	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	OUTN_AUX	AVDD	AVDD	INP_19	VSS	INN_16	INP_40	U
V	VSS	INN_23	VSS	AVDD	EEPROM_SEL	AVDDO	AVDDO	OUTP_47	OUTN_47	AVDDO	OUTP_15	OUTN_15	AVDDO	OUTP_07	OUTN_07	AVDDO	AVDDO	AVDD	AVDD	VSS	INP_16	VSS	V
W	INP_47	AVDD	VSS	NC	AVDDO	OUTP_21	OUTN_21	AVDDO	OUTP_13	OUTN_13	AVDDO	OUTP_39	OUTN_39	AVDDO	OUTP_31	OUTN_31	AVDDO	AVDDO	INN_AUX	INP_AUX	AVDD	INN_18	W
Y	INN_47	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD	INP_18	Y
AA	VSS	VSS	AVDDO	OUTP_22	OUTN_22	AVDDO	OUTP_23	OUTN_23	AVDDO	OUTP_14	OUTN_14	AVDDO	OUTP_05	OUTN_05	AVDDO	OUTP_06	OUTN_06	AVDDO	AVDDO	REFP_PRBS	REFN_PRBS	VSS	AA
AB		VSS	OUTP_20	OUTN_20	VSS	OUTP_44	OUTN_44	VSS	OUTP_12	OUTN_12	VSS	OUTP_36	OUTN_36	VSS	OUTP_04	OUTN_04	VSS	OUTP_28	OUTN_28	VSS	VSS		AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

3.5 M21036 Pin Description

Table 3-2. M21036 Pin Descriptions (1 of 5)

Pin Name	Pin Number(s)	Type	Description
AV_{DD}	C21, G21, J13, K6, M13, N6, R13, T6, D2, G5, J17, L10, M17, P10, R17, U17, D21, H11, J19, L11, M19, P11, R19, U18, F18, H12, J4, L12, M4, P12, R4, U5, F19, H13, J6, L13, M6, P13, R6, V18, F4, H17, K10, L17, N10, P17, T10, V19, G10, H18, K11, L18, N11, P18, T11, V4, G11, H5, K12, L5, N12, P5, T12, W2, G12, H6, K13, L6, N13, P6, T13, W21, G13, J10, K17, M10, N17, R10, T17, Y2, G18, J11, K2, M11, N2, R11, T2, Y21, G2, J12, K21, M12, N21, R12, T21	Power	Analog positive supply
AV_{DDO}	AA12, B19, E15, F15, U7, W14, AA15, B3, E16, F7, U8, W17, AA18, B4, E17, F8, U9, W18, AA19, B7, E6, F9, V10, W5, AA3, D11, E9, U10, V13, W8, AA6, D14, F10, U11, V16, AA9, D17, F11, U12, V17, B10, D5, F12, U13, V6, B13, D8, F13, U14, V7, B16, E12, F14, U15, W11	Power	Analog positive supply
DV_{DDO}	H10, H8, H9	Power	Digital positive supply
V_{SS}	A11, B20, E20, J22, L9, P15, T3, Y20, A14, B22, E3, J3, M1, P16, T7, Y3, A17, C1, F1, J7, M14, P20, T9, Y4, A2, C10, F20, J8, M15, P3, U20, Y5, A20, C11, F22, J9, M16, P7, U3, Y6, A5, C12, F3, K14, M20, P8, V1, Y7, A8, C13, G14, K15, M22, P9, V20, Y8, AA1, C14, G15, K16, M3, R1, V22, Y9, AA2, C15, G20, K20, M7, R14, V3, AA22, C16, G3, K3, M8, R15, W3, AB11, C17, H14, K7, M9, R16, Y10, AB14, C18, H15, K8, N14, R20, Y11, AB17, C19, H16, K9, N15, R22, Y12, AB2, C22, H20, L14, N16, R3, Y13, AB20, C5, H3, L15, N20, R7, Y14, AB21, C6, J1, L16, N3, R8, Y15, AB5, C7, J14, L20, N7, R9, Y16, AB8, C8, J15, L3, N8, T14, Y17, B1, C9, J16, L7, N9, T15, Y18, B2, D20, J20, L8, P14, T20, Y19	Ground	Ground
CONFIGSEL	G6	CMOS input	Hardware ISC select. (100 kΩ internal pull down) H = ISC2 L = ISC1

Table 3-2. M21036 Pin Descriptions (2 of 5)

Pin Name	Pin Number(s)	Type	Description
EEPROM_SEL	V5	CMOS input	EEPROM mode select (100 kΩ internal pull down) H = EEPROM Mode L = Normal Operation
xRESET	C4	CMOS input	Reset the entire device (100 kΩ internal pull-up) H = Normal Operation L = Reset
MSCL	F5	CMOS output	EEprom SCL output pin (open drain output, external pull up > 10 kΩ)
MSDA	C2	CMOS input	EEprom SDA input pin (100 kΩ internal pull-up)
TDI	D4	CMOS input	JTAG data input port (100 kΩ internal pull-up)
TDO	E4	CMOS output	JTAG data output port (open drain output, external pull-up)
TMS	G7	CMOS input	JTAG test mode select input port (100 kΩ internal pull-up)
xALARM	F6	CMOS output	LOS alarm. L=alarm assert, H=alarm de-assert (open drain output, external pull-up)
xINPUTEN	G8	CMOS input	Power up inputs. H=power down, L=power up (100 kΩ internal pull-up) **Note**: Hardware configuration will override register configurations
xOUTPUTEN	G9	CMOS input	Power up outputs. H=power down, L=power up (100 kΩ internal pull-up) **Note**: Hardware configuration will override register configurations
xOVERTEMP	D3	CMOS output	Thermal alarm. L=alarm assert, H=alarm de-assert (open drain output, external pull-up)
xSET	H7	CMOS input	Hardware switch state update (update on H to L transition) (100 kΩ internal pull-down)
CONFIG0	T8	CMOS input	Digital interface mode selection (see Section 5.5) (100 kΩ internal pull down)
CONFIG1	U6	CMOS input	Digital interface mode selection (see Section 5.5) (100 kΩ internal pull down)
TRST	E5	CMOS input	Digital interface mode selection (see Section 5.5) (100 kΩ internal pull down)
MF11	C3	CMOS	I/O Multi-function pin for JTAG (100 kΩ internal pull up)
MF10	G16	CMOS	Multi-function pin for programming interface (high-Z)
MF9	E18	CMOS	I/O Multi-function pin for programming interface (high-Z)
MF8	G17	CMOS	I/O Multi-function pin for programming interface (high-Z)
MF7	F17	CMOS	I/O Multi-function pin for programming interface (high-Z)
MF6	C20	CMOS	I/O Multi-function pin for programming interface (high-Z)
MF5	E19	CMOS	I/O Multi-function pin for programming interface (high-Z)
MF4	A21	CMOS	I/O Multi-function pin for programming interface (high-Z)
MF3	D19	CMOS	I/O Multi-function pin for programming interface (high-Z)

Table 3-2. M21036 Pin Descriptions (3 of 5)

Pin Name	Pin Number(s)	Type	Description
MF2	F16	CMOS	I/O Multi-function pin for programming interface (high-Z)
MF1	D18	CMOS	I/O Multi-function pin for programming interface (high-Z)
MF0	B21	CMOS input	Multi-function pin for programming interface (high-Z)
REFP_PRBS	AA20	PCML input	Positive Reference Clock for PRBS pattern Generator/Checker
REFN_PRBS	AA21	PCML input	Negative Reference Clock for PRBS pattern Generator/Checker Must be properly grounded (as close to the pin as possible)
IN_00[P/N]	F21, E21	PCML input	Data input 00; true / complement
IN_01[P/N]	J21, H21	PCML input	Data input 01; true / complement
IN_02[P/N]	H22, G22	PCML input	Data input 02; true / complement
IN_03[P/N]	K18, J18	PCML input	Data input 03; true / complement
IN_04[P/N]	G4, H4	PCML input	Data input 04; true / complement
IN_05[P/N]	D1, E1	PCML input	Data input 05; true / complement
IN_06[P/N]	H2, J2	PCML input	Data input 06; true / complement
IN_07[P/N]	E2, F2	PCML input	Data input 07; true / complement
IN_08[P/N]	M21, L21	PCML input	Data input 08; true / complement
IN_09[P/N]	N18, M18	PCML input	Data input 09; true / complement
IN_10[P/N]	P22, N22	PCML input	Data input 10; true / complement
IN_11[P/N]	P19, N19	PCML input	Data input 11; true / complement
IN_12[P/N]	K4, L4	PCML input	Data input 12; true / complement
IN_13[P/N]	K1, L1	PCML input	Data input 13; true / complement
IN_14[P/N]	M5, N5	PCML input	Data input 14; true / complement
IN_15[P/N]	L2, M2	PCML input	Data input 15; true / complement
IN_16[P/N]	V21, U21	PCML input	Data input 16; true / complement
IN_17[P/N]	T18, R18	PCML input	Data input 17; true / complement
IN_18[P/N]	Y22, W22	PCML input	Data input 18; true / complement
IN_19[P/N]	U19, T19	PCML input	Data input 19; true / complement
IN_20[P/N]	P2, R2	PCML input	Data input 20; true / complement
IN_21[P/N]	T1, U1	PCML input	Data input 21; true / complement
IN_22[P/N]	R5, T5	PCML input	Data input 22; true / complement
IN_23[P/N]	U2, V2	PCML input	Data input 23; true / complement
IN_24[P/N]	E22, D22	PCML input	Data input 24; true / complement
IN_27[P/N]	H19, G19	PCML input	Data input 27; true / complement
IN_28[P/N]	J5, K5	PCML input	Data input 28; true / complement

Table 3-2. M21036 Pin Descriptions (4 of 5)

Pin Name	Pin Number(s)	Type	Description
IN_31[P/N]	G1, H1	PCML input	Data input 31; true / complement
IN_32[P/N]	L22, K22	PCML input	Data input 32; true / complement
IN_35[P/N]	L19, K19	PCML input	Data input 35; true / complement
IN_36[P/N]	N4, P4	PCML input	Data input 36; true / complement
IN_39[P/N]	N1, P1	PCML input	Data input 39; true / complement
IN_40[P/N]	U22, T22	PCML input	Data input 40; true / complement
IN_43[P/N]	R21, P21	PCML input	Data input 43; true / complement
IN_44[P/N]	T4, U4	PCML input	Data input 44; true / complement
IN_47[P/N]	W1, Y1	PCML input	Data input 47; true / complement
OUT_00[P/N]	A19, A18	PCML output	Data output 00; true / complement
OUT_01[P/N]	D16, D15	PCML output	Data output 01; true / complement
OUT_02[P/N]	B18, B17	PCML output	Data output 02; true / complement
OUT_03[P/N]	B15, B14	PCML output	Data output 03; true / complement
OUT_04[P/N]	AB15, AB16	PCML output	Data output 04; true / complement
OUT_05[P/N]	AA13, AA14	PCML output	Data output 05; true / complement
OUT_06[P/N]	AA16, AA17	PCML output	Data output 06; true / complement
OUT_07[P/N]	V14, V15	PCML output	Data output 07; true / complement
OUT_08[P/N]	A13, A12	PCML output	Data output 08; true / complement
OUT_09[P/N]	D13, D12	PCML output	Data output 09; true / complement
OUT_10[P/N]	B12, B11	PCML output	Data output 10; true / complement
OUT_11[P/N]	E11, E10	PCML output	Data output 11; true / complement
OUT_12[P/N]	AB9, AB10	PCML output	Data output 12; true / complement
OUT_13[P/N]	W9, W10	PCML output	Data output 13; true / complement
OUT_14[P/N]	AA10, AA11	PCML output	Data output 14; true / complement
OUT_15[P/N]	V11, V12	PCML output	Data output 15; true / complement
OUT_16[P/N]	A7, A6	PCML output	Data output 16; true / complement
OUT_17[P/N]	B9, B8	PCML output	Data output 17; true / complement
OUT_18[P/N]	B6, B5	PCML output	Data output 18; true / complement
OUT_19[P/N]	E8, E7	PCML output	Data output 19; true / complement
OUT_20[P/N]	AB3, AB4	PCML output	Data output 20; true / complement
OUT_21[P/N]	W6, W7	PCML output	Data output 21; true / complement
OUT_22[P/N]	AA4, AA5	PCML output	Data output 22; true / complement
OUT_23[P/N]	AA7, AA8	PCML output	Data output 23; true / complement

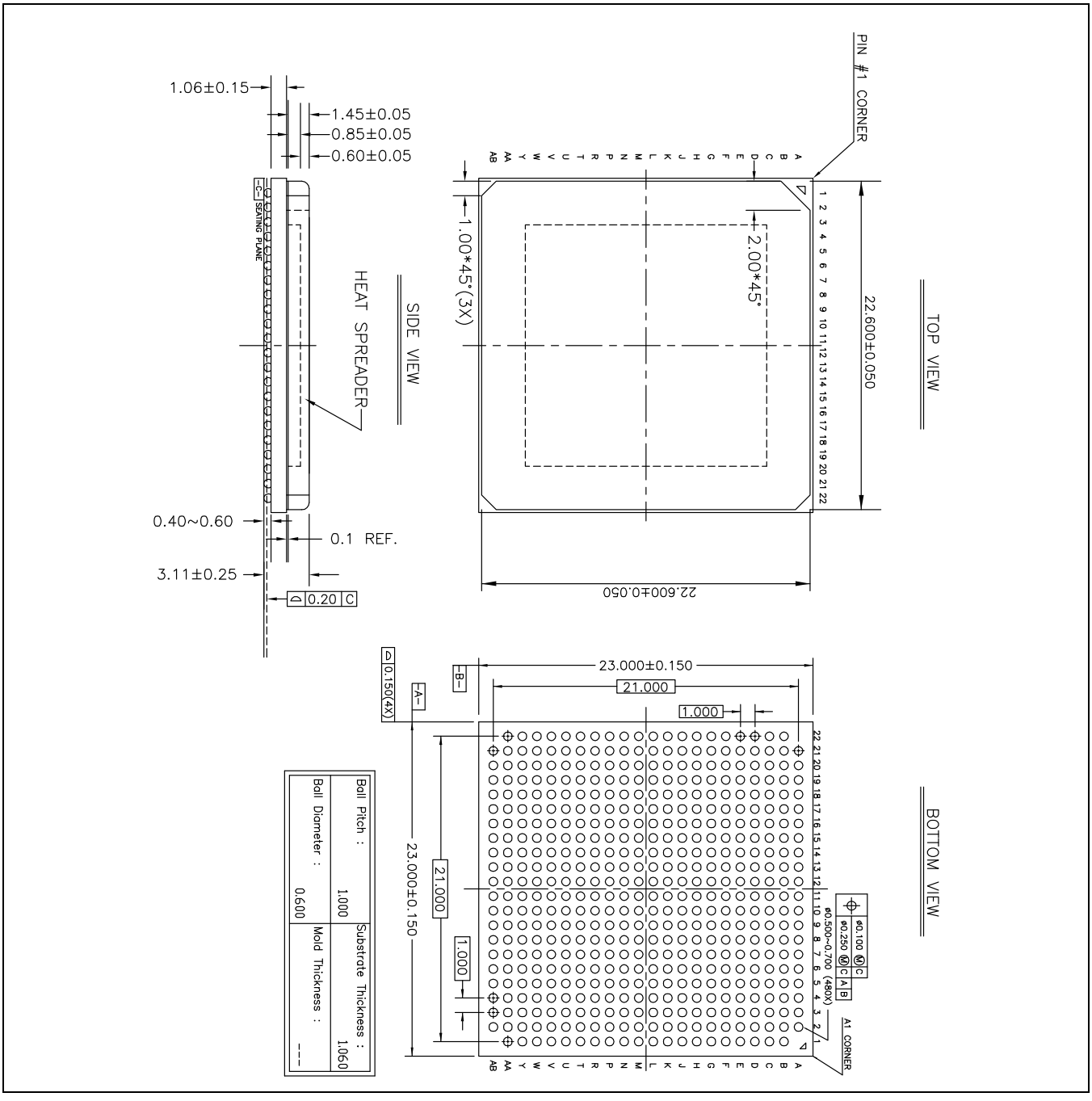
Table 3-2. M21036 Pin Descriptions (5 of 5)

Pin Name	Pin Number(s)	Type	Description
OUT_24[P/N]	A16, A15	PCML output	Data output 24; true / complement
OUT_27[P/N]	E14, E13	PCML output	Data output 27; true / complement
OUT_28[P/N]	AB18, AB19	PCML output	Data output 28; true / complement
OUT_31[P/N]	W15, W16	PCML output	Data output 31; true / complement
OUT_32[P/N]	A10, A9	PCML output	Data output 32; true / complement
OUT_35[P/N]	D10, D9	PCML output	Data output 35; true / complement
OUT_36[P/N]	AB12, AB13	PCML output	Data output 36; true / complement
OUT_39[P/N]	W12, W13	PCML output	Data output 39; true / complement
OUT_40[P/N]	A4, A3	PCML output	Data output 40; true / complement
OUT_43[P/N]	D7, D6	PCML output	Data output 43; true / complement
OUT_44[P/N]	AB6, AB7	PCML output	Data output 44; true / complement
OUT_47[P/N]	V8, V9	PCML output	Data output 47; true / complement
IN_AUX[P/N]	W20, W19	PCML input	Data input AUX; true / complement
OUT_AUX[P/N]	T16, U16	PCML output	Data output AUX; true / complement
N/C	W4	N/A	Do not connect

3.6 M21036 Package Information

The M21036 is packaged in a 23 mm footprint, 480-pin Ball Grid Array (BGA) and complies with the temperatures and profiles outlined in the JEDEC standard IPC/JEDEC J-STD-020.

Figure 3-4. M21036 Packaging Drawing



3.7 M21024 Pinout

Figure 3-5. M21024 Pinout Diagram (Top View of the Package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A		OUTP_19	OUTN_19	VSS	OUTP_18	OUTN_18	VSS	OUTP_10	OUTN_10	VSS	OUTP_08	OUTN_08	VSS	OUTP_02	OUTN_02	VSS	OUTP_01	OUTN_01	VSS	
B	VSS	VSS	AVDDO	AVDDO	AVDDO	OUTP_16	OUTN_16	AVDDO	OUTP_11	OUTN_11	AVDDO	OUTP_03	OUTN_03	AVDDO	OUTP_00	OUTN_00	AVDDO	AVDDO	VSS	INP_01
C	INN_04	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD	INN_01
D	INP_04	AVDD	VSS	MSDA	MF11	TDI	AVDDO	OUTP_17	OUTN_17	AVDDO	OUTP_09	OUTN_09	AVDDO	MF2	MF1	MF4	MF0	VSS	AVDD	VSS
E	VSS	INN_05	VSS	XRESET	TDO	TRST	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	MF10	MF9	MF3	MF6	VSS	AVDD	INP_00
F	INN_07	INP_05	VSS	XOVER TEMP	MSCL	XALARM	TMS	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	MF8	MF7	MF5	VSS	INP_02	INN_00
G	INP_07	AVDD	VSS	CONFIG SEL	XSET	XINPUT EN	XOUTPUT EN	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	INN_02	VSS
H	VSS	INN_06	VSS	AVDD	AVDD	DVDDO	DVDDO	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	INP_03	VSS	AVDD	INP_08
J	INN_13	INP_06	VSS	INN_12	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	INN_03	VSS	INP_09	INN_08
K	INP_13	AVDD	VSS	INP_12	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	INN_09	VSS
L	VSS	INN_14	VSS	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	INP_11	VSS	AVDD	INP_10
M	INN_15	INP_14	VSS	INN_20	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	INN_11	VSS	INP_17	INN_10
N	INP_15	AVDD	VSS	INP_20	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	VSS	INN_17	VSS
P	VSS	INN_21	VSS	AVDD	AVDD	VSS	VSS	VSS	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	INN_AUX	INP_AUX	VSS	AVDD	INP_16
R	INN_23	INP_21	VSS	AVDD	VSS	VSS	CONFIG1	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	VSS	AVDD	AVDD	VSS	INP_18	INN_16
T	INP_23	AVDD	VSS	M4	M1	M0	CONFIG0	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO	OUTP_ AUX	VSS	REFP_ PRBS	VSS	INN_18	VSS
U	VSS	AVDD	VSS	AVDD	AVDD	EEPROM _SEL	GRPLN MODE	AVDDO	OUTN_13	OUTP_13	AVDDO	OUTN_05	OUTP_05	AVDDO	OUTN_ AUX	VSS	REFN_ PRBS	VSS	AVDD	INP_19
V	INN_22	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD	INN_19
W	INP_22	VSS	AVDDO	AVDDO	OUTN_20	OUTP_20	AVDDO	OUTN_23	OUTP_23	AVDDO	OUTN_15	OUTP_15	AVDDO	OUTN_04	OUTP_04	AVDDO	AVDDO	AVDDO	VSS	VSS
Y		VSS	OUTN_21	OUTP_21	VSS	OUTN_22	OUTP_22	VSS	OUTN_12	OUTP_12	VSS	OUTN_14	OUTP_14	VSS	OUTN_06	OUTP_06	VSS	OUTN_07	OUTP_07	

3.8 M21024 Pin Description

Table 3-3. M21024 Pin Descriptions (1 of 4)

Pin Name	Pin Number(s)	Type	Description
AV_{DD}	C19, C2, D19, D2, E19, G10, G11, G12, G16, G17, G2, G9, H10, H11, H12, H16, H19, H4, H5, H9, J10, J11, J12, J16, J5, J9, K10, K11, K12, K16, K17, K2, K5, K9, L10, L11, L12, L16, L19, L4, L5, L9, M10, M11, M12, M16, M5, M9, N10, N11, N12, N16, N17, N2, N5, N9, P10, P11, P12, P19, P4, P5, P9, R16, R17, R4, T2, U19, U2, U4, U5, V19, V2	Power	Analog positive supply
AV_{DDO}	B11, B14, B17, B18, B3, B4, B5, B8, D10, D13, D7, E10, E11, E12, E13, E7, E8, E9, F10, F11, F12, F13, F14, F8, F9, R10, R11, R12, R13, R14, R8, R9, T10, T11, T12, T13, T14, T8, T9, U11, U14, U8, W10, W13, W16, W17, W18, W3, W4, W7	Power	Analog positive supply
DV_{DDO}	H6, H7	Power	Digital positive supply
V_{SS}	A10, A13, A16, A19, A4, A7, B1, B19, B2, C10, C11, C12, C13, C14, C15, C16, C17, C18, C3, C4, C5, C6, C7, C8, C9, D18, D20, D3, E1, E18, E3, F18, F3, G13, G14, G15, G18, G20, G3, G8, H1, H13, H14, H15, H18, H3, H8, J13, J14, J15, J18, J3, J6, J7, J8, K13, K14, K15, K18, K20, K3, K6, K7, K8, L1, L13, L14, L15, L18, L3, L6, L7, L8, M13, M14, M15, M18, M3, M6, M7, M8, N13, N14, N15, N18, N20, N3, N6, N7, N8, P1, P13, P14, P15, P18, P3, P6, P7, P8, R15, R18, R3, R5, R6, T16, T18, T20, T3, U1, U16, U18, U3, V10, V11, V12, V13, V14, V15, V16, V17, V18, V3, V4, V5, V6, V7, V8, V9, W19, W2, W20, Y11, Y14, Y17, Y2, Y5, Y8	Ground	Ground
CONFIGSEL	G4	CMOS input	Hardware ISC select. (100 kΩ internal pull down) H = ISC2 L = ISC1
EEPROM_SEL	U6	CMOS input	EEPROM mode select (100 kΩ internal pull down) H = EEPROM Mode L = Normal Operation
GRPLNMODE	U7	CMOS input	Group/Lane Mode select. (High Z) H = Group Mode L = Lane Mode

Table 3-3. M21024 Pin Descriptions (2 of 4)

Pin Name	Pin Number(s)	Type	Description
xRESET	E4	CMOS input	Reset the entire device (100 kΩ internal pull-up) H = Normal Operation L = Reset
M4	T4	CMOS input	Redundancy Mode Enable (100 kΩ internal pull down) H = Redundancy Mode Enabled L = Redundancy Mode disabled
M1	T5	CMOS input	Redundancy Mode1 Enable, pin.**M4** must be "High" to able to select this mode. 100k Ω internal pull down H = Redundancy Mode1 Enabled L = Redundancy Mode1 disabled
M0	T6	CMOS input	Redundancy Mode0 Enable, pin.**M4** must be "High" to able to select this mode. (100 kΩ internal pull down) H = Redundancy Mode0 Enabled L = Redundancy Mode0 disabled
MSCL	F5	CMOS output	EEprom SCL output pin (open drain output, external pull up > 10 kΩ)
MSDA	D4	CMOS input	EEprom SDA input pin (100 kΩ internal pull-up)
TDI	D6	CMOS input	JTAG data input port (100 kΩ internal pull-up)
TDO	E5	CMOS output	JTAG data output port (open drain output, external pull-up)
TMS	F7	CMOS input	JTAG test mode select input port(100 kΩ internal pull-up)
xALARM	F6	CMOS output	LOS alarm. L=alarm assert, H=alarm de-assert (open drain output, external pull-up)
xINPUTEN	G6	CMOS input	Power up inputs. H=power down, L=power up (100 kΩ internal pull-up) **Note**: Hardware configuration will override register configurations
xOUTPUTEN	G7	CMOS input	Power up outputs. H=power down, L=power up (100 kΩ internal pull-up) **Note**: Hardware configuration will override register configurations
xOVERTEMP	F4	CMOS output	Thermal alarm. L=alarm assert, H=alarm de-assert (open drain output, external pull-up)
xSET	G5	CMOS input	Hardware switch state update (update on H to L transition) (100 kΩ internal pull-down)
CONFIG0	T7	CMOS input	Digital interface mode selection (see Section 4.9) (100 kΩ internal pull down)
CONFIG1	R7	CMOS input	Digital interface mode selection (see Section 4.9) (100 kΩ internal pull down)
TRST	E6	CMOS input	Digital interface mode selection (see Section 4.9) (100 kΩ internal pull down)
MF11	D5	CMOS I/O	Multi-function pin for JTAG (100 kΩ internal pull up)
MF10	E14	CMOS input	Multi-function pin for programming interface (high-Z)

Table 3-3. M21024 Pin Descriptions (3 of 4)

Pin Name	Pin Number(s)	Type	Description
MF9	E15	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF8	F15	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF7	F16	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF6	E17	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF5	F17	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF4	D16	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF3	E16	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF2	D14	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF1	D15	CMOS I/O	Multi-function pin for programming interface (high-Z)
MF0	D17	CMOS input	Multi-function pin for programming interface (high-Z)
REFP_PRBS	T17	PCML input	Positive Reference Clock for PRBS pattern Generator/Checker
REFN_PRBS	U17	PCML input	Negative Reference Clock for PRBS pattern Generator/Checker Must be properly grounded (as close to the pin as possible)
IN0[P/N]	E20, F20	PCML input	Data input 0; input.Group0 Lane0; true / complement
IN1[P/N]	B20, C20	PCML input	Data input 1; input.Group0 Lane1; true / complement
IN2[P/N]	F19, G19	PCML input	Data input 2; input.Group0 Lane2; true / complement
IN3[P/N]	H17, J17	PCML input	Data input 3; input.Group0 Lane3; true / complement
IN4[P/N]	D1, C1	PCML input	Data input 4; input.Group1 Lane4; true / complement
IN5[P/N]	F2, E2	PCML input	Data input 5; input.Group1 Lane5; true / complement
IN6[P/N]	J2, H2	PCML input	Data input 6; input.Group1 Lane6; true / complement
IN7[P/N]	G1, F1	PCML input	Data input 7; input.Group1 Lane7; true / complement
IN8[P/N]	H20, J20	PCML input	Data input 8; input.Group2 Lane8; true / complement
IN9[P/N]	J19, K19	PCML input	Data input 9; input.Group2 Lane9; true / complement
IN10[P/N]	L20, M20	PCML input	Data input 10; input.Group2 Lane10; true / complement
IN11[P/N]	L17, M17	PCML input	Data input 11; input.Group2 Lane11; true / complement
IN12[P/N]	K4, J4	PCML input	Data input 12; input.Group3 Lane12; true / complement
IN13[P/N]	K1, J1	PCML input	Data input 13; input.Group3 Lane13; true / complement
IN14[P/N]	M2, L2	PCML input	Data input 14; input.Group3 Lane14; true / complement
IN15[P/N]	N1, M1	PCML input	Data input 15; input.Group3 Lane15; true / complement
IN16[P/N]	P20, R20	PCML input	Data input 16; input.Group4 Lane16; true / complement
IN17[P/N]	M19, N19	PCML input	Data input 17; input.Group4 Lane17; true / complement
IN18[P/N]	R19, T19	PCML input	Data input 18; input.Group4 Lane18; true / complement
IN19[P/N]	U20, V20	PCML input	Data input 19; input.Group4 Lane19; true / complement

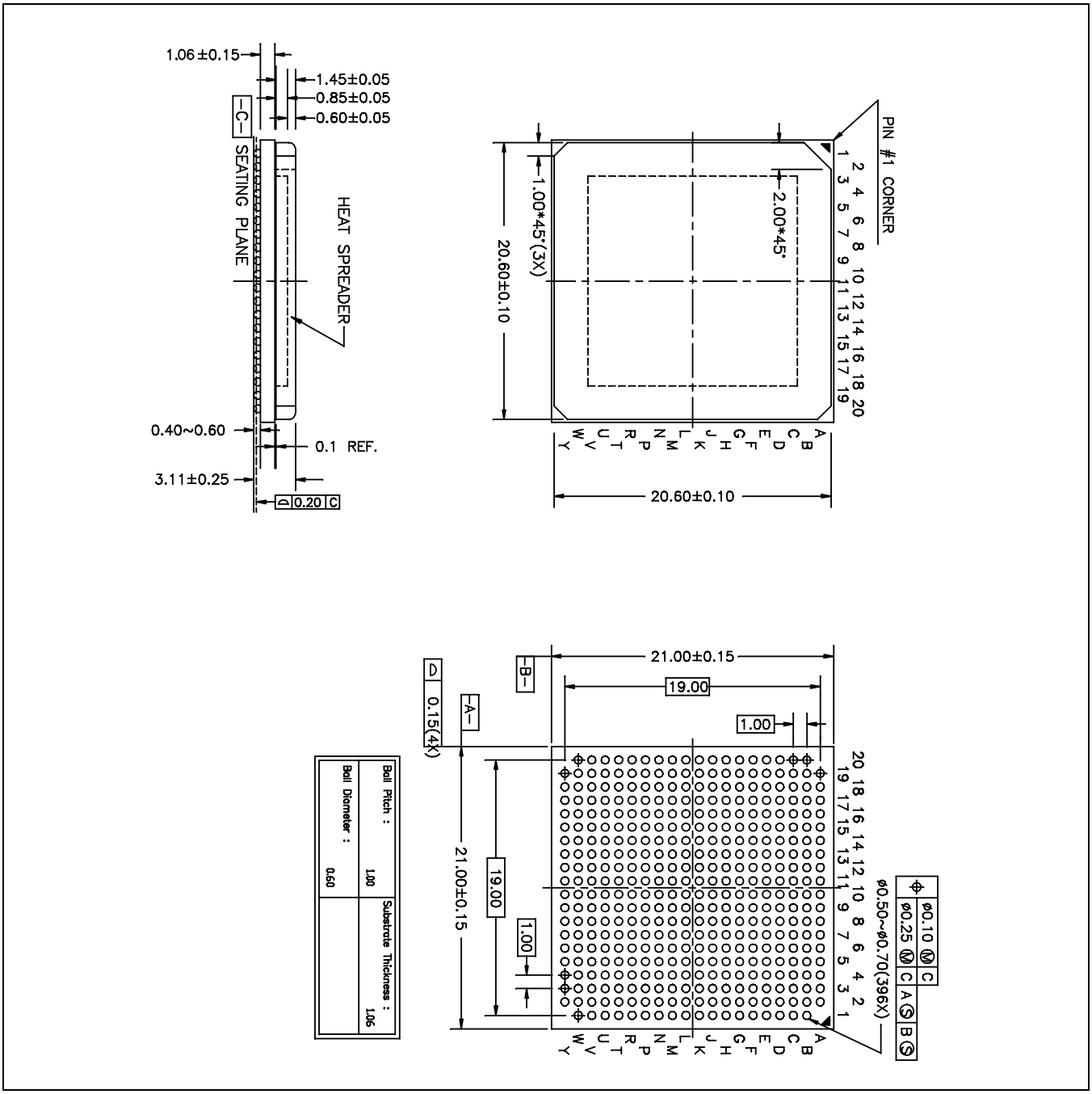
Table 3-3. M21024 Pin Descriptions (4 of 4)

Pin Name	Pin Number(s)	Type	Description
IN20[P/N]	N4, M4	PCML input	Data input 20; input.Group5 Lane20; true / complement
IN21[P/N]	R2, P2	PCML input	Data input 21; input.Group5 Lane21; true / complement
IN22[P/N]	W1, V1	PCML input	Data input 22; input.Group5 Lane22; true / complement
IN23[P/N]	T1, R1	PCML input	Data input 23; input.Group5 Lane23; true / complement
INAUX4[P/N]	P17, P16	PCML input	Data input AUX; true / complement
OUT0[P/N]	B15, B16	PCML output	Data output 0; output.Group0 Lane0; true / complement
OUT1[P/N]	A17, A18	PCML output	Data output 1; output.Group0 Lane1; true / complement
OUT2[P/N]	A14, A15	PCML output	Data output 2; output.Group0 Lane2; true / complement
OUT3[P/N]	B12, B13	PCML output	Data output 3; output.Group0 Lane3; true / complement
OUT4[P/N]	W15, W14	PCML output	Data output 4; output.Group1 Lane4; true / complement
OUT5[P/N]	U13, U12	PCML output	Data output 5; output.Group1 Lane5; true / complement
OUT6[P/N]	Y16, Y15	PCML output	Data output 6; output.Group1 Lane6; true / complement
OUT7[P/N]	Y19, Y18	PCML output	Data output 7; output.Group1 Lane7; true / complement
OUT8[P/N]	A11, A12	PCML output	Data output 8; output.Group2 Lane8; true / complement
OUT9[P/N]	D11, D12	PCML output	Data output 9; output.Group2 Lane9; true / complement
OUT10[P/N]	A8, A9	PCML output	Data output 10; output.Group2 Lane10; true / complement
OUT11[P/N]	B9, B10	PCML output	Data output 11; output.Group2 Lane11; true / complement
OUT12[P/N]	Y10, Y9	PCML output	Data output 12; output.Group3 Lane12; true / complement
OUT13[P/N]	U10, U9	PCML output	Data output 13; output.Group3 Lane13; true / complement
OUT14[P/N]	Y13, Y12	PCML output	Data output 14; output.Group3 Lane14; true / complement
OUT15[P/N]	W12, W11	PCML output	Data output 15; output.Group3 Lane15; true / complement
OUT16[P/N]	B6, B7	PCML output	Data output 16; output.Group4 Lane16; true / complement
OUT17[P/N]	D8, D9	PCML output	Data output 17; output.Group4 Lane17; true / complement
OUT18[P/N]	A5, A6	PCML output	Data output 18; output.Group4 Lane18; true / complement
OUT19[P/N]	A2, A3	PCML output	Data output 19; output.Group4 Lane19; true / complement
OUT20[P/N]	W6, W5	PCML output	Data output 20; output.Group5 Lane20; true / complement
OUT21[P/N]	Y4, Y3	PCML output	Data output 21; output.Group5 Lane21; true / complement
OUT22[P/N]	Y7, Y6	PCML output	Data output 22; output.Group5 Lane22; true / complement
OUT23[P/N]	W9, W8	PCML output	Data output 23; output.Group5 Lane23; true / complement
OUTAUX[P/N]	T15, U15	PCML output	Data output AUX; true / complement

3.9 M21024 Package Information

The M21024 is packaged in a 21 mm footprint, 396-pin Ball Grid Array (BGA) and complies with the temperatures and profiles outlined in the JEDEC standard IPC/JEDEC J-STD-020.

Figure 3-6. M21024 Packaging Drawing



4.0 Functional Description

4.1 General Description

The M21024/M21036/M21048 are medium size, multi-rate, 100 Mbps to 12.5 Gbps, asynchronous 24x24/36x36/48x48 crosspoint switches. The M21024 /M21048 can be configured to switch each lane as an individual lane or in groups of four lanes (lane and group mode respectively). Note that the M21036 does not support group mode. The M21024/M21036/M21048 can be configured globally for all groups/lanes simultaneously using the global page configuration register, Page00h.

The crosspoint configuration is determined by the contents of the Active Switch Configuration (ASC) registers. This register contains the mapping for the source group/lane for that particular output group/lane. Additionally, there are two Intermediate Switch Configurations available (ISC1 and ISC2) that can be loaded into the ASC register by a hardware pin (pin.**xSET**) or software strobe, thus providing synchronous switching.

The M21024/M21036/M21048 are designed to be compatible with multiple standards communication protocols such as InfiniBand, Fibre-Channel, OIF-CEI 2.0, XAUI (1x and 2x) SONET and Serial Video Digital Interface (3G/HD/SD-SDI). Device register configuration is accomplished through any of the integrated 2-wire serial, 4-wire serial or parallel interfaces.

Advanced programmable signal conditioning in the form of input equalization and output de-emphasis are provided to improve performance in large, high data rate systems. The M21024/M21036/M21048 are also designed to pass common-mode signal levels (Electrical Idle) typically associated with PCIe and SAS/SATA used for out-of-band signaling, but the crosspoint is not fully compliant to PCIe/SAS/SATA. For PCIe, refer to MACOM Design Guide (document 21xxx-DG-V2) for PCIe system compatible design. For SAS/SATA, the crosspoint will not support link training. The device incorporates a loss of signal (LOS) detector on each input lane that can be used to squelch that lane output preventing unwanted lane chatter.

The M21024/M21036/M21048 have individually selective power down modes for the input and output sections to assist in power management.

The following figure depicts the functional block diagram of the M21024/M21036/M21048. The various functions and blocks are described in detail in the subsequent sections.

Figure 4-1. M21024, M21036, and M21048 Functional Block Diagram

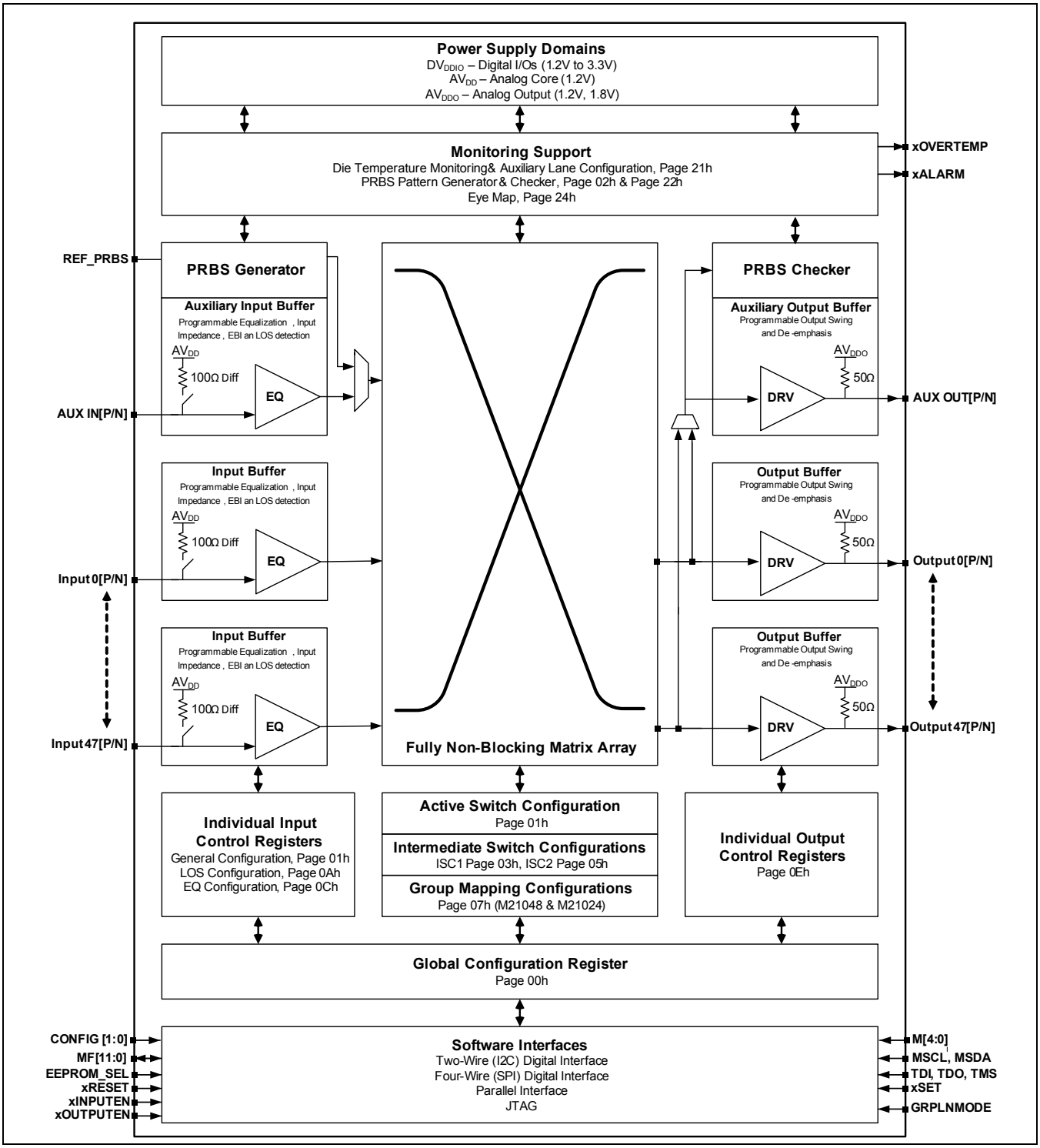


Figure 4-2. High-Speed Differential Input

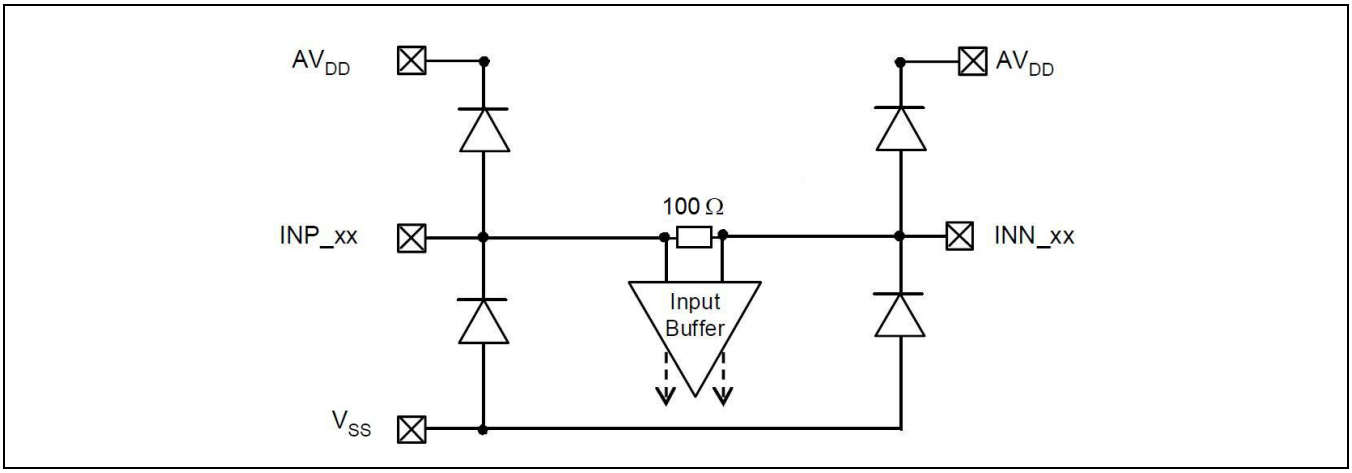


Figure 4-3. High-Speed Differential Output

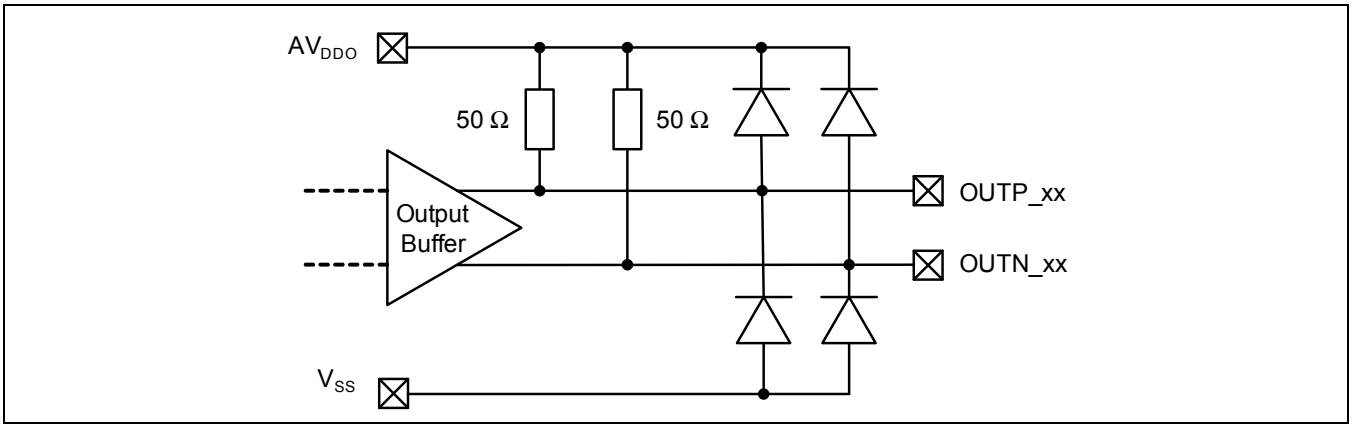


Figure 4-4. Digital Open Drain Logic

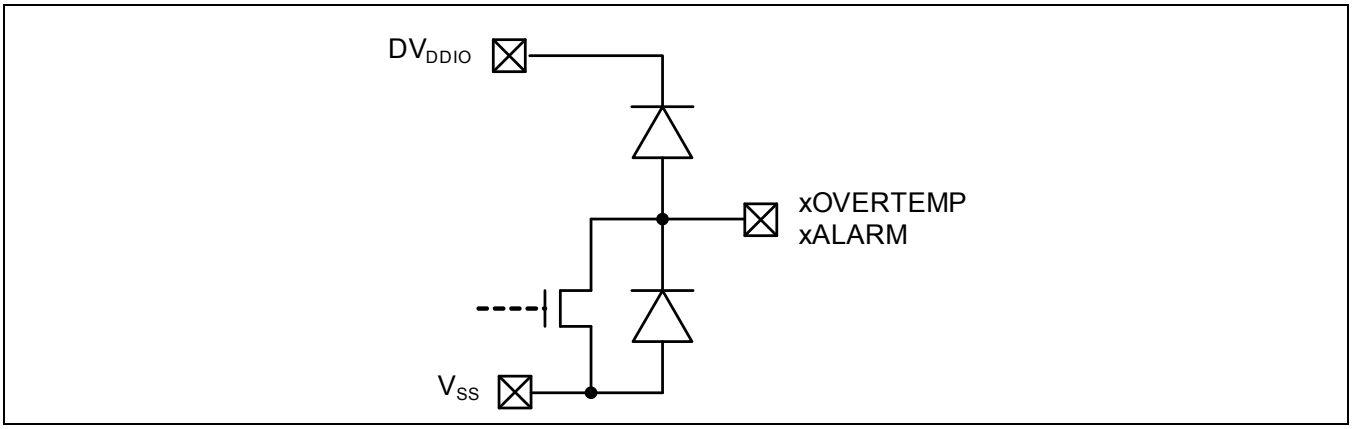


Figure 4-5. Digital CMOS Output

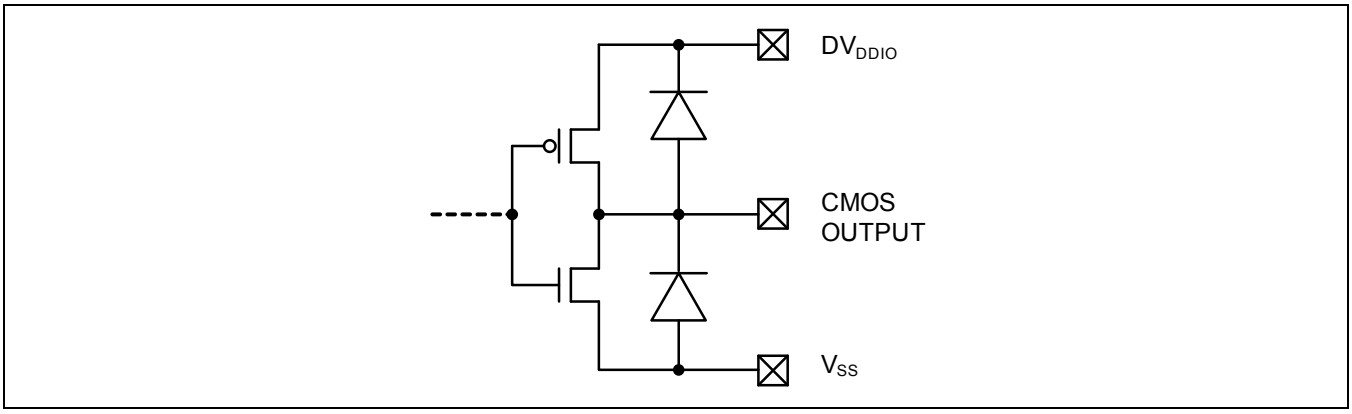


Figure 4-6. Digital CMOS Input

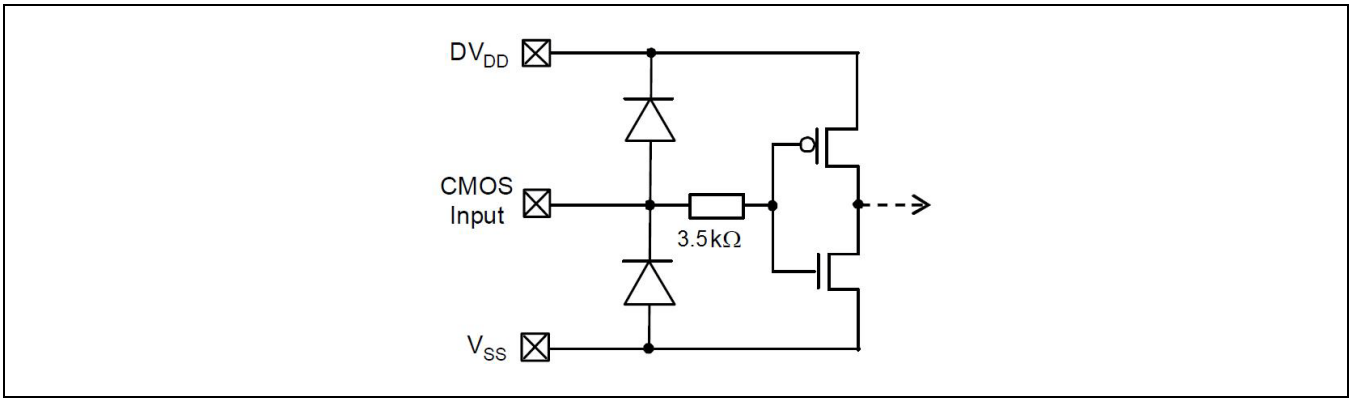


Figure 4-7. Digital CMOS Input with Pull Down

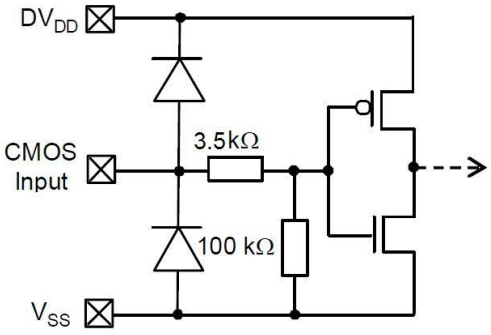
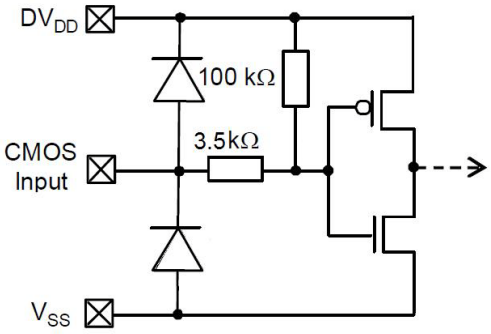


Figure 4-8. Digital CMOS Input with Pull Up



4.2 Power Up

4.2.1 Power on Reset

The M21024/M21036/M21048 initiate a power on reset upon application of supply power at pin.**AV_{DD}** and pin.**DV_{DD}**. A software reset can also be invoked by writing the value AAh to register.**master reset** (page.00h, address.00h). Alternatively, the device may also be reset manually by asserting a logical LOW on pin.**xRST** (pin active low). The soft reset is functionally equivalent to a hard reset. After a reset event, all registers are set to their default state as described in Section 5.0.

A series of hardware pins in conjunction with the default register settings determine the default state of the crosspoint at power up. The hardware pins of interest are described in Section 3.0.

The device configuration after power up, hardware, or software reset depends on hardware pins as defined below:

- The input buffers state is define by pin.**xINPUTEN**.

- If pin.**xINPUTEN** is set to LOW: All input buffers are enabled with termination set to 100 Ω differential termination and input equalization is set to minimum.
- If pin.**xINPUTEN** is set to HIGH: All input buffers are powered down. This includes the LOS detection circuitry. The input termination is set to 100 Ω differential.

- The output buffers state is define by pin.**xOUTPUTEN**.
  - If pin.**xOUTPUTEN** is set to LOW: All output buffers are enabled with termination set to single-ended 50 Ω termination to pin.**AV_{DDO}** and output swing is set to 800 mV_{PPD} and the de-emphasis is set to minimum.
  - If pin.**xOUTPUTEN** is set to HIGH: All output buffers are disabled with termination set to single-ended 50 Ω termination to pin.**AV_{DDO}**.
- The crosspoint switch is set to:
  - M21024/48: Redundancy Mode. This mode is described in Section 4.3.3.
  - M21036: 1-to-1 configuration.

4.2.2 Power up Sequence

The M21024/M21036/M21048 has three different power supplies: DV_{DDO}, AV_{DD}, and AV_{DDO}.

It is recommended to power up DV_{DDO} with AV_{DD} at the same time if possible; this is easily implemented if AV_{DD} = DV_{DDO} = 1.2 V. For DV_{DDO} voltages greater than 1.2 V, two different power supplies are needed. In this case it is recommended to have DV_{DDO} supplied before or with AV_{DD} to avoid control register corruption. If DV_{DDO} is supplied after AV_{DD}, a hardware or software reset is needed to make sure all the registers hold their default value. This reset is needed due to the Power-on Reset (POR) being triggered by AV_{DD}, so if AV_{DD} is supplied before DV_{DDO}, the digital engine does not receive the reset.

There is no power sequence needed for AV_{DDO}, it can be supplied shortly after or before AV_{DD} or DV_{DDO}.

It is recommended to hold pin.**xRESET** LOW for a minimum of 10 µs after all supplies (including the EEPROM) are stabilized (95% of setting point) and before writing or reading any data to the digital interfaces.

It is also recommended to have the input and output buffers disabled at power up, as the rush in current could be too high for the power supply to handle. Staggering the power supply needs can easily implemented by sequentially enabling the input and output buffers by using pin.**xINPUTEN** and pin.**xOUTPUTEN**. This methodology is also recommended if the device is coming out of the standby mode.

NOTE: pin.**xINPUTEN** and pin.**xOUTPUTEN** have to be driven low for normal operation. The hardware configuration will override any register configurations

4.2.3 Power Up/Down States

The M21024/M21036/M21048 have individual selective power up and down modes for the input and output buffers to assist in power management. During operation, all inputs and outputs can be globally powered down and disabled using pin.**xINPUTEN** and pin.**xOUTPUTEN**, or using the global output control register Page00h.Reg0Bh for the output drivers and global input control register Page00h.Reg09h for the input buffers. The hardware control can be overwritten or suppressed through software registers for both the input and output settings, allowing for greater control of the device.

Additionally, the M21024/M21036/M21048 can be set to standby mode by using Page 00h, register.gen config.bit[0]. Please note that it is recommended to have the input and output buffers disabled as the device returns from standby mode, as the rush in current could be too high for the power supply to handle.

4.3 Group/Lane Modes

4.3.1 M21036 Lane Mode

The M21036 does not support Group Mode, only lane mode. In lane mode each lane has its own setup registers and can be configured independently of the other lanes.

4.3.2 M21024/48 Group and Lane Modes

The M21024 and M21048 support both Group and Lane modes. Group mode allows for a single set of control registers to be used to control four input/output lanes.

Group or lane mode is globally controlled by pin.**GRPLNMODE**, but can be overridden by the group/lane mode Page00h, register.**gen config**.bit[7:6].

Many of the registers for individual control are used for both group and lane mode. For example, the contents of a register which determines which input lane is routed to which output lane in lane mode also determines which input group is routed to which output group in group mode.

This implies that the valid M21024/M21036/M21048 register address space varies dynamically with device configuration. In the lane mode, there may be 24 registers (M21024), 36 registers (M21036), or 48 registers (M21048) that determine the individual lane configuration. In group mode, only six of those will be valid registers for the M21024 and 12 for the M21048. The register addresses beyond the active function are not defined.

The M21024/M21048 register memory mapping is divided into pages. Group and lane configuration pages are organized such that the individual register address corresponds to the actual output lane number or actual output group number being controlled.

4.3.3 M21024/M21048 Hard Wired Redundancy Mode

The M21024/M21048 have a built-in, hard-wired, redundancy mode (there is no redundancy mode on the M21036). This is a switch configuration that can be asserted either by means of a hardware pin or by register contents. However, after power up, hardware, or software reset, the hardware pins takes precedence over the register control.

- If pin.**M4**=”HIGH”, then redundancy mode is used regardless of the contents of Page 00h, register.**acl_cntl**.
- If pin.**M4**=”LOW” then Page00h, register.**acl_cntl**.bit[4] determines redundancy or normal mode.

However, Page00h, register.**acl_cntl**.bit[4] by default enables the hard wired redundancy mode. This means that the default configuration is set to redundancy mode unless pin.**M4**=LOW and Page00h, register.**acl_cntl**.bit[4] = "1b".

Note that once the M21024/M21048 goes into Hard Wired Redundancy Mode, the device will:

- Be set automatically to Group Mode Configuration regardless of the status of pin. **GRPLNMODE.**
- The Active Switch Configuration (ASC) page is not enabled, thus the crosspoint configuration is not reflected in any of the registers on Page01h.
- The crosspoint will be set according to Table 4-1 and Table 4-2 below.

Table 4-1. M21048, Redundancy Mode Configuration (Default After Power up, Hardware or Software Reset)

Condition	Configuration
Redundancy Mode	input.group0 to output.group8 and output.group9
	input.group2 to output.group2 and output.group3
	input.group8 to output.group10 and output.group11
	input.group10 to output.group4 and output.group5
Redundancy Mode, pin.**M0** = 0	input.group6 to output.group0
Redundancy Mode, pin.**M0** = 1	input.group4 to output.group0
Redundancy Mode, pin.**M1** = 0	input.group1 to output.group1
Redundancy Mode, pin.**M1** = 1	input.group11 to output.group1
Redundancy Mode, pin.**M2** = 0	input.group3 to output.group6
Redundancy Mode, pin.**M2** = 1	input.group9 to output.group6
Redundancy Mode, pin.**M3** = 0	input.group7 to output.group7
Redundancy Mode, pin.**M3** = 1	input.group5 to output.group7

Table 4-2. M21024, Redundancy Mode Configuration (Default After Power up, Hardware or Software Reset)

Condition	Configuration
Redundancy Mode	input.group0 to output.group2 and output.group3
	input.group2 to output.group4 and output.group5
Redundancy Mode, pin.**M0** = 0	input.group1 to output.group0
Redundancy Mode, pin.**M0** = 1	input.group5 to output.group0
Redundancy Mode, pin.**M1** = 0	input.group3 to output.group1
Redundancy Mode, pin.**M1** = 1	input.group4 to output.group1

4.4 High-Speed Input Lanes

4.4.1 Input Buffer and Equalization Control

The input lanes of the M21024/M21036/M21048 are designed to be AC coupled, using external coupling capacitors, or DC coupled. Input equalization can be configured individually, by lane, by group, or globally across all lanes all groups. The input equalizers can be globally configured using Page00h.Reg0A[4:0]. Individual equalizer "N" control is set using Page0Ch.RegNh[4:0].

4.4.2 Loss of Signal Alarm

The M21024/M21036/M21048 includes Loss of Signal (LOS) Alarms. This function allows the user to monitor the status of each incoming signal on the device. The user has the ability to monitor not only the current state, but also supports latched alarms for extended time period checking.

The LOS Alarms can be configured either globally by the configuration register on the global page or individually on a lane/group basis in the corresponding lane/group LOS configuration register. The LOS is controlled globally by default.

The LOS has two registers used for getting information from the device. The first is the LOS status register (Page00h.Reg50h to Reg55h) which shows the real time state of the LOS. The second is the LOS alarm (Page00h.Reg40h to Reg45h) which will latch any time the LOS status is high. The user is required to clear the LOS alarm with a register write. Each LOS alarm also has a MASK register (Page00h.Reg60h to Reg65h) that is used to mask out that lane/group from triggering pin.**xAlarm**.

In addition to being able to monitor the LOS in software the device also supports pin.**xAlarm** which can be configured to monitor one or all of the LOS signals. Pin.**xAlarm** is configured using the Page00h.Reg07h register located in the global page and has the ability to monitor either the LOS alarm or an individual LOS status.

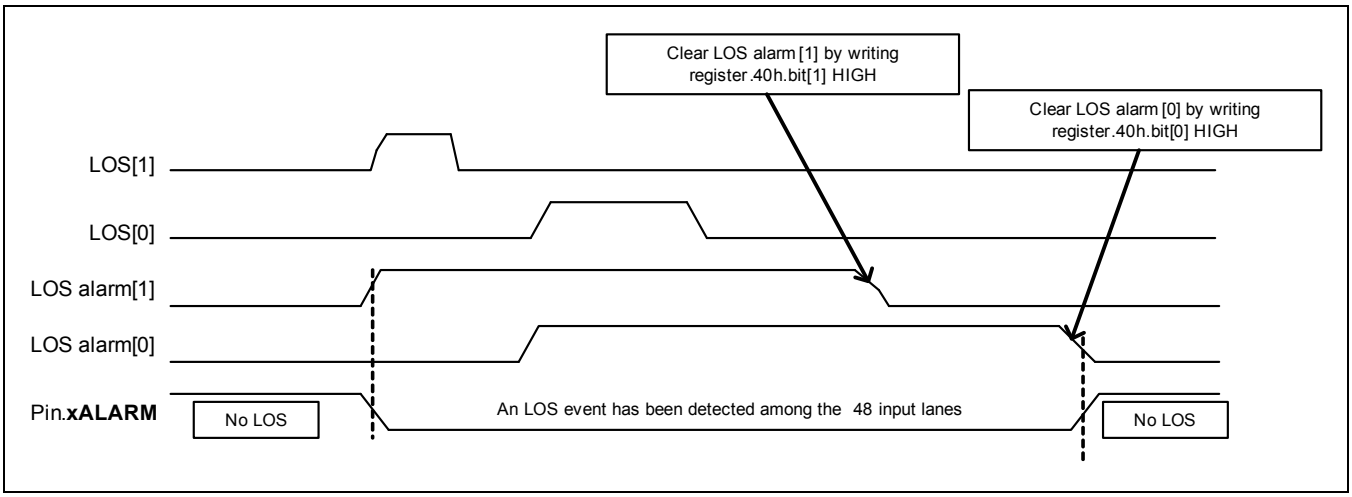
NOTE: Disabling the LOS detection circuit is recommended when signals at data rates below 100 Mbps are present as the low data rate may erroneously trigger an LOS event.

4.4.2.1 Using xAlarm to Monitor LOS Events For All Input Channels, Application Example

This example illustrates a monitoring feature that determines if there are any changes on the signal at any of the input channels. The xAlarm will trigger on any LOS event change. The following procedures are required:

1. Clear all the LOS alarms. Set Page 0h, Registers [45h:40h] to FFh. Notice that in clearing the LOS alarms, pin.**xAlarm** goes HIGH.
2. If there is an LOS event, new signal present or loss, the pin.**xAlarm** will go LOW.

Figure 4-9. Monitoring LOS Globally Using Hardware pin.xALARM

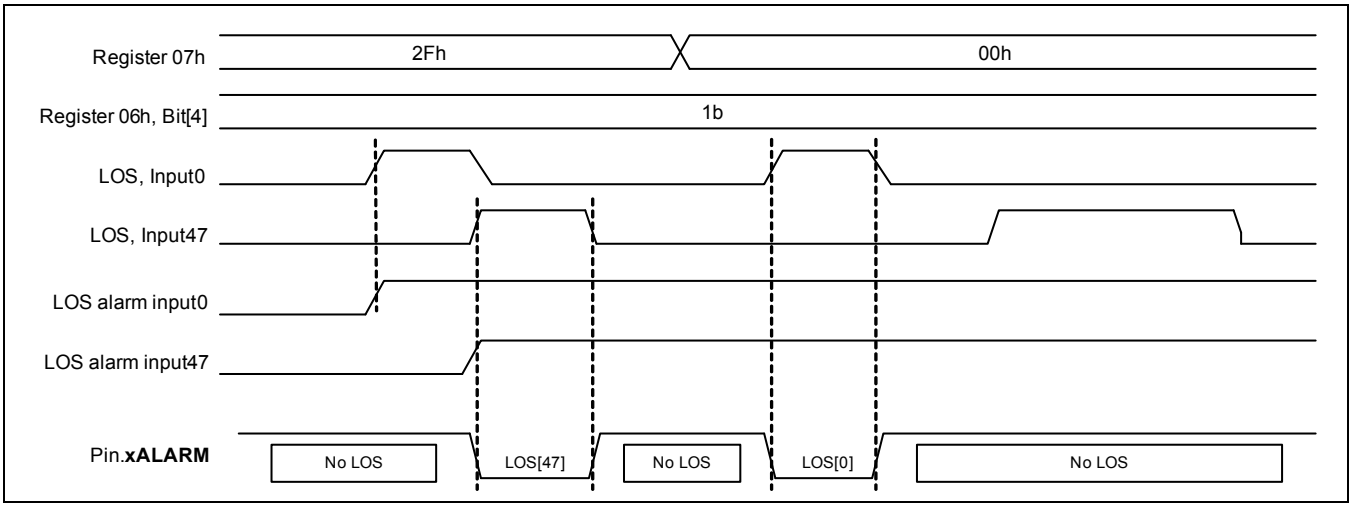


4.4.2.2 Using xAlarm to Monitor LOS Events for an Individual Input Channel, Application Example

This example illustrates a monitoring feature that determines if there are any changes on a particular input channel. The xAlarm will trigger on any LOS event change on this input channel. The following procedures are required:

1. Clear all the LOS alarms. Set Page 0h, Registers [45h:40h] to FFh. Notice that in clearing the LOS alarms, pin.**xAlarm** goes HIGH.
2. Mask the alarms on all the unwanted inputs. For this example input 47 will be monitored, set Page 00h, Registers [64h:60h] to FFh and Register 65h to 7Fh.
3. Enable LOS monitor for an individual lane. Set Page 00h, Register 06h, Bit[4] to 1b.
4. Select the input channel to be monitored. Set Page 00h, Register 07h to 2Fh, to monitor input 47.
5. Pin.**xAlarm** will follow the LOS status on input 47. If there is a LOS on input 47, pin.**xAlarm** will go HIGH or if there is a signal present on input 47, the pin.**xAlarm** will go LOW.

Figure 4-10. Monitoring LOS Individual Lanes Using Hardware pin.xALARM



4.4.3 Squelch and Electrical Idle (EI) Pass-through

The M21024/M21036/M21048 supports out of band signaling (OOB) of PCIe and SAS/SATA protocols. Examples of usage include the COMWAKE, COMINIT, COMRST in SATA/SAS, and COMSAS in SAS. As a result, the M21024/M21036/M21048 output drivers have three output states - high, low and "common mode" as defined within the SAS/SATA protocol, or the Electrical Idle state (EI) as defined within PCIe. Within this text, the common mode output/input state will be referred to only as the Electrical Idle or EI.

The Electrical Idle detection is globally disabled at power up. It can be globally (or individually) enabled using the EI configuration register in the global page (or individual registers see Section 5.0).

Note that the M21048/36/24 is compliant to the SATA GEN1 minimum threshold of 40 mV to not detect the OOB signal. Similarly for SATA GEN2 and GEN3, the M21048/36/24 meets the minimum threshold of 60 mV to not detect the OOB signal. The maximum threshold of 210 mV to detect the OOB signal is met for GEN1, GEN2 and

GEN3. For SAS applications, the threshold levels of 110 mV are not met, the threshold is typically in the 80 mV-100 mV range.

In normal operation, if an EI input signal duration is longer than approximately 5 µs, an LOS alarm will activate, unless the LOS detection is disabled using the LOS configuration register (see Section 4.4.2). This feature can be used in SATA/SAS to distinguish between a valid LOS and regular EI signaling. The PCIe user can either ignore the LOS alarm or disable the feature. The real time EI status on any single lane (regardless of the lane or group mode status) can be monitored on pin.**xAlarm**. The monitor lane is selected with Page00h.Reg07h. This allows the user to measure the duration of the EI signal which may be useful in SATA/SAS applications.

For lane inputs that are AC coupled, non-DC balanced patterns significantly longer than the input RC time-constant will cause the crosspoint outputs to randomly toggle due to the resulting degradation of input noise margin. Similarly, at the output of the M21024/M21036/M21048, very long non-DC balanced patterns may cause significant DC wander, potentially resulting in gross bit distortion upon high-speed data re-start. To remedy this issue, the M21024/M21036/M21048 has an integrated automatic squelch feature. When a channel input LOS is detected, squelch is activated and the lane output level is forced to one of three user defined states (High, Low or EI). The EI state is recommended for AC coupled applications.

Squelch to EI (common mode) level is globally enabled at power up and can be configured using the squelch register on Page00h.Reg05h. Individual lane squelch configuration for a given lane N is accomplished by setting the squelch field of Page00h.Reg09h register.

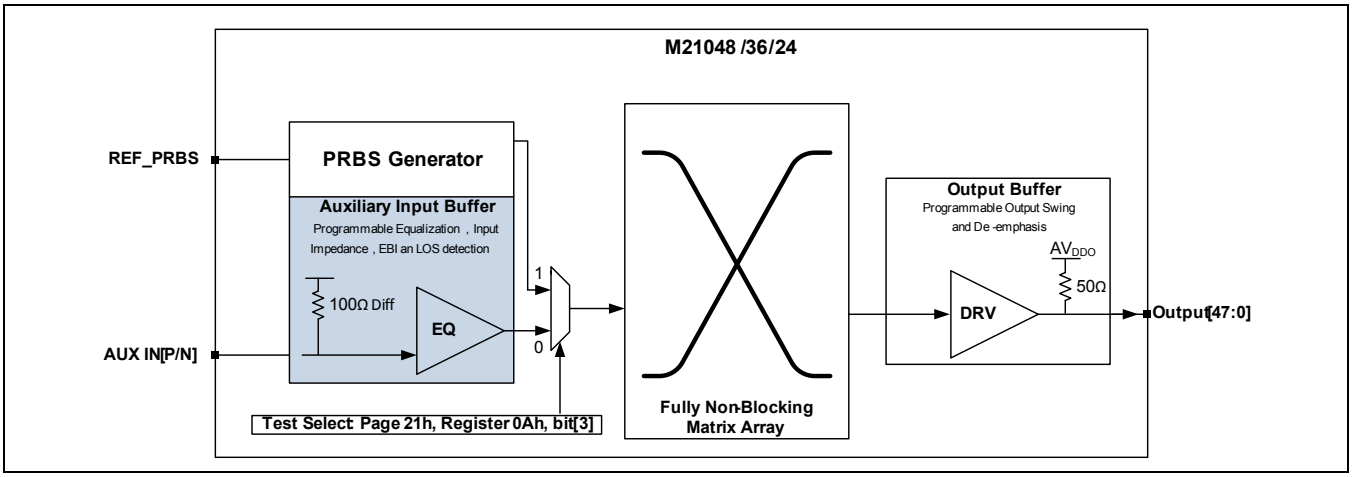
4.4.4 Auxiliary Input Lane

The M21024/M21036/M21048 have an input lane pin.**INP_AUX** and pin.**INN_AUX** available. This lane also features the input equalization, LOS, Squelch and Electrical Idle and input termination capabilities as any primary high-speed input lane.

The output of this auxiliary input lane buffer goes to an input channel on the crosspoint dedicated for test purposes only. To enable the auxiliary input lane to go to the crosspoint register.**test_insel**, (**Page 21h** register 0Ah, bit3) must be set to “0b”.

NOTE: JTAG cannot be performed on the auxiliary channels.

Figure 4-11. Auxiliary Input Buffer



At power up or after a hardware or software reset the auxiliary input lane is powered down by default, to enable the auxiliary input buffer Page 21h, register.**hs_aux_squelch**.bit[0] must be set to “0b”.

In order to further control the auxiliary input buffer lane, refer to Page 21h:

- Auxiliary input lane Electrical Idle control, address 81h
- Auxiliary input lane squelch control, address 80h
- Auxiliary input lane LOS control, address 82h
- Auxiliary input lane Input Termination control, address 83h
- Auxiliary input lane Equalization Level control, address 84h

4.5 High-Speed Output Lanes

4.5.1 Output Drive Levels

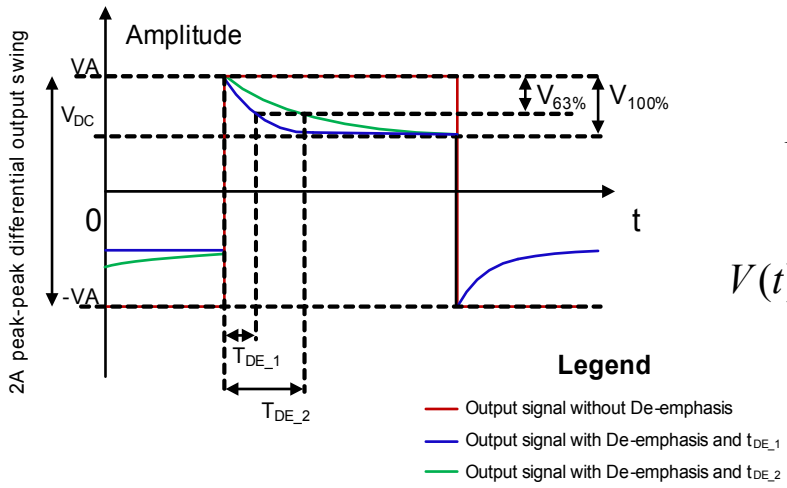
The output lanes of the M21024/M21036/M21048 are designed to be AC coupled, using external coupling capacitors, or DC coupled. Output drive levels can be configured individually, lane by lane, group by group, or globally across all lanes or groups. The outputs can be globally disabled and powered down with pin.**xOUTPUTEN**.

Page00h.Reg0B[7] is used to select either global or individual output buffer control. The output buffer is biased using the supply pin.$\mathbf{AV_{DDO}}$ which can be set to 1.2 V or 1.8 V based on the required differential output swing. The differential output swing can be set from a maximum of 1200 mV_{PPD} (typical) down to a minimum of 600 mV_{PPD} (typical). There are three typical settings defined as 600 mV_{PPD}, 800 mV_{PPD}, and 1200 mV_{PPD}. For typical output swing selected as 1200 mV_{PPD}, the supply pin.$\mathbf{AV_{DDO}}$ must be set to 1.8 V.

4.5.2 Output De-emphasis

The M21024/M21036/M21048 have seven steps (0 dB to ~10.5 dB in ~1.5 dB per step), output de-emphasis capability. The output de-emphasis level can be globally set using Page00h.Reg0B[6:4] or individually using Page0Eh.RegNh[6:4]. The de-emphasis time constant can be similarly set using bit[0] from the same register.

Figure 4-12. Definition of De-emphasis Levels and Duration



$$DE_{Peak\_dB} = 20Log\left(\frac{V_A}{V_{DC}}\right)$$

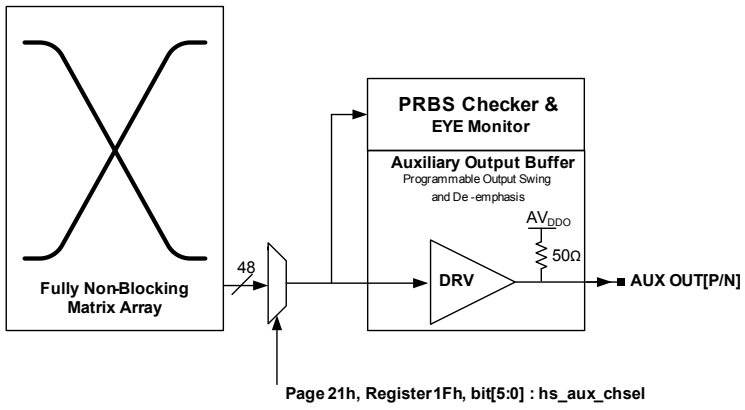
$$V(t) = (V_A - V_{DC}) \times e^{\frac{-t}{\tau_{DE}}} + V_{DC}$$

4.5.3 Auxiliary Output Lane

The M21024/M21036/M21048 have an output lane pin.**OUTP_AUX** and pin.**OUTN_AUX** available. This lane also features the output swing and de-emphasis capabilities as any primary high-speed output lane.

To select which output of the crosspoint the auxiliary output lane will monitor, Page 21h, register.**hs_aux_chsel**.bit[5:0] must be used.

Figure 4-13. Auxiliary Output Buffer



At power up or after a hardware or software reset the auxiliary output lane is powered down by default, to enable the auxiliary output buffer Page 21h, register.**hs_aux_driver**.bit[7] must be set to “1b” and bit [2:1] to "10b".

In order to further control the auxiliary output buffer lane, refer to Page 21h, address 91h:

- Auxiliary Output lane Output swing control, bit[2:1]

- Auxiliary Output lane Output De-emphasis control, bit[6:4]
- Auxiliary Output lane Output De-emphasis time constant control, bit[0]

4.6 Active Switch Configuration (ASC)

There are three methods of changing and/or updating the switching matrix configuration:

- The direct ASC mode by programming the desired switching path registers at page.01h.
- The hardware strobe mode, using pin.**xSET** and selectively loading one of two pre-determined switching maps (ISC1 or ISC2).
- The software strobe mode, using register.**strobe** (page.00h, address.04h) and selectively loading one of two pre-determined switching maps (ISC1 or ISC2).

On power up the ASC is loaded with one of two intermediated switch configuration settings (ISC1 or ISC2). This allows the switch to contain two pre-determined states that become useful for protection switching applications.

4.6.1 Direct ASC Mode (Asynchronous Switching)

In this mode, any input lane can be independently and asynchronously routed to a specific output lane "N". Upon a direct write to the appropriate register.**ascout(N)** (page.01h, address.hex(N)) the new ASC register contents and the new switching configuration map will be immediately asserted, without requiring a hardware or software strobe event.

The device is put in Direct ASC mode by setting pin.**xSET** to LOW and programming register.gen config.bit[5:4] (page.00h, address.03h, bit[5:4]) to 00b.

4.6.2 Hardware Strobe Mode (Synchronous Switching)

The active switching matrix configuration (ASC) may be loaded from any of the two pre-defined configuration registers ISC1 and ISC2 (Intermediate Switch Configuration #1 and #2) located at page.03h and page.05h, respectively, by setting the hardware pin.**CONFIGSEL**:

- Setting pin.**CONFIGSEL** to LOW will transfer the content of the ISC1 to the ASC upon any hardware strobe event.
- Setting pin.**CONFIGSEL** to HIGH will transfer the content of the ISC2 to the ASC upon any hardware strobe event.

To perform the hardware strobe, pin.**xSET** needs to be toggled and the contents of ISC1 or ISC2 will be loaded to the ASC thus performing the synchronous switching.

The device is put in hardware strobe mode by programming register.**gen config**.bit[5:4] (page.00h, address.03h) to 01b. This is also the default setting after any power-up and/or hardware/software reset.

4.6.3 Software Strobe Mode (Synchronous Switching)

In this mode, the ISC register loaded is selected by the strobe register in the global control page. The strobe register is also used to load the value of the selected ISC to the ASC.

- Setting register.strobe[7], Page00h Register 04h to "0b" will transfer the content of the ISC1 to the ASC upon any software strobe event.
- Setting register.strobe[7], Page00h Register 04h to "1b" will transfer the content of the ISC2 to the ASC upon any software strobe event.

To perform the software strobe, set register.**gen config**.bit[6:0] to "55h" and then back to '00h" for normal operation. Upon the strobe, the contents of ISC1 or ISC2 will be loaded to the ASC thus performing the synchronous switching.

The device is put in software strobe mode by programming register.**gen config**.bit[5:4] (page.00h, address.03h) to 10b.

4.7 Junction Temperature Monitor

There are four integrated temperature sensors on the M21024/M21036/M21048, one in each corner of the die. Each sensor has an effective range of approximately -40 °C to +130 °C, stepped in 10 °C increments, with an approximate accuracy of ±10 °C. Sensor configuration is controlled by Page00h.Reg10h and are enabled by default.

The (uncalibrated) readings for the temperature monitor top die corner and bottom die corner sensors are made available in the Page21h.Reg01h and Page21h.Reg02h registers. To increase accuracy of the reading it is recommended to perform a first calibration within the specific environment of the applications. A user provided digital strobe is required to latch the temperature values into the two registers. This is accomplished by the user issuing two consecutive writes to Page00h.Reg10.bit[0]. Two consecutive writes, a “0b” followed by a “1b”, strobes the temperature sensor values into the tempmont and tempmonb registers on the 0-to-1 transition.

Sensor configuration permits an alarm (active low) on pin.**xOVERTEMP** to be activated should the temperature exceed a selected threshold. At power-up the alarm is automatically enabled with a temperature threshold defined with the default value from the tempmon register. The alarm can also be used to automatically shut down the crosspoint output buffers to prevent overheating and possible device damage, using bit 6 of the tempmon register.

4.8 Integrated High-speed PRBS Generator and Checker

The M21048/36/24 has one integrated CDR that requires a reference clock. Since both the PRBS generator and detector requires the use of this CDR, the generator and detector cannot be used at the same time. The CDR has preset settings that allow the designer to have a quick PRBS generator or detector configuration. Please see Page 02h, Address 00h for the list of presets available.

The CDR can also be manually programmed as described in Table 4-3.

Table 4-3. CDR Manual Programming Values

Data Rate Range (Gbps)	Divide Value Page02h, Address 06h, Bit[7:6]	VCO Select Page02h, Address 02, Bit[5]
0.78125 - 1.0625	11b: Divide by 8	0b: VCO Low
1.2375 - 1.375		1b: VCO High
1.5625 - 2.125	10b: Divide by 4	0b: VCO Low
2.475 - 2.75		1b: VCO High
3.125 - 4.25	01b: Divide by 2	0b: VCO Low
4.95 - 5.5		1b: VCO High
6.25 - 8.5	00b: Divide by 1	0b: VCO Low
9.9 - 10.3125		1b: VCO High

Table 4-3 also shows the data rates supported by the CDR. For data rates below 7.5 Gbps, the full temperature range is supported (-40 °C to 85 °C). For data rates above 7.5 Gbps, the CDR can only support -40 °C to 55 °C.

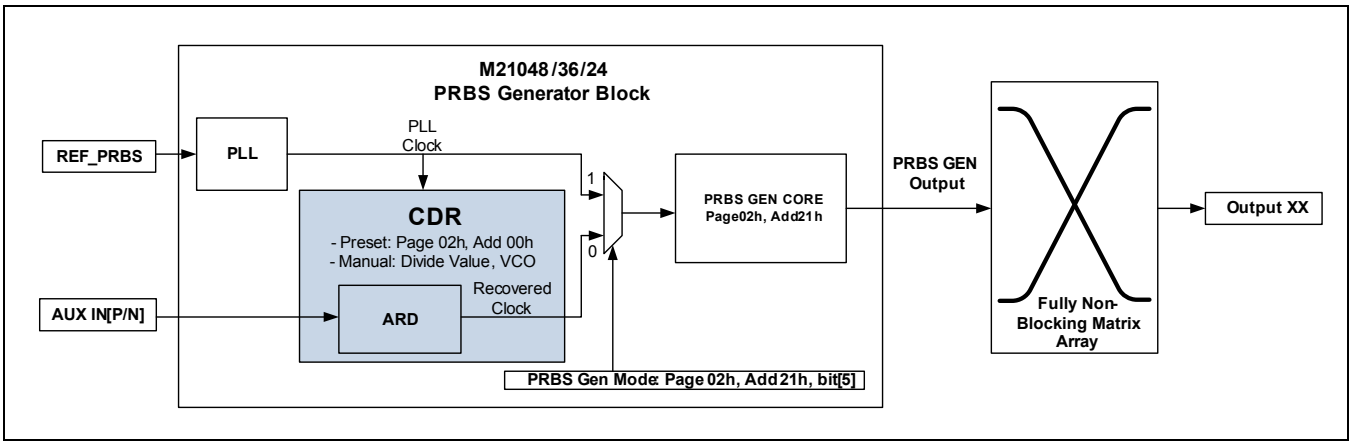
Occasionally upon a re-lock, it can take up to 20 seconds for the data to become error-free. It is recommended to issue a soft reset whenever changing the input signal to the PRBS. It is also highly recommended to write 60h into register 07h in Page 02h for better CDR operation and performance.

4.8.1 Reference Clock

The M21024/36/48 can operate from a crystal or an external reference clock, but better jitter results are obtained with a crystal. The REFP_PRBS (Y20) input must be a 500mVpp to 1200mVpp level signal that is AC coupled. The REFN_PRBS input (ball Y19) should be tied to ground as close to Y19 as possible. The internally biased REFP_PRBS input is high impedance. The standard reference clock frequency 156.25 MHz. For a 4.25Gbps signaling rate, a 125 MHz reference clock frequency is recommended. When supplying an external clock signal a 0.1uF capacitor is recommended.

4.8.2 PRBS Generator

Figure 4-14. PRBS Generator/Auxiliary Input Buffer



The M21024/M21036/M21048 have an integrated PRBS Generator that can be used during system bring-up and optimization. Since the PRBS pattern generation is done at the receiver, the crosspoint core must be programmed to route the PRBS generator to any desired output.

The PRBS generator is designed to be controlled with a total of four controls, all located in the same register. This allows for quick and easy configuration and testing. The first setting is the enable control which is used to power up the generator and mux it into the data path. The enable block is also used to gate the other three settings in the generator. The second and third controls are the pattern select and pattern invert. The PRBS generator has a total of eight different patterns (clock/2, clock/4, clock/8, clock/16, PRBS7, PRBS15, PRBS23 and PRBS31). The final control is the PRBS generator clock source which can either be the CDR PLL or the recovered clock from the input channel.

- PLL or asynchronous mode: In this mode of operation, the PLL clock source is used to generate a PRBS pattern at a rate independent of the system's data rate and is used to help test channels without the need of the rest of the system to be present. In this mode, the data rate is set by the refclock and PLL setting alone. When configured in this mode it is important to disable both the LOS and OOB circuit of the selected input to keep the output from squelching. The ARD registers for the selected input must also be disabled.
- CDR or synchronous mode: In this mode of operation, the recovered clock from the input channel is used when end-to-end channel testing is required. This mode the frequency locks the generator to the input data which allows for easy integration with other PRBS detectors. When the device is configured to use the recovered clock from the input, the CDR PLL needs to be configured to lock to the input rate as is the case in normal operation. The PRBS generator will then track the input signal only replacing the data with the selected pattern.

The PRBS generator is not able to insert bit errors. One method of testing a proper setup is to configure everything as normal and then change the selected pattern. Assuming the system is configured correctly, this will introduce errors. Changing the pattern back to the desired pattern should cause the error to clear, but the detector counters may need to be reset.

4.8.3 Setting the PRBS Generator in PLL Mode at 6.25 Gbps, Application Example

This example uses a 156.25 MHz reference clock and outputs the signal on channel31.

Page Address Data Comment

00 00 AA # GLOBAL RESET

00 00 00 # NORMAL MODE

00 0F 10 # DISABLE REDUNDANCY

00 09 30 # SW ENABLE ALL INPUTS, WITH INDIVIDUAL INPUT/EQ CONTROL (PAGE08/0C)

00 0B 04 # SW ENABLE ALL OUTPUTS, WITH INDIVIDUAL OUTPUT CONTROL (PAGE 0E)

00 03 88 # LANE MODE, DIRECT ASC, ENABLE SMART POWER

01 17 01 # IN1 -> OUT23

01 1F 11 # IN17-> OUT31

0C 01 03 # IN1 EQ

0C 11 03 # IN17 EQ

0E 1F 04 # Out31 Swing to 800mVppd

0E 17 04 # Out23 Swing to 800mVppd

01 1F 30 # PRBS GEN -> OUT31

22 00 80 # PWR UP PRBS GEN/CHECKER

21 0A F8 # SELECT PRBS OUT TO APPLY TO XPT AUX INPUT

21 1F 07 # DIRECT OUT31 TO AUX_OUT

21 91 86 # Power Up Aux_OUT

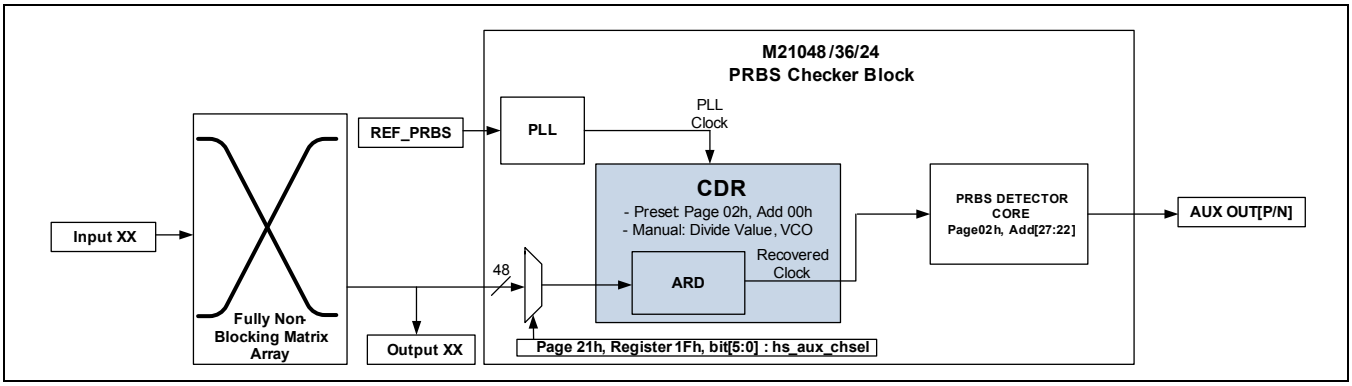
02 00 05 # 6.25Gbps CDR PRESET, 156.25MHZ REFCLK

02 21 3F # GEN PAT PRBS 31, HP polarity

02 06 00 # Divide by 1, After setting Gen pattern to avoid missing the correct divider PRBS Detector

4.8.4 PRBS Detector

Figure 4-15. PRBS Checker Block Diagram



The PRBS detector is designed to be controlled with eight controls located in registers 02h:22-23h. The detector shares the same clock as the generator and can only be operated using the recovered input signal as the phase align is handled by the CDR. There are two modes of operation for the detector: latched and unlatched.

Unlatched operation is used to detect high error rates in a live debug method and uses three controls and one status register. The controls used are detector enable, latch enable, pattern select and pattern invert. The status register is the PRBS status.

Latched operation is used to detect low error rates and system margining. The additional controls used for latched operation are counter length, extended counter length, latch mode and start/done along with the four status counter registers. The counter length and extended counter length are used to select the number of bits that will be compared during a latch interval. The counter length alone will give you full resolution up to 232 bits. When the extended counter is used, the total counter length can be increased to 252, but the error counter is still only 32 bits and will only latch the lower 32 bits of the counter. The extended counter is used to allow deep error scan with low error rates. The latch mode is used to select between latch on error or latch on error-free. The final control is the start/done control and is used to start the error detector window. The detector is started by writing a 1 to start/done control. The control will always return a 0 unless the limit is reached. The PRBS detector is enabled by selecting the latch mode and writing the start bit. The results of the detector can be read from the error count registers. The LOL alarms are used to indicate whether the PRBS detector has locked on to the data pattern.

4.8.5 Setting the PRBS Detector in PLL Mode at 6.25 Gbps, Application Example

This example uses a 156.25 MHz reference clock and outputs the signal on channel31.

Page Address DataComment

00 00 AA # GLOBAL RESET

00 00 00 # NORMAL MODE

00 0F 10 # DISABLE REDUNDANCY

00 09 30 # SW ENABLE ALL INPUTS, WITH INDIVIDUAL INPUT/EQ CONTROL (PAGE 08/0C)

```
00 0B 04        # SW ENABLE ALL OUTPUTS, WITH INDIVIDUAL OUTPUT CONTROL (PAGE 0E)
00 03 88        # LANE MODE, DIRECT ASC, ENABLE SMART POWER
02 00 05        # KR ONLY CDR PRESET FOR 156.25MHZ REFCLK
21 0A F0        # SELECT AUX INPUT to apply to xpt
21 80 1E        # ENABLE AUX IN EQ
21 84 03        # SET AUX IN EQ TO 03
21 81 00        # DISABLE EI PASSTHRU
21 82 38        # DISABLE LOS
21 83 30        # INPUT TERMINATION
01 1F 30        # SELECT AUX INPUT TO OUT31
21 1F 07        # DIRECT OUT31 TO AUX OUT and PRBS Checker
21 91 84        # AUX OUT 800MV SWING, NO DE
22 00 80        # PWR UP PRBS GEN/CHECKER
02 21 00        # PAT GEN DISABLED
02 22 1F        # DETECT PAT PRBS 31, HP Polarity
02 23 F1        # LATCH MODE, START
```

To read the bit errors, please refer to Page 02h Address [27:24].

4.9 Software Interfaces

The registers of the M21024/M21036/M21048 can be configured through three different control interfaces:

1. A 2-wire serial interface operational at the standard data rates of 100 kHz, 400 kHz, and 3.4 MHz.
2. A 4-wire serial interface operational up to 100 MHz for register writes and up to 25 MHz for register reads.
3. A parallel 8-bit address, 8-bit data interface operational up to 100 MHz for register writes and up to 25 MHz for register reads.

Both serial modes support sequential block writes within a page. After the first register write, each additional byte of data is automatically written into the next consecutive register address (burst mode). Burst mode allows all register pages including ISC#1 or ISC#2 pages to be programmed rapidly without the need to precede each data field with an address field.

In general, pin.**DV_{DDO}** should share the same power supply as the host controllers. The M21024/M21036/M21048 can support host controller voltages from 1.2 V to 3.3 V.

From a control perspective, the registers are defined to allow a select number of parameters to be configured individually or globally. With the global option, selection of a feature will apply to all lanes of the part. If the individual option is selected, then each lane or group can be configured individually.

The selection of the control interface (2-wire serial, 4-wire serial, or parallel register interface) to the M21024/M21036/M21048 is enabled and selected with pin.**CONFIG0**, pin.**CONFIG1** and pin.**TRST**, which define the function of pin.**MF[11:0]** as summarized in Table 4-4 below.

The interface selection is latched upon the power-up reset of the part and can't be changed during operation, including software reset. The physical logic level of the control interface (and all low speed digital pins in general) is determined by supply pin.**DV_{DDO}**. For optimal performance, the supply **DV_{DDO}** of the M21024/M21036/M21048 should be connected to the same supply level as the host controller which can vary from 1.2 V to 3.3 V.

In the section below, the pins of the selected interface will refer to the pin by the assigned name in quotes. For example, pin.**MF0** for the 2-wire serial interface will be called "**SCL**".

Table 4-4. Digital Mode Control

Control Pins	Multi-function Pin Name	Pin Location M21024	Pin Location M21036	Pin Location M21048	Control Selected interface				Termination
					2-wire	4-wire	Parallel	JTAG	
CONFIG0		T7	T8	V8	0	1	0	X	pull down[1]
CONFIG1		R7	U6	W8	0	0	1	X	pull down[1]
TRST		E6	E5	D5	0	0	0	1	pull down[1]
	MF11	D5	C3	E4				TCK	pull-up[1]
	MF10	E14	G16	J19			R_xW		high-Z
	MF9	E15	E18	G18		xCS	xCS		high-Z
	MF8	F15	G17	J20	Addr6		A7/D7		high-Z
	MF7	F16	F17	G19	Addr5		A6/D6		high-Z
	MF6	E17	C20	D23	Addr4		A5/D5		high-Z
	MF5	F17	E19	H20	Addr3		A4/D4		high-Z
	MF4	D16	A21	D22	Addr2		A3/D3		high-Z
	MF3	E16	D19	G20	Addr1		A2/D2		high-Z
	MF2	D14	F16	E23	Addr0	SI	A1/D1		high-Z
	MF1	D15	D18	H19	SDA	SO	A0/D0		high-Z
	MF0	D17	B21	E22	SCL	SCLK	CLOCK		high-Z

NOTE:

1. Pull-up/pull-down resistance is an internal 100 kΩ to DV_{DDO} or V_{SS}.

4.9.1 2-wire Serial Digital Interface

The 2-wire slave mode is selected with pin.**TRST**=L, pin.**CONFIG0**=L and pin.**CONFIG1**=L. Each device has an individual address. The device address is determined with Addr[6:0] and it is latched upon power-up reset. In this mode, the M21024/M21036/M21048 is a two-wire slave device that can operate at 100 kHz, 400 kHz, and 3.4 MHz for all allowed voltages seen at pin.**DV_{DDO}**. The pins can drive 500 pF at 100 kHz and 400 kHz, also 100 pF at 3.4 MHz. Figure 4-16 illustrates typical waveforms and timing seen at "**SCL**", "**SDA**" for a Read and Write operation.

Figure 4-16. 2-wire Read and Write Operation Timing Diagram

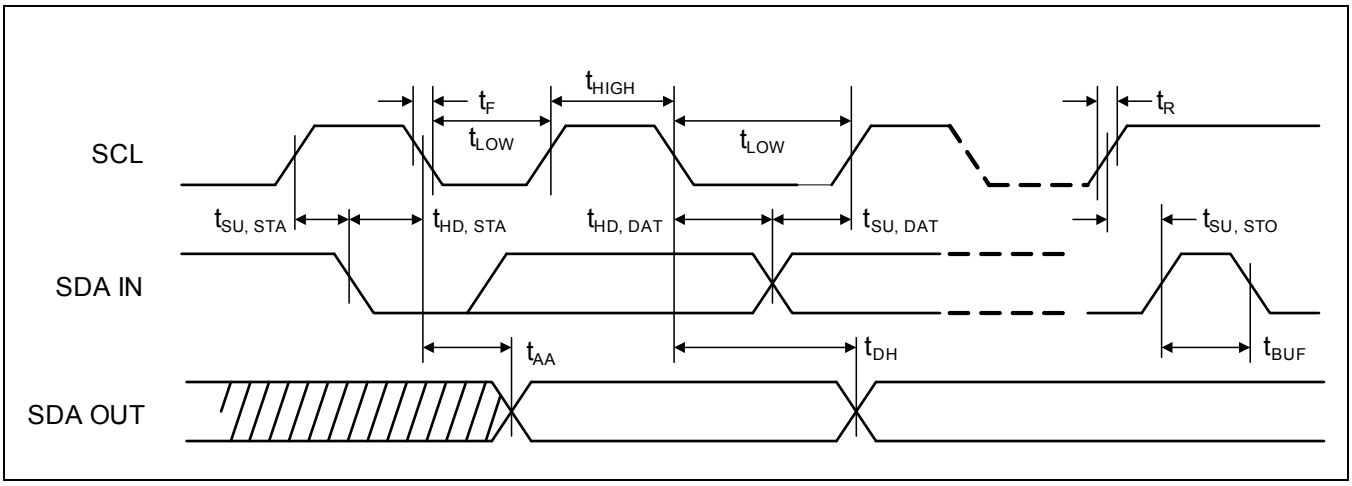


Table 4-5. 2-wire Serial Interface Specifications

Timing Symbol	Description	Standard-Fast Mode			High-Speed Mode			Units
		Min	Typ	Max	Min	Typ	Max	
F_{SCL}	Clock Frequency, SCL	—	—	0.4	—	—	3.4	MHz
t_{AA}	Clock Low to Data Out Valid	50	—	900	0	—	70	ns
t_{DH}	Data Out Hold Time	50	—	—	5	—	—	ns
t_{HDDAT}	Data In Hold Time	0	—	—	0	—	—	ns
t_{HDSTA}	Start Hold Time	200	—	—	160	—	—	ns
t_{HIGH}	Clock Pulse Width High	600	—	—	60	—	—	ns
t_{LOW}	Clock Pulse Width Low	1300	—	—	160	—	—	ns
t_{SUDAT}	Data In Set-up Time	100	—	—	10	—	—	ns
t_{SUSTA}	Start Set-up Time	200	—	—	160	—	—	ns
t_{SUSTO}	Stop Set-up Time	200	—	—	160	—	—	ns

4.9.2 4-wire Serial Digital Interface

The 4-wire serial interface is selected with pin.**TRST**=L, pin.**CONFIG0**=H and pin.**CONFIG1**=L.

The interface shifts data in from the external controller on the rising edge of "**SCLK**". The serial I/O operation is gated by "**xCS.**" Data is shifted to the M21024/M21036/M21048 from the Host (Master) on "**SI**" on the falling edge of "**SCLK**," and shifted out through "**SO**" on the rising edge of "**SCLK**." To address a register, a 10-bit input needs to be shifted, consisting of the first bit (Start Bit, SB = 1), the second bit (Operation Bit, OP = 1 for read, = 0 for write), and the 8-bit address (MSB first).

Figure 4-17. 4-wire Serial Digital Interface

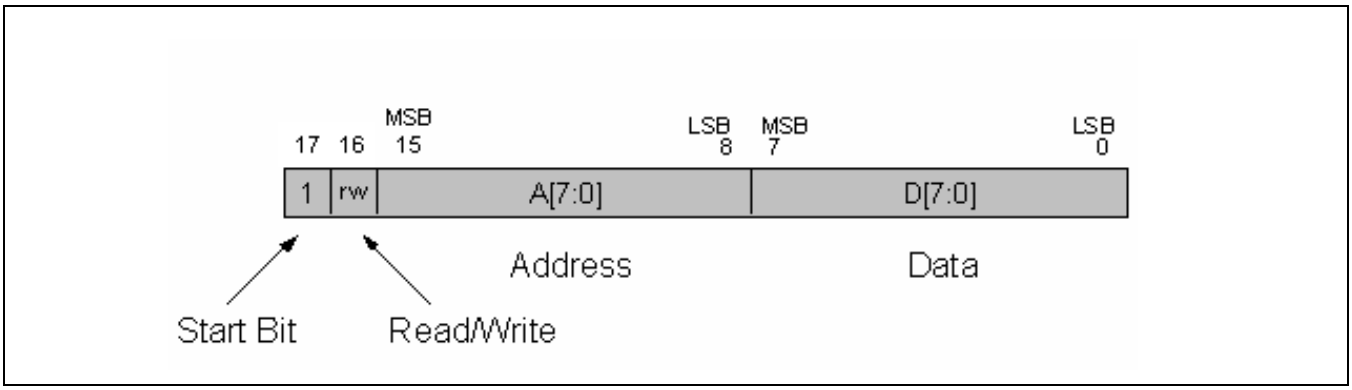


Figure 4-18 and Figure 4-19 illustrate the Serial Write Mode. To initiate a Write sequence, "**xCS**" goes low before the falling edge of "**SCLK.**" On each falling edge of the clock, the 18 bits consisting of the SB = 1, OP = 0, ADDR, and DATA, are latched into the input shift register through "**SI.**" The rising edge of "**xCS**" must occur before the falling edge of "**SCLK**" for the last bit. Upon receipt of the last bit, one additional cycle of "**SCLK**" is necessary before DATA transfers from the input shift register to the addressed register.

The 4-wire serial interface supports multiple consecutive writes. In this case, the address header is not needed and each additional 8 bits of data will be written into consecutive addresses. If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the last read/write cycle.

Figure 4-20 and Figure 4-21 illustrate the Serial Read mode to initiate a read sequence. "**xCS**" goes low before the falling edge of "**SCLK.**" On each falling edge of "**SCLK**", the 10 bits consisting of SB = 1, OP = 1, and the 8-bit ADDR are written to the serial input shift register and copied to the serial output shift register. On the next rising edge after the address LSB, the SB and 8 bits of the DATA are shifted out. On a Write cycle, any bits that follow the expected number of bits are ignored, and only the first 15 bits following SB and OP are used. On a Read cycle, any extra clock cycles will result in the repeat of the data LSB. An invalid SB or OP renders the operation undefined. The falling edge of "**xCS**" always resets the serial operation for a new Read or Write cycle.

Figure 4-18. 4-wire Serial Sequential WRITE Timing Diagram

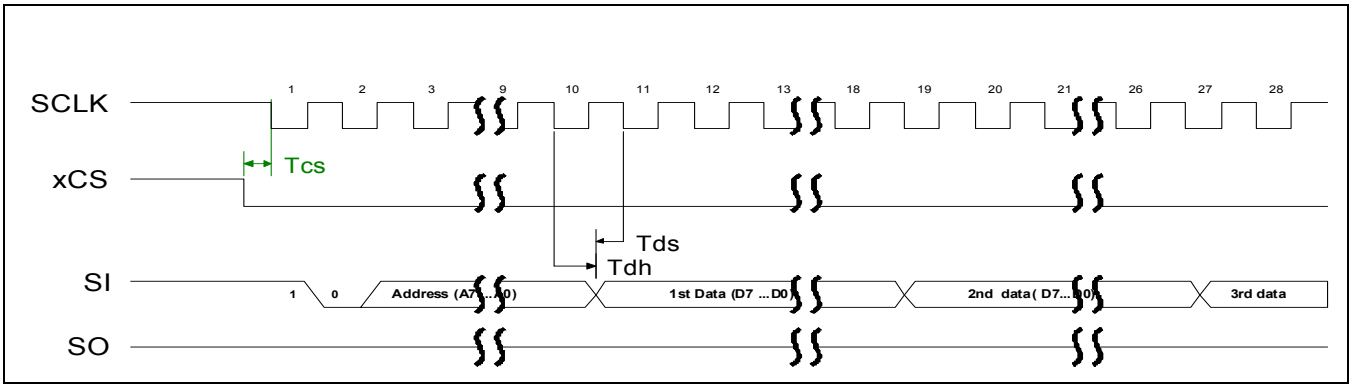


Figure 4-19. 4-wire Random WRITE Timing Diagram

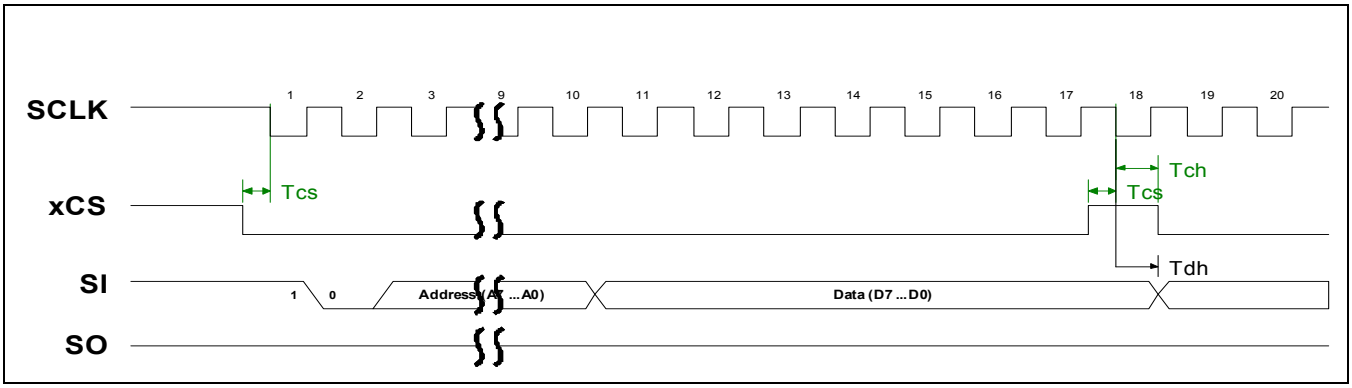


Figure 4-20. 4-wire Sequential READ Timing Diagram

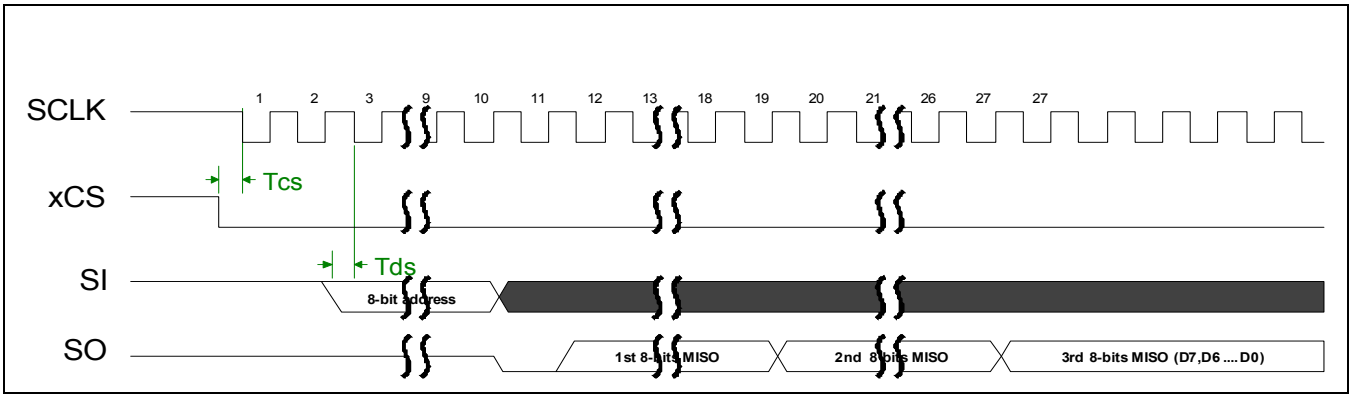


Figure 4-21. 4-wire Random READ Timing Diagram

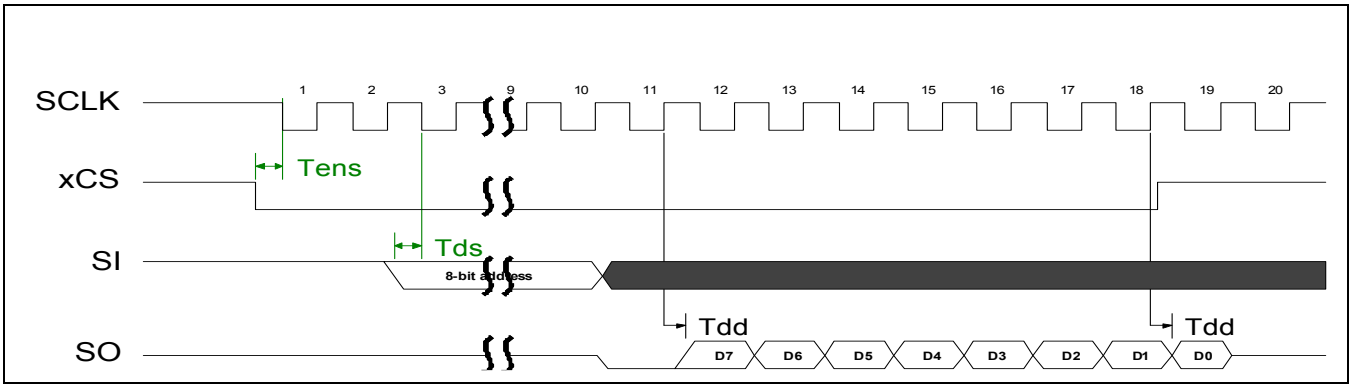


Table 4-6. 4-wire Serial Interface Specifications

Timing Symbol	Description	Min	Typ	Max	Unit
Tds	Data set-up time	2	—	—	ns
Tdh	Data hold time	2.5	—	—	ns
Tcs	xCS set-up time	2	—	—	ns
Tch	xCS hold time	2.5	—	—	ns
Tdd	Read data output delay (for max load capacitor 30 pF and DV_{DDO}@3.3 V)	2	—	16	ns

4.9.3 Parallel Digital Interface

The 8-bit data and 8-bit address parallel interface is selected with pin.**TRST**=L, pin.**CONFIG0**=L and pin.**CONFIG1**=H. "**D[7:0]**" represents the 8 bits of data or "**A[7:0]**" represents the 8 bits of address that share the same pins. The parallel programming interface supports a single address read operation mode and three different write operation modes. The three different write operations enable the user to program a single register address (Single Write Mode), multiple random register addresses (Multiple Write Mode), or multiple consecutive register addresses (Burst Write Mode) in one write cycle. For all read and write operations, "**xCS**" must be low before the "**CLOCK**" rising edge to initiate the sequence and latch the address for the read or write cycle. "**R_xW**"= H during a read cycle and "**R_xW**"= L during a write cycle, and the address is latched on the "**CLOCK**" rising edge. The interface supports clock rates up to 100 MHz for write operations and clock rates up to 25 MHz for read operations.

Figure 4-22 illustrates waveforms and timing for a single read operation. During a read cycle, the read data will be output on the "next" falling "**CLOCK**" edge after the address is latched, and will be asserted on the Addr/Data bus after a propagation time of T_{driver}. and then the Addr/Data bus will stop driving the bus and "**xCS**" should be set H to complete the read operation.

Figure 4-22. Parallel Single Read Timing Diagram

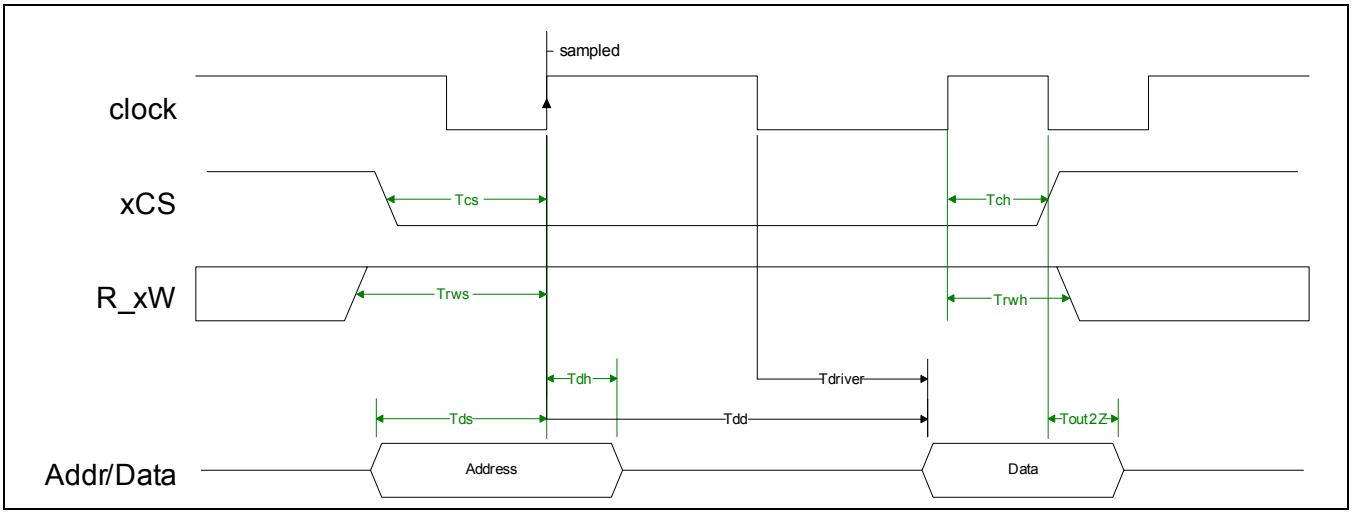


Figure 4-23 illustrates waveforms and timing for a single write operation. During a single write operation, the "**xCS**" pin and "**R_xW**" pin must be set L before the rising "**CLOCK**" edge to initiate the sequence. The target address is latched on the first rising "**CLOCK**" edge and the data for the target address is latched on the next rising "**CLOCK**" edge. After the data is latched, the "**xCS**" pin and "**R_xW**" pin should be set H to complete the single write operation.

Figure 4-23. Parallel Single Write Timing Diagram

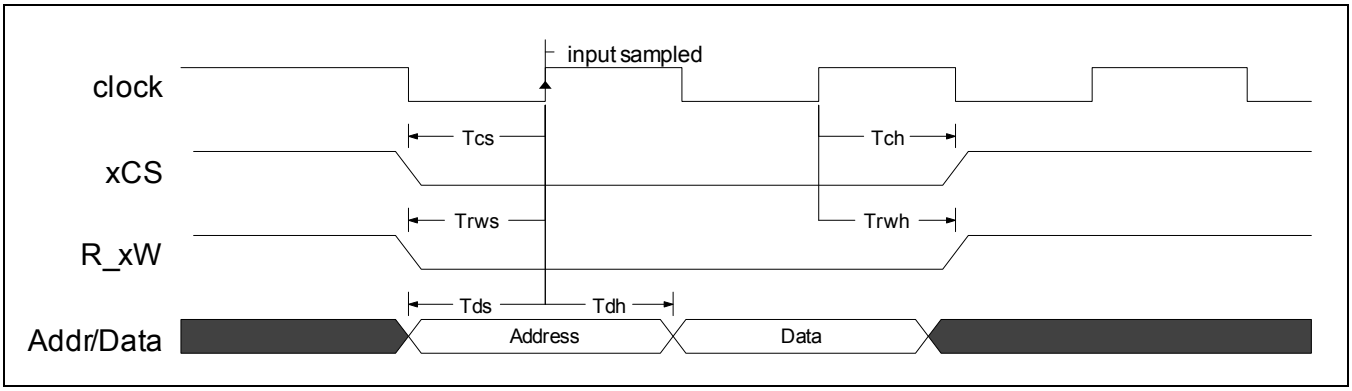


Figure 4-24 illustrates waveforms and timing for a multiple write operation, where several device addresses are changed in one sequence. During a multiple write operation, the "**xCS**" pin and "**R_xW**" pin must be set L before the rising "**CLOCK**" edge to initiate the sequence. The first target address is latched on the first rising "**CLOCK**" edge and the data for the target address is latched on the next rising "**CLOCK**" edge. Additional registers can be written to by changing the target address and data values before each subsequent rising "**CLOCK**" edge as long as he "**xCS**" pin and "**R_xW**" pins are held L. Note that it takes two clock cycles for each register write, one cycle to latch the target address and one cycle to latch the data. After the data is latched on the last target address, the "**xCS**" pin and "**R_xW**" pin should be set H to complete the multiple write operation.

Figure 4-24. Parallel Multiple Write Timing Diagram

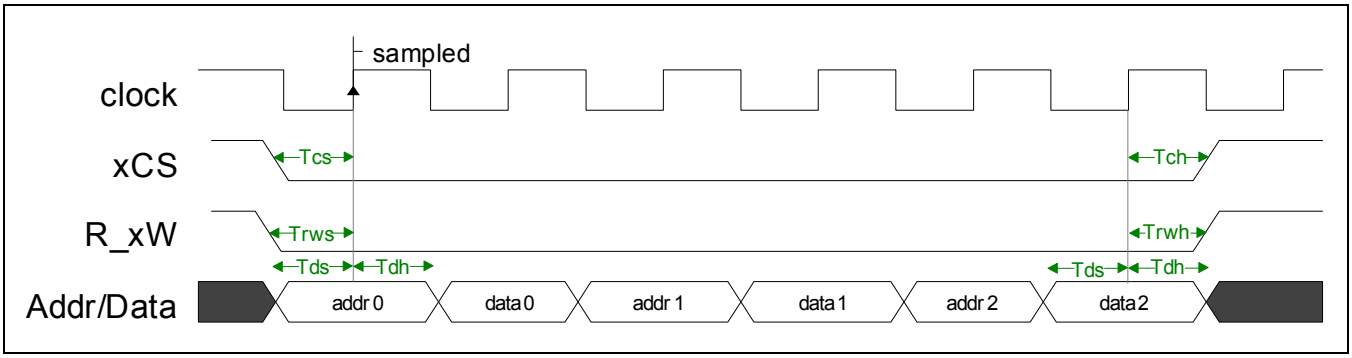


Figure 4-25 illustrates waveforms and timing for a burst write operation, where several consecutive device addresses are changed in one sequence. During a burst write operation, the "**xCS**" pin and "**R_xW**" pin must be set L before the rising "**CLOCK**" edge to initiate the sequence. The Addr/Data bust must be set to a value of FEh before the first rising "**CLOCK**" edge to configure the parallel interface for burst write programming. The Addr/Data bus must be set to the desired register page value before the second rising "**CLOCK**" edge, followed by the starting target address on the next rising "**CLOCK**" edge. On each following rising "**CLOCK**" edge, the value on the Addr/Data bus will be written into sequential device addresses until the burst write operation is complete. The burst write sequence will be complete when either the "**xCS**" pin is set H or the target address reaches a value of FFh. For most pages, the address is mapped to the device input or output lane/group number. Burst write mode is designed to quickly program entire continuous pages such as ISC#1 and ISC#2 to allow the crosspoint to quickly change states. In the parallel mode with the clock running at 100 MHz, 48 lanes can be programmed with 51 clock cycles for data resulting in a 510 ns configuration time.

Figure 4-25. Parallel Burst Write Timing Diagram

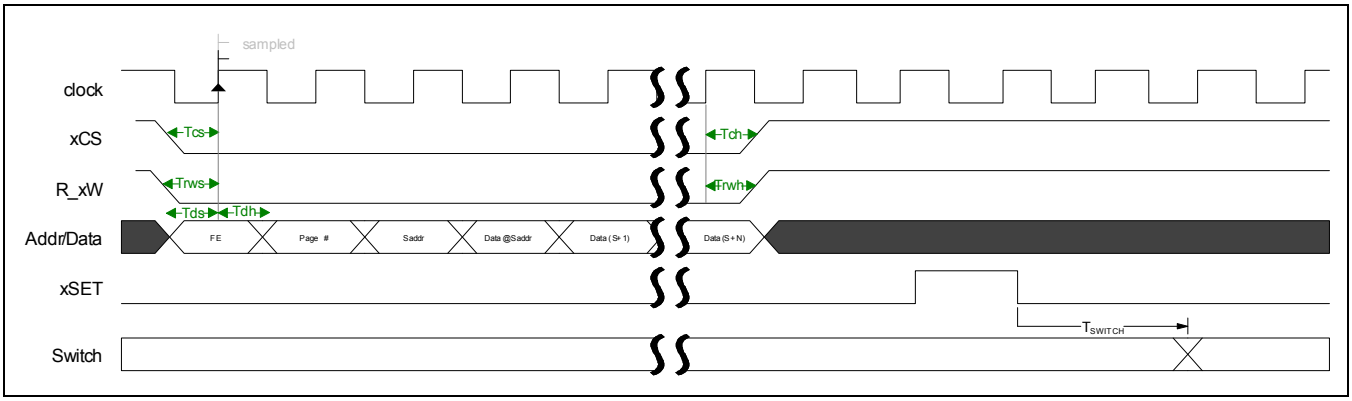


Table 4-7. Parallel Interface Specifications

Timing Symbol	Description	Min	Typ	Max	Unit
Tds	Data/address set-up time	1.5	—	—	ns
Tdh	Data/address Hold time	3.5	—	—	ns
Tcs	xCS Set-up time	1.5	—	—	ns
Tch	xCS Hold time/	3.5	—	—	ns
Trws	R_xW set up time	1.5	—	—	ns
Trwh	R_xW Hold time	3.5	—	—	ns
Tdd	Read data output delay	—	—	33	ns
Tout2Z	Read Data output delay to end	1	—	6	ns
Tdriver	Read data output delay to valid	1	—	—	ns

NOTE:

1. In read mode the parallel outputs are specified for a maximum load capacitor of 30 pF and DV_{DDO} at 3.3 V.

4.9.4 JTAG

The M21024/M21036/M21048 may be configured in the scan mode that can support JTAG (for customer applications) and ATPG test scan (for MACOM testing). JTAG mode is enabled with pin.**TRST**=H.

Typical JTAG operation can be performed using pin.**TDI**, pin.**TDO** and pin.**TMS**. The JTAG clock can be applied to pin.**MF11** or “TCK”.

For further information, consult your local sales resource.

4.9.5 EEPROM Download

The M21024/M21036/M21048 has the capability of optionally loading code from an external EEPROM (AT24C04B). Interfacing the M21024/M21036/M21048 with the EEPROM is achieved using pin.**MSDA** (bidirectional input receiving and sending data from/to the AT24C04B) and pin.**MSCL** (open drain output). Initiating a download sequence is achieved by setting pin.**EEPROM_SEL** high, or setting pin.**EEPROM_SEL** low and writing Page00h.Reg72h[1]. Whenever a download sequence (or re-download) is requested the M21024/M21036/M21048 will first issue the protocol reset required for the Atmel EEPROM. Then the M21024/M21036/M21048 initiates a sequence read command and generates a 400 kHz (maximum speed) clock at pin.**MSCL** to the external AT24C04B, starting at register.00h (at page 0 of AT24C04B) and ending at register.7Fh (at page 1 of AT24C04B). The 400 bytes from the external EEPROM are loaded sequentially to the M21024/M21036/M21048 at page.07h, page.00h, page.01h, page.03h, page.05h, page.08h, page.0Ah, page.0Ch, page.0Eh and page.02h. The mapping from AT24C04B to the M21024/M21036/M21048 is indicated in Table 4-8.

NOTE: at power on, hold the hardware reset pin LOW for a minimum of 10 µs after all supplies (include EEPROM supply) stabilize (95% of setting point) and before writing or reading any data from/to digital interfaces.

Table 4-8. Register Mapping from AT24C04B to M21048/M21036/M21024

AT24C04B Address	M21048 Address
Page 0,	
00h to 01h	Page.07h, 00h to 01h
02h to 0Fh	Page.00h, 03h to 10h
10h to 3Fh	Page.01h, 00h to 2Fh
40h to 6Fh	Page.03h, 00h to 2Fh
70h to 9Fh	Page.05h, 00h to 2Fh
A0h to CFh	Page.08h, 00h to 2Fh
D0h to FFh	Page.0Ah, 00h to 2Fh
Page 1,	
00h to 2Fh	Page.0Ch, 00h to 2Fh
30h to 5Fh	Page.0Eh, 00h to 2Fh
60h to 8Fh	Page.02h, 00h to 2Fh

5.0 Control Register Descriptions

Table 5-1. Register Summary

Page	Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	FFh	pagesel	Page Select								00'h	R/W
00h	00h	master reset	reset								00'h	R/W
00h	01h	ChipCode	chipcode								00'h	R
00h	02h	rev code	rev code								na	R
00h	03h	gen config	lane/group		strobe_sel		smartpwr_en	fe_smartpwr_en	Reserved	standby	18'h	R/W
00h	04h	strobe	isc_sel	setting							00'h	R/W
00h	05h	squelch	squelch mode		Reserved			squelch level		Reserved	86'h	R/W
00h	06h	ei config	gbl_EI_en		en_EI_mon	en_los_mon	gbl_EI_fe		gbl_EI_degl	Reserved	80'h	R/W
00h	07h	monchansel	mon_chan								00'h	R/W
00h	08h	losconfig	LOS enable		LOS threshold			Reserved	LOS delay	Reserved	C0'h	R/W
00h	09h	gbinbuf	gbl_inbuf_sel	gbl_eqlvl_sel	gbl_inbuf		sw_xinen	Reserved			F0'h	R/W
00h	0Ah	inputeq	Reserved			eq level					00'h	R/W
00h	0Bh	outputbuf	gbl_out_bufsel	gbl_outde_lvl			sw_xouten	gbl_out_lvl		out_de_freq	84'h	R/W
00h	0Ch	grpchas	gblch		Reserved						C0'h	R/W
00h	0Fh	asc_ctrl	Reserved			fallback	xor_with_m3	xor_with_m2	xor_with_m1	xor_with_m0	00'h	R/W
00h	10h	tempmon	dis_xovertemp	xovertemp_out_dis	xovertemp_pol	jtemp_alarm_th			en_temp_mon	strobe_temp	1E'h	R/W
00h	40h-45h : 01h	LOS alarm(M)	lane (8M+7)	lane (8M+6)	lane(8M+5)	lane (8M+4)	lane (8M+3)	lane (8M+2)	lane (8M+1)	lane (8M+0)	00'h	R/W
00h	50h-55h : 01h	stat alarm(M)	lane (8M+7)	lane (8M+6)	lane(8M+5)	lane (8M+4)	lane (8M+3)	lane (8M+2)	lane (8M+1)	lane (8M+0)	na	R
00h	60h-65h : 01h	mask alarm(M)	lane (8M+7)	lane (8M+6)	lane(8M+5)	lane (8M+4)	lane (8M+3)	lane (8M+2)	lane (8M+1)	lane (8M+0)	00'h	R/W
01h	00h-2Eh : 01h	ascout(N)	ascout								00'h	R/W
02h	00h	CDR Preset	Preset								00'h	R/W
02h	01h	CDR: PLL Divide Ratio	div2 enable	div ratio							00'h	R/W
02h	02h	CDR: PLL Control	quad pd	vco over-ride	vco select	lbw over-ride	PLL LBW		Reserved		00'h	R/W
02h	03h	CDR: Interrupt Mask	PLL LOL Mask	LOR Mask	Reserved		PRBS Mask	Reserved		LOL Mask	08'h	R/W
02h	04h	CDR: CRU Control A	leak override	LOL Limits				leak gain			00'h	R/W
02h	05h	CDR: CRU Control B	peaking				lbw				00'h	R/W
02h	06h	CDR: ARD Control	Divide Value		ARD Disable	Range over-ride	Div8_Valid	Div4_Valid	Div2_valid	Div1_valid	00'h	R/W
02h	07h	CDR: EQ Control	CH pd	scaling_override	peak_scaling	soft reset	unused	unused			00'h	R/W
02h	08h	Reserved	Reserved								03'h	R/W
02h	09h	Reserved	Reserved								00'h	R/W
02h	0Ah	Reserved	Reserved								00'h	R/W
02h	0Bh	Reserved	Reserved								00'h	R/W
02h	0Ch	Reserved	Reserved								00'h	R/W
02h	0Dh	Reserved	Reserved								00'h	R/W
02h	0Eh	Reserved	Reserved								00'h	R/W
02h	0Fh	Reserved	Reserved								10'h	R/W
02h	10h	Reserved	Reserved								00'h	R
02h	11h	Reserved	Reserved								00'h	R

Table 5-1. Register Summary

Page	Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
02h	12h	Reserved	Reserved								00'h	R
02h	13h	Reserved	Reserved								00'h	R
02h	14h	Reserved	Reserved								00'h	R
02h	15h	Reserved	Reserved								00'h	R
02h	16h	Reserved	Reserved								00'h	R
02h	17h	Reserved	Reserved								00'h	R
02h	18h	CDR: ARD Control 2	LOL_CRU	LOL_ARD	ARD_LEN		Single Threshold		pattern		00'h	R/W
02h	19h	CDR: Gain Value	Reserved	gain value							7F'h	R/W
02h	1Ah	Reserved	Reserved	Reserved							40'h	R/W
02h	1Bh	Reserved	Reserved	Reserved							40'h	R/W
02h	1Ch	Reserved	Reserved	Reserved							40'h	R/W
02h	1Dh	Reserved	Reserved	Reserved							40'h	R/W
02h	1Eh	Reserved	Reserved								00'h	R/W
02h	1Fh	Reserved	Reserved		Reserved						20'h	R/W
02h	20h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00'h	R/W
02h	21h	CDR : PRBS Gen	Reserved		PRBS Mode	enable	pattern invert	pattern			00'h	R/W
02h	22h	CDR: PRBS Detector Control	len			enable	pattern invert	pattern			00'h	R/W
02h	23h	CDR: PRBS Detector Status	Latch Enable	Extended Length			Reserved		Latch Error	full/start	00'h	R/W
02h	24h	CDR: PRBS Error Count 0	count								00'h	R
02h	25h	CDR : PRBS Error Count 1	count								00'h	R
02h	26h	CDR : PRBS Error Count 2	count								00'h	R
02h	27h	CDR : PRBS Error Count 3	count								00'h	R
02h	48h	CDR : CDR Status	PLL_LOL	LOR	Reserved	PRBS	Reserved		LOL	Reserved	00'h	R
02h	49h	CDR : CDR Delta	PLL_LOL Delta	LOR Delta	Reserved	PRBS Delta	Reserved		LOL Delta	Reserved	00'h	R
03h	00h	isc1out(N)	iscout								00'h	R/W
05h	00h	iscout2(N)	iscout								00'h	R/W
07h	00h	grpmapIn0	grp_map7	grp_map6	grp_map5	grp_map4	grp_map3	grp_map2	grp_map1	grp_map0	FF'h	R/W
07h	01h	grpmapIn1	Reserved				grp_map11	grp_map10	grp_map9	grp_map8	FF'h	R/W
08h	00h-2Fh : 01h	inbufctrl(N)	inbuf_en		losen	ebi_en	squelch		sq_level		EB'h	R/W
0Ah	00h-2Fh : 01h	inthresh(N)	los_thresh			oob_back_end	Reserved			polflip	01'h	R/W
0Ch	00h-2Fh : 01h	InEQ0	Reserved			eq level					00'h	R/W
0Eh	00h-2Fh : 01h	outbuf0	Reserved	outde_lvl			Reserved	out_lvl		outde_freq	04'h	R/W
21h	01h	tempmont	temp_tl				temp_tr				na	R
21h	02h	tempmonb	temp_bl				temp_br				na	R
21h	08h	fe_debug0	unused	los_hysteresis_dis	pd_dcd_dig_eq	en_dcd_ana_eq	pd_dcd_dig_la	en_dcd_ana_la	la_dcd_gain	eq_dcd_gain	00'h	R/W
21h	09h	fe_debug1	unused	pd_hys_oob0	Reserved				unused	Reserved	00'h	R/W
21h	0Ah	out_debug0	pd_dcd_dig_out	en_dcd_ana_out	pd_dcd_dig_xpt	en_dcd_ana_xpt	test_insel	pd_afe_test	unused		F4'h	R/W
21h	0Bh	fe_debug2	Reserved					oob_vcm_dac			13'h	R/W
21h	1Fh	hs_aux_chsel	hs_aux_en		chsel						3F'h	R/W
21h	80h	hs_aux_squelch	Reserved		cht_oob_vcm_dac			cht_sq_level		cht_dis	1F'h	R/W
21h	81h	hs_aux_ei	Reserved	ebi_en	Reserved		ebi_fe	Reserved	gbl_ebi_degl	unused	00'h	R/W
21h	82h	hs_aux_los	Reserved	LOS enable	LOS threshold			LOS cal force	LOS delay	Reserved	38'h	R/W
21h	83h	hs_aux_term	Reserved		cht_gbl_inbuf		Reserved				00'h	R/W
21h	84h	hs_aux_eq	Reserved			cht_eq_level					00'h	R/W
21h	91h	hs_aux_driver	testout_en_cur	outde_lvl			Reserved	out_lvl		OutDE_freq	00'h	R/W

Table 5-1. Register Summary

Page	Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
21h	A0h	dvddo_drv	Reserved				drv_mon	Reserved	force_high_low		00'h	R/W
22h	00h	Aux Input channel config_reg1	en_gen_check	unused	Reserved		unused	Reserved			00'h	R/W
24h	00h	reserved	Reserved								00'h	R/W

5.1 Page 00h

Page: 00h
Address: FFh
Register Name: pagesel
Default Value: 00'h
Description: Determines the active register page selection. The FFh address is unique in that it references the same register, irrespective of page selection.

Bit(s)	Name	Description	Default	Type
[7:0]	Page Select	00000000b: Global Configuration page [default] 00000001b: Crosspoint Active Switch Configuration (ASC) Page 00000010b: PRBS Pattern Generator/Checker Configuration Page 00000011b: Crosspoint Intermediate Switch Configuration #1 (ISC1) Page 00000101b: Crosspoint Intermediate Switch Configuration #2 (ISC2) Page 00000111b: Intra-Group Switching: Group Mapping 00001000b: Individual Input Buffer Configuration 00001010b: Individual Input Buffer LOS Configuration 00001100b: Individual Input Buffer Equalization Configuration 00001110b: Individual Output Buffer Configuration 00100001b: Temperature Monitor & Auxiliary Lane Configuration 00100010b: PRBS Pattern Generator/Checker Enable	00000000b	R/W

Page: 00h
Address: 00h
Register Name: master reset
Default Value: 00'h
Description: Global reset. Resets all registers to default value.

Bit(s)	Name	Description	Default	Type
[7:0]	reset	00000000b: Normal operation 10101010b: Assert global reset	00000000b	R/W

Page: 00h
Address: 01h
Register Name: ChipCode
Default Value:
Description: Product identification code.

Bit(s)	Name	Description	Default	Type
[7:0]	chipcode	M21048 (48x48) M21036 (36x36) M21024 (24x24)	00101100b 00111100b 00101101b	R

Page: 00h
Address: 02h
Register Name: rev code
Default Value: 00'h
Description: Product revision code

Bit(s)	Name	Description	Default	Type
[7:0]	rev code	Revision code M21048/36/24	00000001b	R

Page: 00h
Address: 03h
Register Name: gen config
Default Value: 18'h
Description: General configuration register.

Bit(s)	Name	Description	Default	Type
[7:6]	lane/group	Lane mode assigns each channel to a lane (e.g. M21048 has 48 individual lanes) Group mode assigns 4 channels to a group (e.g. M21048 has 12 individual groups) After selection, many of the registers (I/O, switch state, etc), address and associated data is mapped to either lanes or group. 00b: Lane/group mode selected with hardware pin.**GRPLNMODE** 01b: Register selection group mode (4 channels to a group) 10b: Register selection lane mode (1 channel to a lane) 11b: Undefined	00b	R/W
[5:4]	strobe_sel	Determines if the switch state update strobe will be determined with registers or hardware pins (It is recommended to set pin.xSET=L before setting these two bits) 00b: Direct ASC mode. Update switch configuration on each ASC register write 01b: Hardware strobe ASC mode. Update switch configuration with pin.**xSET** and choose ISC with pin.**CONFIGSEL** 10b: Software strobe ASC mode. Update switch configuration on write to register.**strobe**.bit[6:0] address.04h 11b: Undefined	01b	R/W
[3]	smartpwr_en	Enables automatically shut down unused paths within the core to reduce overall power dissipation 0b: Disable smart power 1b: Enable smart power	1b	R/W
[2]	fe_smartpwr_en	Front End power status. Unused lanes (from cross-point programming) are automatically powered down. 0b: Unused lanes are not powered down 1b: Unused lanes are automatically powered down	0b	R/W
[1]	Reserved	Reserved	0b	R/W
[0]	standby	0b: Power-up the device 1b: Power-down and enter the device in standby mode	0b	R/W

NOTES:

1. When the front end offset correction loops are enabled, setting fe_smartpwr_en to 1 will increase the time needed to reconfigure the switch.

Page: 00h
Address: 04h
Register Name: strobe
Default Value: 00'h
Description: Strobe ASC strobe and control register.

Bit(s)	Name	Description	Default	Type
[7]	isc_sel	Register ISC1/ISC2 selection (enabled with GenConfig[5]=1b) 0b: Selects ISC1 as the active state to become ASC upon strobe 1b: Selects ISC2 as the active state to become ASC upon strobe	0b	R/W
[6:0]	setting	Register strobe (synchronously change the switch state) (enabled with GenConfig[5]=1b) 0000000b: Normal operation 1010101b: Register strobe causes ISC1 or ISC2 to become the ASC, changing the switch state	000000b	R/W

Page: 00h
Address: 05h
Register Name: squelch
Default Value: 86'h
Description: Output squelch configuraion register.

Bit(s)	Name	Description	Default	Type
[7:6]	squelch mode	Global squelch operation mode or select on an individual basis 00b: Squelch outputs on an individual basis using register.**inbufctrl(N)** address(N), page.08h 01b: Global disable squelch on LOS for all outputs 10b: Global enable squelch on LOS for all outputs to levels defined by bits [2:1] below 11b: Globally force all outputs to squelch level defined by bits [2:1] below	10b	R/W
[5:3]	Reserved	Reserved	000b	R/W
[2:1]	squelch level	Global squelch level selection when squelch[7:6]!=00b 00b: Unused 01b: Output H on squelch (recommended for DC coupled cases) 10b: Output L on squelch (recommended for DC coupled cases) 11b: Output EI level (common mode) on squelch (recommended for AC coupled cases)	11b	R/W
[0]	Reserved	Reserved	0b	R/W

Page: 00h
Address: 06h
Register Name: ei config
Default Value: 80'h
Description: Electrical Idle State and xALARM configuration register.

Bit(s)	Name	Description	Default	Type
[7:6]	gbl_EI_en	Global enables or disables the EI passthrough function (or select individual selection) 00b: Settings determined on an individual lane/group basis using register.**inbufctrl(N)** address.hex(N), page 08h 01b: Reserved 10b: Global disable Electrical Bus Idle state pass through 11b: Global enable Electrical Bus Idle state pass through	10b	R/W
[5]	en_EI_mon	Allows individual lane EI duration to be measured on pin.**xALARM** 0b: Normal operation (pin.**xALARM** monitors all LOS) 1b: Monitor individual EI on pin.**xALARM** using register.**monchansel**, address.07h, page 00h	0b	R/W
[4]	en_los_mon	Allows individual lane LOS to be monitored on pin.**xALARM** using register.**monchansel**, address.07h, page 00h 0b: Normal operation (pin.**xALARM** monitors all LOS) 1b: Monitor individual LOS on pin.**xALARM** using register.**monchansel**, address.07h, page 00h	0b	R/W
[3:2]	gbl_EI_fe	Global selects front end or back end EI detection (or select individual selection) 00b: Global EI detection on front end 10b: Global EI detection on back end 11b: Setting determined on an individual lane/group basis using register.**inthresh(N)** address.hex(N), page 0Ah.	00b	R/W
[1]	gbl_EI_degl	Global deglitching on EI 0b: Global disable deglitching on EI 1b: Global enable deglitching on EI	0b	R/W
[0]	Reserved	Reserved	0b	R/W

Page: 00h
Address: 07h
Register Name: monchansel
Default Value: 00'h
Description: xALARM selection register for LOS or EI lane monitoring

Bit(s)	Name	Description	Default	Type
[7:0]	mon_chan	Selects the channel regardless of lane/group mode to monitor on pin.**xALARM** when register.**eiconfig[5:4]**=11b, address 60h, page 00h 00000000b: Monitor input 0 on pin.**xALARM** 00000001b: Monitor input lane 1, hex(1) = 01h, LOS or EI on pin.**xALARM** 00010111b: Monitor input lane 23, hex(23) = 17h, EI or LOS on pin.**xALARM** (max value for the M21024) 00101111b: Monitor input 47 on xAlarm (last input for M21048)	00000000b	R/W

Page: 00h
Address: 08h
Register Name: losconfig
Default Value: C0'h
Description: LOS alarm configuration register.

Bit(s)	Name	Description	Default	Type
[7:6]	LOS enable	Globally enable/disable loss of signal detection (or select individual selection) 00b: Settings determined on an individual lane/group basis using register.**inbufctrl(N)**, address.hex(N), page 08h and register.**inthresh(N)**, address.hex(N), page 0Ah 01b: Undefined 10b: Globally disables LOS detection on all inputs 11b: Globally enables LOS detection on all inputs	11b	R/W
[5:3]	LOS threshold	Global LOS threshold configuration when register.**losconfig[7:6]**=11b 000b: Minimum threshold 001b: ... 010b: ... 011b: Maximum threshold 100b: Reserved 101b: Reserved 110b: Reserved 111b: LOS complete power down	000b	R/W
[2]	Reserved	Reserved	0b	R/W
[1]	LOS delay	Global LOS integration time (can't be set individualy) 0b: Declare LOS after approx 5 µs of no data 1b: Declare LOS after approx 1 µs of no data	0b	R/W
[0]	Reserved	Reserved	0b	R/W

Page: 00h
Address: 09h
Register Name: gbinbuf
Default Value: F0'h
Description: Input buffer configuration register.

Bit(s)	Name	Description	Default	Type
[7]	gbl_inbuf_sel	Global buffer termination and power status (or select individual selection) 1b: Global input buffer configuration set with bits[5:4] below 0b: Individual input buffer configuration using register.**inbufctrl(N)**, address.hex(N), page 08h	1b	R/W
[6]	gbl_eqlvl_sel	Global Input equalizer Setting (or select individual selection) 1b: Global input equalizer level set with register.**inputeq**, address.0A, page 00h 0b: Individual input equalizer level set with register.**ineq**(N), address.hex(N) page 0Ch	1b	R/W
[5:4]	gbl_inbuf	Sets global input buffer selection when gbinbuf[7]=1b 11b: Enable inputs with 100 Ω source termination 10b: Enable inputs with High-Z input source termination 01b: Power down with 100 Ω source termination 00b: Power down and high-Z termination	11b	R/W
[3]	sw_xinen	0b: Software enable for all 48 input buffers 1b: Software disable for all 48 input buffers	0b	R/W
[2:0]	Reserved	Reserved	000b	R/W

Page: 00h
Address: 0Ah
Register Name: inputeq
Default Value: 00'h
Description: Global Equalization configuration register.

Bit(s)	Name	Description	Default	Type
[7:5]	Reserved	Reserved	000b	R/W
[4:0]	eq level	Sets EQ level when register.**gbinbuf[6]**=1b, address.09h, page 00h 00h: Minimum equalization level (~3 dB) 05h: Equalization level ~8 dB 07h: ... 09h: Equalization level ~12 dB 0Ah: Equalization level ~13 dB 0Bh: Equalization level ~15 dB 0Ch: Equalization level ~17 dB 0Fh: ... 10h: Equalization level ~19 dB 12h: Equalization level ~20 dB 14h: Equalization level ~22 dB 16h: ... 17h: Equalization level ~23 dB 19h: ... 1Bh: Equalization level ~24 dB 1Eh: ... 1Fh: Maximum equalization level (~27 dB)	00000b	R/W

NOTES:

1. The equalization levels given are for a Nyquist frequency of 5.75 GHz or 11.5 Gbps operation. For other data rates and their Nyquist frequencies please extrapolate. For example, at 5.75 GHz we have the maximum equalization level of -27 dB, for a Nyquist frequency of 3.125 GHz (6.25 Gbps), the maximum equalization level would be ~14.7 dB.

Page: 00h
Address: 0Bh
Register Name: outputbuf
Default Value: 84'h
Description: Output buffer configuration register.

Bit(s)	Name	Description	Default	Type
[7]	gbl_out_bufsel	Global output buffer output level and de-emphasis setting (or select individual selection) 1b: Global output configuration set with bits [6:4], [2:0] below 0b: Individual input configuration using register.**outbuf(N)**, address.hex(N), page.0Eh	1b	R/W
[6:4]	gbl_outde_lvl	Global enables output de-emphasis level selection when outputbuf[7]=1b 000b: Output de-emphasis disabled 001b: Lowest de-emphasis setting (~1.5 dB) 010b: De-emphasis setting ~3 dB 011b: De-emphasis setting ~4.5 dB 100b: De-emphasis setting ~6 dB 101b: De-emphasis setting ~7.5 dB 110b: De-emphasis setting ~9 dB 111b: Highest de-emphasis setting ~10.5 dB	000b	R/W
[3]	sw_xouten	0b: Software enable for all 48 output drivers 1b: Software disable for all 48 output drivers	0b	R/W
[2:1]	gbl_out_lvl	Global sets the output swing level of each output buffer when outputbuf[7]=1b 00b: Power down 01b: 600 mV_{PPD} Swing 10b: 800 mV_{PPD} Swing 11b: 1200 mV_{PPD} Swing	10b	R/W
[0]	out_de_freq	Global selection of de-emphasis time constant when outputbuf[7]=1b 0b: Nominal boosting time constant 1b: 2x higher nominal time constant	0b	R/W

Page: 00h
Address: 0Ch
Register Name: grpchas
Default Value: C0'h
Description: Global group lane input order assignment register (M21036 does not support group mode)

Bit(s)	Name	Description	Default	Type
[7:6]	gblch	11b: Set input.gouping{0,1,2,3} --> output.grouping{0,1,2,3} globally 10b: Set input.gouping{0,1,2,3} --> output.grouping{3,2,1,0} globally 01b: Unused 00b: Individual group channel input order assigned with register.**grpmapln0** and register.**grpmaln1**, page.07h	11b	R/W
[5:0]	Reserved	Reserved	000000b	R/W

NOTES:

1. Use of this register is controlled by register.**gen config**, address.03h, page.00h and pin.**GRPLNMODE.**

Page: 00h
Address: 0Fh
Register Name: asc_ctrl
Default Value: 00'h
Description: ASC group mode, hard wired redundancy switch control. This does not apply to the M21036 (M21036 does not support group mode)

Bit(s)	Name	Description	Default	Type
[7:5]	RSVD	Reserved	000b	R/W
[4]	fallback	0b: Enable the hard wired redundancy switch 1b: Disable the redundancy switch and enable the ASC page if pin.M4=0 (device not in group mode)	0b	R/W
[3]	xor_with_m3	M21048 – redundancy switch for output.group.7 0b: If pin.M3=0 input.group.3 --> output.group.7; if pin.M3=1 input.group.9 --> output.group.7 1b: If pin.M3=0 input.group.9 --> output.group.7; if pin.M3=1 input.group.3 --> output.group.7 M21024 – Non Applicable	0b	R/W
[2]	xor_with_m2	M21048 – redundancy switch for output.group.6 0b: If pin.M2=0 input.group.7 --> output.group.6; if pin.M2=1 input.group.5 --> output.group.6 1b: If pin.M2=0 input.group.5 --> output.group.6; if pin.M2=1 input.group.7 --> output.group.6 M21024 – Non Applicable	0b	R/W
[1]	xor_with_m1	M21048 – redundancy switch for output.group.1 0b: If pin.M1=0 input.group.1 --> output.group.1; if pin.M1=1 input.group.11 --> output.group.1 1b: If pin.M1=0 input.group.11 --> output.group.1; if pin.M1=1 input.group.1 --> output.group.1 M21024 – redundancy switch for output.group.1 0b: If pin.M1=0 input.group.3 --> output.group.1; if pin.M1=1 input.group.4 --> output.group.1 1b: If pin.M1=0 input.group.4 --> output.group.1; if pin.M1=1 input.group.3 --> output.group.1	0b	R/W

Bit(s)	Name	Description	Default	Type
[0]	xor_with_m0	M21048 – redundancy switch for output.group.0 0b: If pin.M0=0 input.group.6 --> output.group.0; if pin.M0=1 input.group.4 --> output.group.0 1b: If pin.M0=0 input.group.4 --> output.group.0; if pin.M0=1 input.group.6 --> output.group.0 M21024 – redundancy switch for output.group.0 0b: If pin.M0=0 input.group.1 --> output.group.0; if pin.M0=1 input.group.5 --> output.group.0 1b: If pin.M0=0 input.group.5 --> output.group.0; if pin.M0=1 input.group.1 --> output.group.0	0b	R/W

NOTES:

1. This register is not used for the M21036.

Page: 00h
Address: 10h
Register Name: tempmon
Default Value: 1E'h
Description: Control for the four on-die temperature monitors.

Bit(s)	Name	Description	Default	Type
[7]	dis_xovertemp	0b: Pin.**xOVERTEMP** alarm active 1b: Pin.**xOVERTEMP** alarm disabled	0b	R/W
[6]	xovertemp_out_dis	Disable automatically all output drivers on overtemp flag event, 0b: Do not disable output drivers on over temperature alarm. 1b: Disable all output drivers automatically on over temperature alarm.	0b	R/W
[5]	xovertemp_pol	Pin.**xOVERTEMP** polarity 0b: Pin.**xOVERTEMP** alarm is set to LOW whenever T_{JUNC} exceed temp threshold defined with bits[4:2] below 1b: Pin.**xOVERTEMP** alarm is set to HIGH whenever T_{JUNC} exceed temp threshold defined with bits[4:2] below	0b	R/W
[4:2]	jtemp_alarm_th	Temperature thresholds for asserting pin.**xOVERTEMP** alarm. The threshold values are approximate and are NOT guaranteed. 000b: 50 °C 001b: 65 °C 010b: 80 °C 011b: 95 °C 100b: 110 °C 101b: 115 °C 110b: 125 °C 111b: 130 °C	111b	R/W
[1]	en_temp_mon	0b: Disable temperature monitor 1b: Enable temperature monitor	1b	R/W
[0]	strobe_temp	Strobes ADC for temperature measurement 0b: Hold last read temperature values into register.**tempmont**, address.01h, page.21h and register.**tempmonb**, address.02h, page.21h. 1b: On rising edge of this bit, strobe and load the temperature sensor values into register.**tempmont**, address.01h, page.21h and register.**tempmonb**, address.02h, page.21h.	0b	R/W

Page: 00h

Address: HEX(64 + n) n=0...5
40h 41h 42h 43h 44h 45h

Register Name: LOS alarm(M)

Default Value: 00'h

Description: M=[0..5] for M21048 & M21036, M=[0..2] for M21024
Individual lane LOS alarm monitor latch.
The register values are set upon LOS detection. Values are NOT automatically cleared when the LOS condition discontinues. Any set bit persists until reset by the appropriate user write or a global reset.

Bit(s)	Name	Description	Default	Type
[7]	lane (8M+7)	0b: Input lane (**M***8 + 7) LOS, read 0b = no LOS 1b: Input lane (**M***8 + 7) LOS, read 1b = LOS flag, write 1b = clear	0b	R/W
[6]	lane (8M+6)	0b: Input lane (**M***8 + 6) LOS, read 0b = no LOS 1b: Input lane (**M***8 + 6) LOS, read 1b = LOS flag, write 1b = clear	0b	R/W
[5]	lane(8M+5)	0b: Input lane (**M***8 + 5) LOS, read 0b = no LOS 1b: Input lane (**M***8 + 5) LOS, read 1b = LOS flag, write 1b = clear	0b	R/W
[4]	lane (8M+4)	0b: Input lane (**M***8 + 4) LOS, read 0b = no LOS 1b: Input lane (**M***8 + 4) LOS, read 1b = LOS flag, write 1b = clear	0b	R/W
[3]	lane (8M+3)	0b: Input lane (**M***8 + 3) LOS, read 0b = no LOS 1b: Input lane (**M***8 + 3) LOS, read 1b = LOS flag, write 1b = clear	0b	R/W
[2]	lane (8M+2)	0b: Input lane (**M***8 + 2) LOS, read 0b = no LOS 1b: Input lane (**M***8 + 2) LOS, read 1b = LOS flag, write 1b = clear	0b	R/W
[1]	lane (8M+1)	0b: Input lane (**M***8 + 1) LOS, read 0b = no LOS 1b: Input lane (**M***8 + 1) LOS, read 1b = LOS flag, write 1b = clear	0b	R/W
[0]	lane (8M+0)	0b: Input lane (**M***8 + 0) LOS, read 0b = no LOS 1b: Input lane (**M***8 + 0) LOS, read 1b = LOS flag, write 1b = clear	0b	R/W

NOTES:

1. The M21024 has only 24 valid lane assignments.
2. The M21048 has only 48 valid lane assignments.
3. The M21036 has only 36 valid lane assignments.
4. Default values depend on the status seen at the LOS detector. Will be at "zero" assuming a signal is detected on all input lanes.

Page: 00h

Address: HEX(80 + n) n=0...5
50h 51h 52h 53h 54h 55h

Register Name: stat alarm(M)

Default Value: na

Description: M=[0..5] for M21048 & M21036, M=[0..2] for M21024
Individual lane LOS alarm monitor
The register values are actively set and re-set upon any detected change in LOS status.

Bit(s)	Name	Description	Default	Type
[7]	lane (8M+7)	0b: Input lane (**M***8 + 7) LOS, read 1b = LOS flag, read **0b** = no LOS		R
[6]	lane (8M+6)	0b: Input lane (**M***8 + 6) LOS, read 1b = LOS flag, read **0b** = no LOS		R
[5]	lane(8M+5)	0b: Input lane (**M***8 + 5) LOS, read 1b = LOS flag, read **0b** = no LOS		R
[4]	lane (8M+4)	0b: Input lane (**M***8 + 4) LOS, read 1b = LOS flag, read **0b** = no LOS		R
[3]	lane (8M+3)	0b: Input lane (**M***8 + 3) LOS, read 1b = LOS flag, read **0b** = no LOS		R
[2]	lane (8M+2)	0b: Input lane (**M***8 + 2) LOS, read 1b = LOS flag, read **0b** = no LOS		R
[1]	lane (8M+1)	0b: Input lane (**M***8 + 1) LOS, read 1b = LOS flag, read **0b** = no LOS		R
[0]	lane (8M+0)	0b: Input lane (**M***8 + 0) LOS, read 1b = LOS flag, read **0b** = no LOS		R

NOTES:

1. The M21024 has only 24 valid lane assignments.
2. The M21048 has only 48 valid lane assignments.
3. The M21036 has only 36 valid lane assignments.

Page: 00h

Address: HEX(96 + n) n=0...5
60h 61h 62h 63h 64h 65h

Register Name: mask alarm(M)

Default Value: 00'h

Description: M=[0..5] for M21048 & M21036, M=[0..2] for M21024
Individual mask LOS alarm wired OR lane mask.
The register masks the individual lanes that are "wired-or" to the pin.**xALARM**.
Any set bit persists until reset by the appropriate user write or a global reset.

Bit(s)	Name	Description	Default	Type
[7]	lane (8M+7)	0b: Input lane (**M***8 + 7) LOS, 0b = include this lane 1b: Input lane (**M***8 + 7) LOS, 1b = mask out this lane	0b	R/W
[6]	lane (8M+6)	0b: Input lane (**M***8 + 6) LOS, 0b = include this lane 1b: Input lane (**M***8 + 6) LOS, 1b = mask out this lane	0b	R/W
[5]	lane(8M+5)	0b: Input lane (**M***8 + 5) LOS, 0b = include this lane 1b: Input lane (**M***8 + 5) LOS, 1b = mask out this lane	0b	R/W
[4]	lane (8M+4)	0b: Input lane (**M***8 + 4) LOS, 0b = include this lane 1b: Input lane (**M***8 + 4) LOS, 1b = mask out this lane	0b	R/W
[3]	lane (8M+3)	0b: Input lane (**M***8 + 3) LOS, 0b = include this lane 1b: Input lane (**M***8 + 3) LOS, 1b = mask out this lane	0b	R/W
[2]	lane (8M+2)	0b: Input lane (**M***8 + 2) LOS, 0b = include this lane 1b: Input lane (**M***8 + 2) LOS, 1b = mask out this lane	0b	R/W
[1]	lane (8M+1)	0b: Input lane (**M***8 + 1) LOS, 0b = include this lane 1b: Input lane (**M***8 + 1) LOS, 1b = mask out this lane	0b	R/W
[0]	lane (8M+0)	0b: Input lane (**M***8 + 0) LOS, 0b = include this lane 1b: Input lane (**M***8 + 0) LOS, 1b = mask out this lane	0b	R/W

NOTES:

1. The M21024 has only 24 valid lane assignments.
2. The M21048 has only 48 valid lane assignments.
3. The M21036 has only 36 valid lane assignments.

5.2 Page 01h

Page: 01h

Address: HEX(0 + n*0) n=0...47
00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh 0Eh 0Fh 10h 11h 12h 13h 14h 15h 16h 17h 18h 19h 1Ah 1Bh 1Ch 1Dh 1Eh 1Fh
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh

Register Name: ascout(N)

Default Value: 00'h

Description: Active switch configuration (ASC) for output lane N (lane mode), or group N (group mode).
Writing to this register causes the switch state to change immediately in an asynchronous manner.
Behavior is dependent on the content of register.**gen config**.bit[7:6], address.03h, page.00h and pin.**GRPLNMODE.**

Bit(s)	Name	Description	Default	Type
[7:0]	ascout	ASC contains the current switch state. Writing to this register will cause the switch state to change immediately in an asynchronous manner. Input (mapped to data) and output (define by the address) channel mapping is dependent on lane/group selection, register.**gen config**.bit[7:6] and pin.**GRPLNMODE** 00000000b: Route input lane/group 0 to output lane/group N 00000001b: Route input lane/group 1 to output lane/group N 00000101b: Route input lane/group 5 to output lane/group N (last available group for the M21024) 00000110b: Route input lane/group 6 to output lane/group N 00b: Route input lane/group N to output lane/group N [default] 00001011b: Route input lane/group 11 to output lane/group N (last available group for the M21048) 00001100b: Route input lane 12 to output lane N 00010111b: Route input lane 23 to output lane N (last available lane for the M21024) 00101111b: Route input lane 47 to output lane N (last available lane for the M21048) 00110000b: Route internal high speed PRBS lane to output lane N 00111111b: Power down switch lane N	00000000b	R/W

NOTES:

1. The M21024 has only 24 valid lane assignments and 6 valid group assignments. Valid addresses are [00h..17h] in lane mode, [00..05h] in group mode.
2. The M21048 has only 48 valid lane assignments and 12 valid group assignments. Valid addresses are [00h..2Fh] in lane mode, [00..0Bh] in group mode.
3. The M21036 has only 36 valid lane assignments. It has the same lane assignment as the M21048 without channels 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46.

5.3 Page 02h

Page: 02h
Address: 00h
Register Name: CDR Preset
Default Value: 00'h
Description:
CDR Presets. EEPROM Down-loadable

Bit(s)	Name	Description	Default	Type
[7:0]	Preset	00000000b: 10G KR / XAUI / GbE with 156.25 MHz Reference Clock 00000001b: 10G KR Only with 156.25 MHz Reference Clock 00000010b: GbE Only with 125 MHz Reference Clock 00000011b: GbE Only with 156.25 MHz Reference Clock 00000100b: XAUI Only with 125 MHz Reference Clock 00000101b: XAUI Only with 156.25 MHz Reference Clock 00000110b: XAUI Only with 62.5 MHz Reference Clock 00001000b: FibreChannel with 125 MHz Reference Clock 00001001b: FibreChannel with 106.25 MHz Reference Clock 00001010b: FibreChannel with 62.5 MHz Reference Clock 00001011b: FibreChannel with 212.5 MHz Reference Clock 00010000b: SATA/SAS with 125 MHz Reference Clock (SSC off) 00010001b: SATA/SAS with 125 MHz Reference Clock (SSC on) 00010010b: SATA/SAS with 150 MHz Reference Clock (SSC off) 00010011b: SATA/SAS with 150 MHz Reference Clock (SSC on) 00010100b: SATA/SAS with 62.5 MHz Reference Clock (SSC off) 00010101b: SATA/SAS with 62.5 MHz Reference Clock (SSC on) 00011000b: InfiniBand with 125 MHz Reference Clock 00011001b: InfiniBand with 100.5 MHz Reference Clock 00011010b: InfiniBand with 62.5 MHz Reference Clock 00100000b: PCI-Express with 125 MHz Reference Clock (SSC off) 00100001b: PCI-Express with 125 MHz Reference Clock (SSC on) 00100010b: PCI-Express with 100 MHz Reference Clock (SSC off) 00100011b: PCI-Express with 100 MHz Reference Clock (SSC on) 00100100b: PCI-Express with 62.5 MHz Reference Clock (SSC off) 00100101b: PCI-Express with 62.5 MHz Reference Clock (SSC on) 00101000b: SONET with 155.52 MHz Reference Clock 00101001b: SONET with 77.76 MHz Reference Clock 00101010b: SONET with 311.04 MHz Reference Clock 00110000b: 10G FEC with 32x Clock Multiplier 00110001b: 10G FEC with 64x Clock Multiplier 00110010b: 10G FEC with 16x Clock Multiplier 00110011b: 10G FEC with 40x Clock Multiplier	00000000b	R/W

Bit(s)	Name	Description	Default	Type
[7:0] (cont.)		00110100b: 10G FEC with 50x Clock Multiplier 00110101b: 10G FEC with 60x Clock Multiplier 00110110b: 10G FEC with 80x Clock Multiplier 01000000b: 7.5 GHz with 125 MHz Reference Clock 01000001b: 7.5 GHz with 156.25 MHz Reference Clock 01000010b: 7.5 GHz with 62.5 MHz Reference Clock 01000011b: 7.5 GHz with 312.5 MHz Reference Clock		

NOTES:

1. See preset tab to see default values for all registers.
2. For codes not shown above, default is 10G with 125 MHz reference clock.

Page: 02h
Address: 01h
Register Name: CDR: PLL Divide Ratio
Default Value: 00'h
Description: CDR div2 enable and div ratio. EEPROM Downloadable

Bit(s)	Name	Description	Default	Type
[7]	div2 enable	0b: Enabled 1b: Disabled	0b	R/W
[6:0]	div ratio	Use default value 0000000b: Multiply Refclk by 1 0001000b: Multiply Refclk by 16 1000000b: Multiply Refclk by 64 1111111b: Multiply Refclk by 127	0000000b	R/W

NOTES:

1. When set to 00h, this register will contain the default value, based on the CDR preset register.
2. When set to any value other than 00h, the register value will be used instead of the default value.
3. Since the default of this register is 00h,, it will not read back 00h at reset.
4. The 7 LSB's represent a number (0-127), with values less than 16 treated as being 16. The number in these bits is multiplied by two to create the effective PLL multiplication ratio. As an example, to get to 10.3125GHz in the PLL with a 156.25 MHz Reference clock, these bits should be set to 21h (multiply by 66).
5. The reference clock divide-by-two circuit should be enabled only for three possible reasons: The first is when the reference clock frequency is greater than 250 MHz. The second is when a multiplier less than 32 is required. The final reason is to get a non-modulo-two multiplication factor (e.g. 65).

Page: 02h
Address: 02h
Register Name: CDR: PLL Control
Default Value: 00'h
Description: CDR PLL control. EEPROM Downloadable

Bit(s)	Name	Description	Default	Type
[7]	quad pd	0b: Normal operation 1b: Power down	0b	R/W
[6]	vco over-ride	0b: Use default value 1b: Over-ride	0b	R/W
[5]	vco select	0b: Vco low 1b: Vco high	0b	R/W
[4]	lbw over-ride	0b: Normal operation 1b: Over-ride	0b	R/W
[3:2]	PLL LBW	00b: Lowest 01b: ... 10b: ... 11b: Highest	00b	R/W
[1:0]	Reserved	Reserved	00b	R/W

NOTES:

1. When bit 6 is 0, bit 5 will read back the default value, based on the CDR preset register.
2. When bit 4 is 0, bits [3:2] will read back the default value, based on the CDR preset register.
3. Since the default state of bits 6 and 4 is 0, this register will not read back 00h at reset.

Page: 02h
Address: 03h
Register Name: CDR: Interrupt Mask
Default Value: 08'h
Description: CDR Interrupt Mask. EEPROM Downloadable

Bit(s)	Name	Description	Default	Type
[7]	PLL LOL Mask	0b: PLL LOL change generates interrupt 1b: PLL LOL change does not generate interrupt	0b	R/W
[6]	LOR Mask	0b: NOREF change generates interrupt 1b: NOREF change does not generate interrupt	0b	R/W
[5:4]	Reserved	Reserved	00b	R/W
[3]	PRBS Mask	0b: PRBS Detector change generates interrupt 1b: PRBS Detector change does not generate interrupt	1b	R/W
[2:1]	RSVD	Reserved	00b	R/W
[0]	LOL Mask	0b: LOL change generates interrupt 1b: LOL change does not generate interrupt	0b	R/W

Page: 02h
Address: 04h
Register Name: CDR: CRU Control A
Default Value: 00'h
Description: CDR CRU Control A. EEPROM Downloadable

Bit(s)	Name	Description	Default	Type
[7]	leak override	0b: Use default value 1b: Override leakage control	0b	R/W
[6:3]	LOL Limits	0000b: 91 ppm Assert Limit, 61 ppm De-Assert Limit 0001b: 122 ppm Assert Limit, 91 ppm De-Assert Limit 0010b: 183 ppm Assert Limit, 122 ppm De-Assert Limit 0011b: 244 ppm Assert Limit, 183 ppm De-Assert Limit 0100b: 366 ppm Assert Limit, 244 ppm De-Assert Limit 0101b: 488 ppm Assert Limit, 366 ppm De-Assert Limit 0110b: 732 ppm Assert Limit, 488 ppm De-Assert Limit 0111b: 1k ppm Assert Limit, 732 ppm De-Assert Limit 1000b: 1.5k ppm Assert Limit, 1k ppm De-Assert Limit 1001b: 2k ppm Assert Limit, 1.5k ppm De-Assert Limit 1010b: 3k ppm Assert Limit, 2k ppm De-Assert Limit 1011b: 4k ppm Assert Limit, 3k ppm De-Assert Limit 1100b: 6k ppm Assert Limit, 4k ppm De-Assert Limit 1101b: 8k ppm Assert Limit, 6k ppm De-Assert Limit 1110b: LOL Disabled; Leakage sign set to 1 1111b: LOL Disabled; Leakage sign set to 0	0000b	R/W
[2:0]	leak gain	000b: 0.95 ppm Leakage 001b: 1.91 ppm Leakage 010b: 3.81 ppm Leakage 011b: 7.63 ppm Leakage 100b: 15.3 ppm Leakage 101b: 30.5 ppm Leakage 111b: Disable Leakage	000b	R/W

NOTES:

1. When bit 7 is 1, bits [6:0] read out the default value, based on the CDR Preset register value.
2. Because the default value of bit 7 is 0, this register will not read 00h at reset.

Page: 02h
Address: 05h
Register Name: CDR: CRU Control B
Default Value: 00'h
Description: CDR CRU Control B. EEPROM Downloadable

Bit(s)	Name	Description	Default	Type
[7:4]	peaking	0000b: Use default value 0001b: Minimum Peaking 0010b: ... 0011b: ... 0100b: ... 0101b: ... 0110b: ... 0111b: ... 1000b: ... 1001b: ... 1010b: ... 1011b: ... 1100b: ... 1101b: ... 1110b: Maximum Peaking 1111b: Disable second order loop	0000b	R/W
[3:0]	lbw	0000b: Use default value 0001b: Normal 0010b: 1.5X Normal 0011b: 2X Normal 0100b: 3X Normal 0101b: 4X Normal 0110b: 6X Normal 0111b: 8X Normal 1000b: 12X Normal 1001b: 0.75X Normal 1010b: 0.5X Normal 1011b: 0.375X Normal 1100b: 0.25X Normal 1101b: 0.1875X Normal 1110b: 0.125X Normal 1111b: CDR Tracking disabled	0000b	R/W

NOTES:

1. When bits [7:4] are set to 0h, they will read back the default value, as determined by the CDR Preset register value.
2. When bits [3:0] are set to 0h, they will read back the default value, as determined by the CDR Preset register value.
3. Since the default value for this register is 00h, at reset it will not read back 00h.

Page: 02h
Address: 06h
Register Name: CDR: ARD Control
Default Value: 00'h
Description: CDR ARD control. EEPROM Downloadable

Bit(s)	Name	Description	Default	Type
[7:6]	Divide Value	00b: Divide-by-1 (6.25 Gbps-11.88 Gbps operation) 01b: Divide-by-2 (3.125 Gbps-6.00 Gbps operation) 10b: Divide-by-4 (1.5625 Gbps - 3.00 Gbps operation) 11b: Divide-by-8 (78.125 Mbps - 1.50 Gbps operation)	00b	R/W
[5]	ARD Disable	0b: ARD Enabled 1b: ARD Disabled	0b	R/W
[4]	Range over-ride	0b: Use default valid ranges 1b: Over-ride valid ranges	0b	R/W
[3]	Div8_Valid	0b: Divide-by-8 is valid for ARD searching 1b: Divide-by-8 is invalid for ARD searching	0b	R/W
[2]	Div4_Valid	0b: Divide-by-4 is valid for ARD searching 1b: Divide-by-4 is invalid for ARD searching	0b	R/W
[1]	Div2_valid	0b: Divide-by-2 is valid for ARD searching 1b: Divide-by-2 is invalid for ARD searching	0b	R/W
[0]	Div1_valid	0b: Divide-by-1 is valid for ARD searching 1b: Divide-by-1 is invalid for ARD searching	0b	R/W

NOTES:

1. Writing bits [7:6] will set the divide value; if ARD is enabled, the divide value may change before readback.
2. The valid range bits [3:0] read back the default values as set by the CDR Preset register value when bit 4 is set to 0.
3. When bit 4 is set to 1, the valid range bits [3:0] read back their actual value; for normal operation, at least one of these bits should be set to 1, or ARD must be disabled.
4. Because the range over-ride bit is set to 0, bits [3:0] will not read back as 0h at reset.
5. Because ARD is enabled by default, bits [7:6] may or may not read back as 00b at reset.

Page: 02h
Address: 07h
Register Name: CDR: EQ Control
Default Value: 00'h
Description: CDR EQ control. EEPROM Downloadable

Bit(s)	Name	Description	Default	Type
[7]	CH pd	0b: Normal operation 1b: Power down	0b	R/W
[6]	scaling_override	0b: Use default prescale scaling value 1b: Override prescale scaling value	0b	R/W
[5]	peak_scaling	0b: Constant peaking with prescale 1b: Peaking increases with prescale	0b	R/W
[4]	soft reset	0b: Normal operation 1b: Reset CDR registers	0b	R/W
[3:0]	Reserved	Reserved	0b	R/W

NOTES:

1. Bit [5] reads back the default value when bit [6] is set to 0. Increasing peaking with prescale results in constant SSC tolerance, so is enabled with SSC modes, to allow lower peaking with low prescale values.

Page: 02h
Address: 18h
Register Name: CDR: ARD Control 2
Default Value: 00'h
Description: CDR: ARD control Register 2

Bit(s)	Name	Description	Default	Type
[7]	LOL_CRU	0b: LOL_CRU is not asserted (CRU frequency is within ppm limits) 1b: LOL_CRU is asserted (CRU frequency is beyond ppm limits)	0b	R
[6]	LOL_ARD	0b: LOL_ARD is not asserted (single and missed bit counters are satisfied) 1b: LOL_ARD is asserted (single or missed bit counter is not satisfied)	0b	R/W
[5:4]	ARD_LEN	00b: ARD works over 8192 bit chunks 01b: ARD works over 16384 bit chunks 10b: ARD works over 32768 bit chunks 11b: ARD works over 65536 bit chunks	00b	R/W
[3:2]	Single Threshold	00b: LOLHI asserted if single_bit_count <= 96 01b: LOLHI asserted if single_bit_count <= 64 10b: LOLHI asserted if single_bit_count <= 48 11b: LOLHI asserted if single_bit_count <= 128	00b	R/W
[1:0]	pattern	00b: LOLLO asserted if missed_bit_count >= 4 01b: LOLLO asserted if missed_bit_count >= 8 10b: LOLLO asserted if missed_bit_count >= 16 11b: LOLLO asserted if missed_bit_count >= 32	00b	R/W

Page: 02h
Address: 19h
Register Name: CDR: Gain Value
Default Value: 7F'h
Description: CDR: Gain Coefficient Value

Bit(s)	Name	Description	Default	Type
[7]	Reserved	Reserved	0b	R/W
[6:0]	gain value	0000000b: Minimum 1111111b: Max	1111111b	R/W

NOTES:

1. When read, this register reports the value that the DFE coefficient algorithm has for the GAIN value; when written, the register value is deposited into the GAIN coefficient, and adaptation proceeds (unless held).
2. Due to DFE coefficient adaptation, after reset, this register may not read 7Fh.

Page: 02h
Address: 21h
Register Name: CDR : PRBS Gen
Default Value: 00'h
Description: CDR: PRBS Gen

Bit(s)	Name	Description	Default	Type
[7:6]	Reserved	Reserved	00b	R/W
[5]	PRBS Mode	0b: PRBS generator runs off extracted clock of Rx 1b: PRBS Generator runs off PLL clock	0b	R/W
[4]	enable	0b: Disable PRBS Generation 1b: Enable PRBS Generation	0b	R/W
[3]	pattern invert	0b: Use normal polarity for output pattern 1b: Invert polarity of output pattern	0b	R/W
[2:0]	pattern	000b: 1010 clock pattern 001b: 1100 clock pattern 010b: 11110000 clock pattern 011b: 1111111100000000 clock pattern 100b: PRBS7 101b: PRBS15 110b: PRBS23 111b: PRBS31	000b	R/W

Page: 02h
Address: 22h
Register Name: CDR: PRBS Detector Control
Default Value: 00'h
Description: CDR : PRBS Detector Control

Bit(s)	Name	Description	Default	Type
[7:5]	len	000b: Count errors in 2^8 bits 001b: Count errors in 2^10 bits 010b: Count errors in 2^12 bits 011b: Count errors in 2^16 bits 100b: Count errors in 2^20 bits 101b: Count errors in 2^24 bits 110b: Count errors in 2^28 bits 111b: Count errors in 2^32 bits	000b	R/W
[4]	enable	0b: Disable PRBS Detection 1b: Enable PRBS Detection	0b	R/W
[3]	pattern invert	0b: Use normal polarity for output pattern 1b: Invert polarity of output pattern	0b	R/W
[2:0]	pattern	000b: 1010 clock pattern 001b: 1100 clock pattern 010b: 11110000 clock pattern 011b: 1111111100000000 clock pattern 100b: PRBS7 101b: PRBS15 110b: PRBS23 111b: PRBS31	000b	R/W

Page: 02h
Address: 23h
Register Name: CDR: PRBS Detector Status
Default Value: 00'h
Description: CDR : PRBS Detector Control B

Bit(s)	Name	Description	Default	Type
[7]	Latch Enable	0b: Use unlatched PRBS detection (gross pass/fail indication only) 1b: Use Latched PRBS detection (able to read error rate)	0b	R
[6:4]	Extended Length	000b: No extension to counter length 001b: 4 bit extension to counter length 010b: 8 bit extension to counter length 011b: 12 bit extension to counter length 100b: 16 bit extension to counter length 101b: 20 bit extension to counter length 110b: 24 bit extension to counter length 111b: Untimed error count	000b	R/W
[3:2]	Reserved	Reserved	00b	R
[1]	Latch Error	0b: Error free when PRBS detection latched 1b: Not Error free when PRBS detection latched	0b	R
[0]	full/start	0b: PRBS Error Counter has not reached limit 1b: PRBS Error counter is at limit	0b	R/W

NOTES:

1. Writing a 1 to bit 0 starts the PRBS error counter.

Page: 02h
Address: 24h
Register Name: CDR: PRBS Error Count 0
Default Value: 00'h
Description: CDR: PRBS Error Count 0

Bit(s)	Name	Description	Default	Type
[7:0]	count	00000000b: PRBS Errors counted, bits [7:0]	00000000b	R

Page: 02h
Address: 25h
Register Name: CDR : PRBS Error Count 1
Default Value: 00'h
Description: CDR: PRBS Error Count 1

Bit(s)	Name	Description	Default	Type
[7:0]	count	00000000b: PRBS Errors counted, bits [15:8]	00000000b	R

Page: 02h
Address: 26h
Register Name: CDR : PRBS Error Count 2
Default Value: 00'h
Description: CDR : PRBS Error Count 2

Bit(s)	Name	Description	Default	Type
[7:0]	count	00000000b: PRBS Errors counted, bits [23:16]	00000000b	R

Page: 02h
Address: 27h
Register Name: CDR : PRBS Error Count 3
Default Value: 00'h
Description: CDR : PRBS Error Count 3

Bit(s)	Name	Description	Default	Type
[7:0]	count	00000000b: PRBS Errors counted, bits [31:24]	00000000b	R

NOTES:

1. CDR BankA on pg2, CDR BankC on pg4

Page: 02h
Address: 48h
Register Name: CDR : CDR Status
Default Value: 00'h
Description: CDR : CDR Status

Bit(s)	Name	Description	Default	Type
[7]	PLL_LOL	0b: PLL is in lock 1b: PLL is out of lock	0b	R
[6]	LOR	0b: PLL is receiving a reference clock 1b: PLL is not receiving a reference clock	0b	R
[5:1]	Reserved	Reserved	0b	R
0	LOL	0b: Channel is locked 01b: Channel is not locked	0b	R

NOTES:

1. Since this register represents the status of the part, it may not read 00'h at reset.

Page: 02h
Address: 49h
Register Name: CDR : CDR Delta
Default Value: 00'h
Description: CDR : CDR Delta

Bit(s)	Name	Description	Default	Type
[7]	PLL_LOL Delta	0b: No change in PLL_LOL since last write to this register 1b: PLL_LOL has changed since last write to this register	0b	R
[6]	LOR Delta	0b: No Change in LOR since last write to this register 1b: LOR has changed since last write to this register	0b	R
[5]	Reserved	Reserved	0b	R
[4]	PRBS Delta	0b: No change in PRBS since last write to this register 1b: PRBS has changed since last write to this register	0b	R
[3:2]	Reserved	Reserved	00b	R
[1]	LOL Delta	0b: No change in LOL since last write to this register 1b: LOL has changed since last write to this register	0b	R
[0]	Reserved	Reserved	0b	R

NOTES:

1. Writing to this register clears all delta bits.
2. Since this register represents the state of the part, at reset, it may not read 00.

5.4 Page 03h

Page: 03h
Address: 00h
Register Name: isc1out(N)
Default Value: 00'h
Description: Intermediate Switch Configuration #1 (ISC1) for output lane N (lane mode), or group N (group mode).
Writing to this register may cause the switch state to change immediately in an asynchronous manner.
Behavior is dependent on the content of register.**gen config**.bit[7:6], address.03h, page.00h and pin.**GRPLNMODE**.
The M21036 does not support group mode.
Default: the switch is in one to one configuration.

Bit(s)	Name	Description	Default	Type
[7:0]	iscout	00000000b: Route input lane/group 0 to output lane/group N 00000001b: Route input lane/group 1 to output lane/group N 00000101b: Route input lane/group 5 to output lane/group N (last available group for the M21024) 00000110b: Route input lane/group 6 to output lane/group N 00001011b: Route input lane/group 11 to output lane/group N (last available group for the M21048) 00001100b: Route input lane 12 to output lane N 00010111b: Route input lane 23 to output lane N (last available lane for the M21024) 00101111b: Route input lane 47 to output lane N (last available lane for the M21048) 00110000b: Route internal high speed PRBS lane to output lane N 00111111b: Power down switch lane N	00000000b	R/W

NOTES:

1. The M21024 has only 24 valid lane assignments and 6 valid group assignments. Valid addresses are [00h..17h] in lane mode, [00..05h] in group mode.
2. The M21048 has only 48 valid lane assignments and 12 valid group assignments. Valid addresses are [00h..2Fh] in lane mode, [00..0Bh] in group mode.
3. The M21036 has only 36 valid lane assignments. It has the same lane assignment as the M21048 without channels 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46.

5.5 Page 05h

Page: 05h
Address: 00h
Register Name: iscout2(N)
Default Value: 00'h
Description: Intermediate Switch Configuration #2 (ISC2) for output lane N (lane mode), or group N (group mode).
Writing to this register may cause the switch state to change immediately in an asynchronous manner.
Behavior is dependent on the content of register.**gen config**.bit[7:6], address.03h, page.00h and pin.**GRPLNMODE**.
The M21036 does not support group mode.
Default: the switch is in all broadcast from input lane 0.

Bit(s)	Name	Description	Default	Type
[7:0]	iscout	00000000b: Route input lane/group 0 to output lane/group N 00000001b: Route input lane/group 1 to output lane/group N 00000101b: Route input lane/group 5 to output lane/group N (last available group for the M21024) 00000110b: Route input lane/group 6 to output lane/group N 00001011b: Route input lane/group 11 to output lane/group N (last available group for the M21048) 00001100b: Route input lane 12 to output lane N 00010111b: Route input lane 23 to output lane N (last available lane for the M21024) 00101111b: Route input lane 47 to output lane N (last available lane for the M21048) 00110000b: Route internal high speed PRBS lane to output lane N 00111111b: Power down switch lane N	00000000b	R/W

NOTES:

1. The M21024 has only 24 valid lane assignments and 6 valid group assignments. Valid addresses are [00h..17h] in lane mode, [00..05h] in group mode.
2. The M21048 has only 48 valid lane assignments and 12 valid group assignments. Valid addresses are [00h..2Fh] in lane mode, [00..0Bh] in group mode.
3. The M21036 has only 36 valid lane assignments. It has the same lane assignment as the M21048 without channels 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46.

5.6 Page 07h

Page: 07h
Address: 00h
Register Name: grpmapIn0
Default Value: FF'h
Description: Group mode intra-lane mapping register #1
Determines the intra-group mapping when activated by register.**grpchass**.bit[7], address.0Ch, page.00h
The device must be in group mode as set by register.**gen config**.bit[7:6], address.03h, page.00h and/or pin.**GRPLNMODE**.
The M21036 does not support group mode.

Bit(s)	Name	Description	Default	Type
[7]	grp_map7	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 7 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 7	1b	R/W
[6]	grp_map6	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 6 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 6	1b	R/W
[5]	grp_map5	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 5 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 5	1b	R/W
[4]	grp_map4	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 4 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 4	1b	R/W
[3]	grp_map3	Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 3 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 3	1b	R/W
[2]	grp_map2	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 2 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 2	1b	R/W
[1]	grp_map1	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 1 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 1	1b	R/W
[0]	grp_map0	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 0 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 0	1b	R/W

Page: 07h
Address: 01h
Register Name: grpmapIn1
Default Value: FF'h
Description: Group mode intra-lane mapping register #2
Determines the intra-group mapping when activated by register.**grpchass**.bit[7], address.0Ch, page.00h
The device must be in group mode as set by register.**gen config**.bit[7:6], address.03h, page.00h and/or pin.**GRPLNMODE**.
The M21036 does not support group mode.

Bit(s)	Name	Description	Default	Type
[7:4]	Reserved	Reserved	1111b	R/W
[3]	grp_map11	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 11 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 11	1b	R/W
[2]	grp_map10	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 10 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 10	1b	R/W
[1]	grp_map9	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 9 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 9	1b	R/W
[0]	grp_map8	0b: Set grouping{0,1,2,3} --> grouping{3,2,1,0} for output group 8 1b: Set grouping{0,1,2,3} --> grouping{0,1,2,3} for output group 8	1b	R/W

5.7 Page 08h

Page: 08h

Address: HEX(0 + n*0) n=0...47
00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh 0Eh 0Fh 10h 11h 12h 13h 14h 15h 16h 17h 18h 19h 1Ah 1Bh 1Ch 1Dh 1Eh 1Fh
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh

Register Name: inbufctrl(N)

Default Value: EB'h

Description: Individual input buffer and squelch control for input lane N (lane mode), or group N (group mode).
This register controls the source termination and EI/OOB/LOS detection.
OOB is detected at the input of the part, hence squelch is associated with the input lane. this is contrary to the general practice in this document of defining control relative to the output lane.
Behavior is dependent on the content of register.**gen config**.bit[7:6], address.03h, page.00h and pin.**GRPLNMODE**.
The M21036 does not support group mode.

Bit(s)	Name	Description	Default	Type
[7:6]	inbuf_en	Determines individual group/lane input buffer selection when register.**gbinbuf[7]**=0b, address.09h, page.00h 00b: Power down and high-Z termination 01b: Power down with source termination 10b: Enable input N with High-Z input source termination 11b: Enable input N with source termination	11b	R/W
[5]	losen	Enables individual group/lane LOS detection when register.**losconfig[7:6]**=00b, address.08h, page.00h 0b: Disable LOS detection on group/lane 1b: Enable LOS detection on group/lane	1b	R/W
[4]	ebi_en	Enables individual group/lane EBI pass through when page 00h register.**ebiconfig[7:6]**=00b, address.06h, page.00h 0b: Disable EI detection 1b: Enable EI detection	0b	R/W

Bit(s)	Name	Description	Default	Type
[3:2]	squelch	Determines the group/lane squelch operational mode when register.**squelch[7:6]**=00b, address.05h, page.00h 00b: Reserved 01b: Disable squelch on LOS 10b: Enable squelch on LOS to squelch level defined in register.i**nbufctrl(N).bit**[1:0] 11b: Force output N to squelch level defined in register.**inbufctrl(N)**.bit[1:0]	10b	R/W
[1:0]	sq_level	Selects individual group/lane squelch level selection when register.**squelch**[7:6]=00b, address.05h, page.00h 00b: Reserved 01b: Output H on squelch (recommended for DC coupled cases) 10b: Output L on squelch (recommended for DC coupled cases) 11b: Output EI level (common mode) on squelch (recommended for AC coupled cases)	11b	R/W

NOTES:

1. The M21024 has only 24 valid lane assignments and 6 valid group assignments. Valid addresses are [00h..17h] in lane mode, [00..05h] in group mode.
2. The M21048 has only 48 valid lane assignments and 12 valid group assignments. Valid addresses are [00h..2Fh] in lane mode, [00..0Bh] in group mode.
3. The M21036 has only 36 valid lane assignments. It has the same lane assignment as the M21048 without channels 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46.

5.8 Page 0Ah

Page: 0Ah

Address: HEX(0 + n) n=0...47
00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh 0Eh 0Fh 10h 11h 12h 13h 14h 15h 16h 17h 18h 19h 1Ah 1Bh 1Ch 1Dh 1Eh 1Fh
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh

Register Name: inthresh(N)

Default Value: 01'h

Description: Individual LOS input threshold detection setting for lane N (lane mode), or group N (group mode).
Behavior is dependent on the content of register.**gen config**.bit[7:6], address.03h, page.00h and pin.**GRPLNMODE**.
The M21036 does not support group mode.
Threshold values in the table below are approximate and NOT guaranteed.

Bit(s)	Name	Description	Default	Type
[7:5]	los_thresh	Individual group/lane LOS threshold configuration when register.**losconfig**[7:6]=00b, address.08h, page.00h 000b: Minimum threshold 001b: ... 010b: ... 011b: Maximum threshold 100b: Reserved 101b: Reserved 110b: Reserved 111b: LOS complete power down	000b	R/W
[4]	oob_back_end	0b: Selects front end OOB circuit 1b: Selects back end OOB circuit	0b	R/W
[3:1]	Reserved	Reserved	000b	R/W
[0]	polflip	0b: Invert differential signal polarity + in → - out, - in → + out 1b: Normal differential signal passthrough + in → + out, - in → - out	1b	R/W

NOTES:

1. The M21024 has only 24 valid lane assignments and 6 valid group assignments. Valid addresses are [00h..17h] in lane mode, [00..05h] in group mode.
2. The M21048 has only 48 valid lane assignments and 12 valid group assignments. Valid addresses are [00h..2Fh] in lane mode, [00..0Bh] in group mode.
3. The M21036 has only 36 valid lane assignments. It has the same lane assignment as the M21048 without channels 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46.

5.9 Page 0Ch

Page: 0Ch

Address: HEX(0 + n) n=0...47
00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh 0Eh 0Fh 10h 11h 12h 13h 14h 15h 16h 17h 18h 19h 1Ah 1Bh 1Ch 1Dh 1Eh 1Fh
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh

Register Name: InEQ0

Default Value: 00'h

Description: Individual input equalizer control for input lane N (lane mode), or group N (group mode).
Behavior is dependent on the content of register.**gen config**.bit[7:6], address.03h, page.00h and pin.**GRPLNMODE**.
The M21036 does not support group mode.

Bit(s)	Name	Description	Default	Type
[7:5]	Reserved	Reserved		R/W
[4:0]	eq level	Individual input equalizer control when register.**gbinbuf**[6]=0b, address.09h, page.00h 00h: Minimum equalization level (~3 dB) 05h: Equalization level ~8 dB 07h: ... 09h: Equalization level ~12 dB 0Ah: Equalization level ~13 dB 0Bh: Equalization level ~15 dB 0Ch: Equalization level ~17 dB 0Fh: ... 10h: Equalization level ~19 dB 12h: Equalization level ~20 dB 14h: Equalization level ~22 dB 16h: ... 17h: Equalization level ~23 dB 19h: ... 1Bh: Equalization level ~24 dB 1Eh: ... 1Fh: Maximum equalization level(~27 dB)	00000b	R/W

NOTES:

1. The M21024 has only 24 valid lane assignments and 6 valid group assignments. Valid addresses are [00h..17h] in lane mode, [00..05h] in group mode.
2. The M21048 has only 48 valid lane assignments and 12 valid group assignments. Valid addresses are [00h..2Fh] in lane mode, [00..0Bh] in group mode.
3. The M21036 has only 36 valid lane assignments. It has the same lane assignment as the M21048 without channels 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46.
4. The equalization levels given are for a Nyquist frequency of 5.75 GHz or 11.5 Gbps operation. For other data rates and their Nyquist frequencies please extrapolate. For example, at 5.75 GHz we have the maximum equalization level of -27 dB, for a Nyquist frequency of 3.125 GHz (6.25 Gbps), the maximum equalization level would be ~14.7 dB.

5.10 Page 0Eh

Page: 0Eh

Address: HEX(0 + n) n=0...47
00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh 0Eh 0Fh 10h 11h 12h 13h 14h 15h 16h 17h 18h 19h 1Ah 1Bh 1Ch 1Dh 1Eh 1Fh
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh

Register Name: outbuf0

Default Value: 04'h

Description: Individual output buffer control for output lane N (lane mode), or group N (group mode).
Behavior is dependent on the content of register.**gen config**.bit[7:6], address.03h, page.00h and pin.**GRPLNMODE**.
The M21036 does not support group mode.
Output level swings tabled below are approximate and NOT guaranteed

Bit(s)	Name	Description	Default	Type
[7]	Reserved	Reserved	0b	R/W
[6:4]	outde_lvl	Individual de-emphasis level selection when register.**outputbuf**[7]=0b, address.0Bh, page.00h 000b: Output de-emphasis disabled 001b: Lowest de-emphasis setting (~1.5 dB) 010b: De-emphasis setting ~3 dB 011b: De-emphasis setting ~4.5 dB 100b: De-emphasis setting ~6 dB 101b: De-emphasis setting ~7.5 dB 110b: De-emphasis setting ~9 dB 111b: Highest de-emphasis setting ~10.5 dB	000b	R/W
[3]	Reserved	Reserved	0b	R/W
[2:1]	out_lvl	Individual output swing level selection when register.**outputbuf**[7]=0b, address.0Bh, page.00h 00b: Power down 01b: 600 mV_{PPD} Swing 10b: 800 mV_{PPD} Swing 11b: 1200 mV_{PPD} Swing	10b	R/W
[0]	outde_freq	Individual de-emphasis time constant selection when register.**outputbuf**[7]=0b, address.0Bh, page.00h 0b: Nominal boosting time constant 1b: 2x higher boosting time constant	0b	R/W

NOTES:

1. The M21024 has only 24 valid lane assignments and 6 valid group assignments. Valid addresses are [00h..17h] in lane mode, [00..05h] in group mode.
2. The M21048 has only 48 valid lane assignments and 12 valid group assignments. Valid addresses are [00h..2Fh] in lane mode, [00..0Bh] in group mode.
3. The M21036 has only 36 valid lane assignments. It has the same lane assignment as the M21048 without channels 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46.

5.11 Page 21h

Page: 21h
Address: 01h
Register Name: tempmont
Default Value: na
Description: Die top left and right temperature monitor readings.

Bit(s)	Name	Description	Default	Type
[7:4]	temp_tl	0000b: Die top left temperature reading – same definition as [3:0] below 1111b: ...		R
[3:0]	temp_tr	Die top right temperature reading. 0000b: T_{CASE} < -45 °C 0001b: Range T_{CASE} [-45 : -40] °C 0010b: Range T_{CASE} [-40 : -30] °C 0011b: Range T_{CASE} [-30 : -25] °C 0100b: Range T_{CASE} [-25 : -10] °C 0101b: Range T_{CASE} [-10 : 20] °C 0110b: Range T_{CASE} [20 : 35] °C 0111b: Range T_{CASE} [35 : 50] °C 1000b: Range T_{CASE} [50 : 65] °C 1001b: Range T_{CASE} [65 : 80] °C 1010b: Range T_{CASE} [80 : 95] °C 1011b: Range T_{CASE} [95 : 110] °C 1100b: Range T_{CASE} [110 : 115] °C 1101b: Range T_{CASE} [115 : 125] °C 1110b: Range T_{CASE} [125 : 130] °C 1111b: Range T_{CASE} > 130 °C		R

NOTES:

1. Temperature values are approximate, and are NOT guaranteed.

Page: 21h
Address: 02h
Register Name: tempmonb
Default Value: na
Description: Die bottom left and right temperature monitor readings.

Bit(s)	Name	Description	Default	Type
[7:4]	temp_bl	0000b: Die bottom left temperature reading – same definition as in register.**tempmont**, address.01h, page.21h [3:0]		R
[3:0]	temp_br	0000b: Die bottom right temperature reading – same definition as in register.**tempmont**, address.01h, page.21h [3:0]		R

NOTES:

1. Temperature values are approximate, and are NOT guaranteed.

Page: 21h
Address: 0Ah
Register Name: out_debug0
Default Value: F4'h
Description: Global switch and output offset correction loop selection for all lanes.
Select external aux high speed input or prbs generator
Enable aux test circuitry

Bit(s)	Name	Description	Default	Type
[7:4]	Reserved	Reserved	1b	R/W
[3]	test_insel	Test input channel select 0b: Select auxiliary high speed test input (testinp/m) 1b: Select on-chip prbs generator	0b	R/W
[2]	pd_afe_test	ob: enable afe_cdr testability 1b: disable afe_cdr testability	1b	R/W
[1:0]	Reserved	Reserved	00b	R/W

Page: 21h
Address: 1Fh
Register Name: hs_aux_chsel
Default Value: 3F'h
Description: Selects which of the available lanes is directed to the high speed auxiliary output.

Bit(s)	Name	Description	Default	Type
[7:6]	hs_aux_en	00b: Enable the high speed auxiliary lane circuitry	00b	R/W
[5:0]	chsel	Select which switching core output lane is to be routed to the auxiliary output lane 000000b: Select switch core output 0 000001b: Select switch core output 1 000010b: Select switch core output 2 000011b: Select switch core output 3 000100b: Select switch core output 28 000101b: Select switch core output 29 (not available for M21036) 000110b: Select switch core output 30 (not available for M21036) 000111b: Select switch core output 31 001000b: Select switch core output 24 001001b: Select switch core output 25 (not available for M21036) 001010b: Select switch core output 26 (not available for M21036) 001011b: Select switch core output 27 001100b: Select switch core output 4 001101b: Select switch core output 5 001110b: Select switch core output 6 001111b: Select switch core output 7 010000b: Select switch core output 8 010001b: Select switch core output 9 010010b: Select switch core output 10 010011b: Select switch core output 11 010100b: Select switch core output 36 010101b: Select switch core output 37 (not available for M21036) 010110b: Select switch core output 38 (not available for M21036) 010111b: Select switch core output 39 011000b: Select switch core output 32 011001b: Select switch core output 33 (not available for M21036) 011010b: Select switch core output 34 (not available for M21036) 011011b: Select switch core output 35 011100b: Select switch core output 12 011101b: Select switch core output 13 011110b: Select switch core output 14 011111b: Select switch core output 15 100000b: Select switch core output 16	111111b	R/W

Bit(s)	Name	Description	Default	Type
[5.0] (cont.)		100001b: Select switch core output 17 100010b: Select switch core output 18 100011b: Select switch core output 19 100100b: Select switch core output 44 100101b: Select switch core output 45 (not available for M21036) 100110b: Select switch core output 46 (not available for M21036) 100111b: Select switch core output 47 (last core output to be monitored in M21048 & M21036) 101000b: Select switch core output 40 101001b: Select switch core output 41 (not available for M21036) 101010b: Select switch core output 42 (not available for M21036) 101011b: Select switch core output 43 101100b: Select switch core output 20 101101b: Select switch core output 21 101110b: Select switch core output 22 101111b: Select switch core output 23 (last core output to be monitored in M21024) 111111b: Power down auxiliary lane		

Page: 21h
Address: 80h
Register Name: hs_aux_squelch
Default Value: 1F'h
Description: High speed auxiliary lane enable/disable, OOB and squelch control.

Bit(s)	Name	Description	Default	Type
[7:6]	Reserved	Reserved	00b	R/W
[5:3]	cht_oob_vcm_dac	000b: Minimum OOB threshold detection 011b: Normal operation 111b: Maximum OOB threshold detection	011b	R/W
[2:1]	cht_sq_level	Squelch level selection for the high speed auxiliary lane 00b: Reserved 01b: Output H on squelch (recommended for DC coupled cases) 10b: Output L on squelch (recommended for DC coupled cases) 11b: Output EI level (common mode) on squelch (recommended for AC coupled cases)	11b	R/W
[0]	cht_dis	Power down the high speed auxiliary lane 0b: Enable the high speed auxiliary lane equalizer 1b: Disable the high speed auxiliary lane equalizer	1b	R/W

Page: 21h
Address: 81h
Register Name: hs_aux_ei
Default Value: 00'h
Description: Auxiliary lane EI pass-through control.

Bit(s)	Name	Description	Default	Type
[7]	Reserved	Reserved	0b	R/W
[6]	ebi_en	High speed auxiliary lane EI pass through enable 0b: Disable electrical bus idle state pass through 1b: Enable electrical bus idle state pass through	0b	R/W
[5:4]	Reserved	Reserved	00b	R/W
[3]	ebi_fe	Selects front end or back end EI detection 00b: EI detection on front end 10b: EI detection on back end	00b	R/W
[2:0]	Reserved	Reserved	0b	R/W

Page: 21h
Address: 82h
Register Name: hs_aux_los
Default Value: 38'h
Description: High-speed auxiliary lane LOS alarm configuration (threshold, calibration, delay…)

Bit(s)	Name	Description	Default	Type
[7]	Reserved	Reserved	0b	R/W
[6]	LOS enable	High speed auxiliary lane LOS enable 0b: Disables LOS detection 1b: Enables LOS detection	0b	R/W
[5:3]	LOS threshold	High speed auxiliary lane LOS threshold configuration 000b: Minimum threshold detection level 001b: ... 010b: ... 011b: ... 100b: ... 101b: ... 110b: Maximum threshold detection level 111b: Power down the LOS detection circuit	111b	R/W
[2]	Reserved	Reserved	0b	R/W
[1]	LOS delay	High speed auxiliary lane LOS time constant 0b: Declare LOS after approx 5 µs of no data 1b: Declare LOS after approx 1 µs of no data	0b	R/W
[0]	Reserved	Reserved	0b	R/W

Page: 21h
Address: 83h
Register Name: hs_aux_term
Default Value: 00'h
Description: High speed auxiliary lane input termination control.

Bit(s)	Name	Description	Default	Type
[7:6]	Reserved	Reserved	00b	R/W
[5:4]	cht_gbl_inbuf	11b: Enable input with source termination 10b: Enable input with High-Z input source termination 01b: Power down with source termination 00b: Power down and high-Z termination	00b	R/W
[3:0]	Reserved	Reserved	0000b	R/W

Page: 21h
Address: 84h
Register Name: hs_aux_eq
Default Value: 00'h
Description: High speed auxiliary lane equalizer control.

Bit(s)	Name	Description	Default	Type
[7:5]	Reserved	Reserved		R/W
[4:0]	cht_eq_level	00h: Minimum equalization level (~3 dB) 05h: Equalization level ~8 dB 07h: ... 09h: Equalization level ~12 dB 0Ah: Equalization level ~13 dB 0Bh: Equalization level ~15 dB 0Ch: Equalization level ~17 dB 0Fh: ... 10h: Equalization level ~19 dB 12h: Equalization level ~20 dB 14h: Equalization level ~22 dB 16h: ... 17h: Equalization level ~23 dB 19h: ... 1Bh: Equalization level ~24 dB 1Eh: ... 1Fh: Maximum equalization level (~27 dB)		R/W

NOTES:

1. The equalization levels given are for a Nyquist frequency of 5.75 GHz or 11.5 Gbps operation. For other data rates and their Nyquist frequencies please extrapolate. For example, at 5.75 GHz we have the maximum equalization level of -27 dB, for a Nyquist frequency of 3.125 GHz (6.25 Gbps), the maximum equalization level would be ~14.7 dB.

Page: 21h
Address: 91h
Register Name: hs_aux_driver
Default Value: 00'h
Description: High speed auxiliary output driver control.

Bit(s)	Name	Description	Default	Type
[7]	testout_en	0b: Auxiliary Output Disabled 1b: Auxiliary Output Enabled	0b	R/W
[6:4]	outde_lvl	High speed auxiliary output de-emphasis level selection 000b: Output de-emphasis disabled 001b: Lowest de-emphasis setting (~1.5 dB) 010b: De-emphasis setting ~3 dB 011b: De-emphasis setting ~4.5 dB 100b: De-emphasis setting ~6 dB 101b: De-emphasis setting ~7.5 dB 110b: De-emphasis setting ~9.5 dB 111b: Highest de-emphasis setting ~10.5 dB	000b	R/W
[3]	Reserved	Reserved	0b	R/W
[2:1]	out_lvl	High speed auxiliary output swing level selection 00b: Power down 01b: 600 mV_{PPD} Swing 10b: 800 mV_{PPD} Swing 11b: 1200 mV_{PPD} Swing	00b	R/W
[0]	OutDE_freq	High speed auxiliary de-emphasis time constant selection 0b: Nominal boosting time constant 1b: 2x higher boosting time constant		R/W

Page: 21h
Address: A0h
Register Name: dvddo_drv
Default Value: 00'h
Description: digital_io drive select register

Bit(s)	Name	Description	Default	Type
[7:4]	Reserved	Reserved	0000b	R/W
[3]	drv_mon	0b: Normal operation 1b: Monitor output drive select at pin.**xALARM**	0b	R/W
[2]	RSVD	Reserved	0b	R/W
[1:0]	force_high_low	00b: Automatic DV_{DDO} detection enabled 10b: Force high output drive 1b: Force standard output drive	00b	R/W

5.12 Page 22h

Page: 22h
Address: 00h
Register Name: Aux Input channel config_reg1
Default Value: 00'h
Description: Power down control of the prbs generator and checker.

Bit(s)	Name	Description	Default	Type
[7]	en_gen_check	0b: Power down the prbs generator and checker 1b: Enable the prbs generator and checker	0b	R/W
[6:0]	Reserved	0b: Unused 1b: Unused	0b	R/W