

MXP-100G

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20170521

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CHANGE NOTE						
APPRO.AUTHO.						
ORIGINATOR						
MXP-100G						1/46

BATTERY INPUT 1

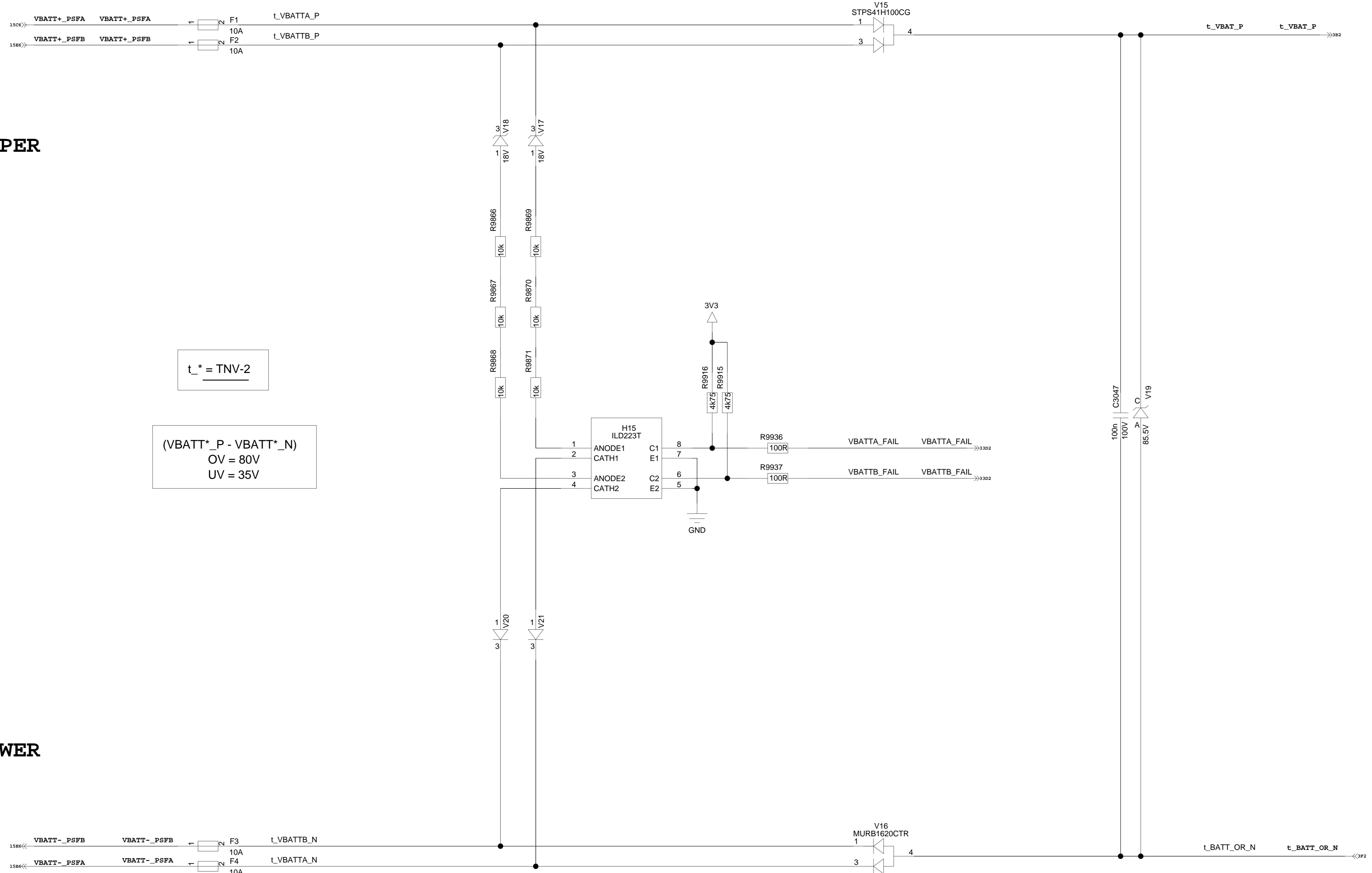
UPPER

BACKPLANE

LOWER

/BATT*_P - VBATT*_N
OV = 80V
UV = 35V

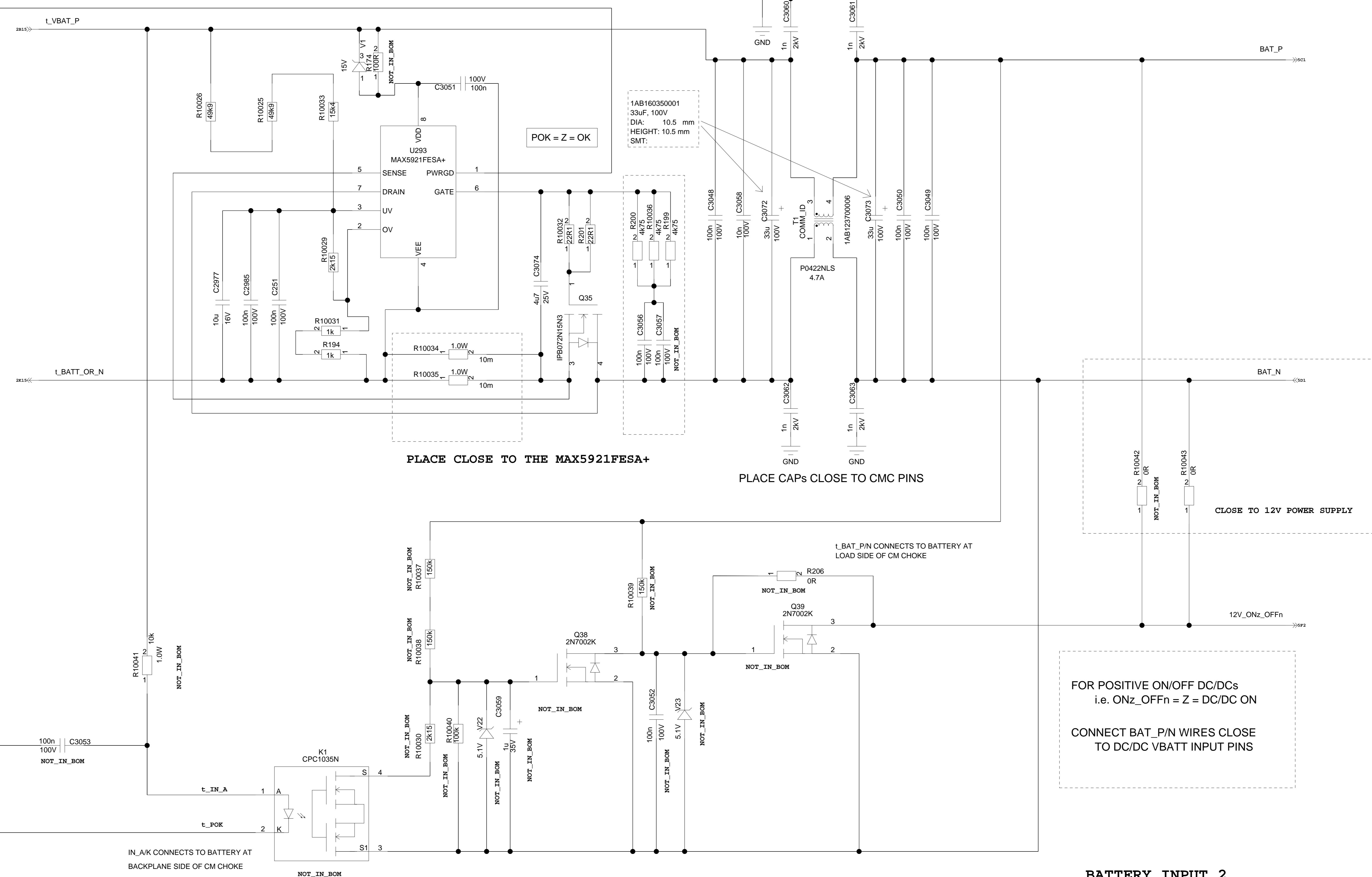
$$t_{-}^{*} = \frac{TNV-2}{2}$$



BATTERY INPUT 1

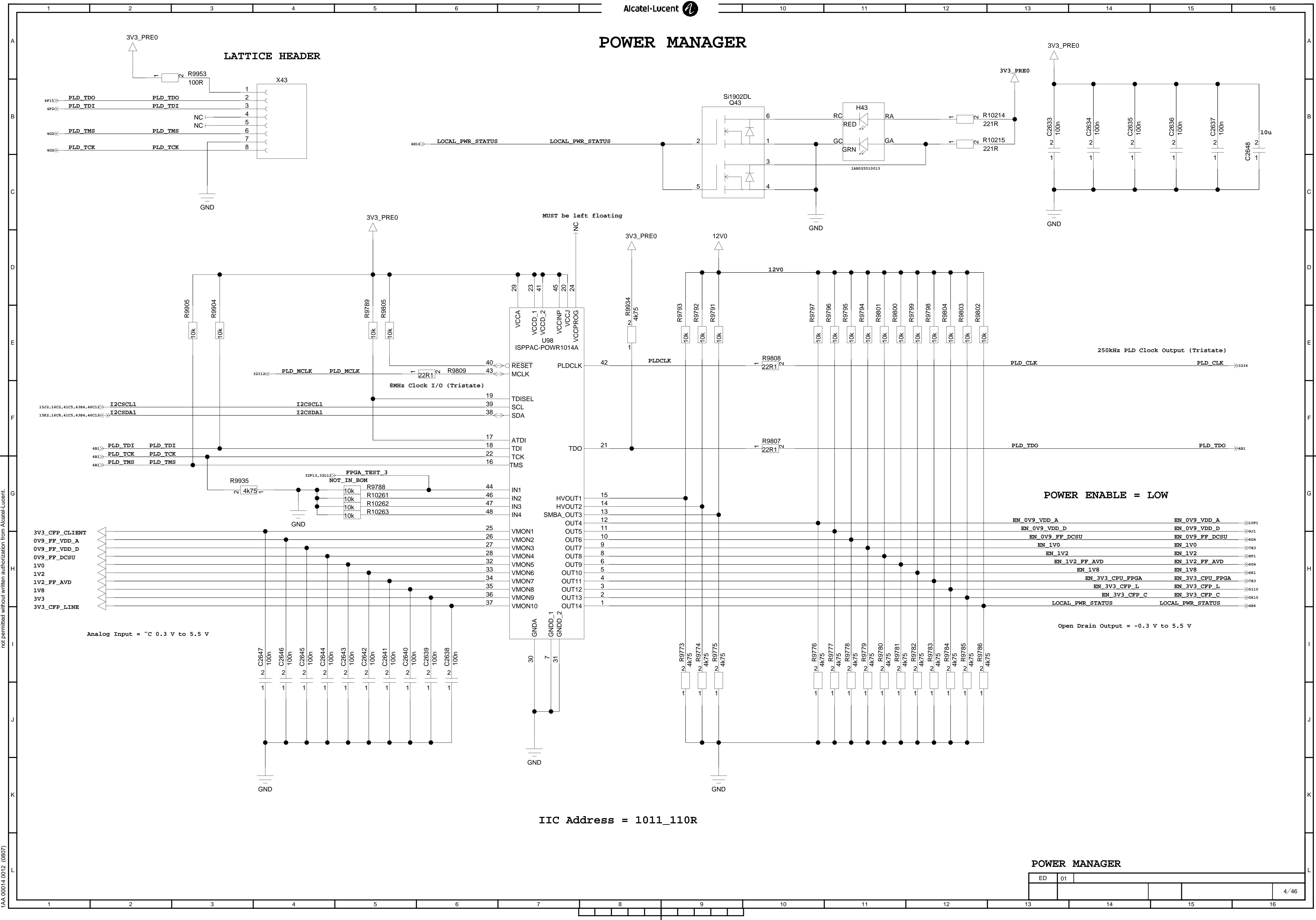
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BATTERY INPUT 2



POWER MANAGER

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POS LOGIC

PRIMARY POWER 1V8,1V2_FF,0V9_DCSU

LOCATE CLOSE TO MODULE

$$V_{out} = (1184/R) + 0.592 = 1.814V$$

With OCP,OTP Protection

4H16 » EN_1V2_FF_AVD EN_1V2_FF_AVD 2 R9980 1k 2

4H16 » EN_0V9_FF_DCSU EN_0V9_FF_DCSU 2 R9981 1k 5

Si1902DL Q37

6 1 3 4

R9982 1k 2 1

R9983 1k 2 1

GND

POS LOGIC

$$ut = 0.5 * (1 + R2/R3) = 1.2V$$


 $V_{out} = 0.5 * (1 + R_2/R_3)$
SET = LOW = Core SLOW V = 0.925V
SET = HIGH = Core FAST V = 0.875V

ANSWER

CM1502DL
Q6

CLOSE TO U296

10J1, 32E13, 9K7, 9L1

ED 01

1V8_PRE

5A

Q34
FDMS8460

R9842
1k

C2655
10u

V14
15V

C2659

C2660

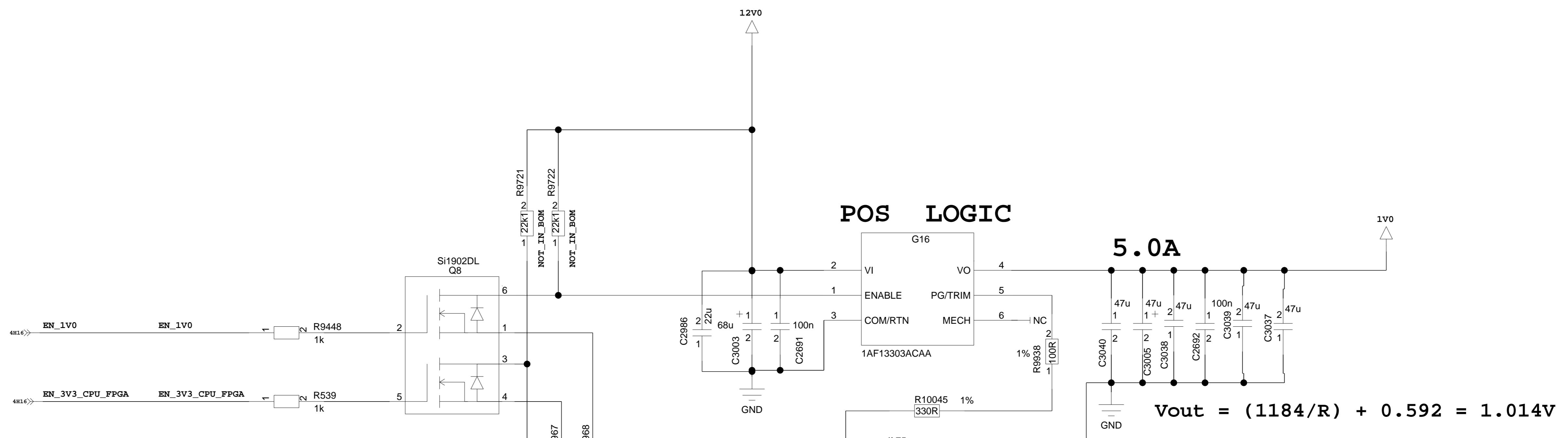
C2664
100n

GND

GND

5A

PRIMARY POWER 1V0, 3V3

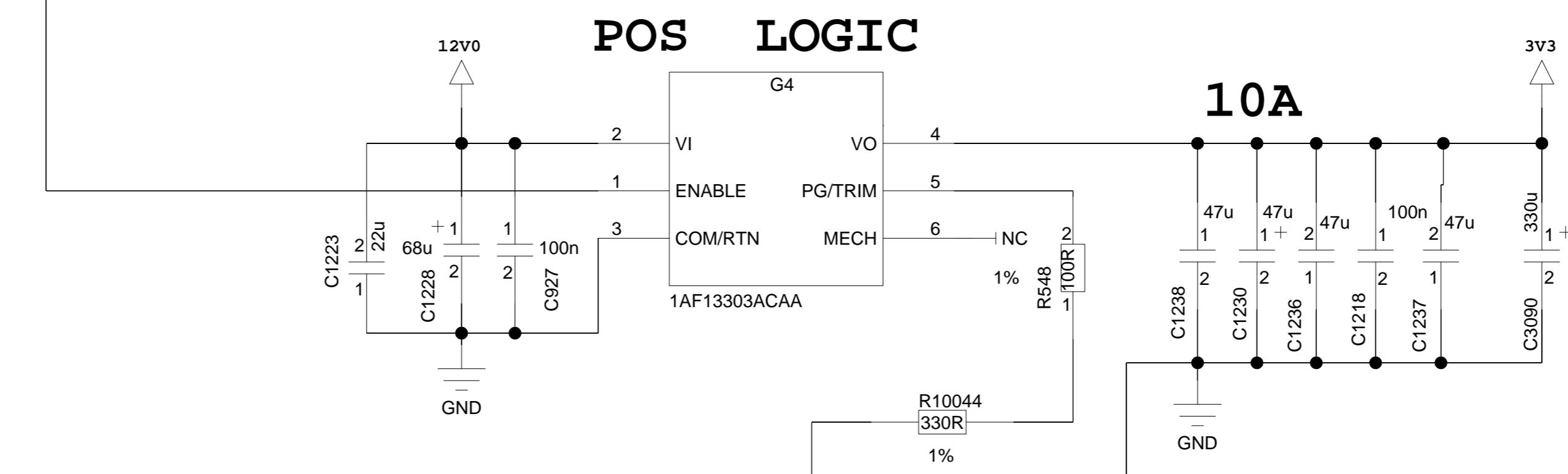


5.0A

$$V_{out} = (1184/R) + 0.592 = 1.014V$$

With OCP,OTP Protection

POS LOGIC



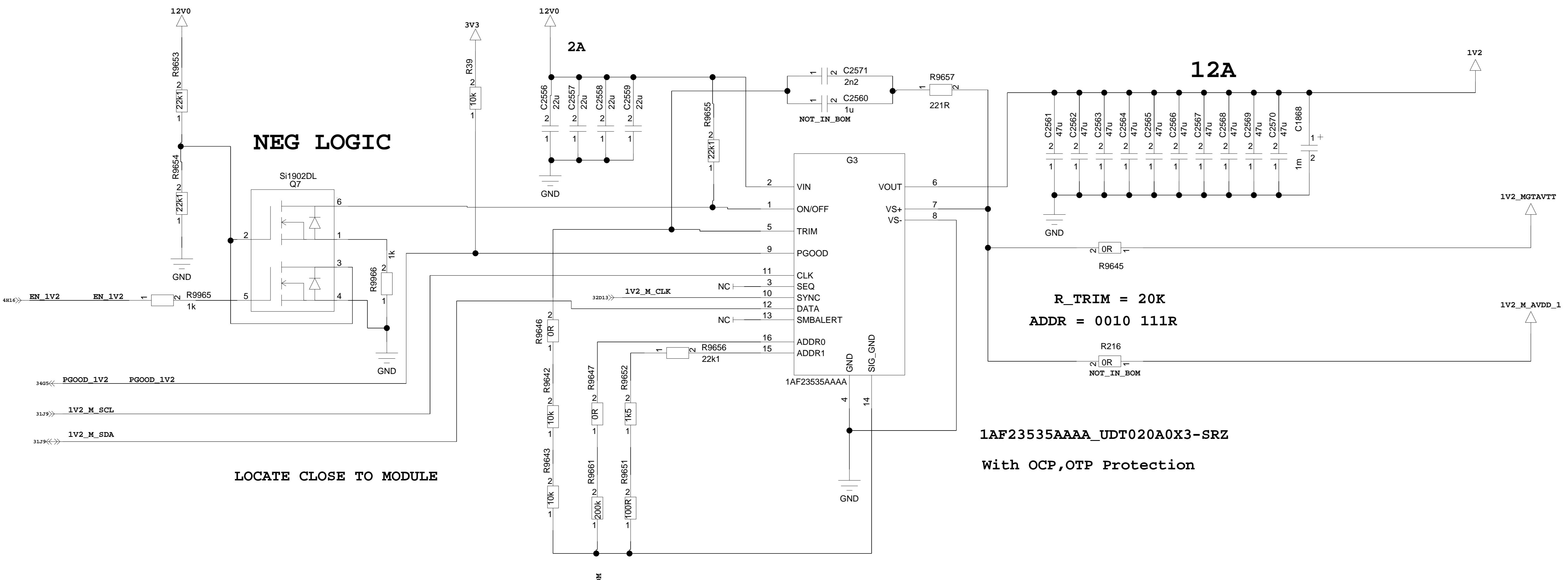
LOCATE CLOSE TO MODULE With OCP,OTP Protection

$$V_{out} = (1184/R) + 0.592 = 3.345V$$

PRIMARY POWER 1V0, 3V3

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R9661 IS JUST FOR IIC TEST USAGE

PRIMARY POWER 1V2

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FLEXFRAMER POWER SUPPLY 1

Sense Path if FF is not assembled

GND

CP,OTP Protection

HIGH = GOOD

SET = LOW = Core SLOW V = 0.925V
SET = HIGH = Core FAST V = 0.875V

FLEXFRAMER POWER SUPPLY 1

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With OCP,OTP Protection
MDT040A0X3-SRPHZ SYNC Min 510k, typ k, 720k
SLDN-40E1AT SYNC Min 320k, typ k, Max 480k

NEG LOGIC

ADDR = 0010 000R

LOCATE CLOSE TO MODULE

HIGH = GOOD

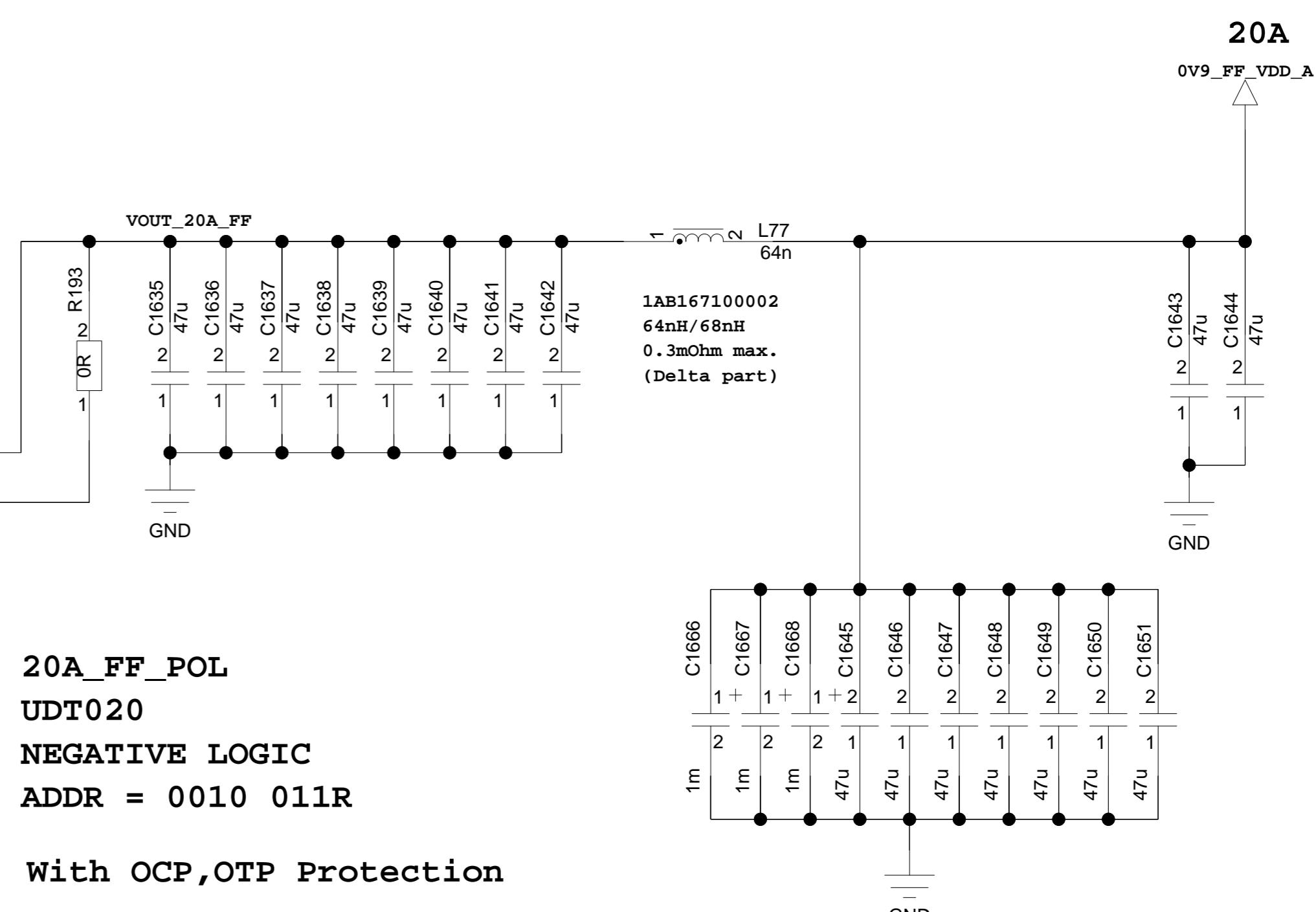
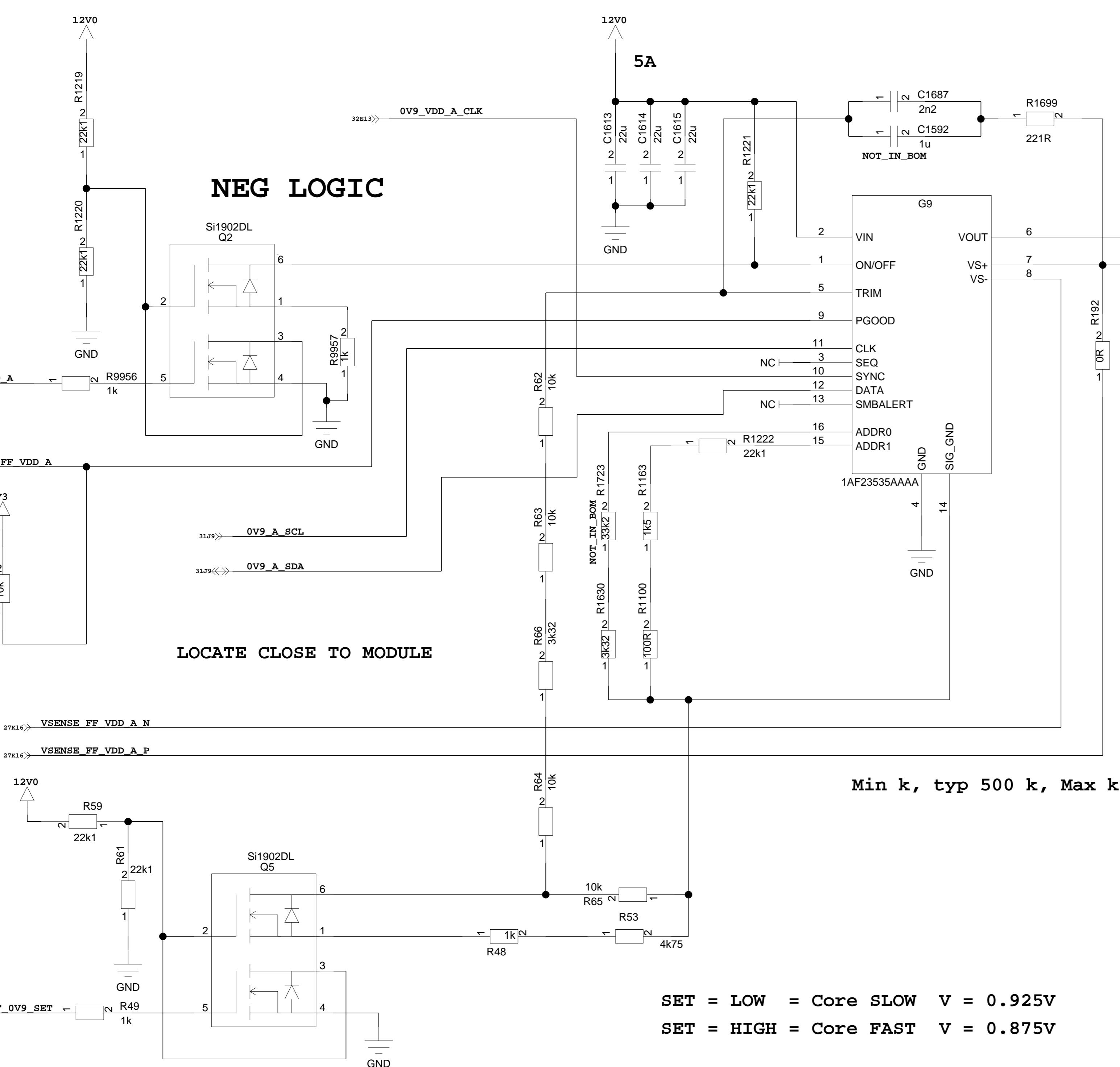
PGOOD_0V9_FF_VDD_D_2

MFP POWER SUPPLY 1

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11AAA 00014 0012 (0807)

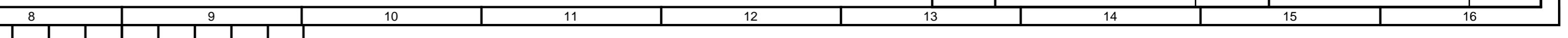
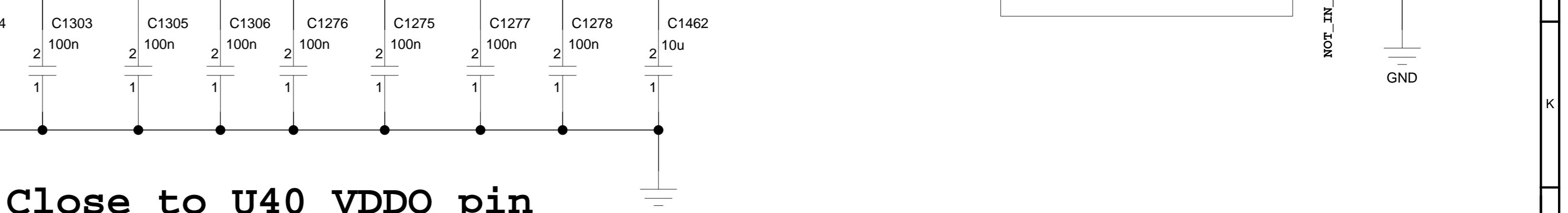
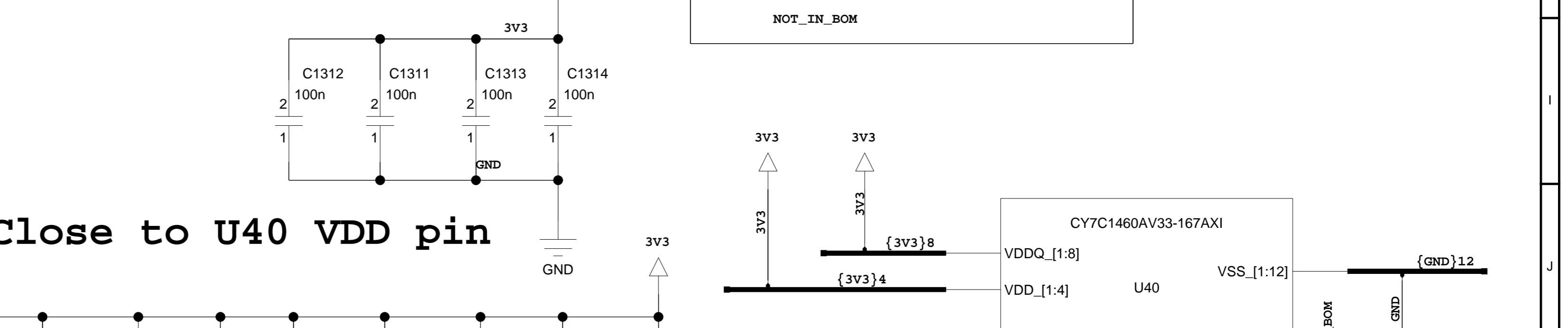
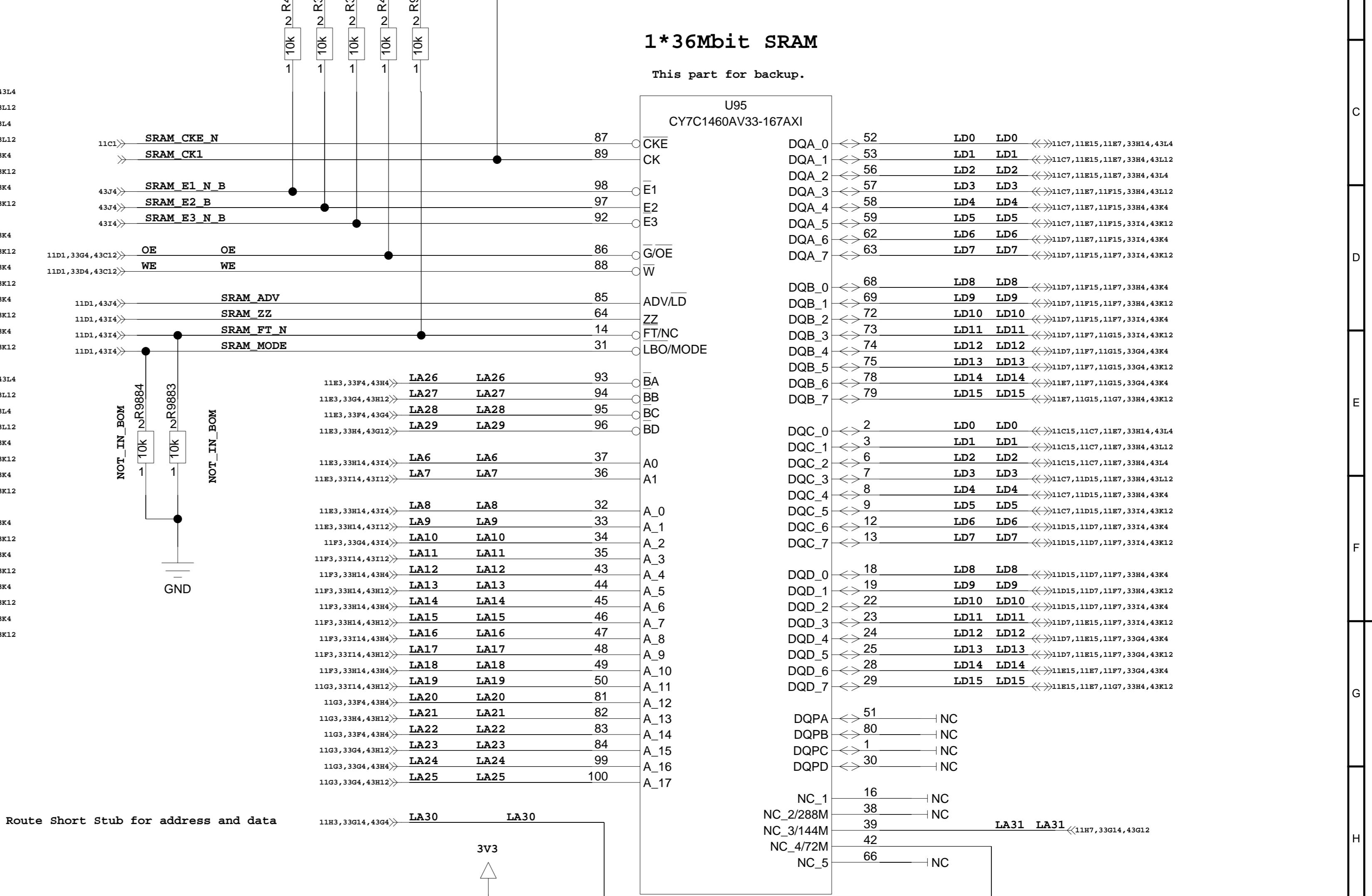
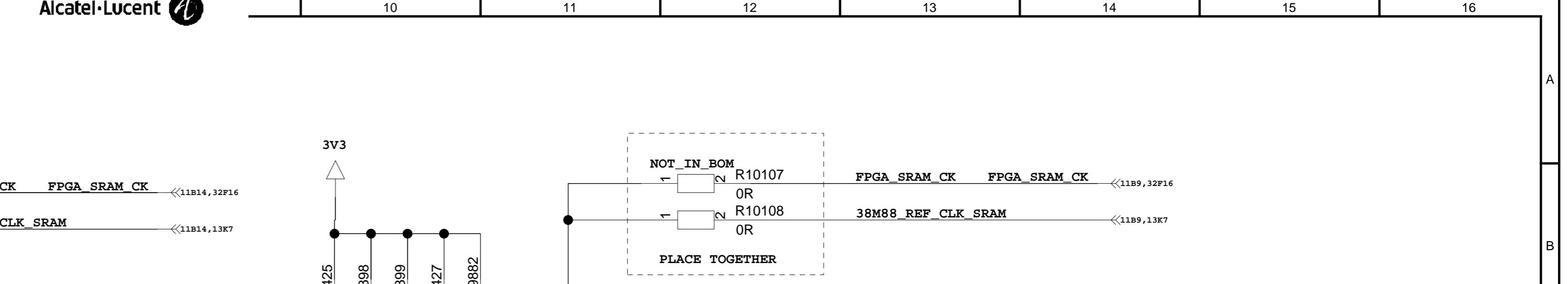
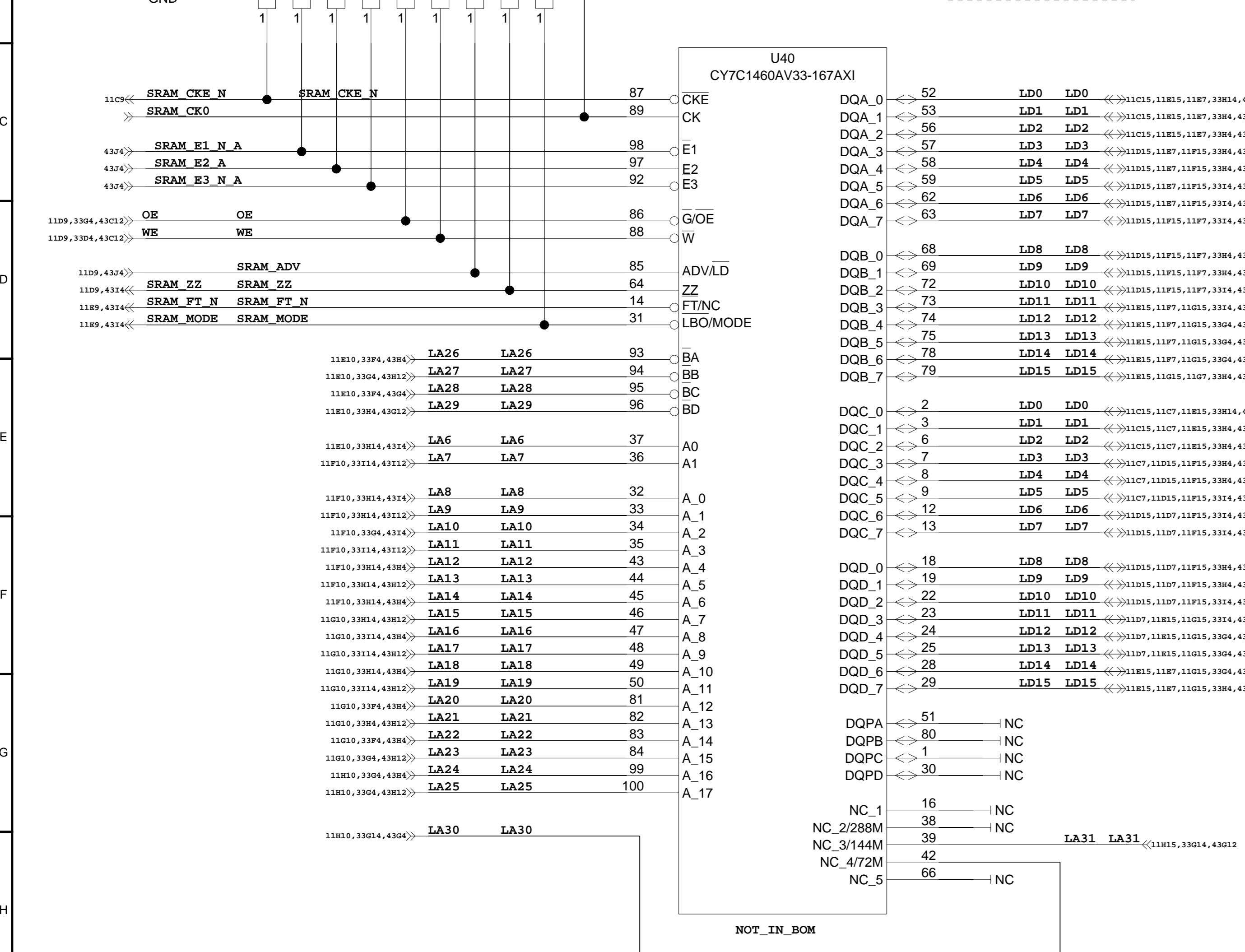
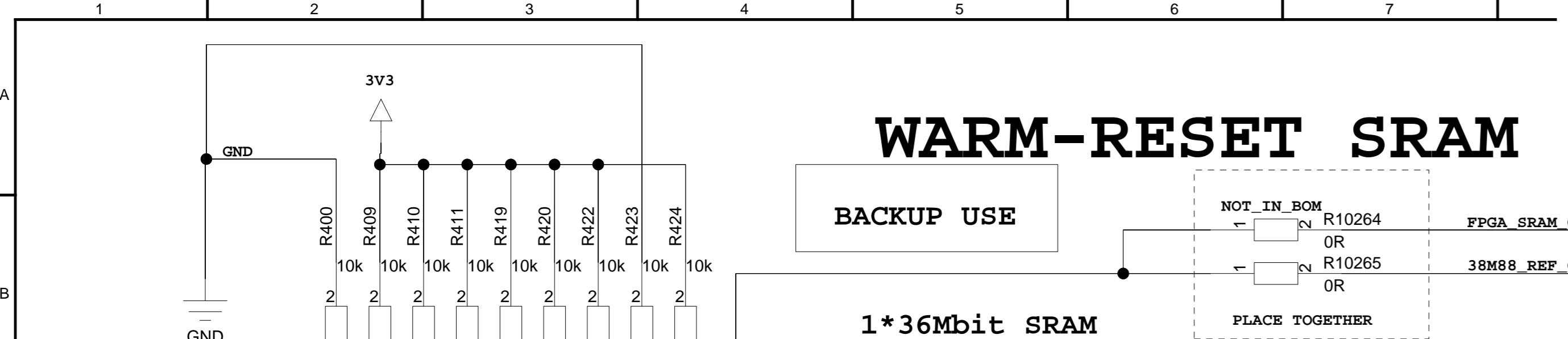
FLEXFRAMER POWER SUPPLY 2



NOTE for G9 (UDT020):

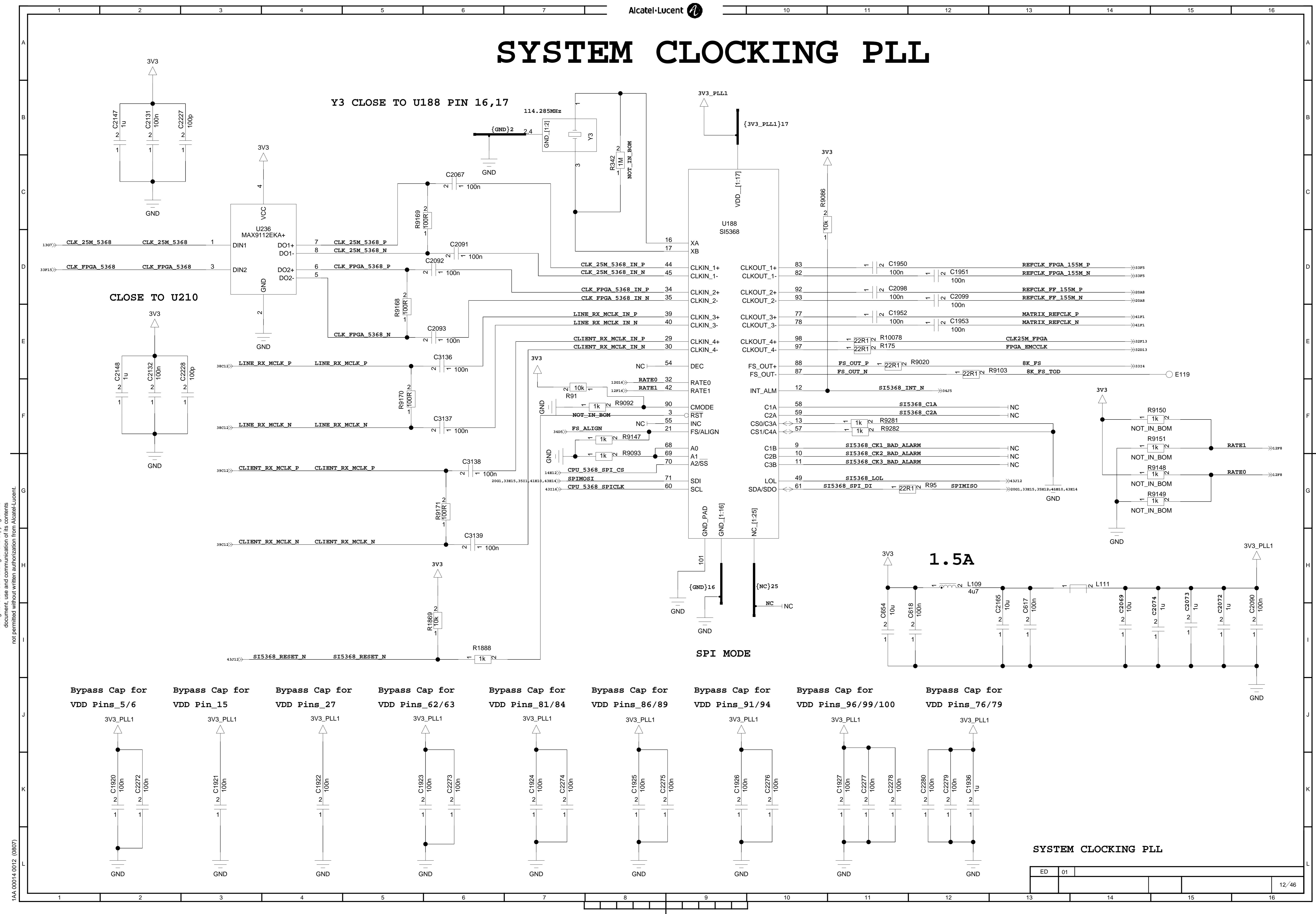
Sensitive, high-impedance, analog pins
TRIM and SIG_GND on the one hand side
and digital traces CLK, DATA and SMBALERT
on the other hand side, have to be separated
as good/far as possible in the layout!

R1723 IS JUST FOR IIC TEST USAGE



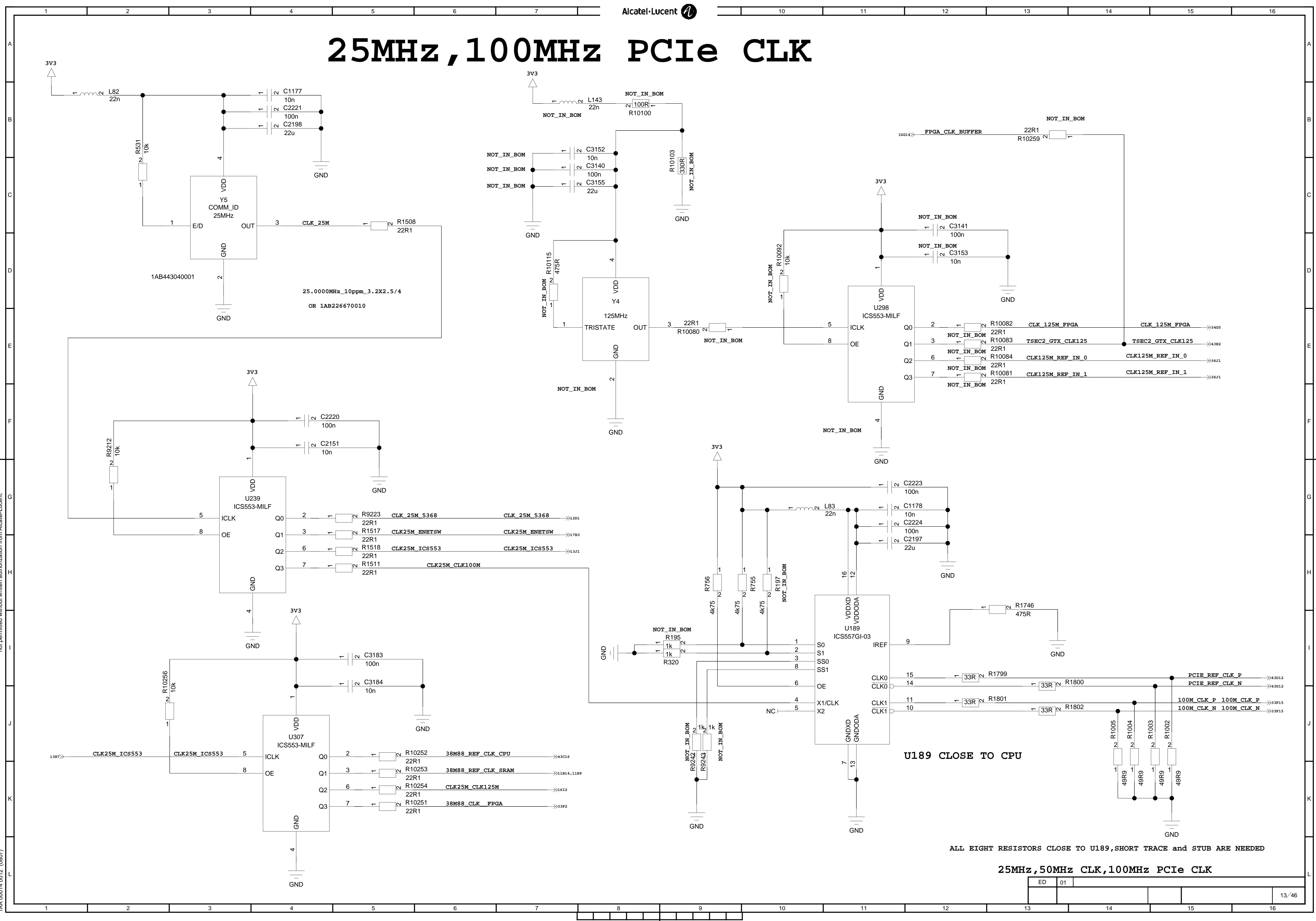
SYSTEM CLOCKING PLL

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25MHz, 100MHz PCIe CLK

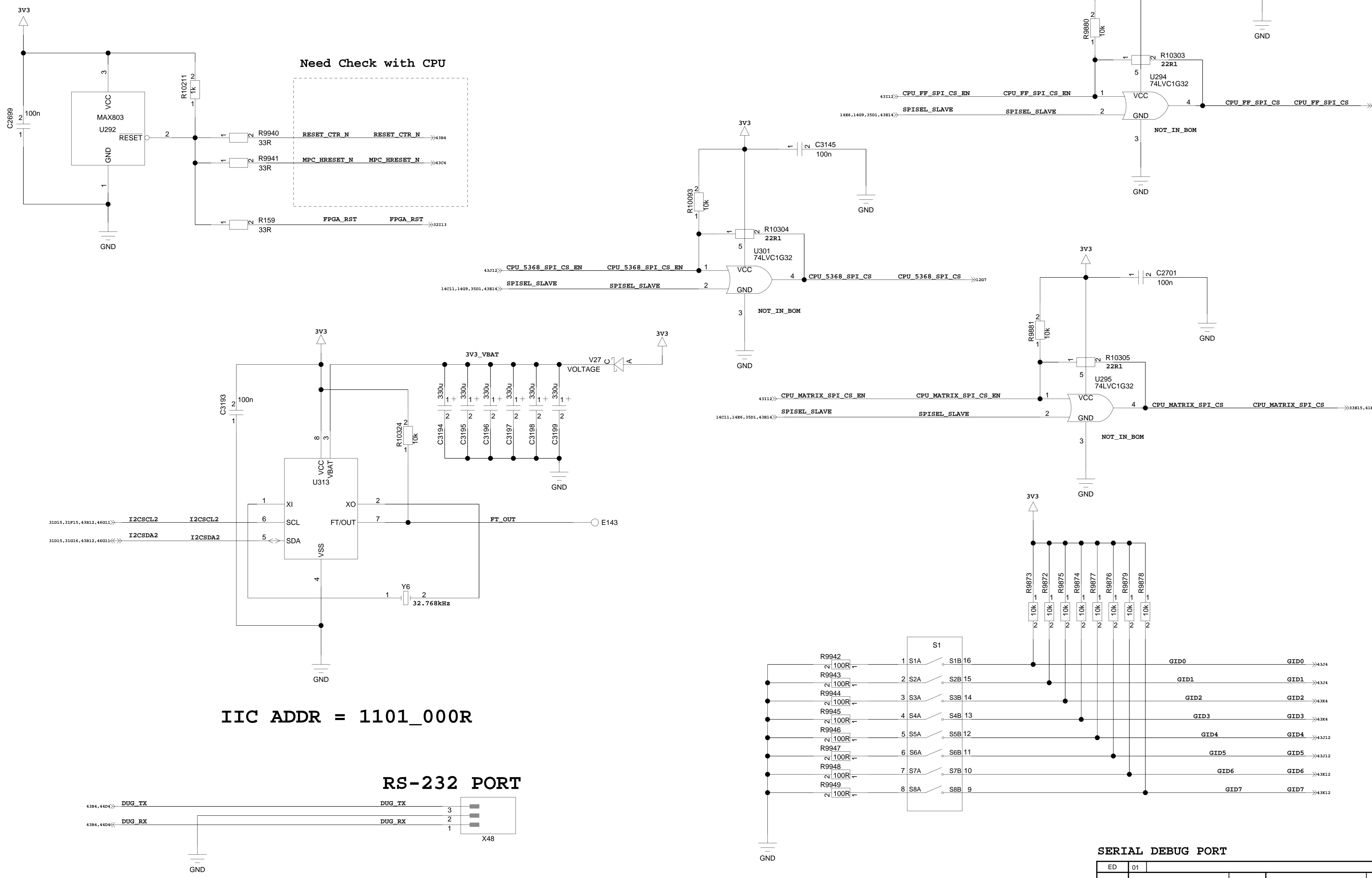
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SERIAL DEBUG PORT

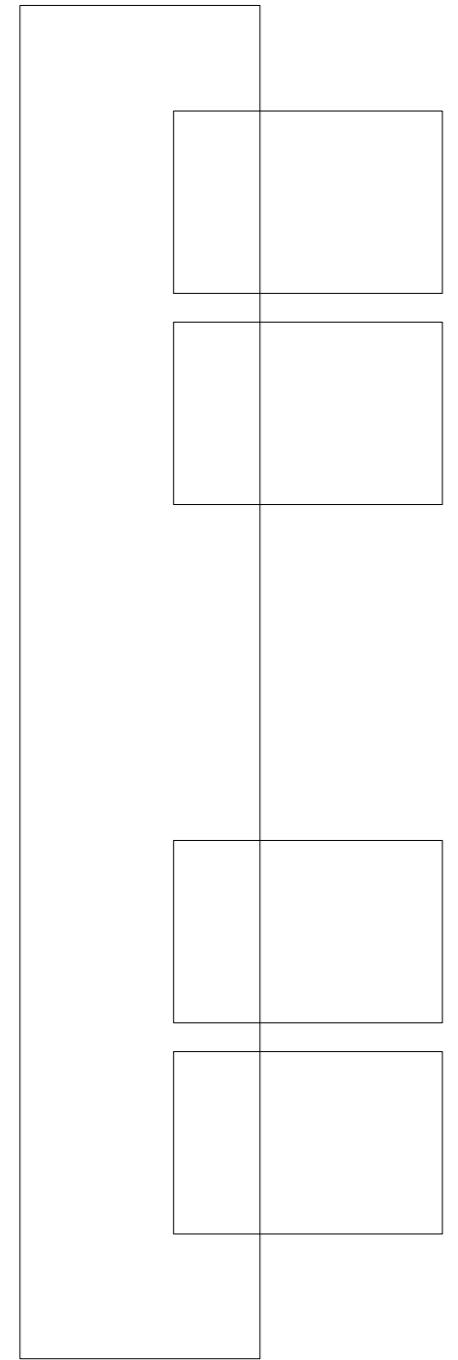
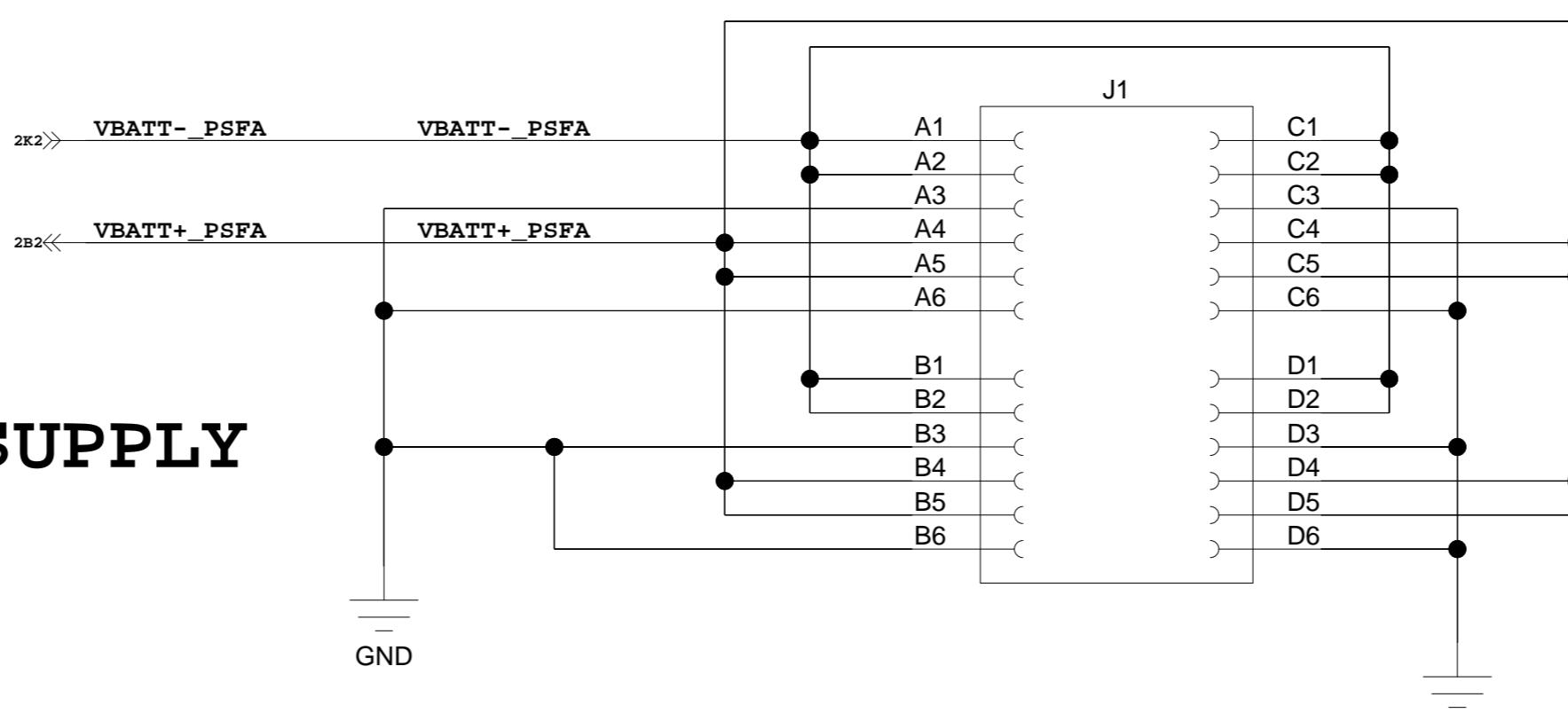
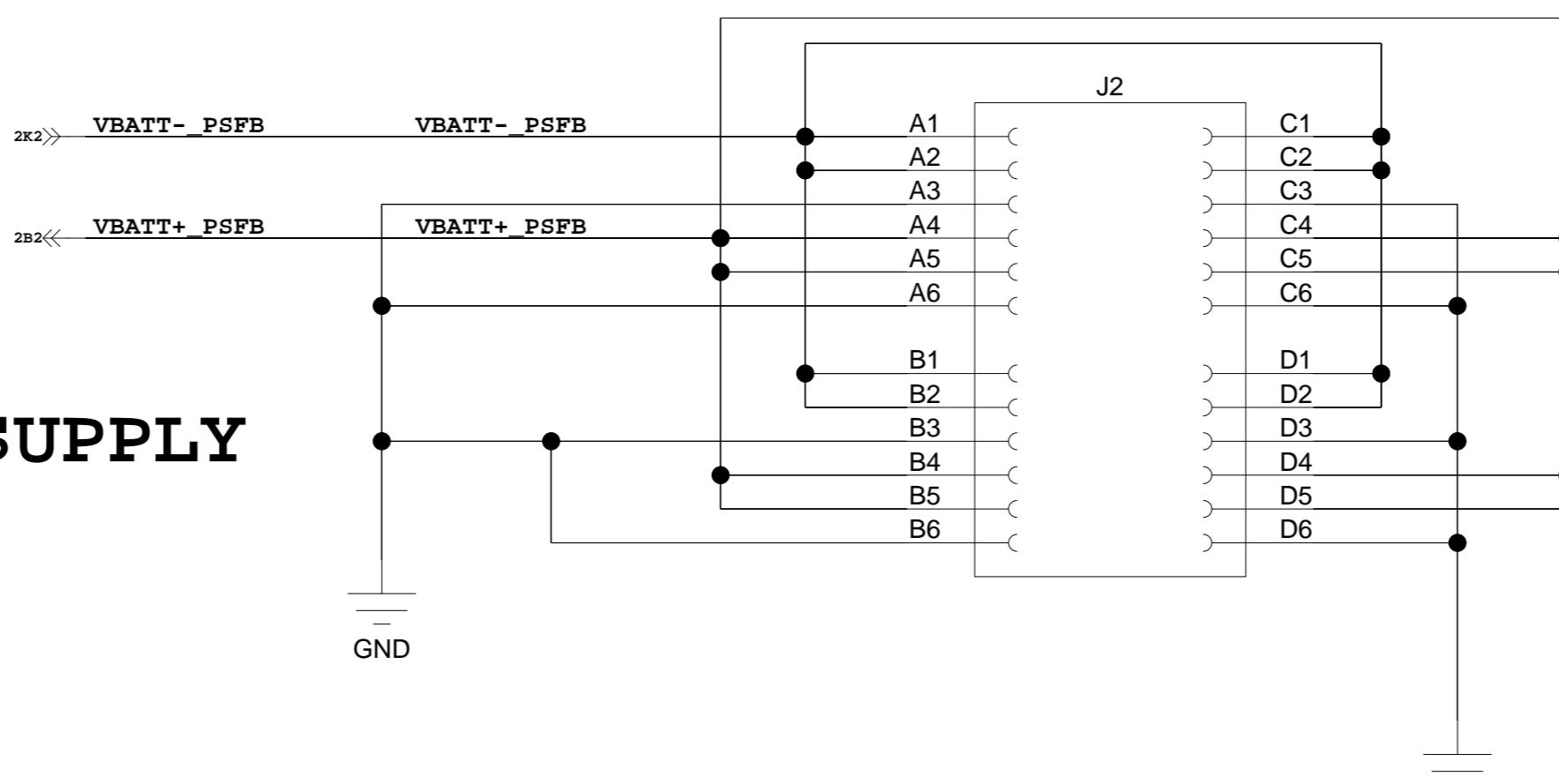
IIC ADDR = 1101_000R

RS-232 PORT

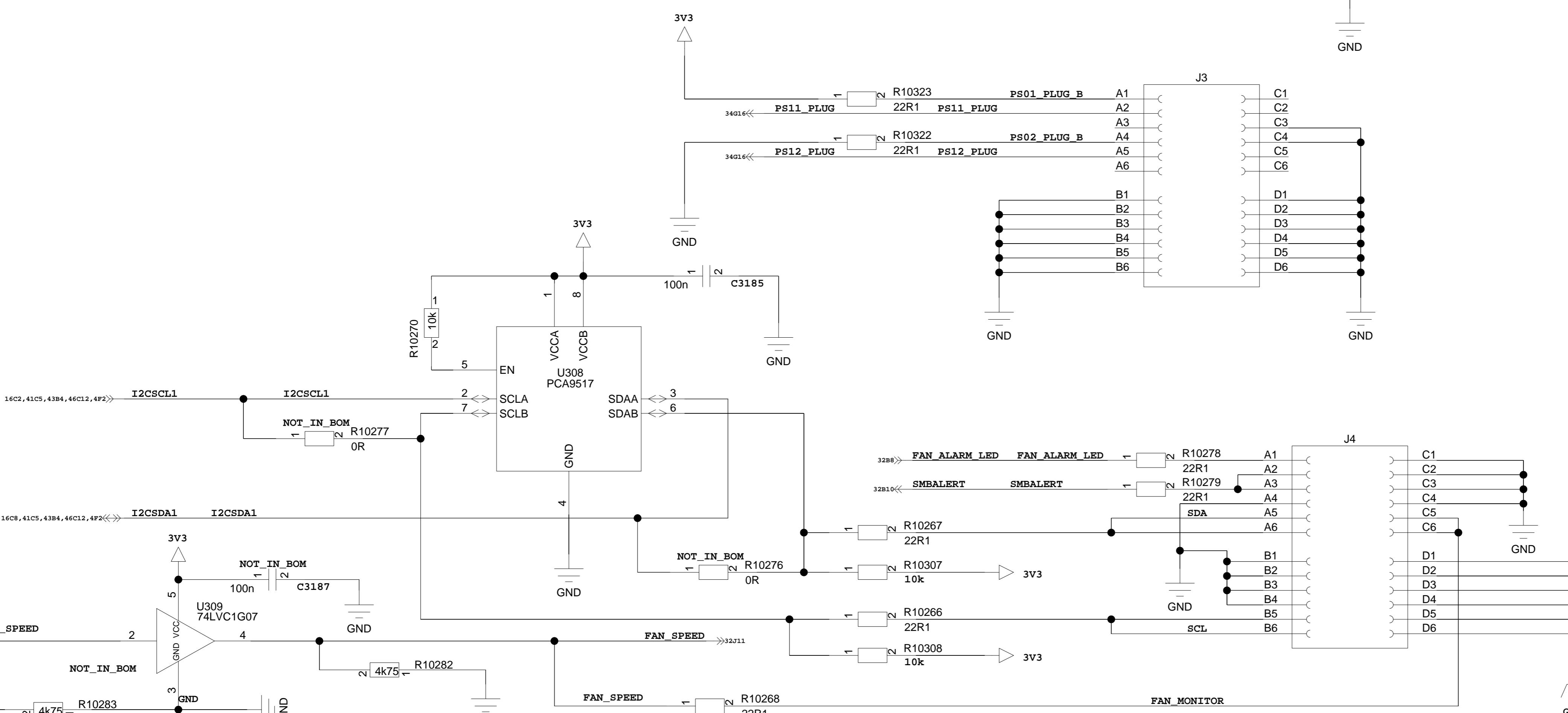


A B C D E F G H I J K L

MAIN BOARD BACKPLANE CONNECTOR LOCATION

**J1****J2****J3****J4****POWER A SUPPLY****POWER B SUPPLY**

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**BATTERY POWER CONNECTOR**

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REMOTE INVENTORY, I2C BUS TRANSLATOR & TEST HEADER

1AB195600005

I2C ADDRESS = 1010 010R

$$V_{out} = 0.5 * (1 + R2/R3) = 2.5V$$

U5 FOR FPGA GTP REFERENCE

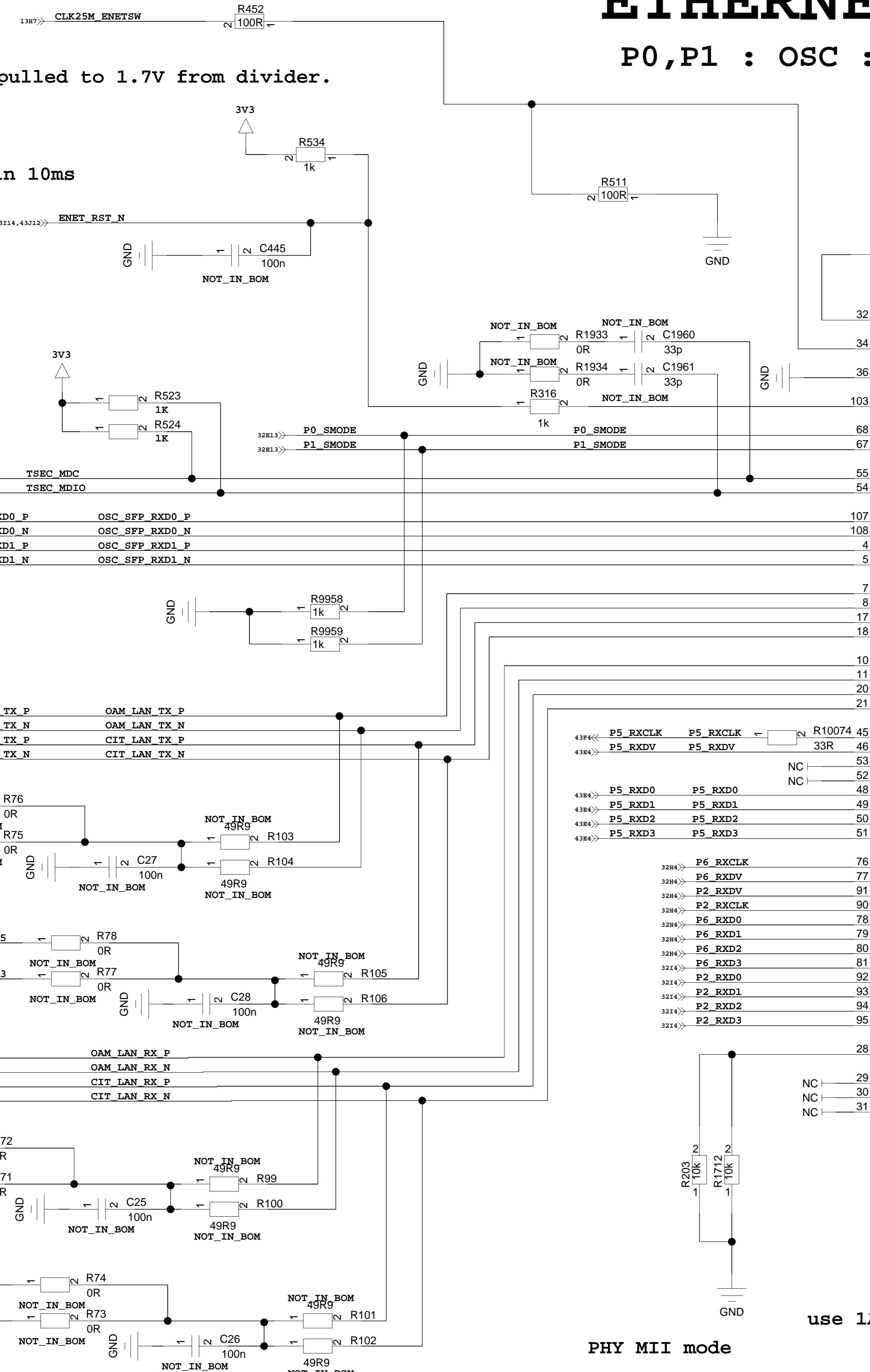
REMOTE INVENTORY

ETHERNET SWITCH

P0, P1 : OSC : 100BASE-FX / 1000BASE-X

CLK25M_ENETSW pulled to 1.7V from divider.

Min 10ms

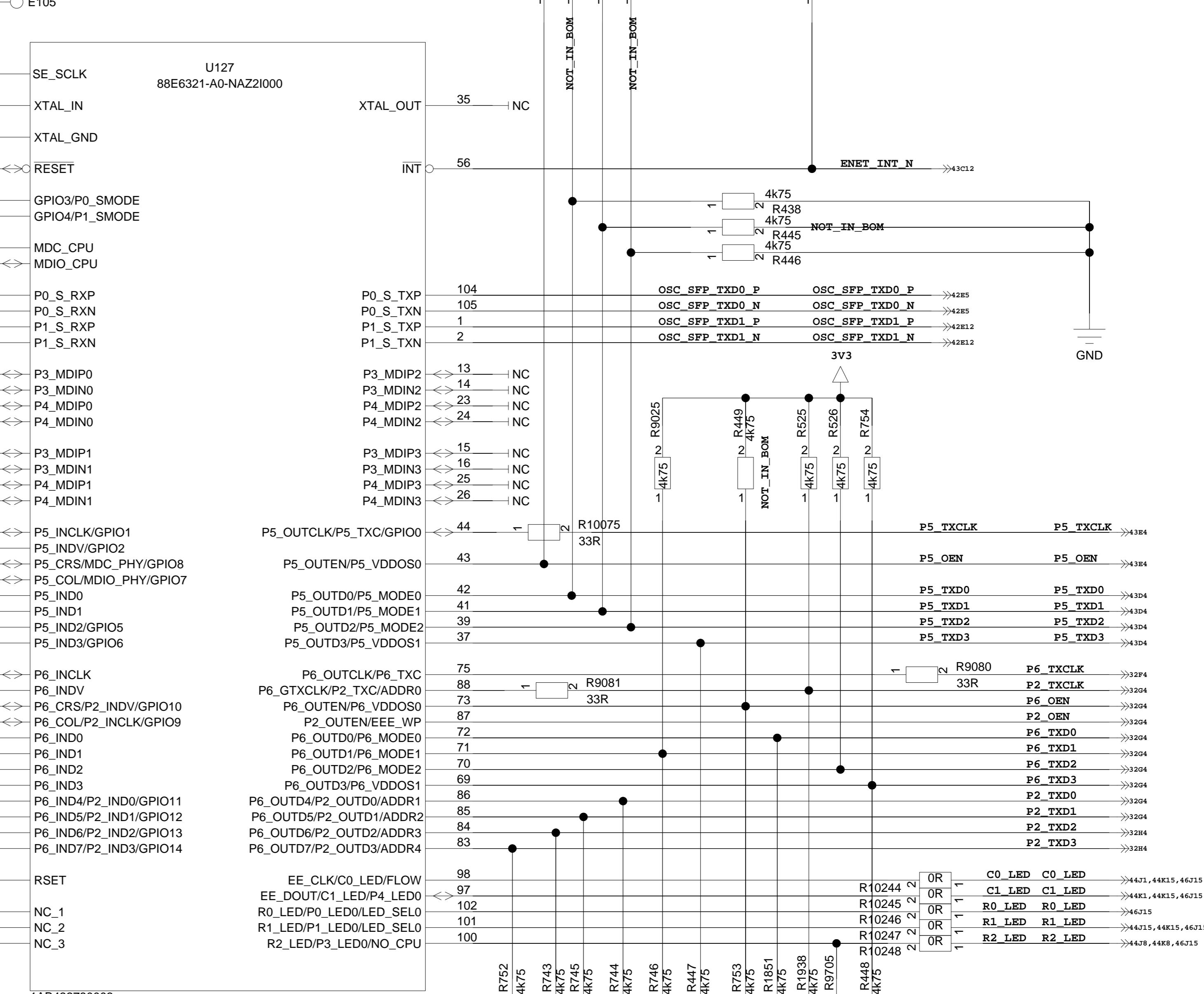


use 1AB432780003, industrial version

PHY MII mode
P5 : MII / 3V3 INTERFACE

MAC MODE

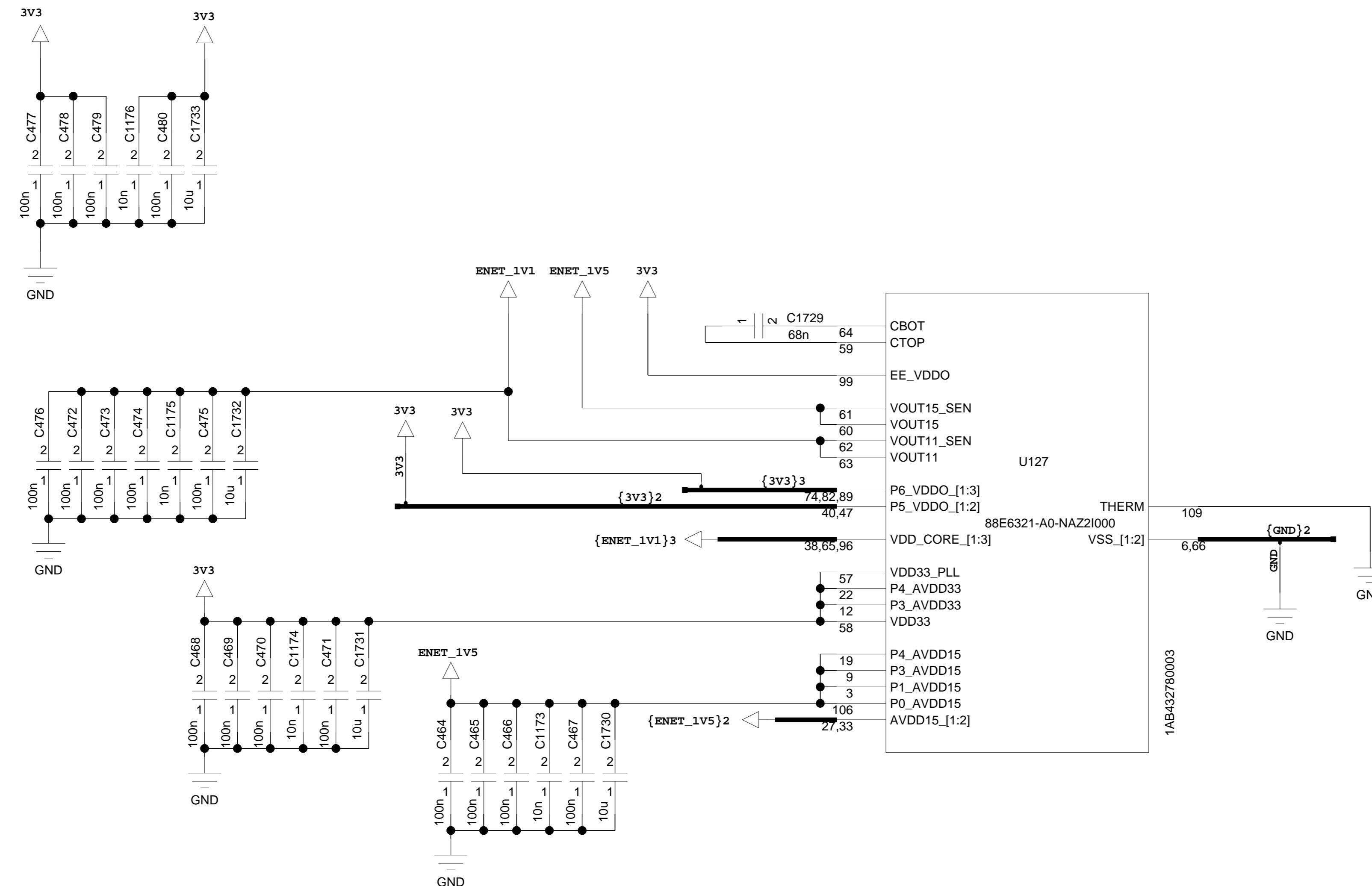
SMI ADDR = 00010 = 0x02
ADDR[4:0]n = 0x1D



ETHERNET SWITCH

ETHERNET SWITCH POWER

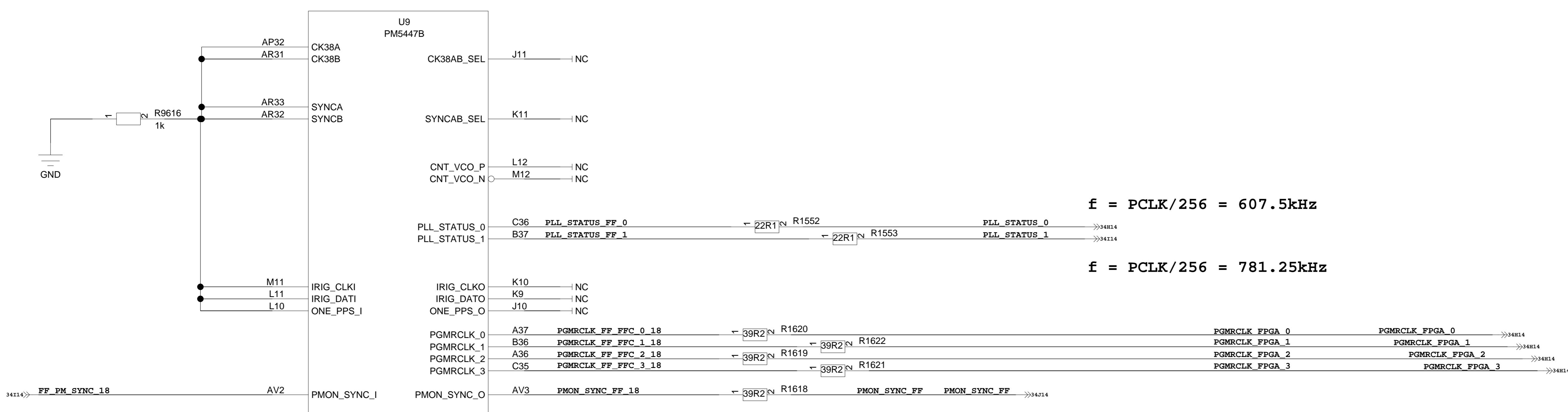
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ETHERNET SWITCH POWER

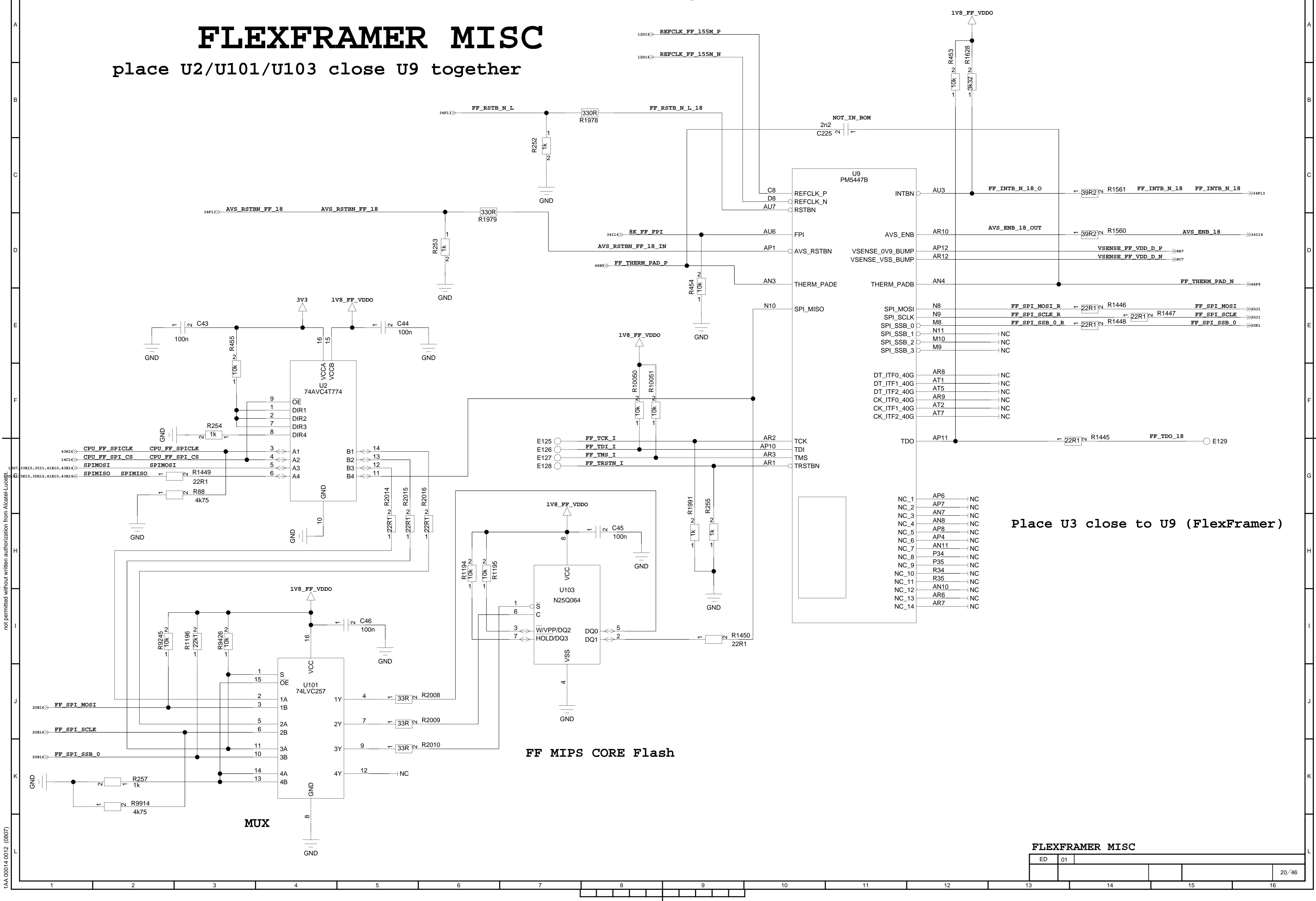
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FLEXFRAMER CLK/SYNC/PTP



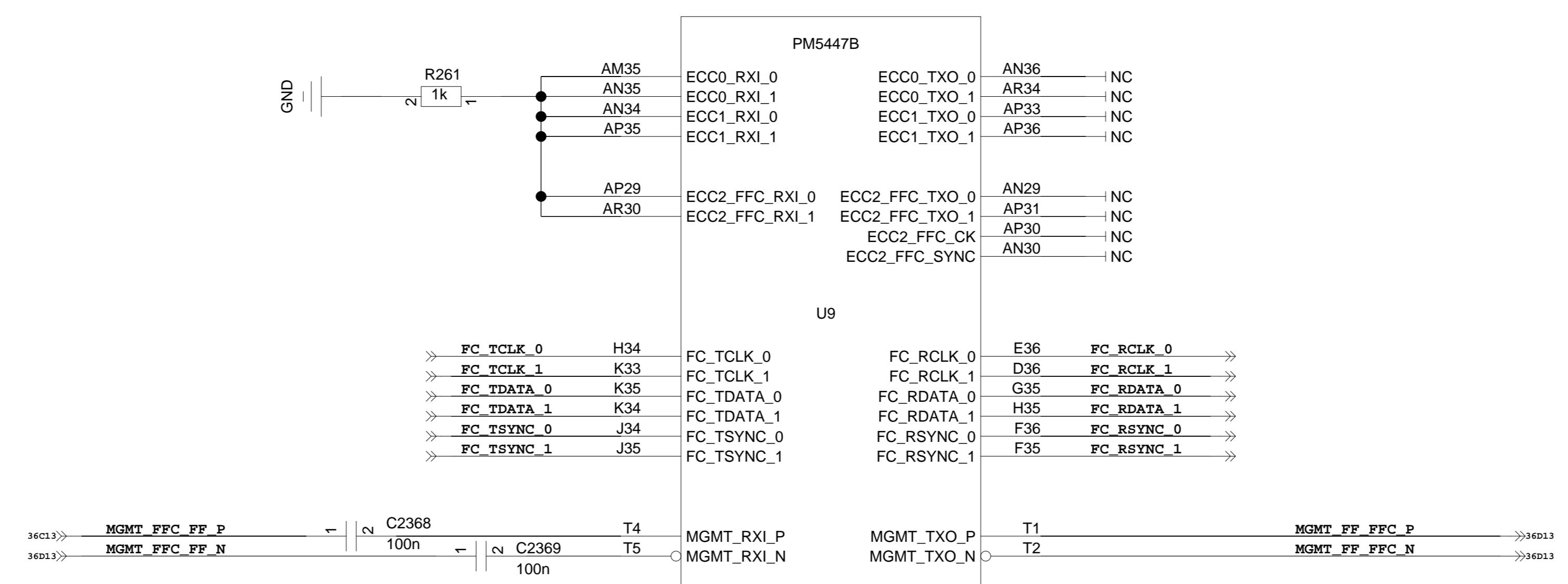
FLEXFRAMER MISC

place U2/U101/U103 close U9 together



Place U3 close to U9 (FlexFramer)

FLEXFRAMER ECC/FC/MGMT



FLEXFRAMER LINE

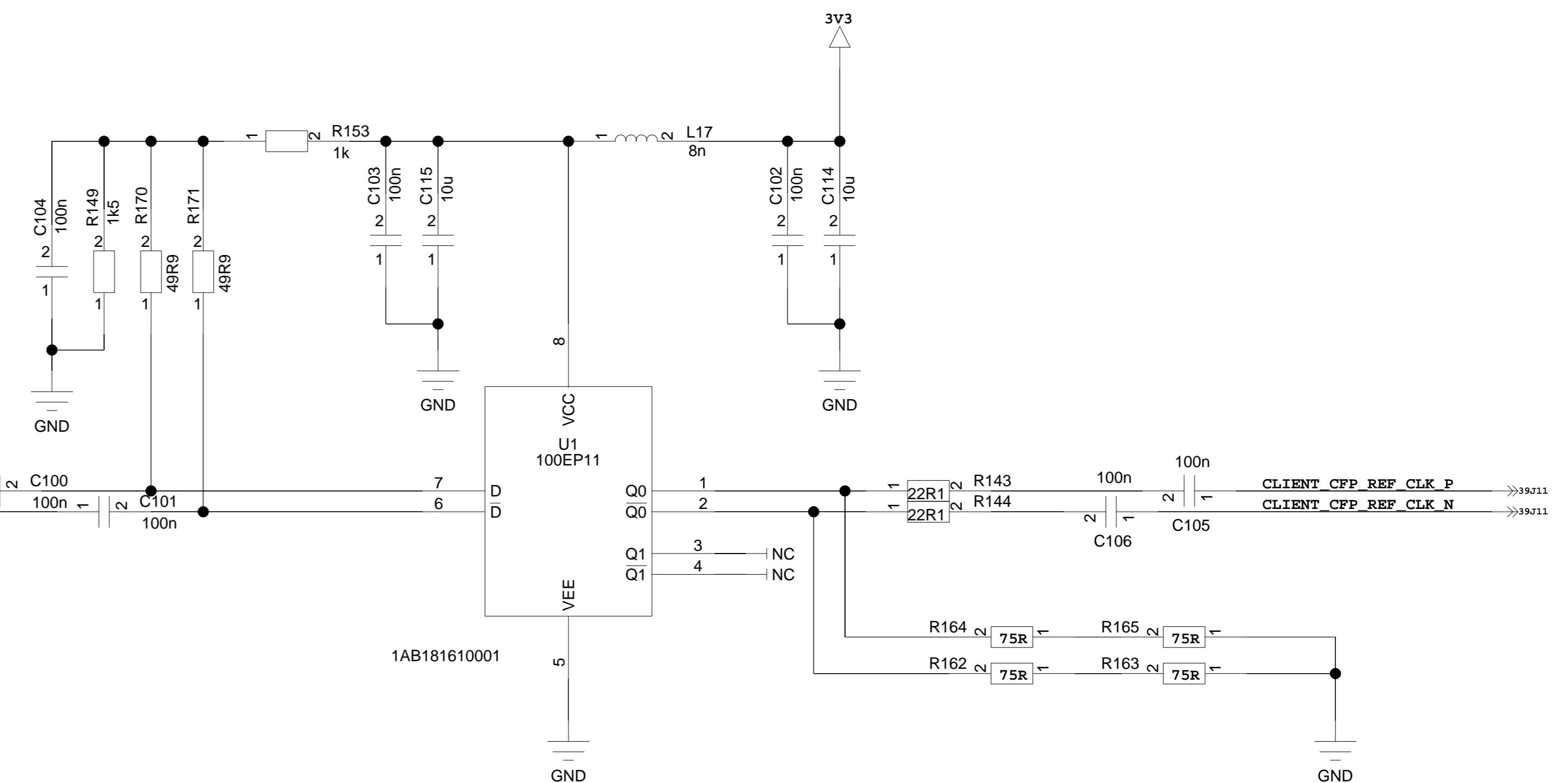
RX DC COUPLING FROM M21036 TX AC COUPLING TO M21036

	U9 PM5447B	
34D13>>	RX_LOS_SFP+_FF_0	RX_LOS_SFP+_FF_0
34D13>>	RX_LOS_SFP+_FF_1	T9
34E13>>	RX_LOS_SFP+_FF_2	U11
34E13>>	RX_LOS_SFP+_FF_3	T11
34E13>>	RX_LOS_SFP+_FF_4	T10
34E13>>	RX_LOS_SFP+_FF_5	R8
34E13>>	RX_LOS_SFP+_FF_6	R10
34E13>>	RX_LOS_SFP+_FF_7	R9
34E13>>	RX_LOS_SFP+_FF_8	P8
34E13>>	RX_LOS_SFP+_FF_9	R11
34E13>>	RX_LOS_SFP+_FF_10	P10
34E13>>	RX_LOS_SFP+_FF_11	P11

	U9 PM5447B		
LINE_LOS_0	LINE_REFCLK_0_P	L1	CLIENT_FF_REF_CLK_P
LINE_LOS_1	LINE_REFCLK_0_N	L2	CLIENT_FF_REF_CLK_N
LINE_LOS_2	LINE_REFCLK_1_P	C100	100n
LINE_LOS_3	LINE_REFCLK_1_N	C101	100n
LINE_LOS_4	LINE_REFCLK_2_P	100n	
LINE_LOS_5	LINE_REFCLK_2_N	100n	
LINE_LOS_6	LINE_REFCLK_3_P	100n	
LINE_LOS_7	LINE_REFCLK_3_N	100n	
LINE_LOS_8	LINE_REFCLK_4_P	100n	
LINE_LOS_9	LINE_REFCLK_4_N	100n	
LINE_LOS_10	LINE_REFCLK_5_P	100n	
LINE_LOS_11	LINE_REFCLK_5_N	100n	
	LINE_REFCLK_6_P	100n	
	LINE_REFCLK_6_N	100n	
	LINE_REFCLK_7_P	100n	
	LINE_REFCLK_7_N	100n	
	LINE_REFCLK_8_P	100n	
	LINE_REFCLK_8_N	100n	
	LINE_REFCLK_9_P	100n	
	LINE_REFCLK_9_N	100n	
	LINE_REFCLK_10_P	100n	
	LINE_REFCLK_10_N	100n	
	LINE_REFCLK_11_P	100n	
	LINE_REFCLK_11_N	100n	

	AM5	AM6	AM7	AK5	AK6	AJ6	AJ7	AH5	AH6	AG6	AG7	AE5	AE6	AD6	AD7	AC5	AC6	AC7	AE5	AE6	AE7	AD6	AD7	AC5	AC6	AC7	AB6	AB7	AA5	AA6	Y6	Y7																
40F15>>	LINE_RXI_0_P	LINE_RXI_0_N	LINE_RXI_1_P	LINE_RXI_1_N	LINE_RXI_2_P	LINE_RXI_2_N	LINE_RXI_3_P	LINE_RXI_3_N	LINE_RXI_4_P	LINE_RXI_4_N	LINE_RXI_5_P	LINE_RXI_5_N	LINE_RXI_6_P	LINE_RXI_6_N	LINE_RXI_7_P	LINE_RXI_7_N	LINE_RXI_8_P	LINE_RXI_8_N	LINE_RXI_9_P	LINE_RXI_9_N	LINE_RXI_10_P	LINE_RXI_10_N	LINE_RXI_11_P	LINE_RXI_11_N	LINE_RXI_0_P	LINE_RXI_0_N	LINE_RXI_1_P	LINE_RXI_1_N	LINE_RXI_2_P	LINE_RXI_2_N	LINE_RXI_3_P	LINE_RXI_3_N	LINE_RXI_4_P	LINE_RXI_4_N	LINE_RXI_5_P	LINE_RXI_5_N	LINE_RXI_6_P	LINE_RXI_6_N	LINE_RXI_7_P	LINE_RXI_7_N	LINE_RXI_8_P	LINE_RXI_8_N	LINE_RXI_9_P	LINE_RXI_9_N	LINE_RXI_10_P	LINE_RXI_10_N	LINE_RXI_11_P	LINE_RXI_11_N

	AM1	AM2	AL2	AL3	AK1	AK2	AJ2	AJ3	AH1	AH2	AG2	AG3	AE1	AE2	AD2	AD3	AC1	AC2	AC3	AE1	AE2	AD2	AD3	AC1	AC2	AC3	AB2	AB3	AA1	AA2	Y2	Y3																																
	LINE_RXO_0_P	1	2	2	100n	1	2	2	100n	1	2	100n	1	2	2	100n	1	2	2	100n	1	2	2	100n	1	2	2	100n	1	2	2	100n	1	2	2	100n	1	2	2	100n	1	2	2	100n	1	2	2	100n																



FLEXFRAMER LINE

ED	01			
				22/46

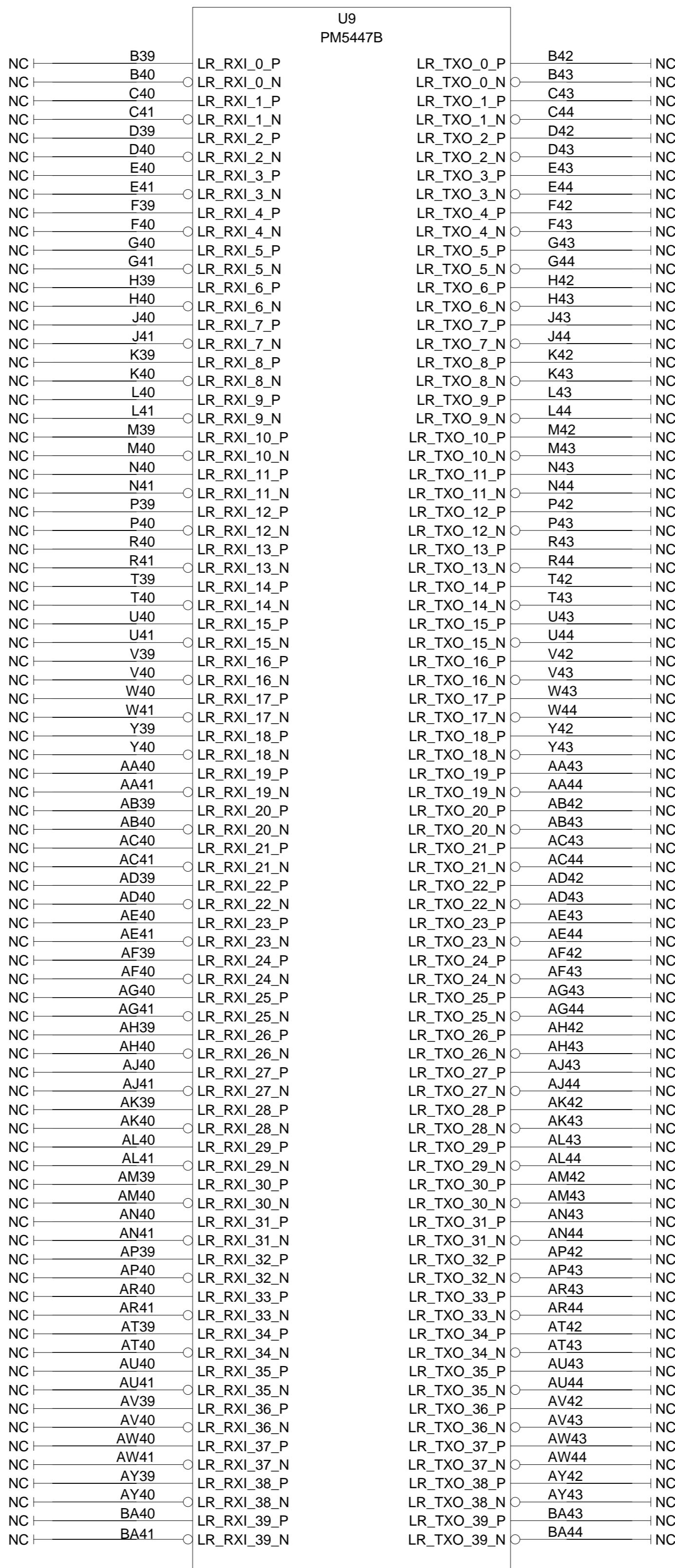
FLEXFRAMER BACKPLANE LR

LR 0

LR 0

LR 1

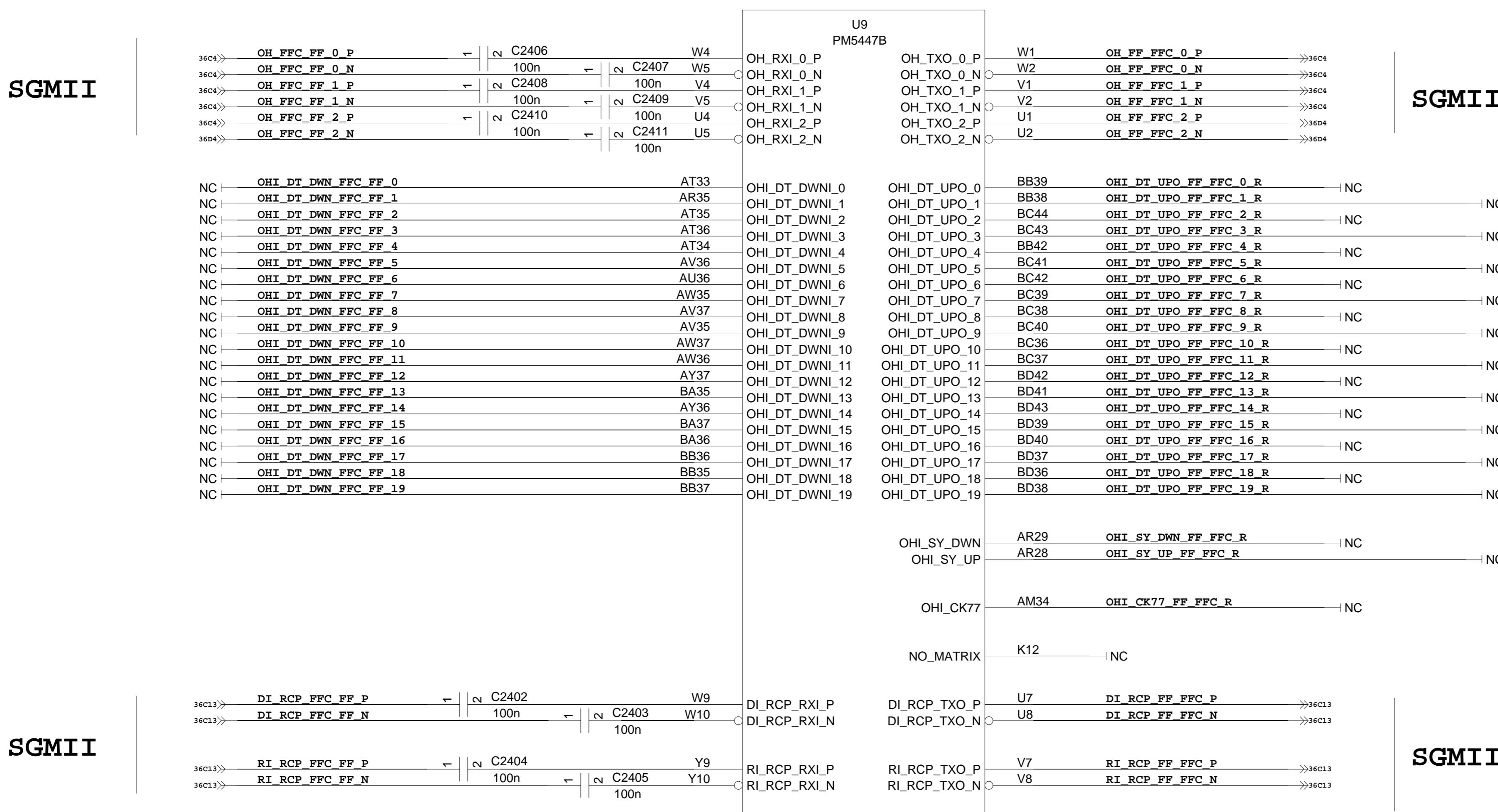
LR 1



FLEXFRAMER BACKPLANE LR

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23/46				

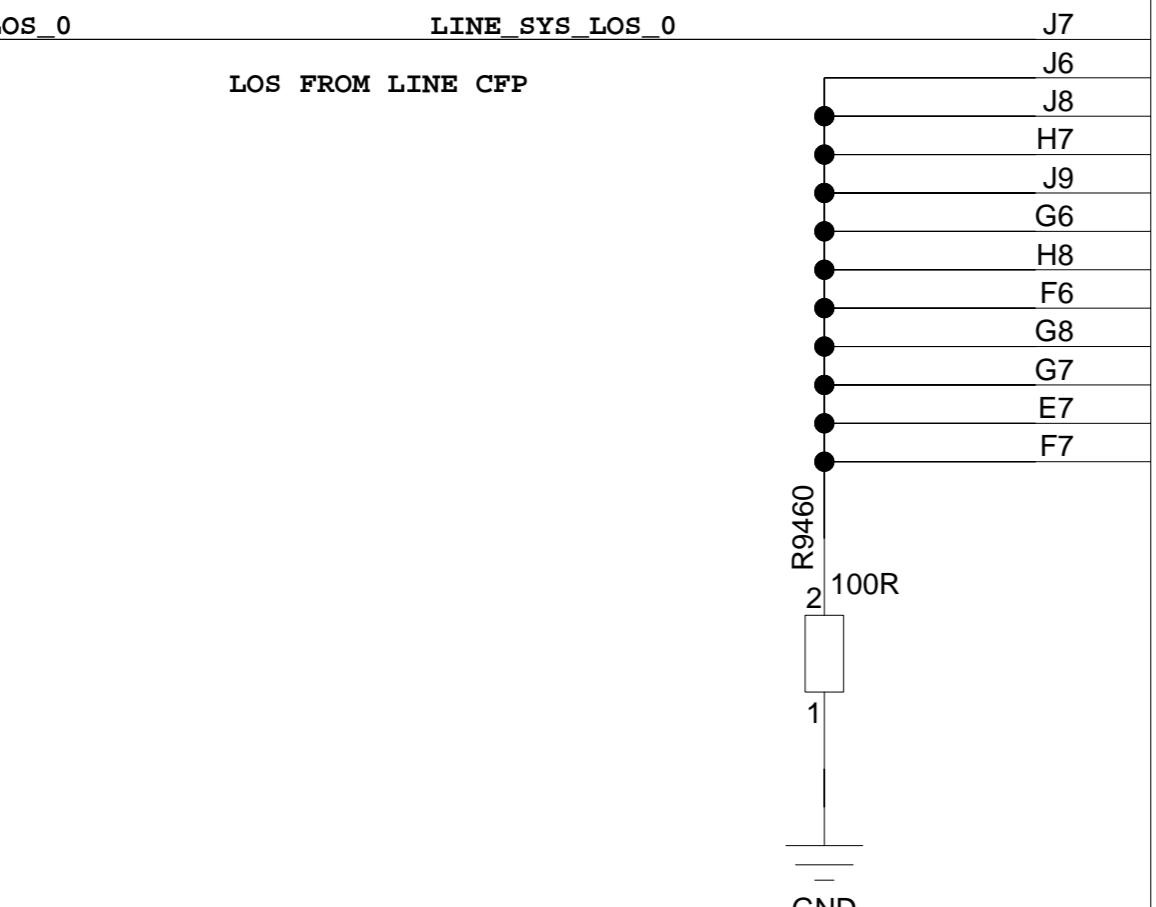
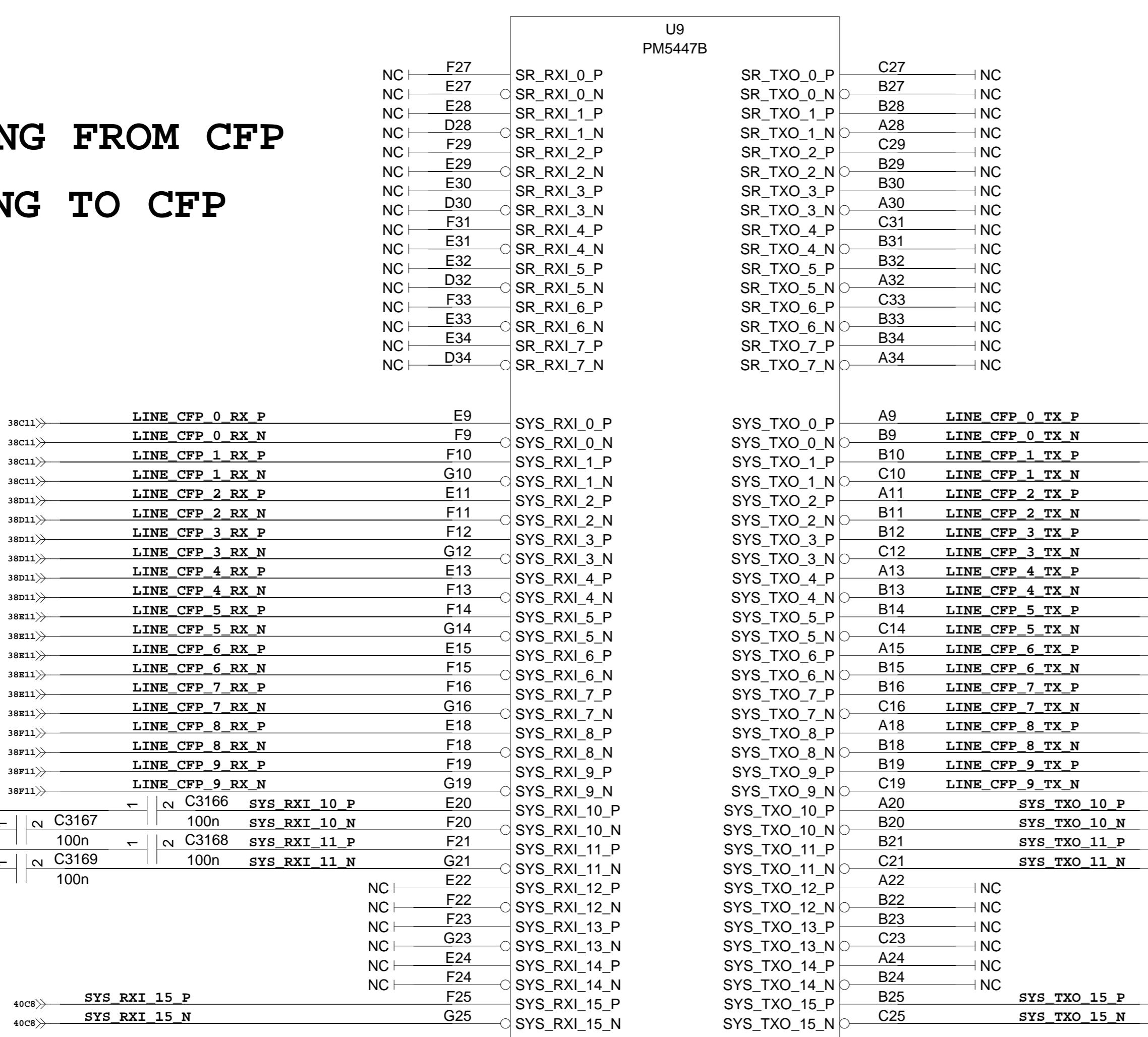
FLEXFRAMER OH/OHI



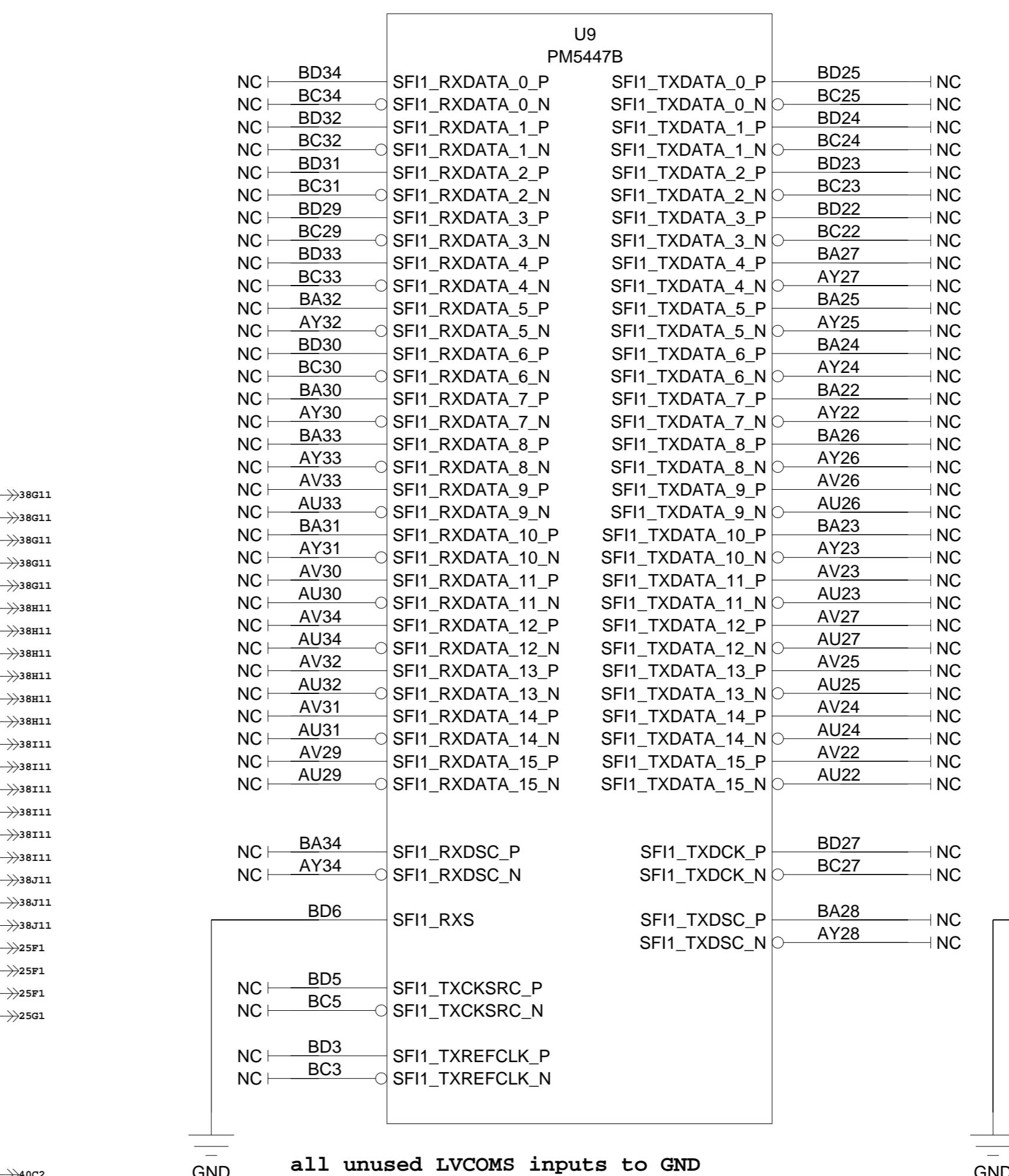
FLEXFRAMER SFI-5.1/SYS/SR

RX AC COUPLING FROM CFP

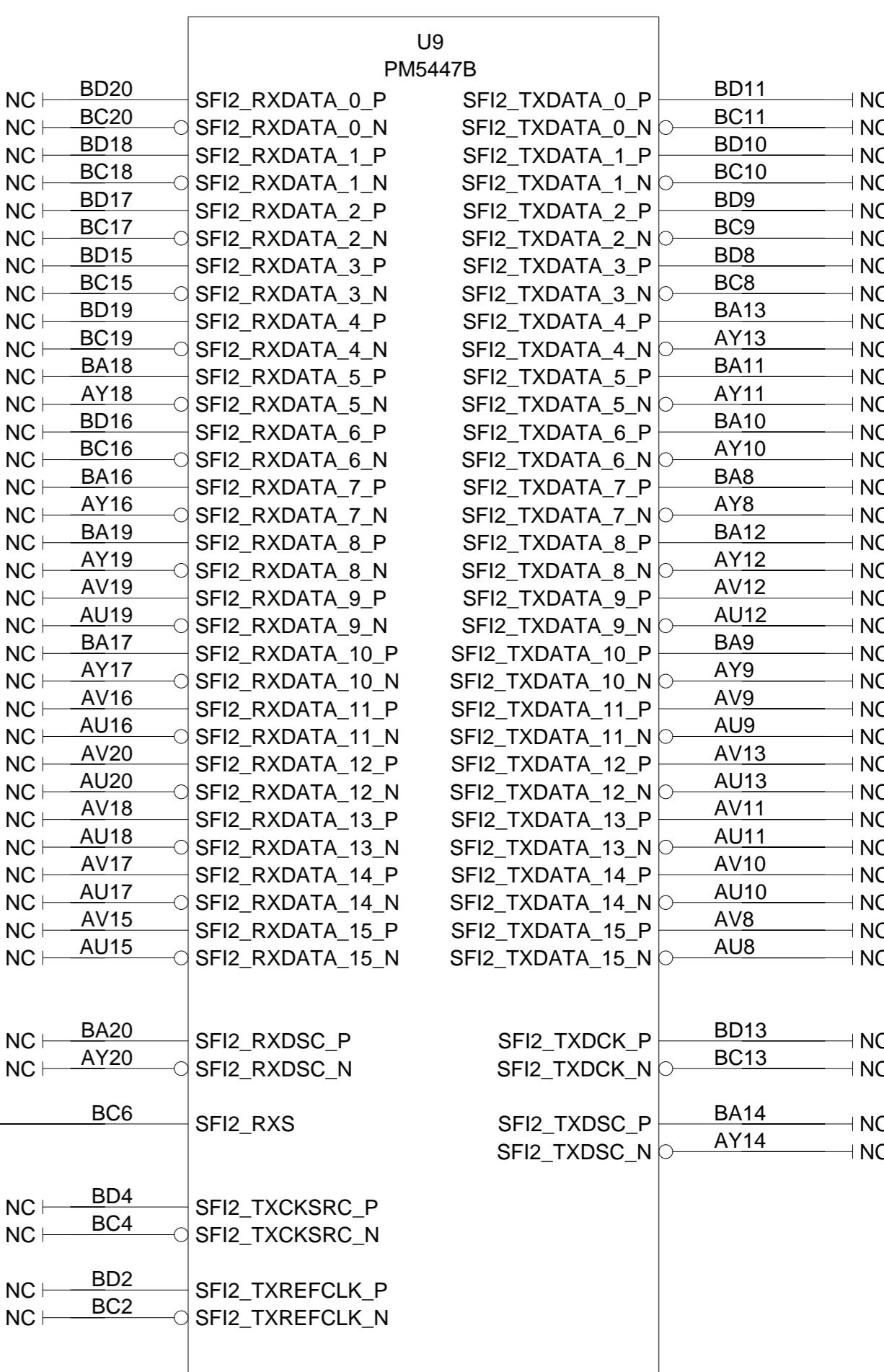
TX AC COUPLING TO CFP



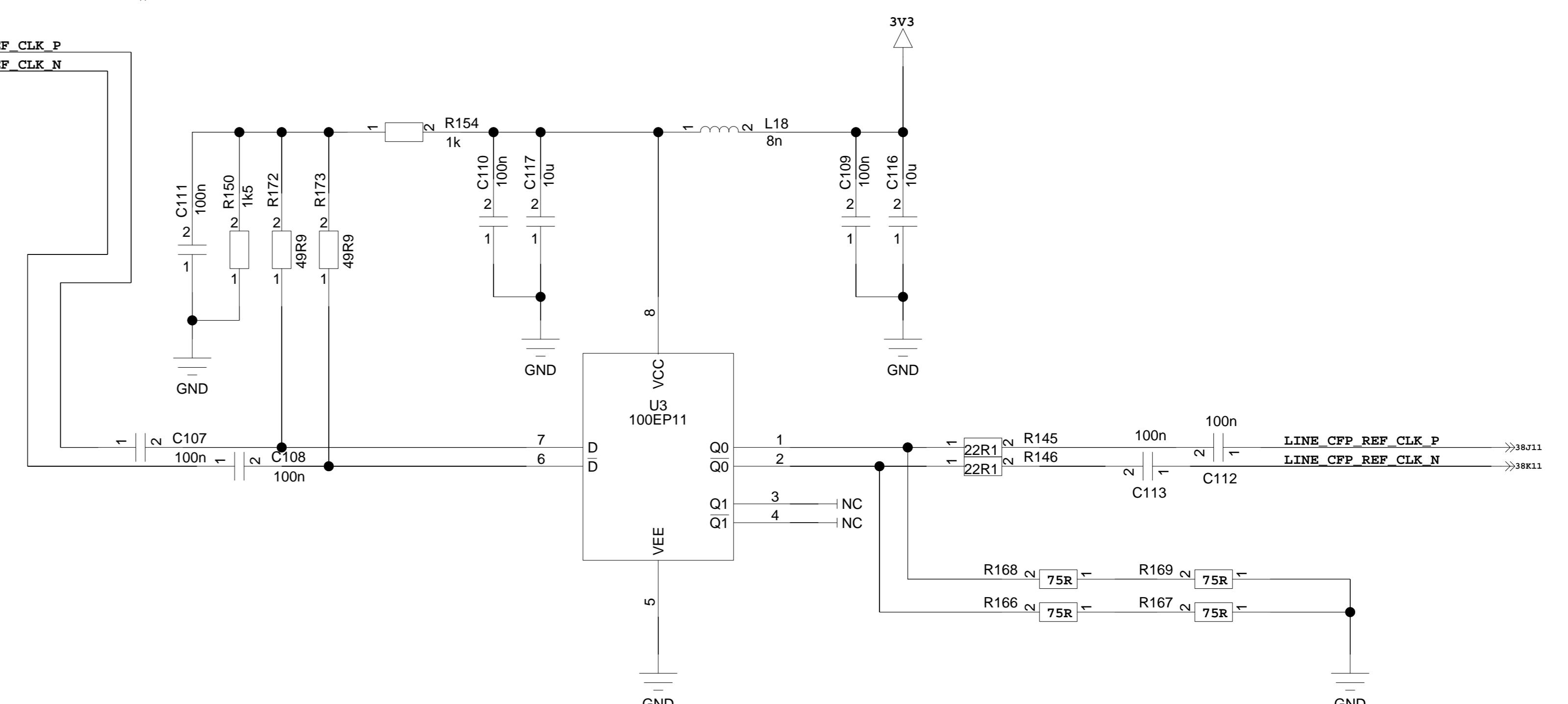
all unused LVCOMS inputs to GND



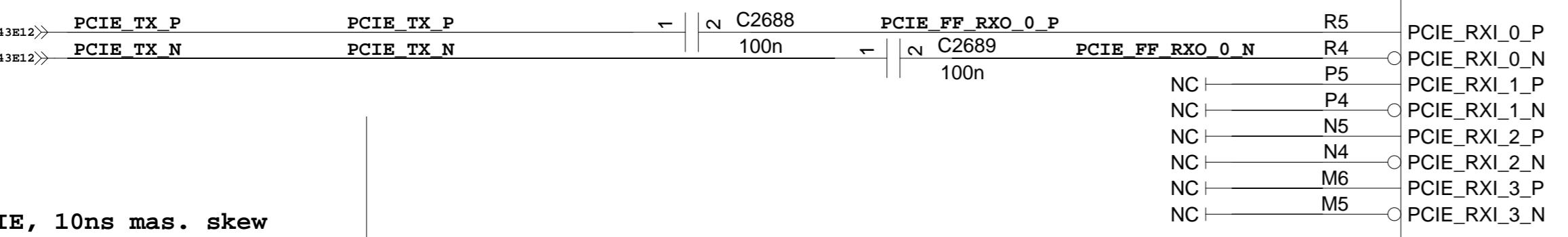
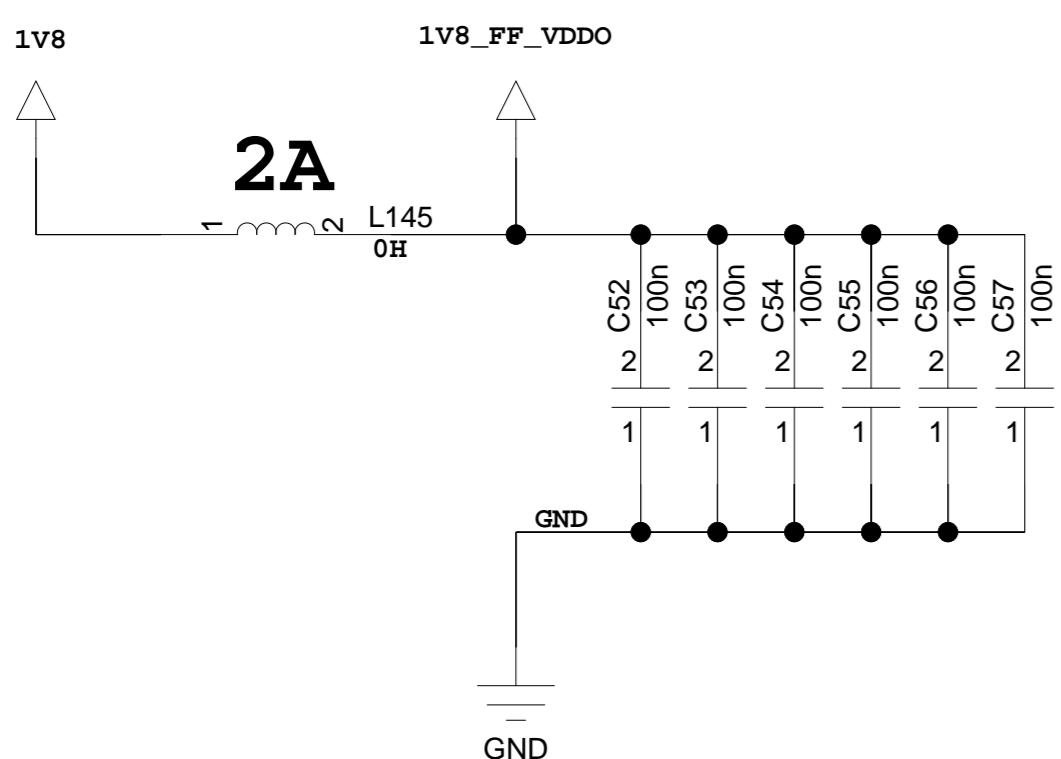
all unused LVCOMS inputs to GND



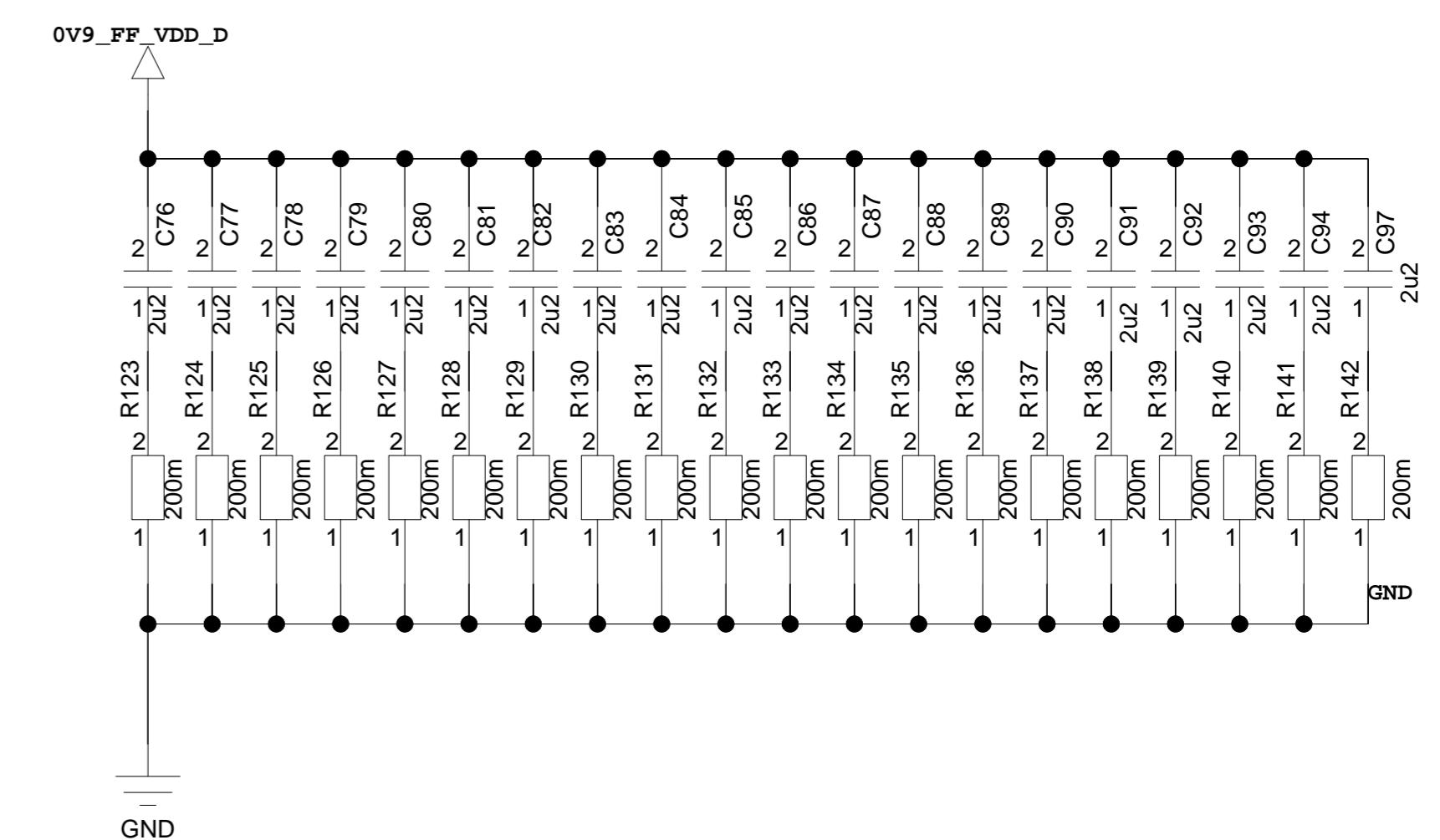
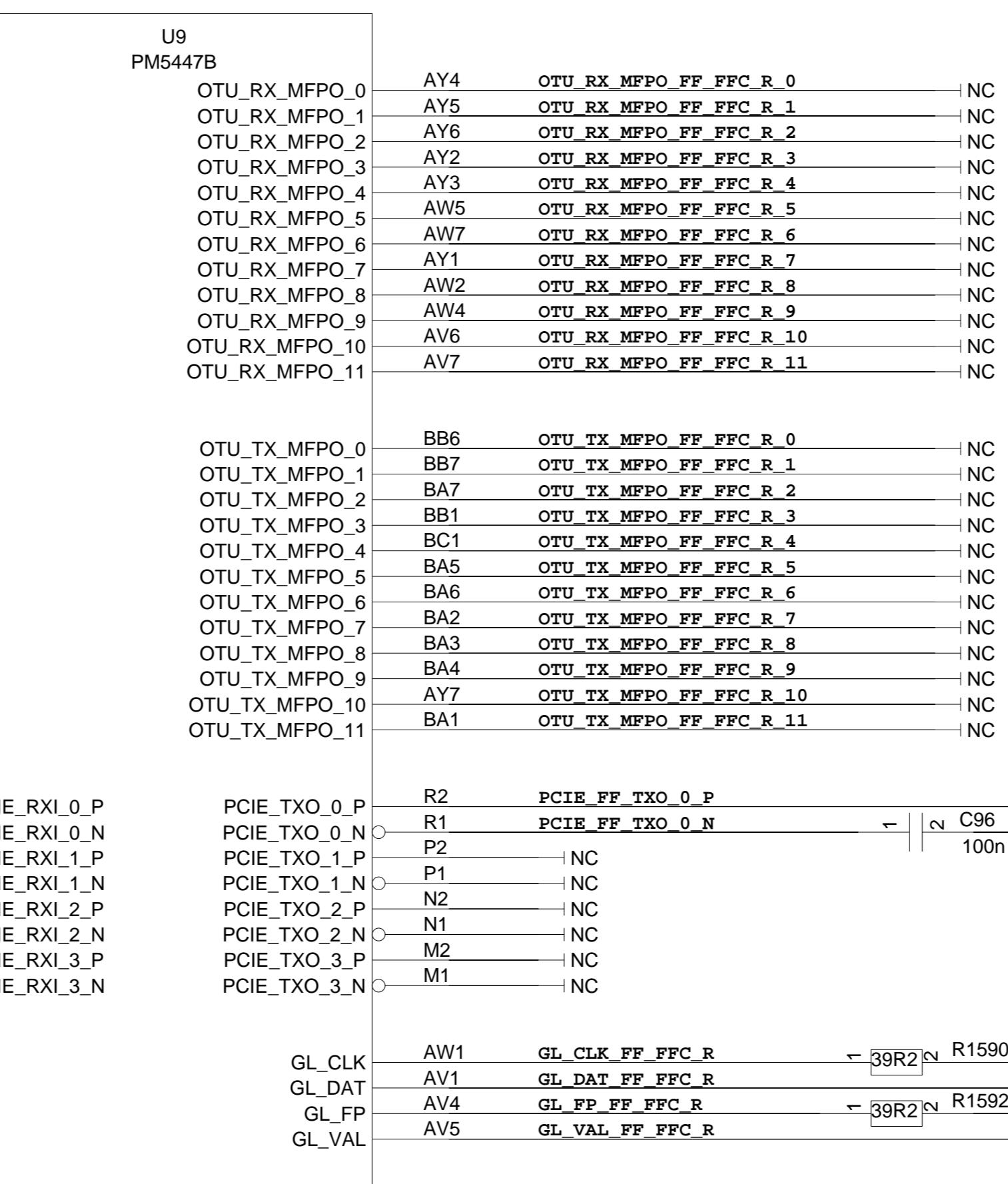
all unused LVCOMS inputs to GND



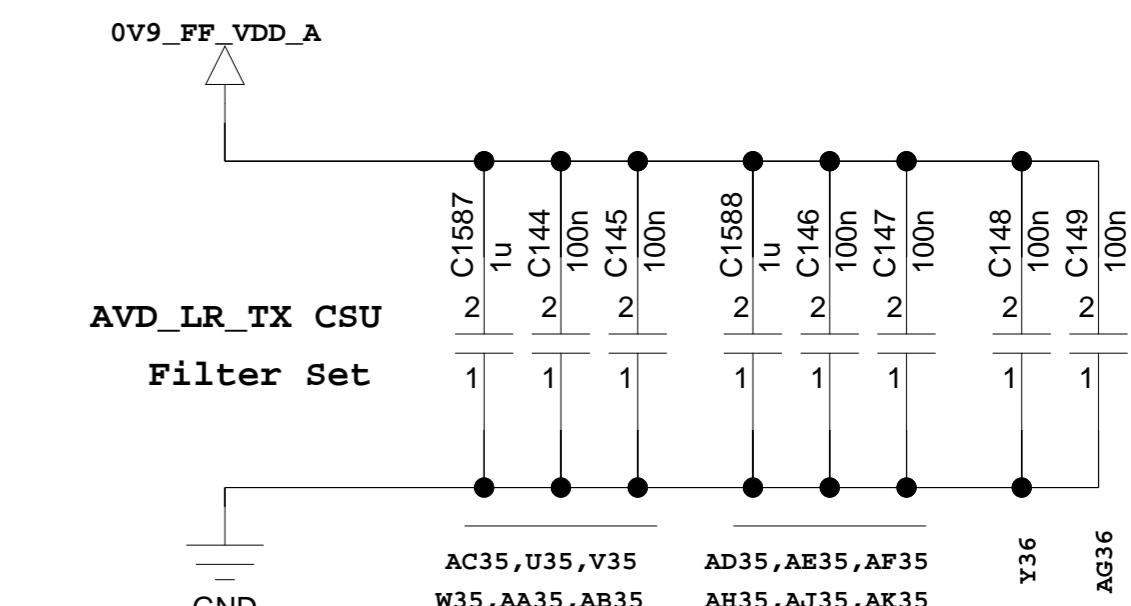
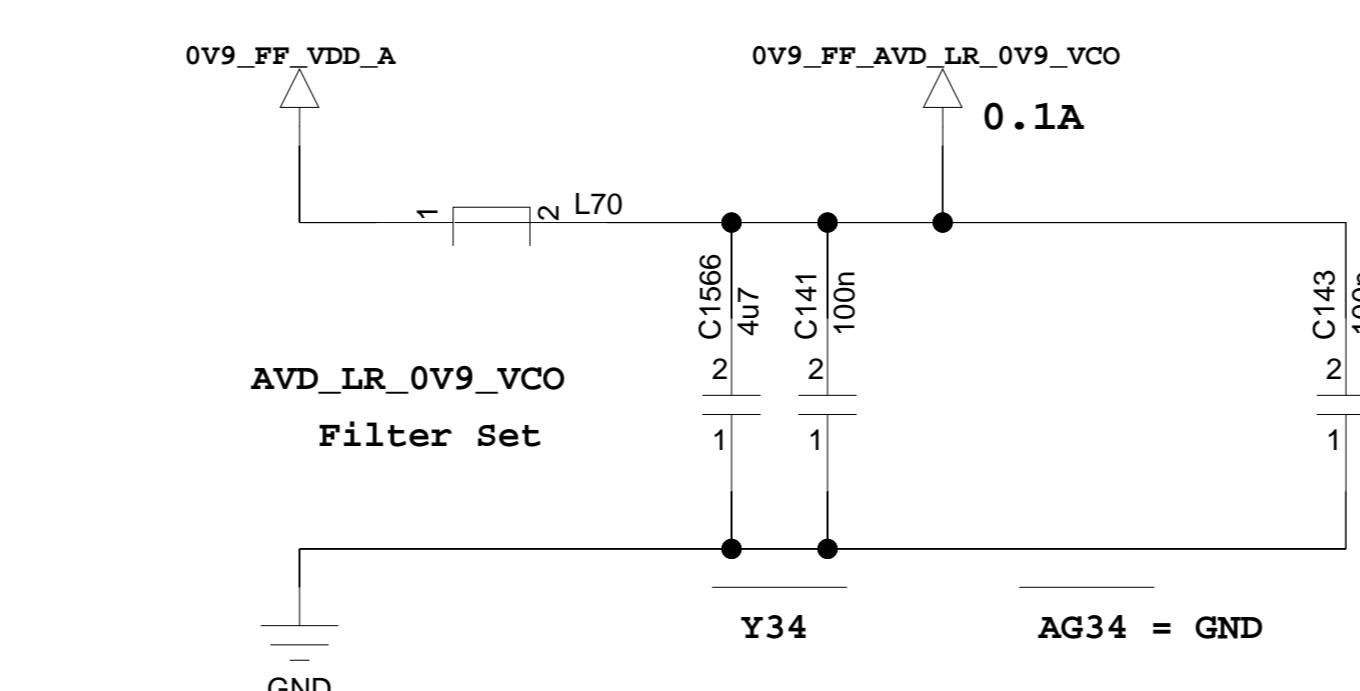
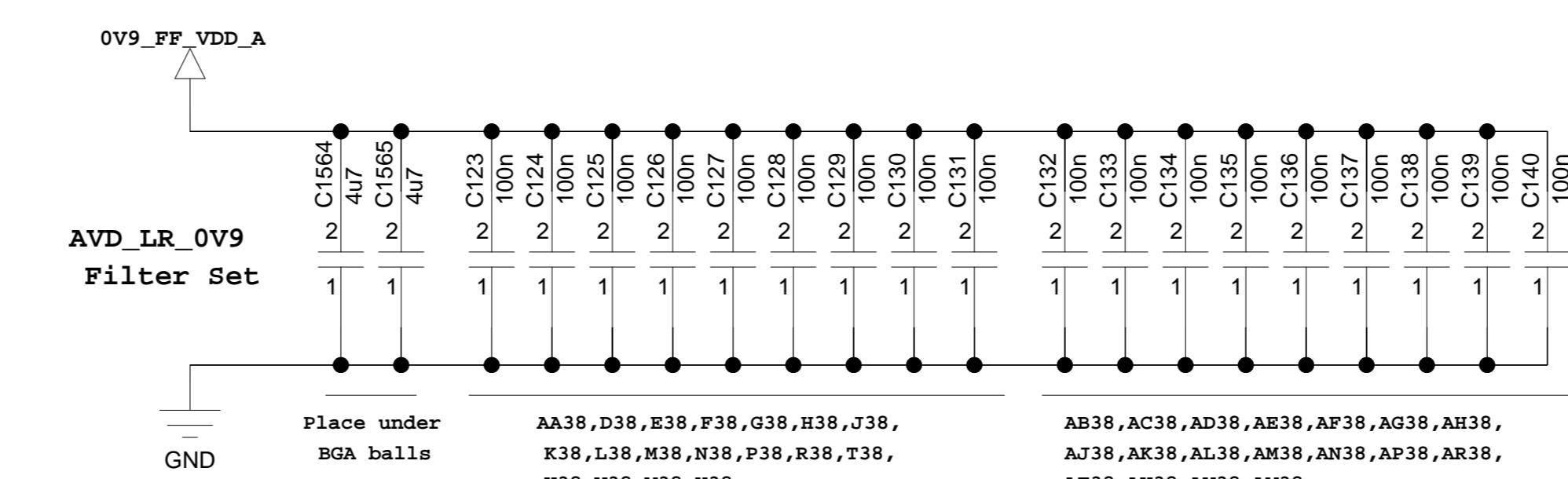
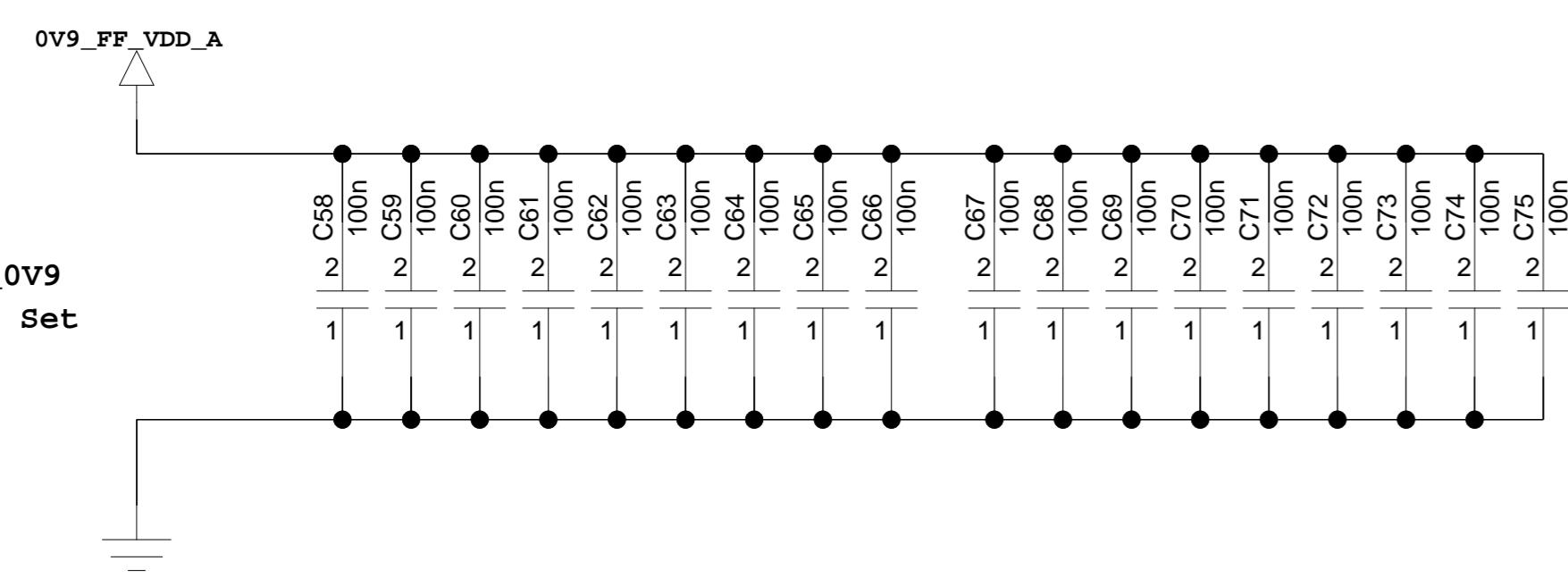
FLEXFRAMER MFPO/PCIE/GL/POWER



PCIE, 10ns mas. skew
PCIE, 85 OHm Impedance

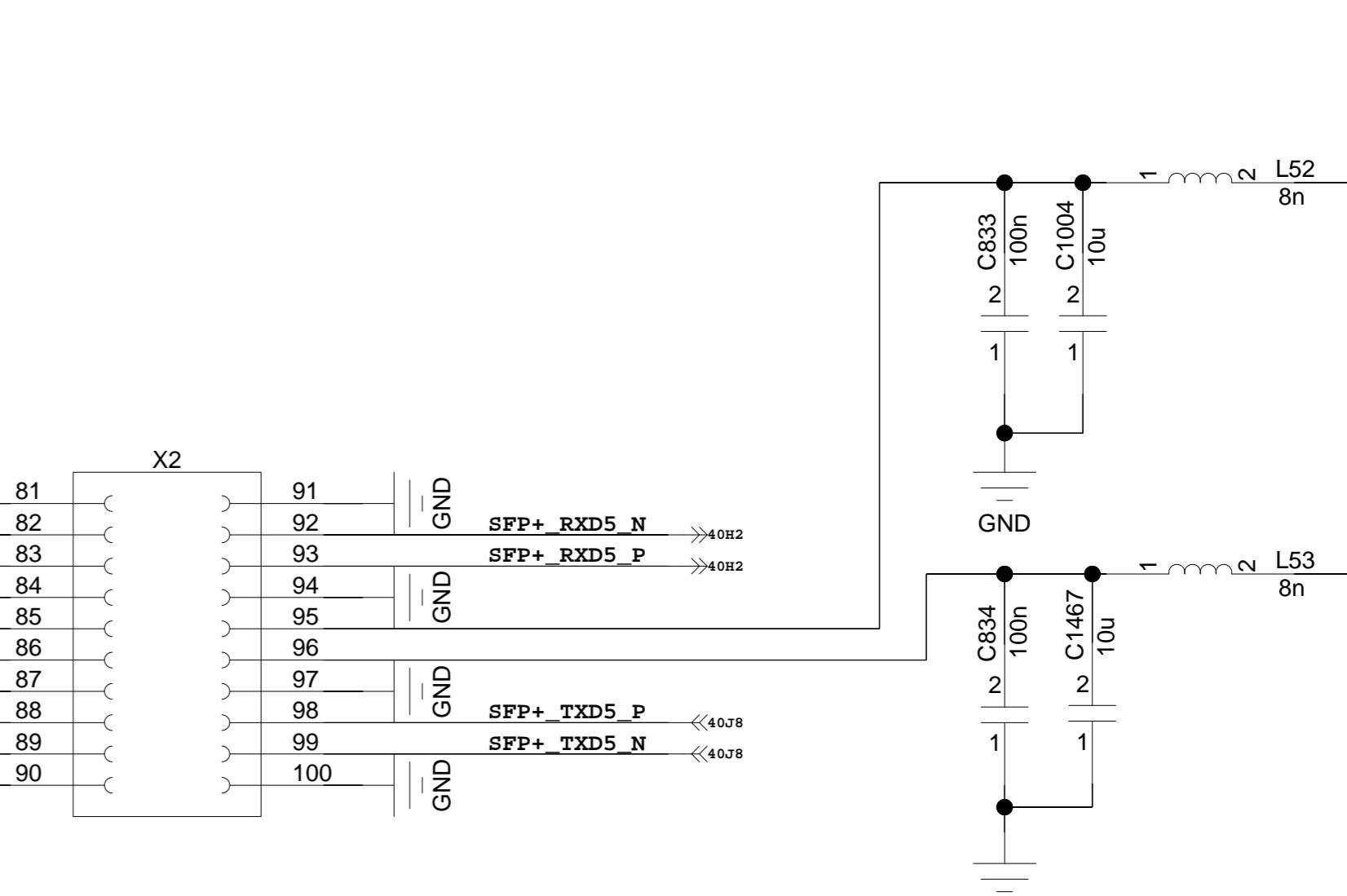
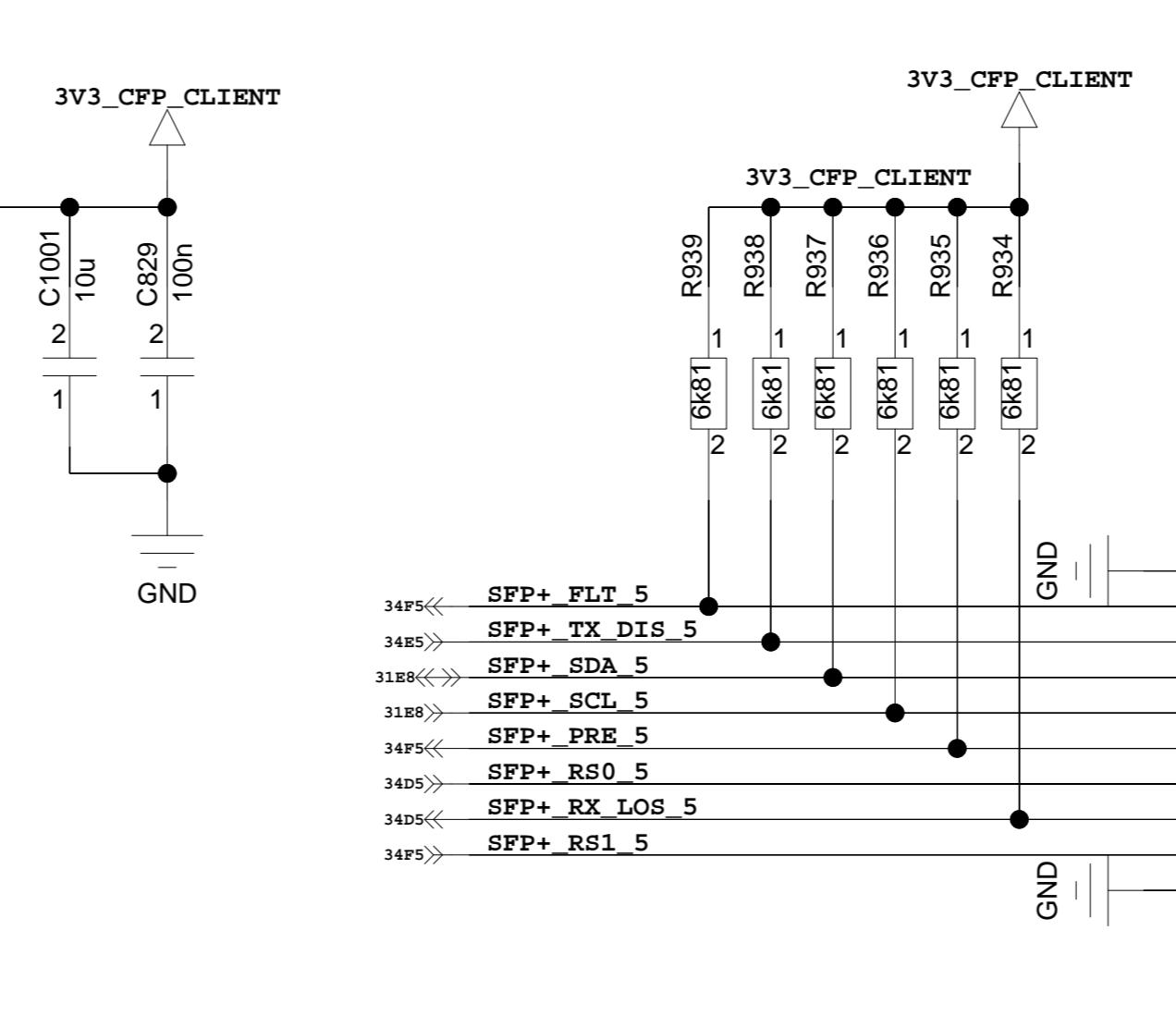
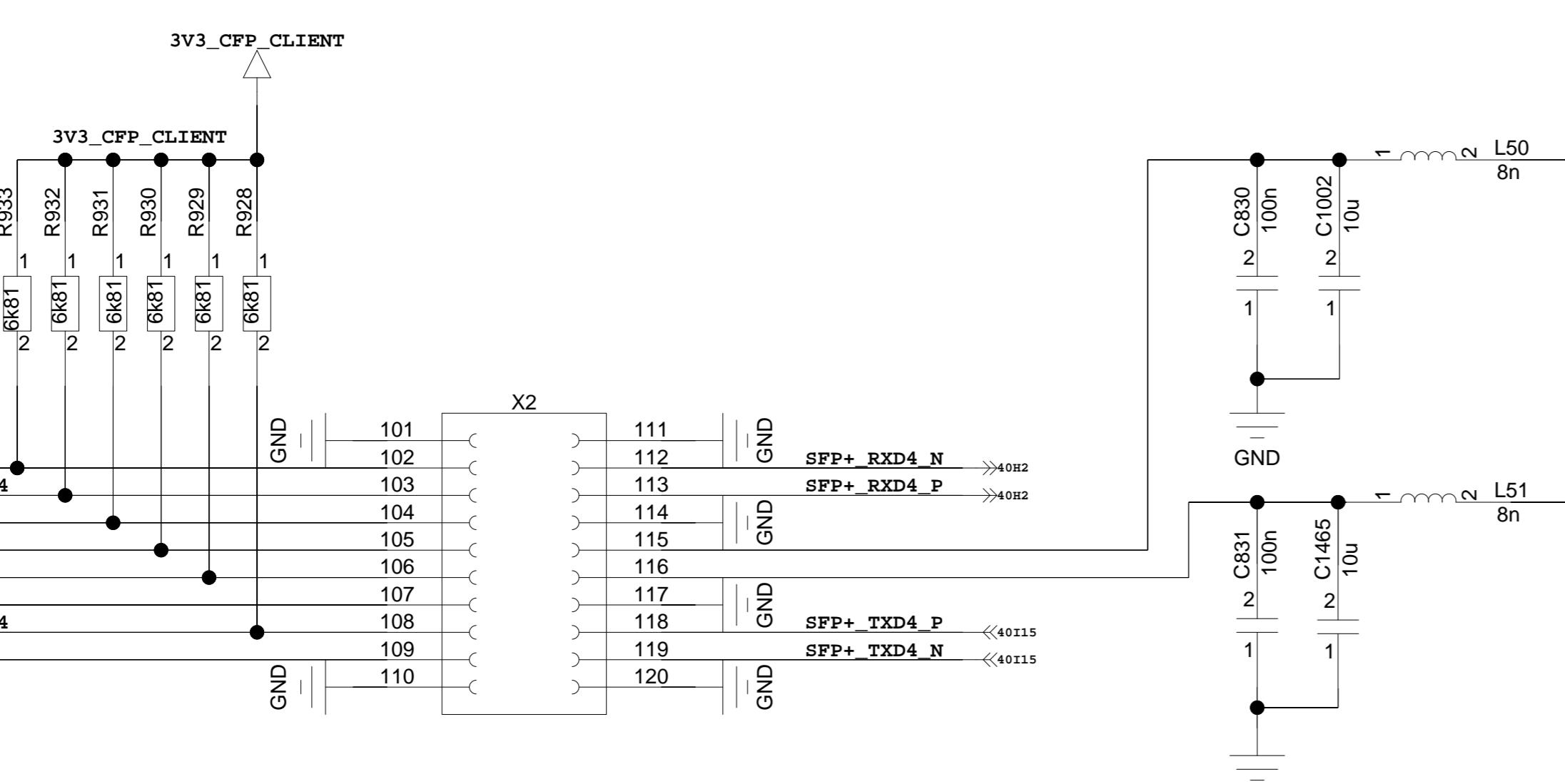
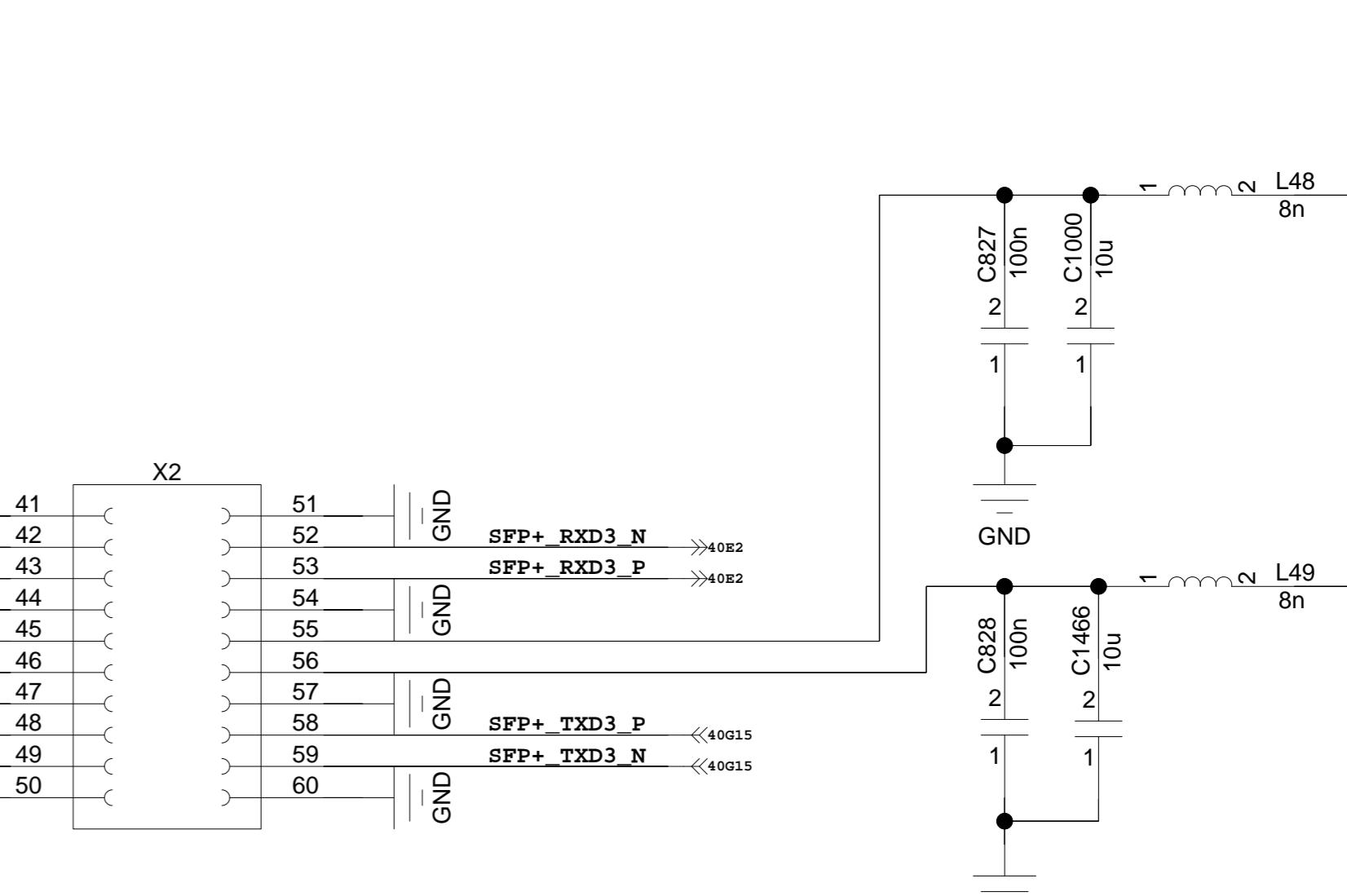
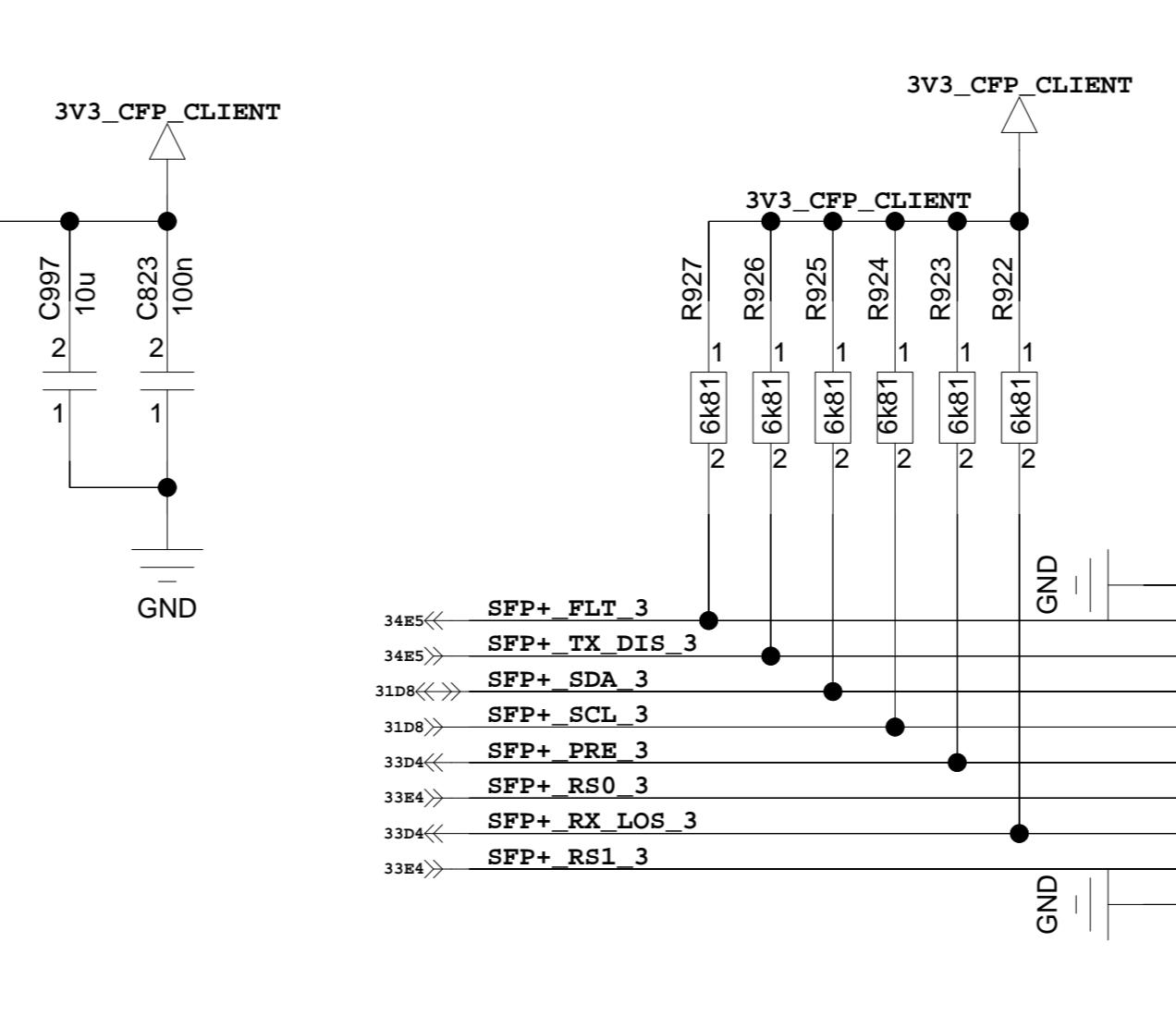
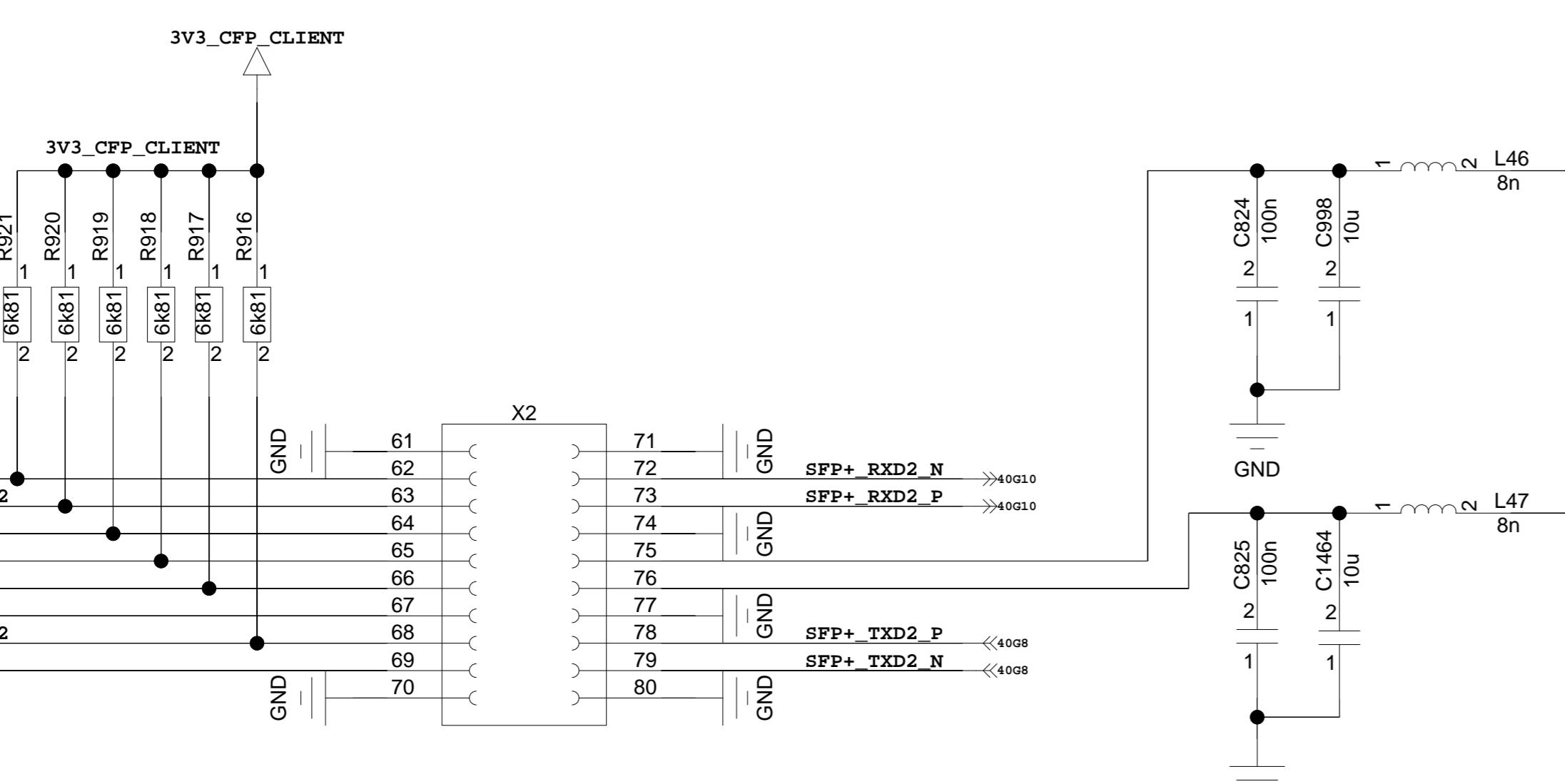
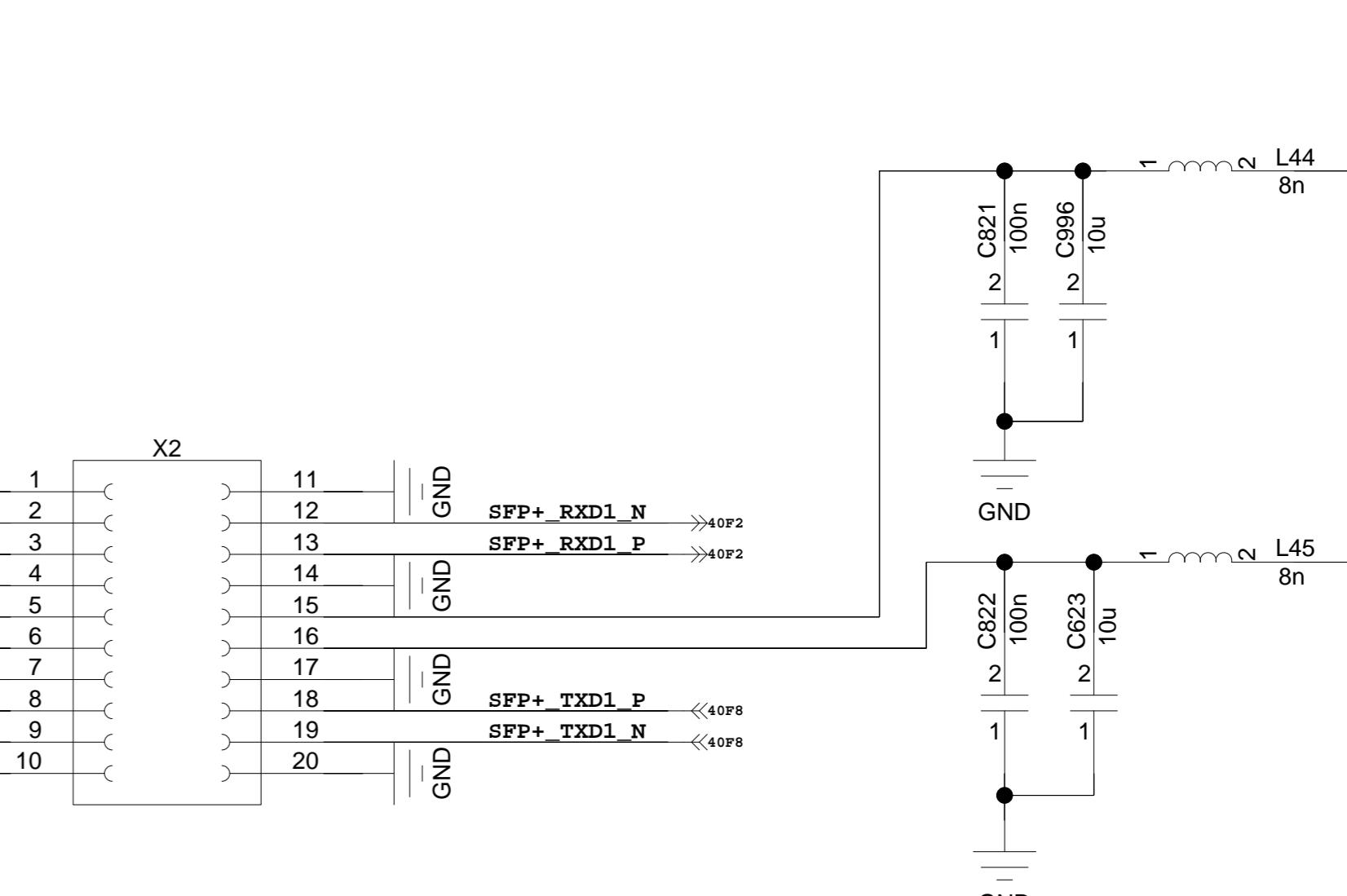
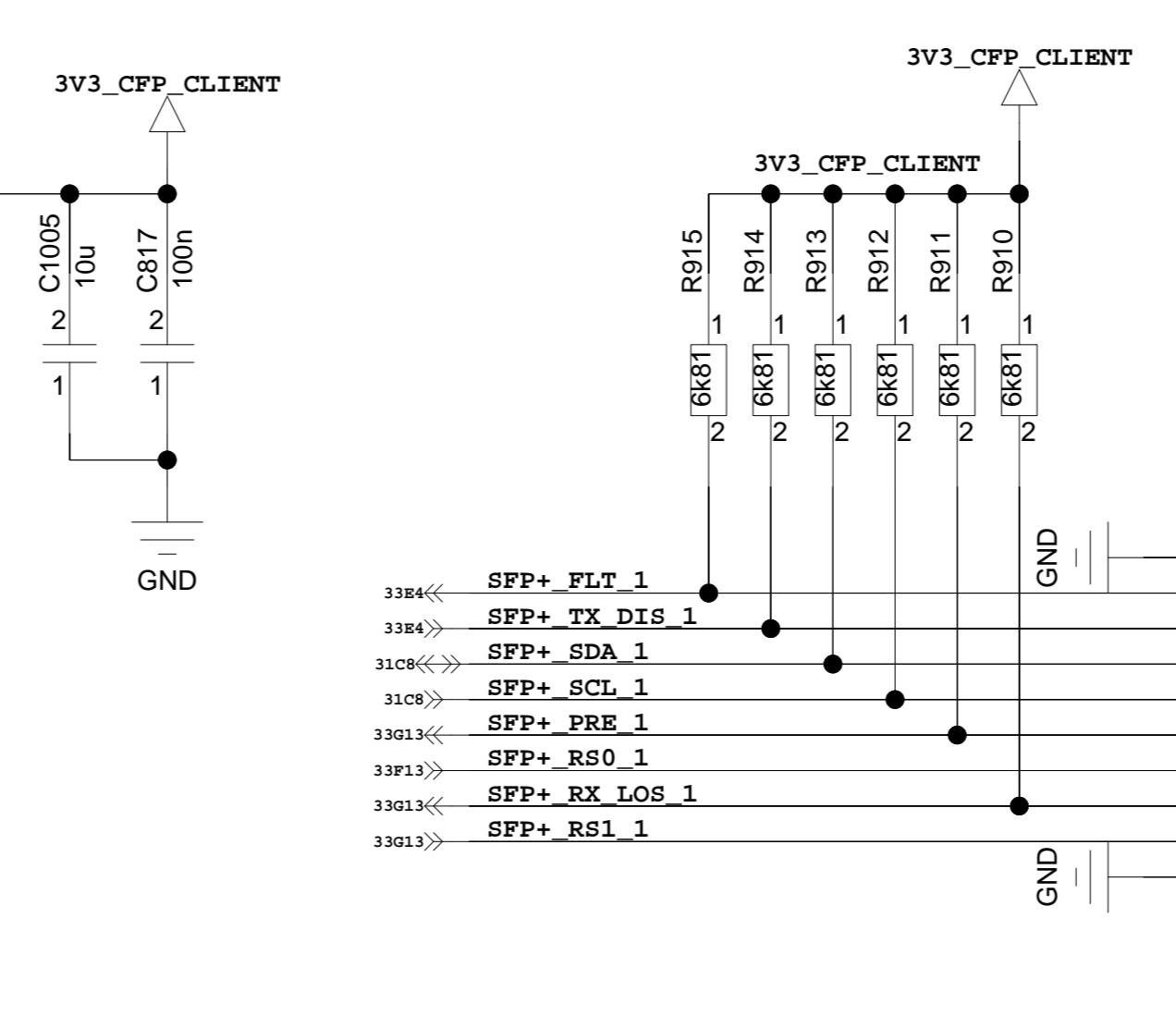
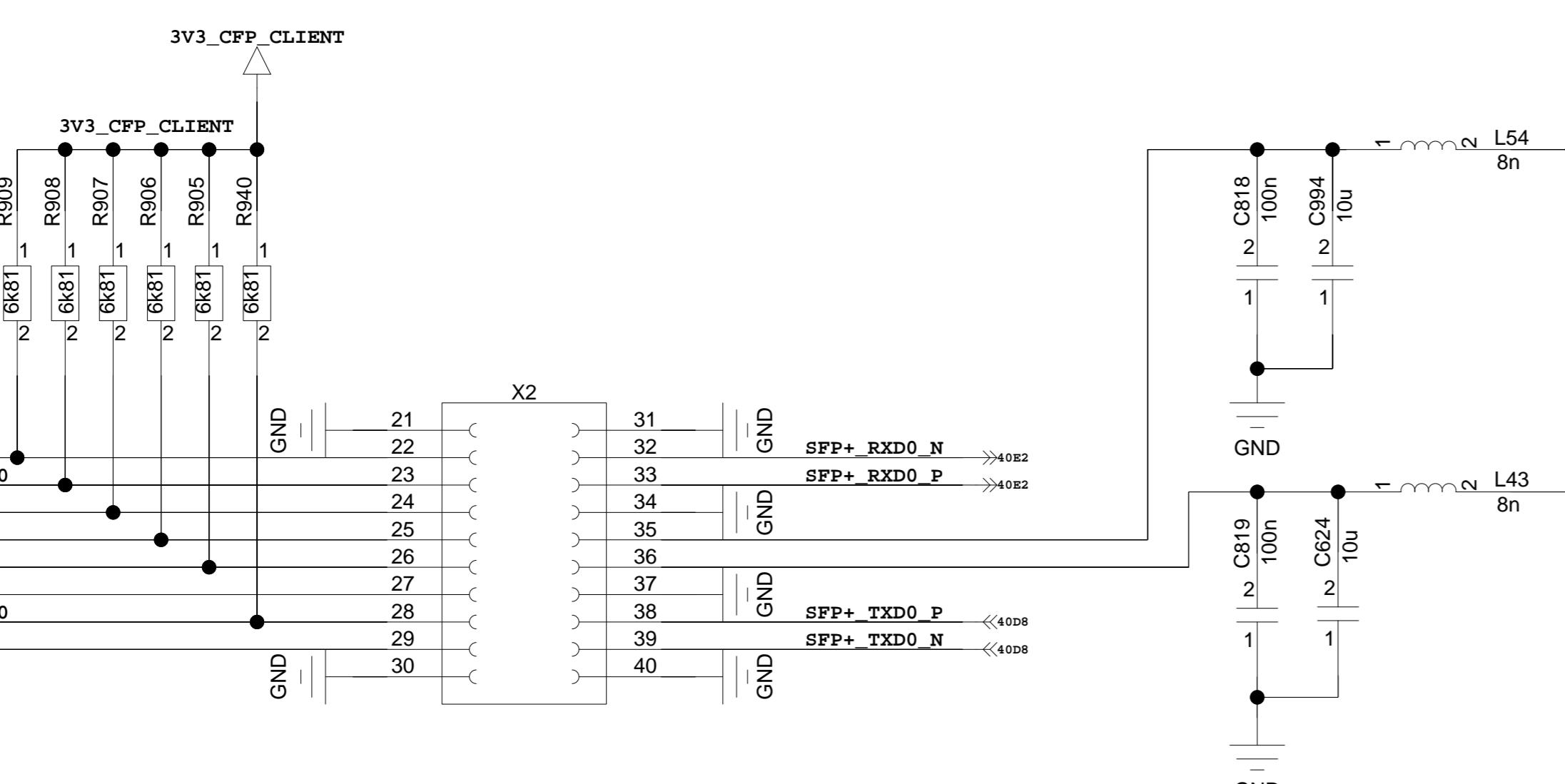


PCIE, 10ns mas. skew



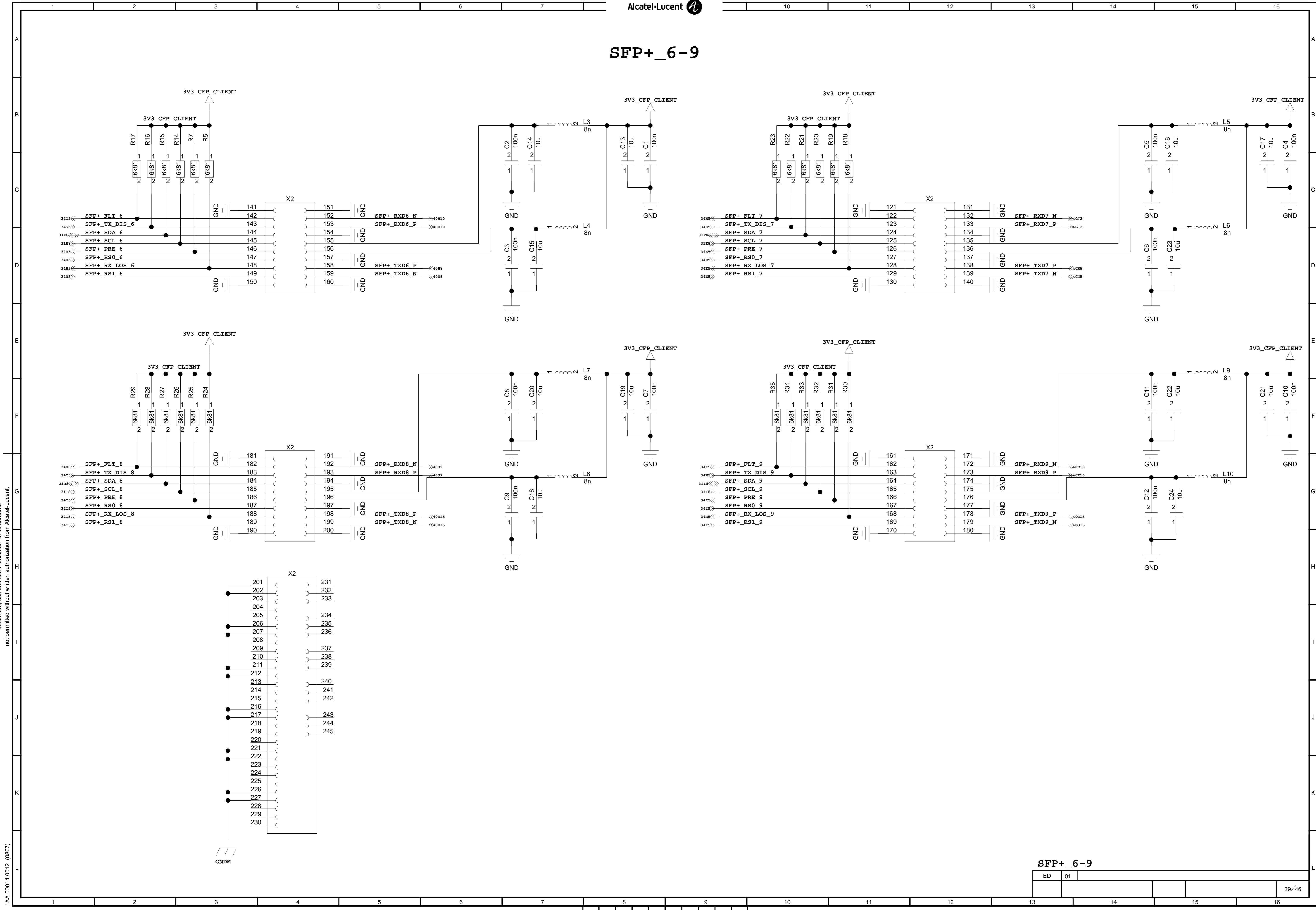
FLEXFRAMER MFPO/PCIE/GL/POWER

SFP+_0-5



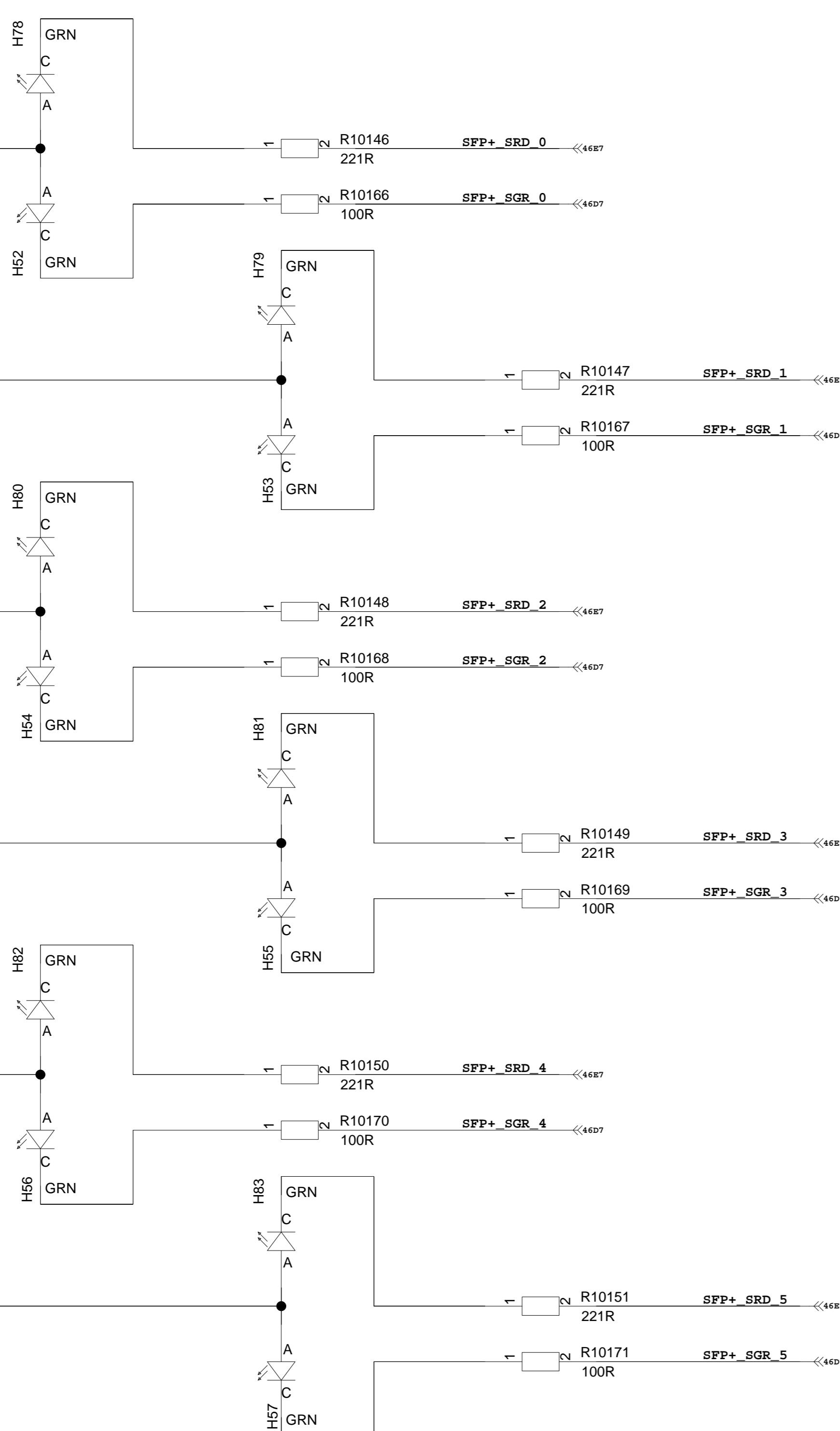
SFP+_0-5

SFP+_6-9

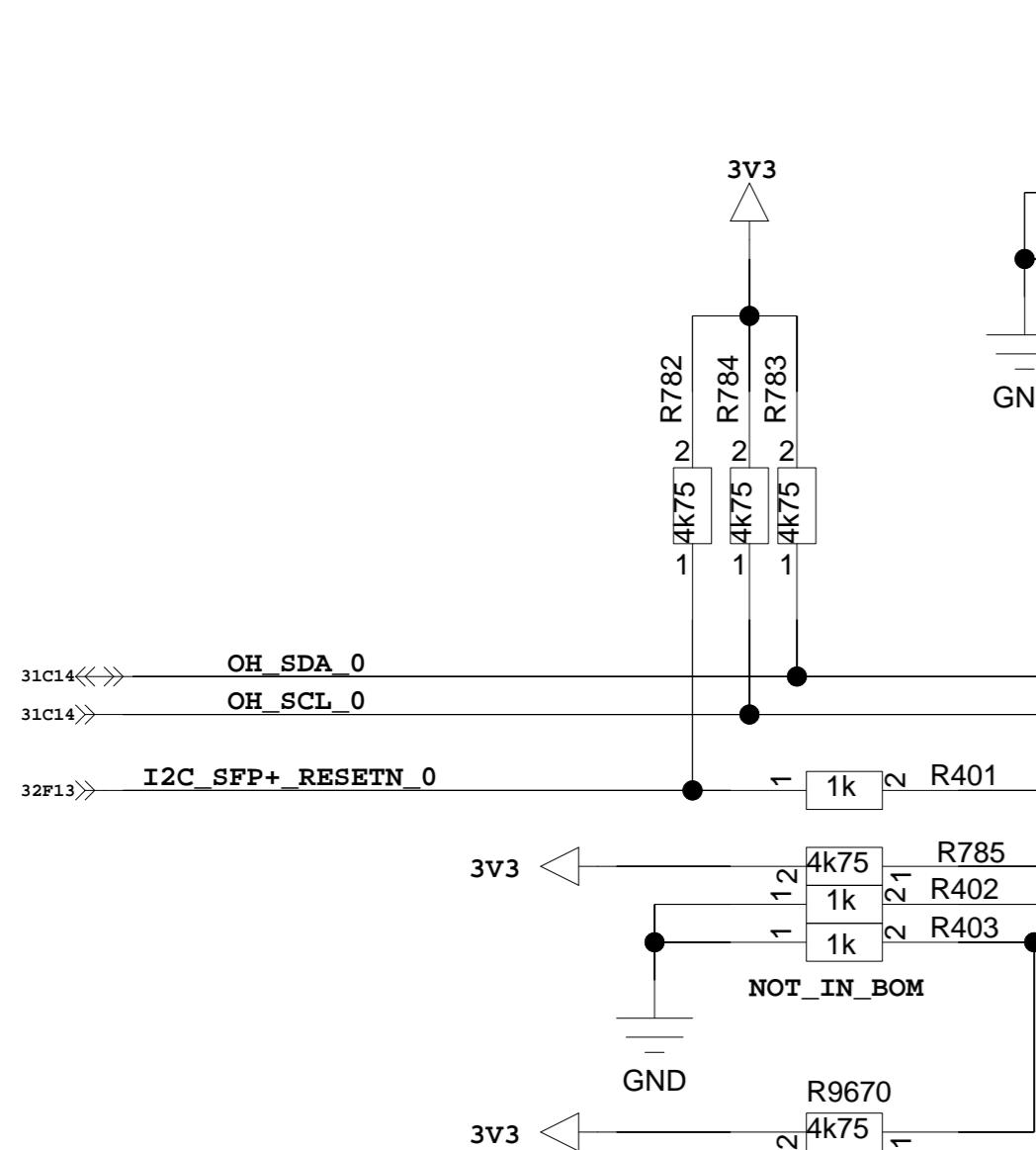


SFP+ LINK/PORT LEDS PART 1

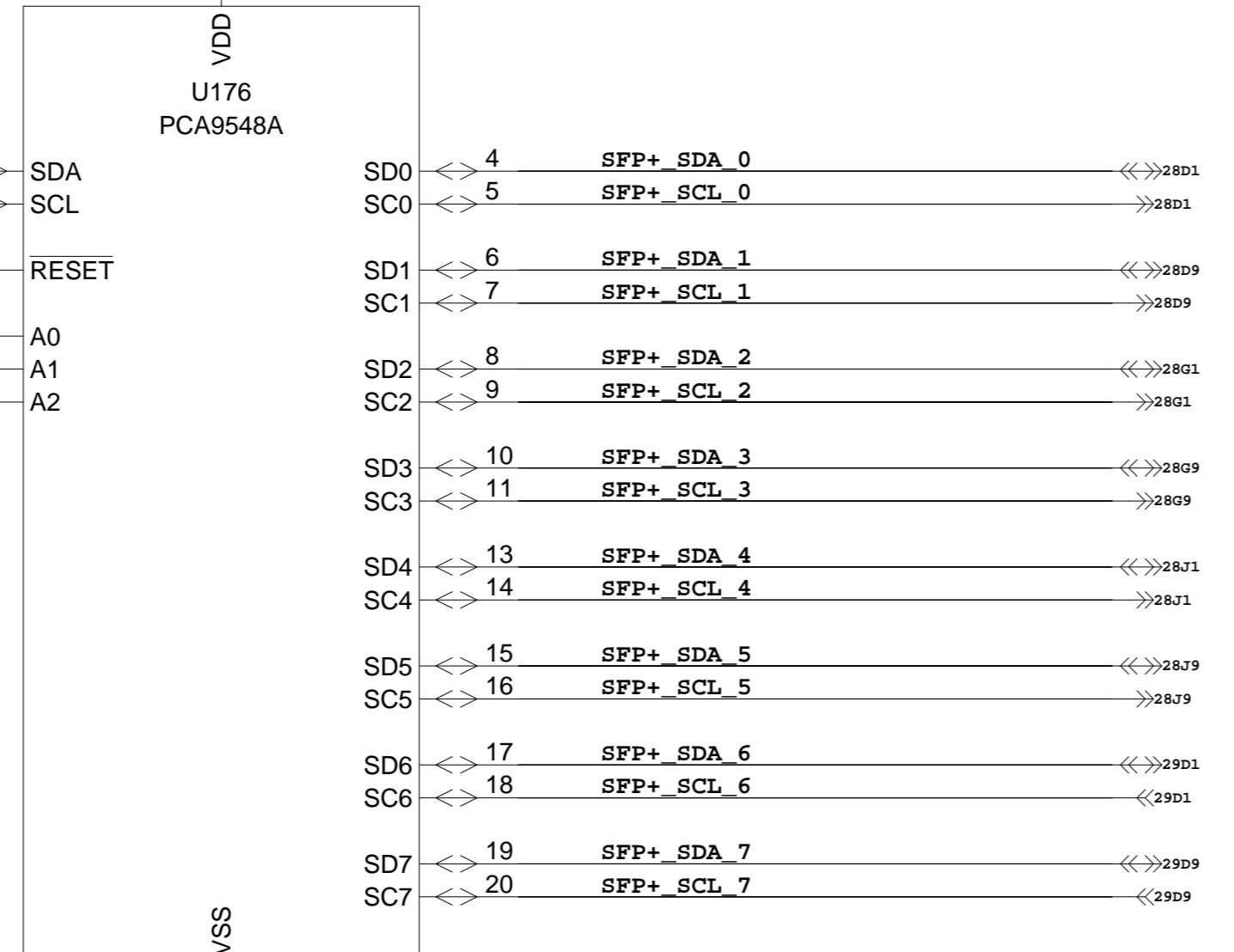
STATUS LEDS



I2C EXPANDERS



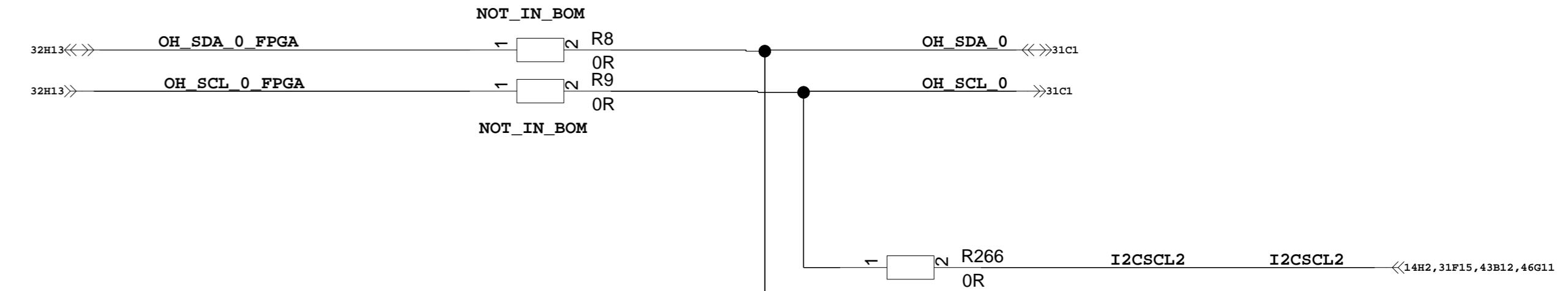
I2C ADDRESS = 1110 101R



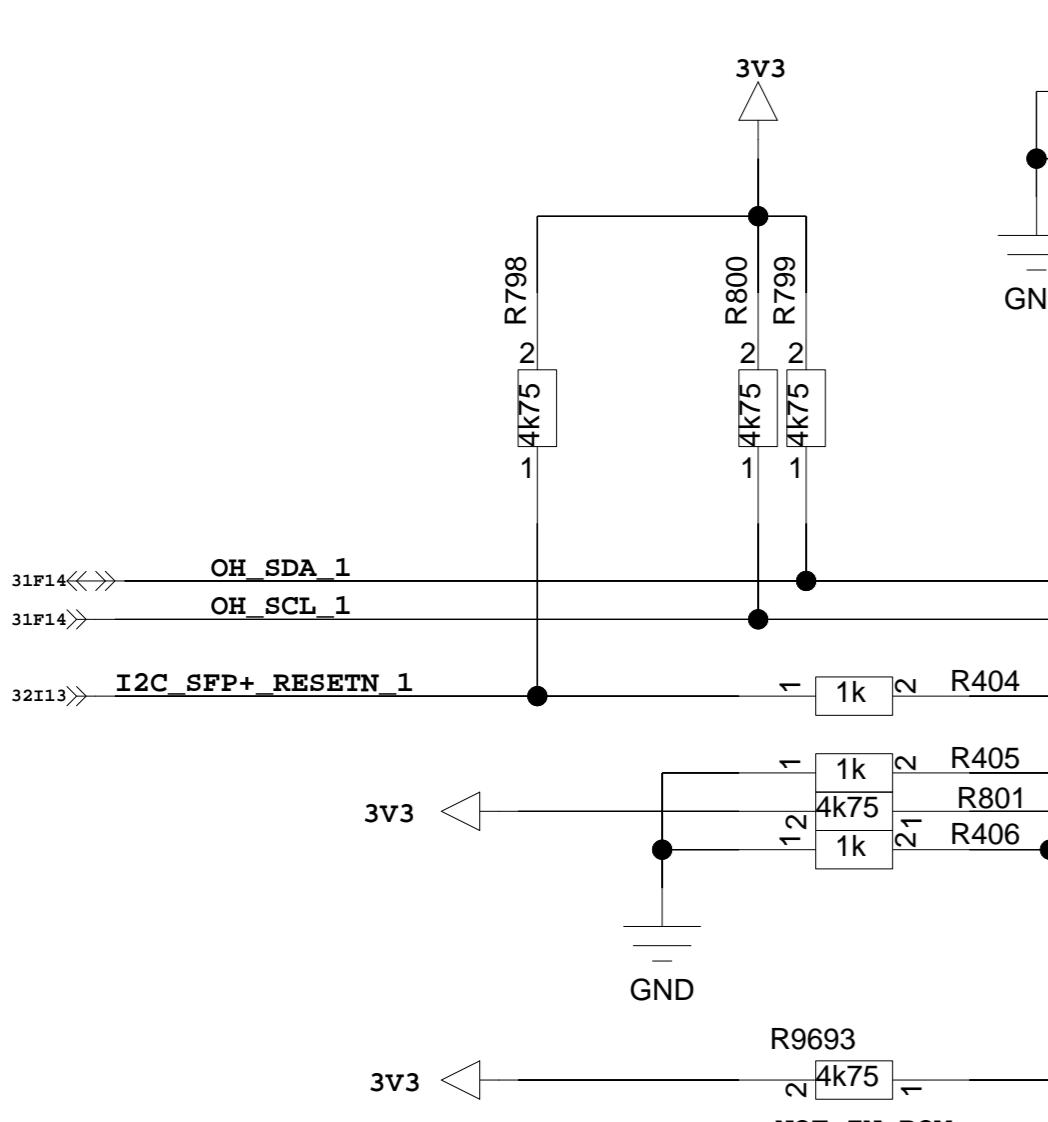
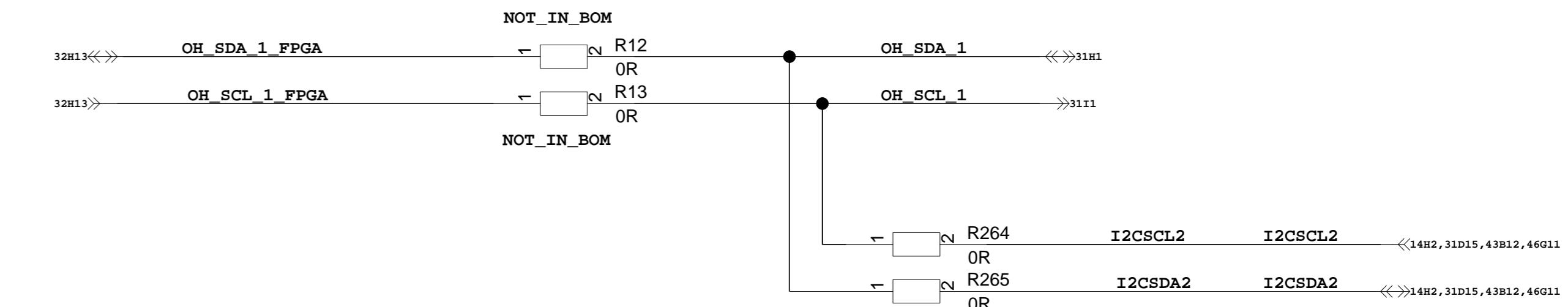
U176 PCA9548A

SD0 \leftrightarrow 4 SFP+ SDA 0 \leftrightarrow 28D1
 SC0 \leftrightarrow 5 SFP+ SCL 0 \rightarrow 28D1
 SD1 \leftrightarrow 6 SFP+ SDA 1 \leftrightarrow 28D9
 SC1 \leftrightarrow 7 SFP+ SCL 1 \rightarrow 28D9
 SD2 \leftrightarrow 8 SFP+ SDA 2 \leftrightarrow 28G1
 SC2 \leftrightarrow 9 SFP+ SCL 2 \rightarrow 28G1
 SD3 \leftrightarrow 10 SFP+ SDA 3 \leftrightarrow 28G9
 SC3 \leftrightarrow 11 SFP+ SCL 3 \rightarrow 28G9
 SD4 \leftrightarrow 13 SFP+ SDA 4 \leftrightarrow 28J1
 SC4 \leftrightarrow 14 SFP+ SCL 4 \rightarrow 28J1
 SD5 \leftrightarrow 15 SFP+ SDA 5 \leftrightarrow 28J9
 SC5 \leftrightarrow 16 SFP+ SCL 5 \rightarrow 28J9
 SD6 \leftrightarrow 17 SFP+ SDA 6 \leftrightarrow 29D1
 SC6 \leftrightarrow 18 SFP+ SCL 6 \rightarrow 29D1
 SD7 \leftrightarrow 19 SFP+ SDA 7 \leftrightarrow 29D9
 SC7 \leftrightarrow 20 SFP+ SCL 7 \rightarrow 29D9

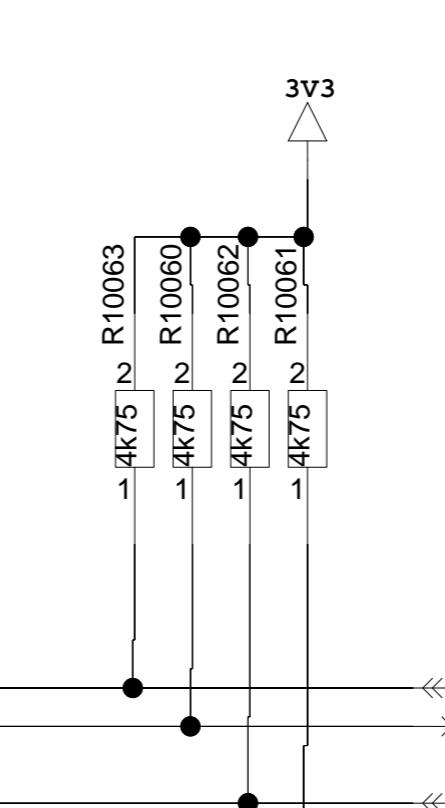
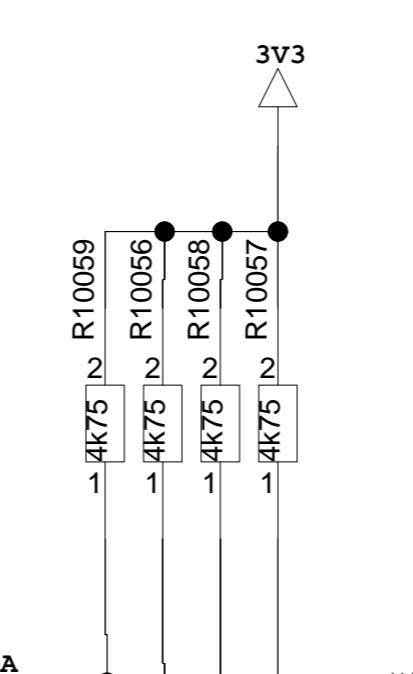
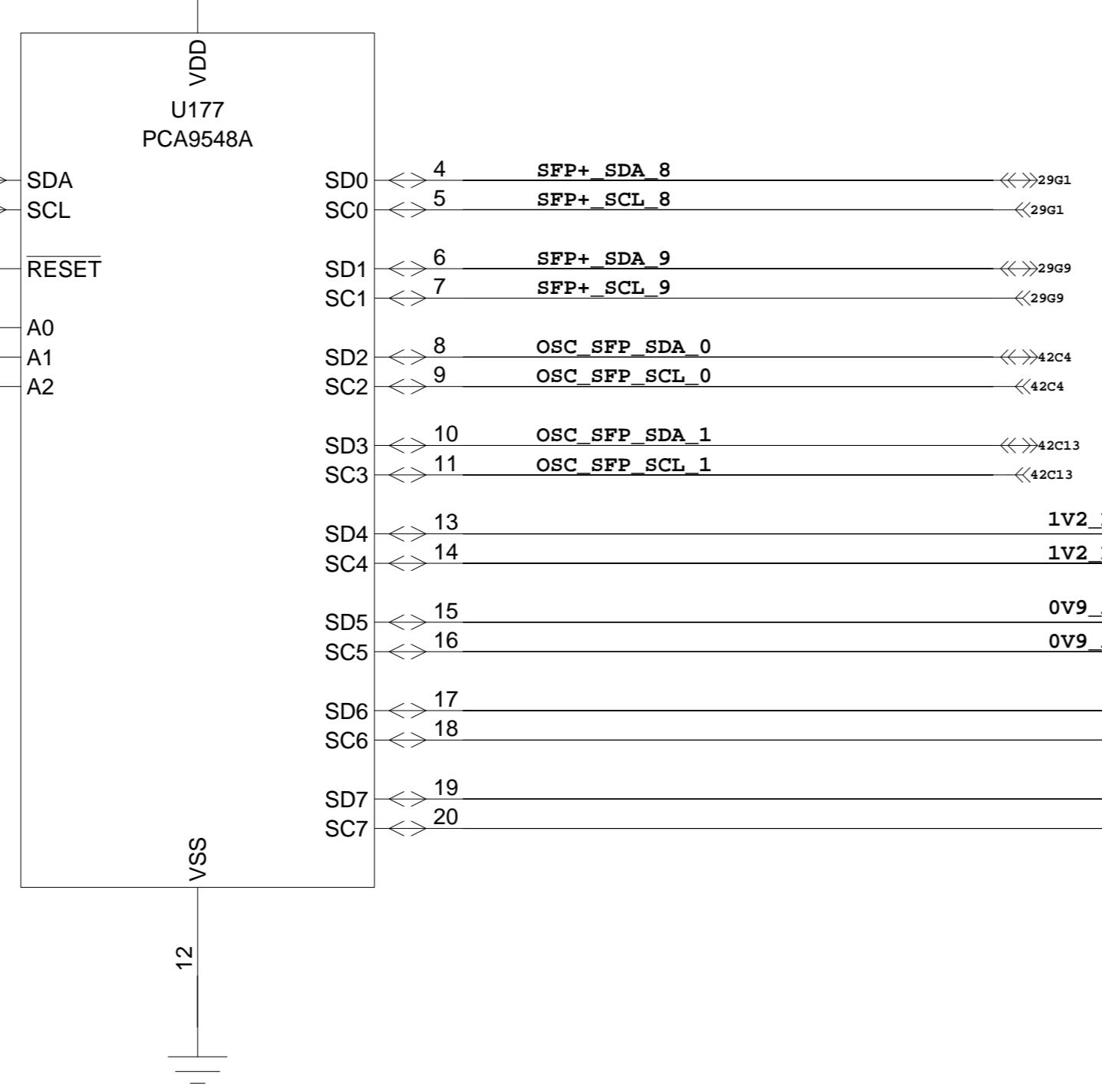
ALL CLOSE TO U176



ALL CLOSE TO U177



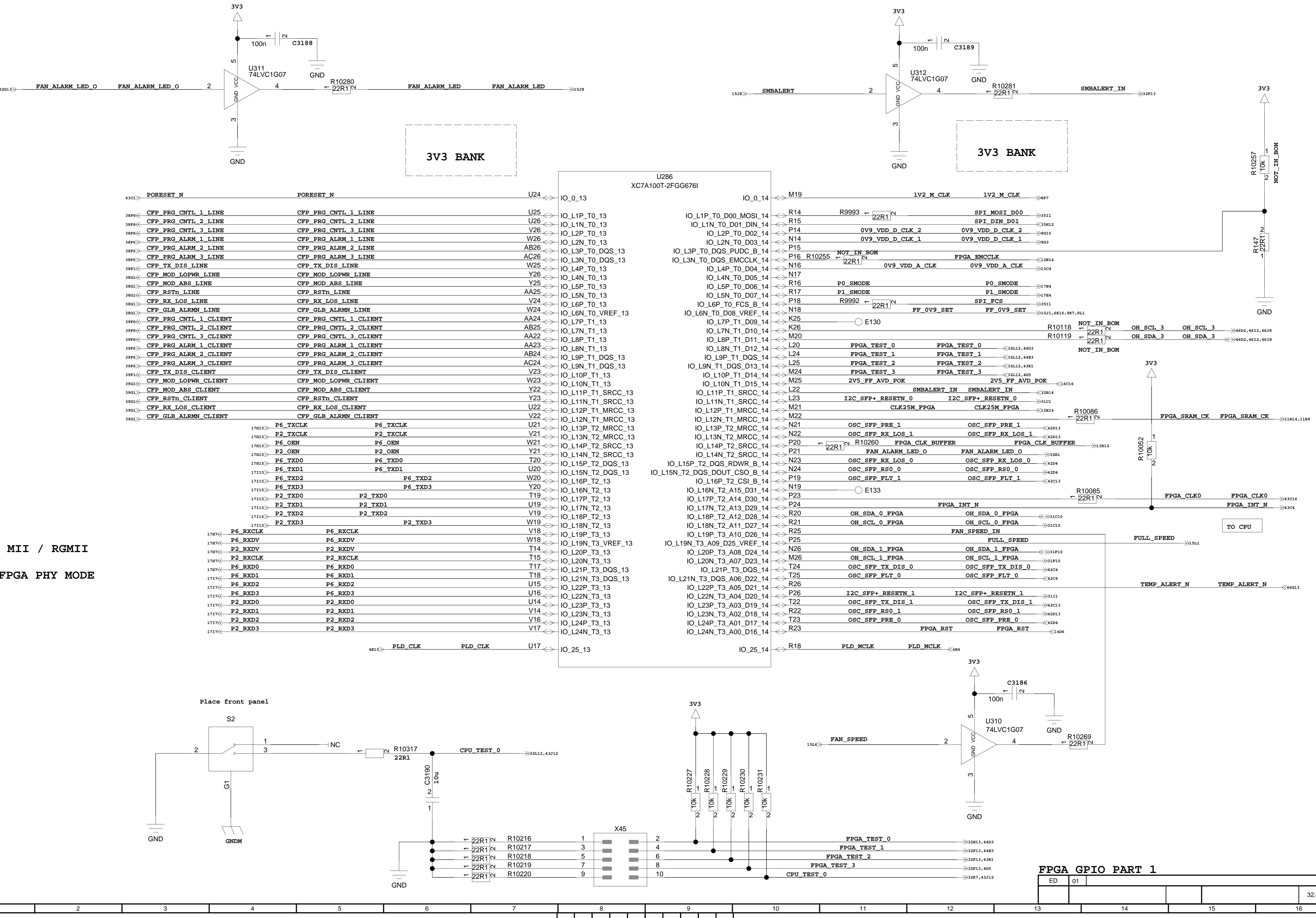
I2C ADDRESS = 1110 010R



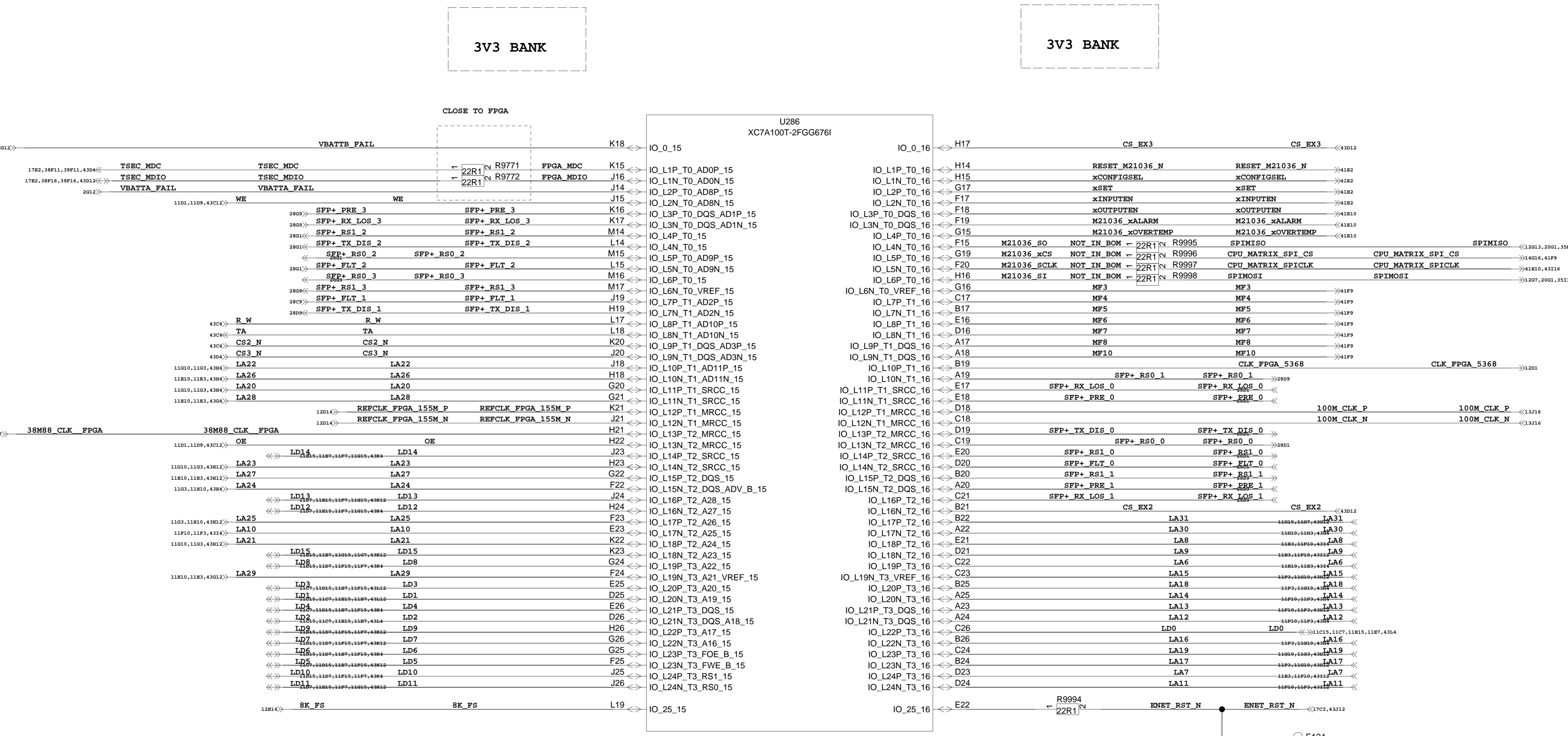
I2C EXPANDERS

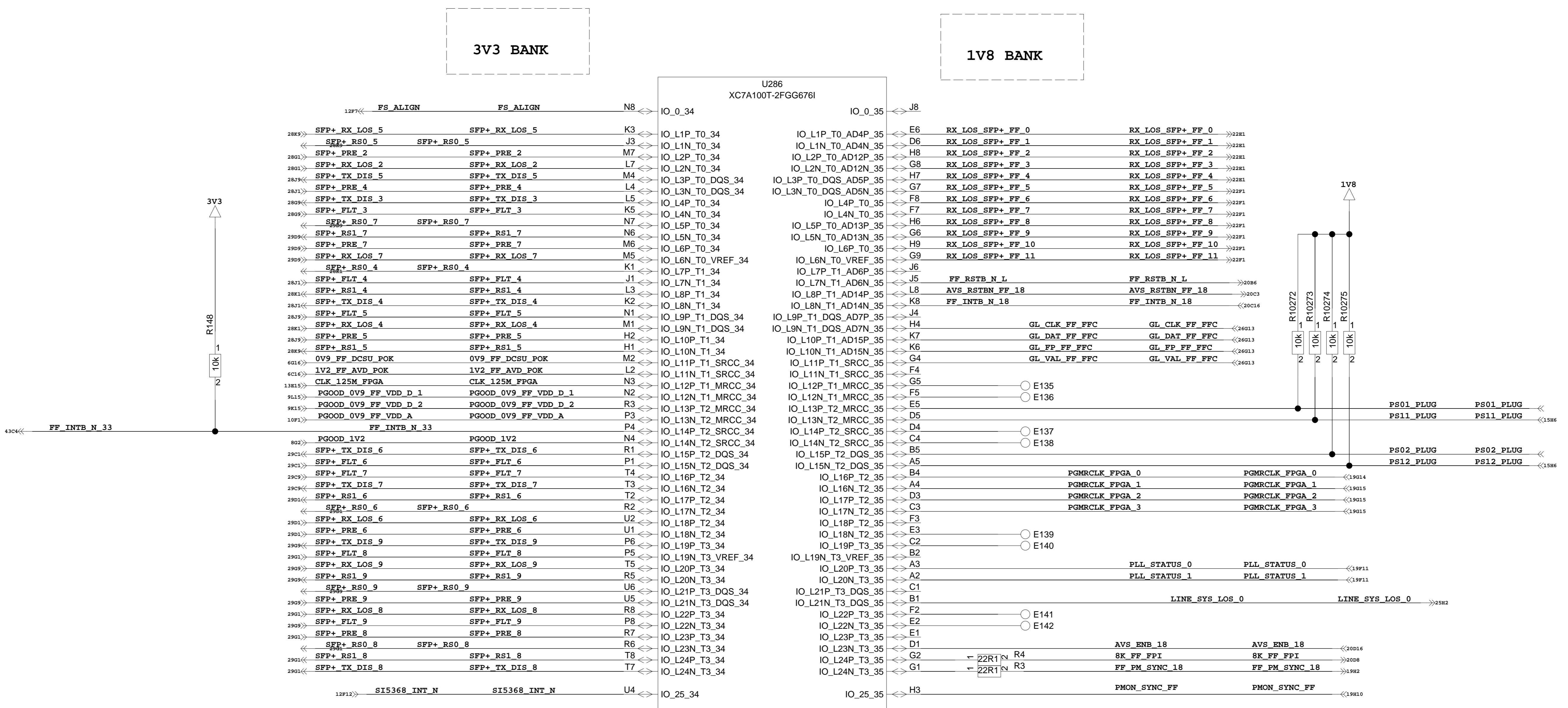
ED	01				

FPGA GPIO PART 1

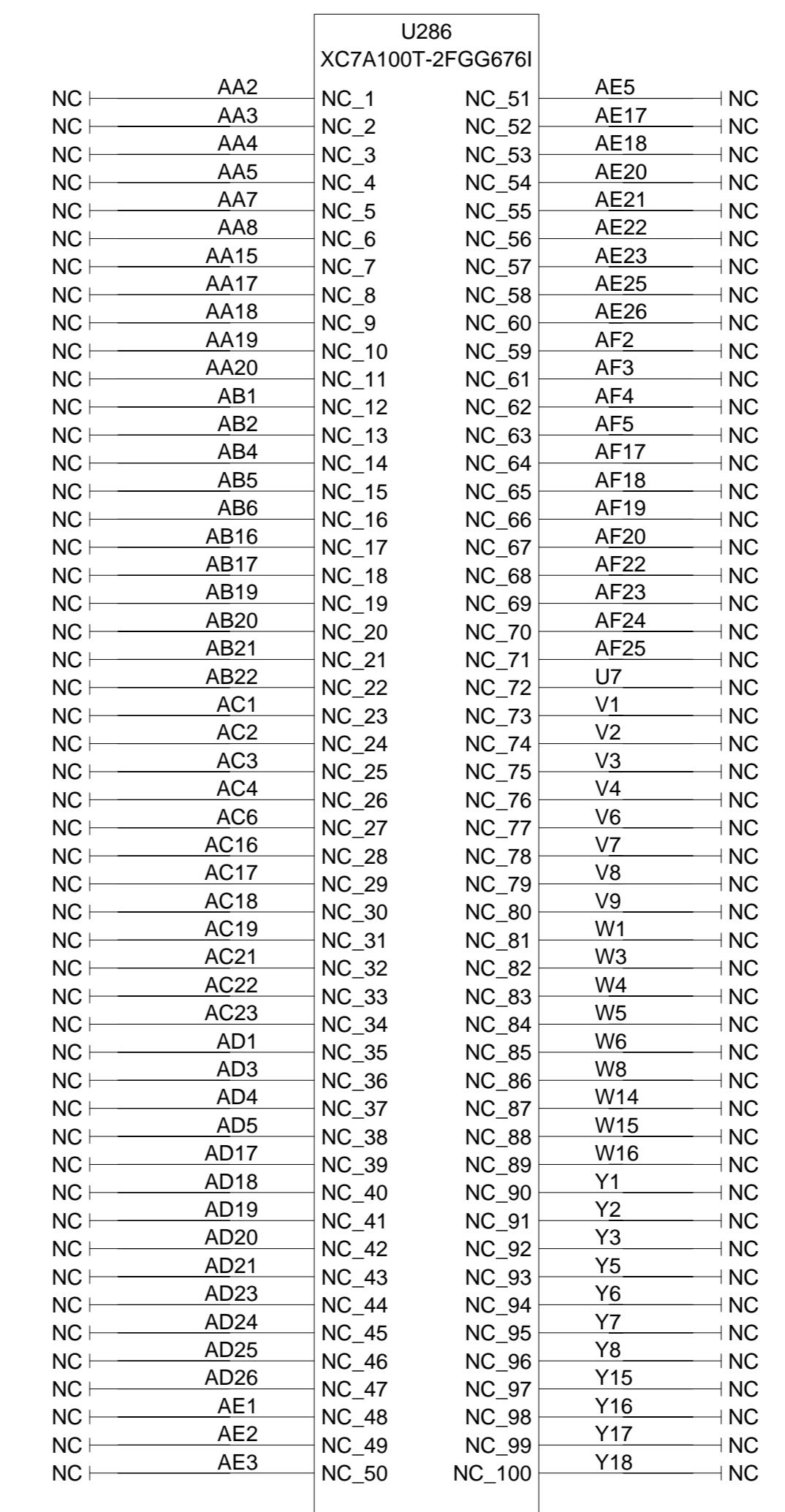
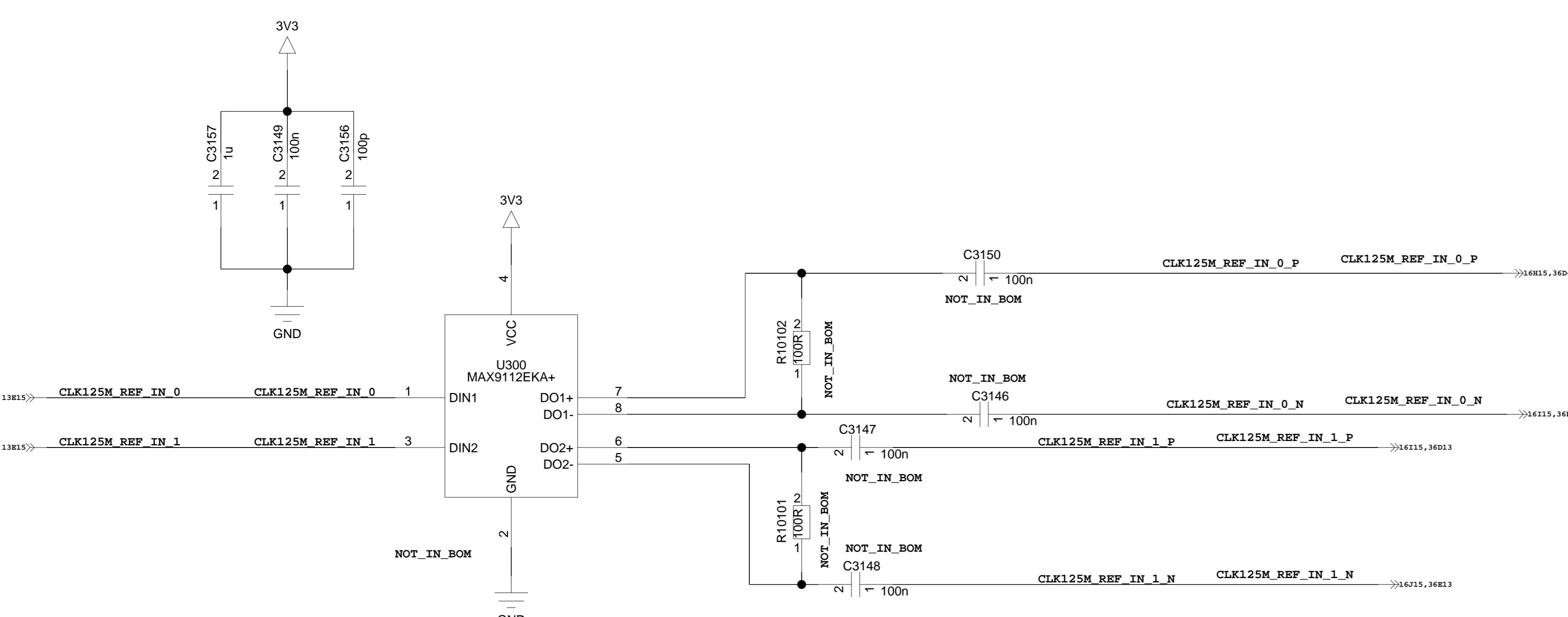
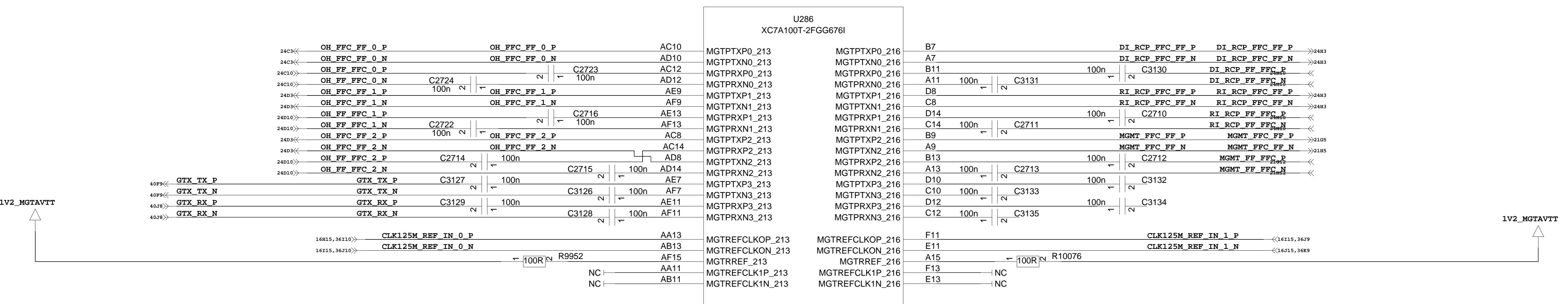


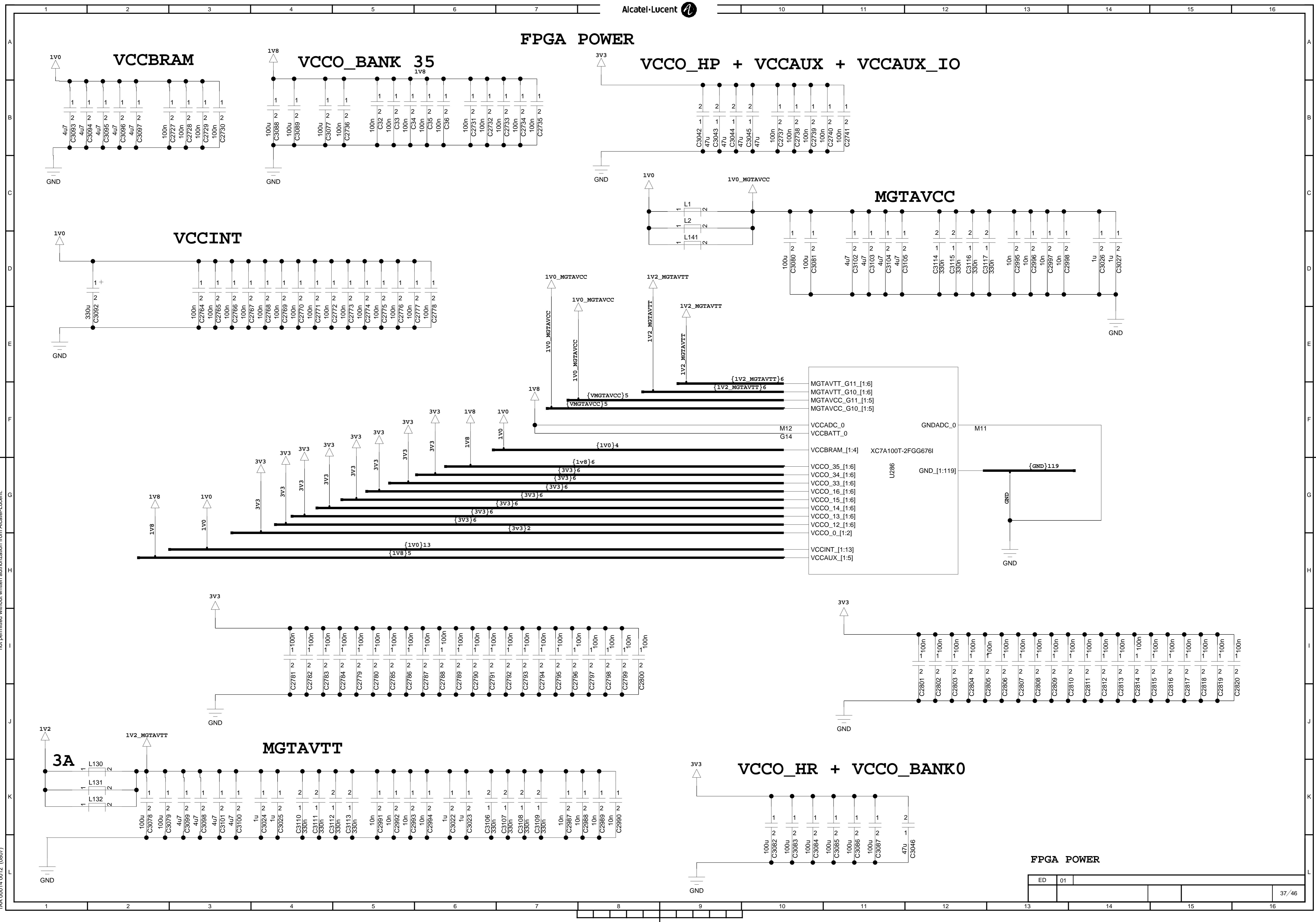
FPGA GPIO PART 2



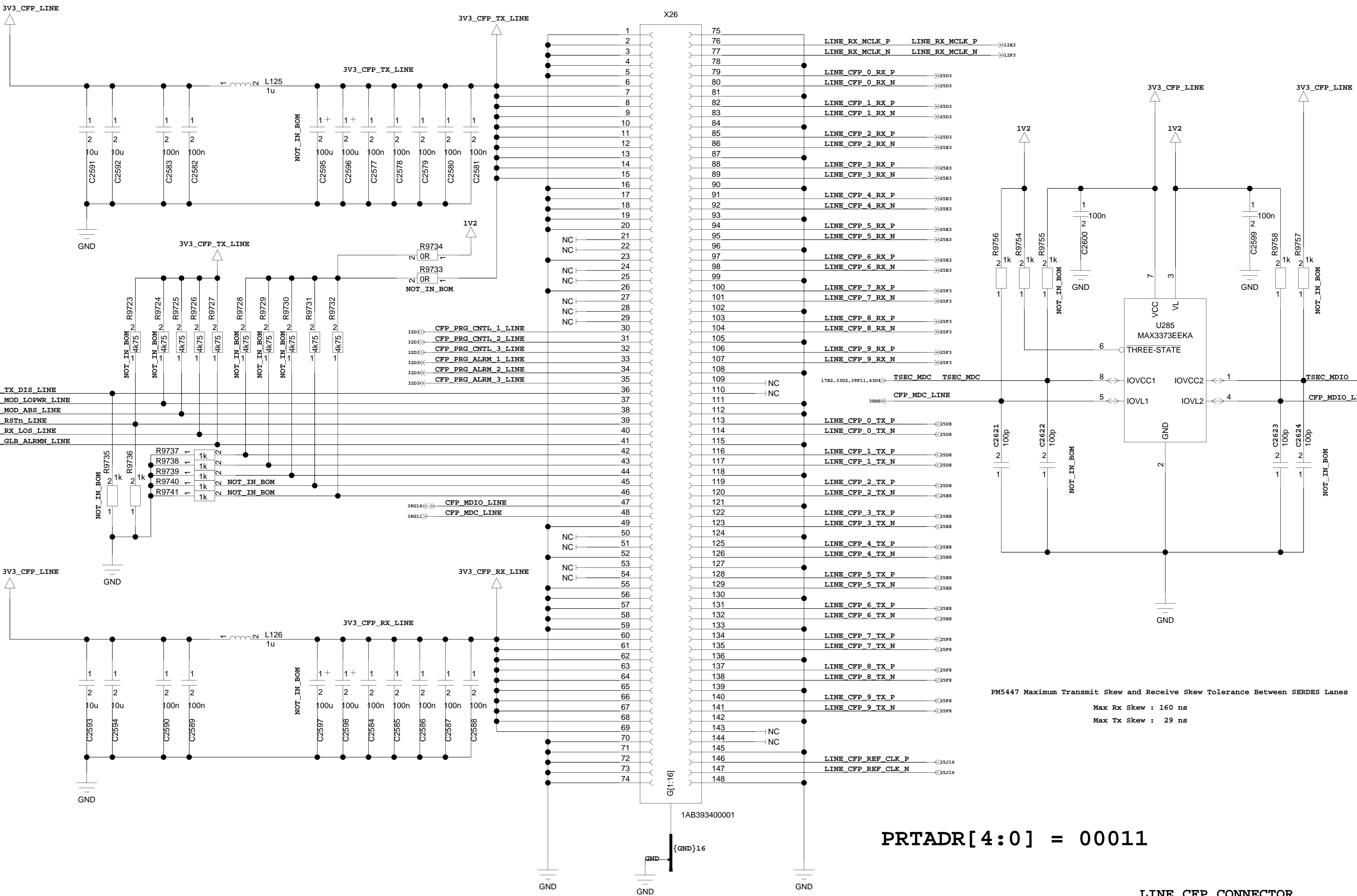


FPGA GTX PORTS





LINE CFP CONNECTOR



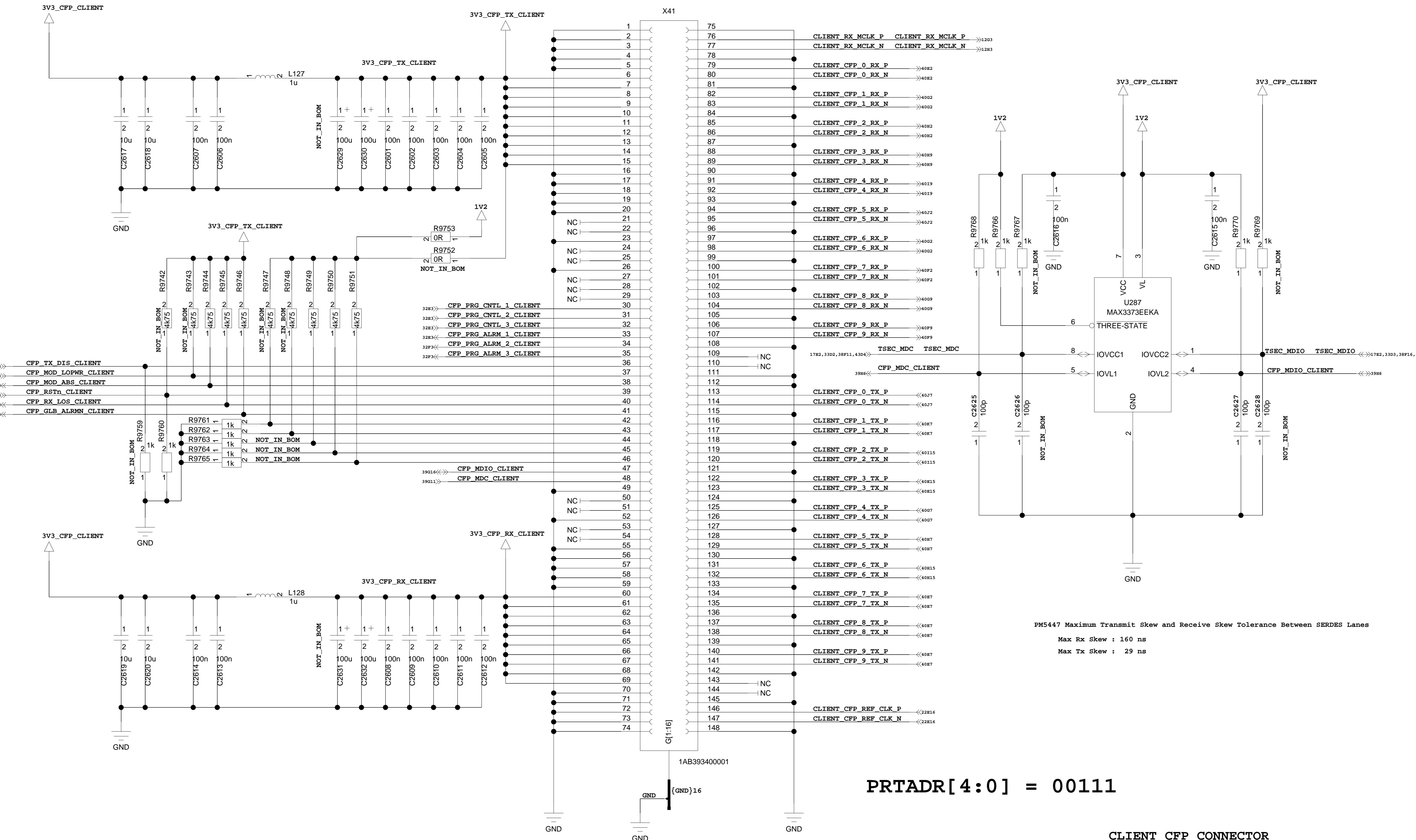
PRTADR[4:0] = 00011

LINE CFP CONNECTOR

ED	01				L
				38/46	

CLIENT CFP CONNECTOR

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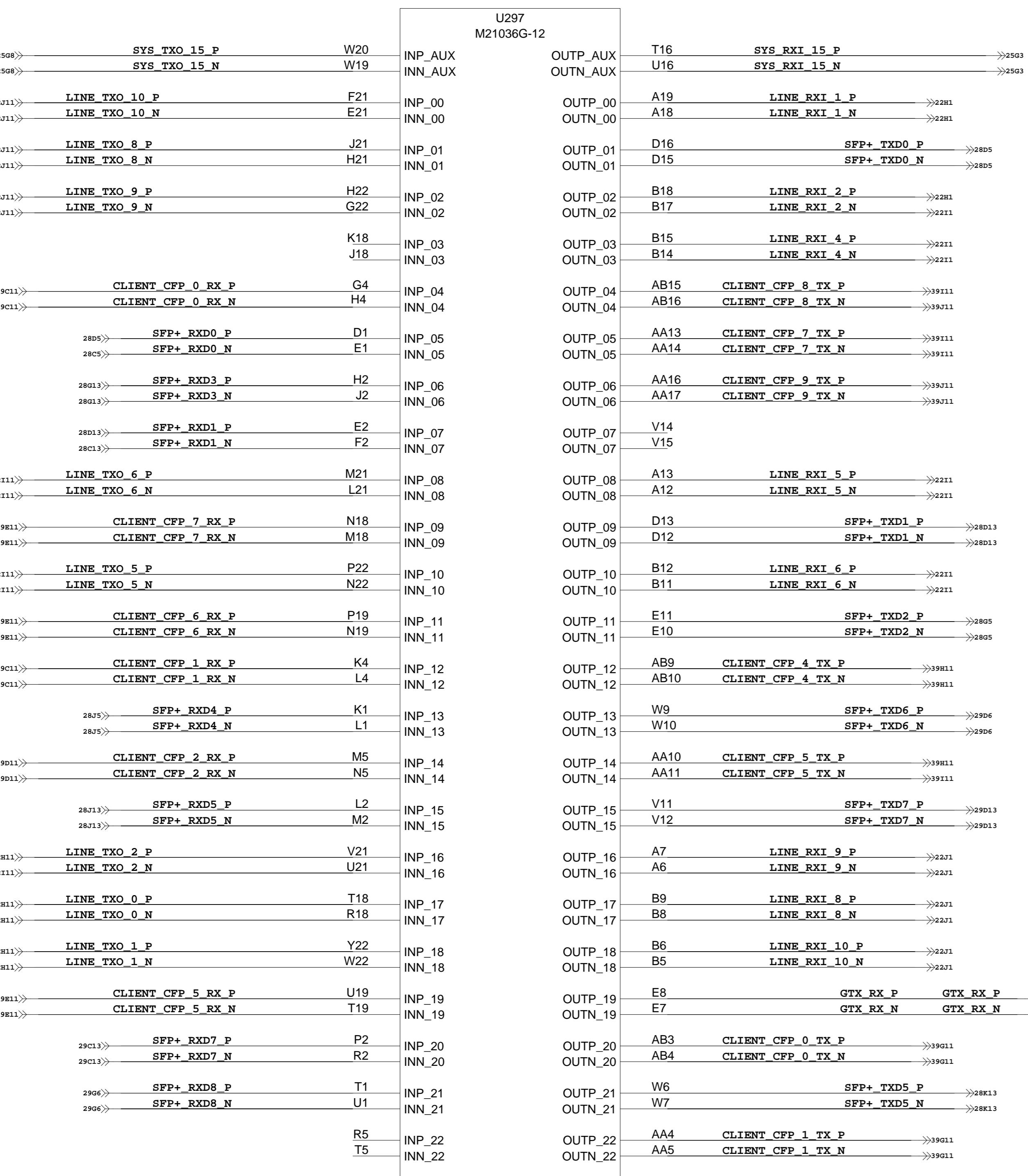


PRTADR[4 : 0] = 00111

ENT CFP CONNECTOR

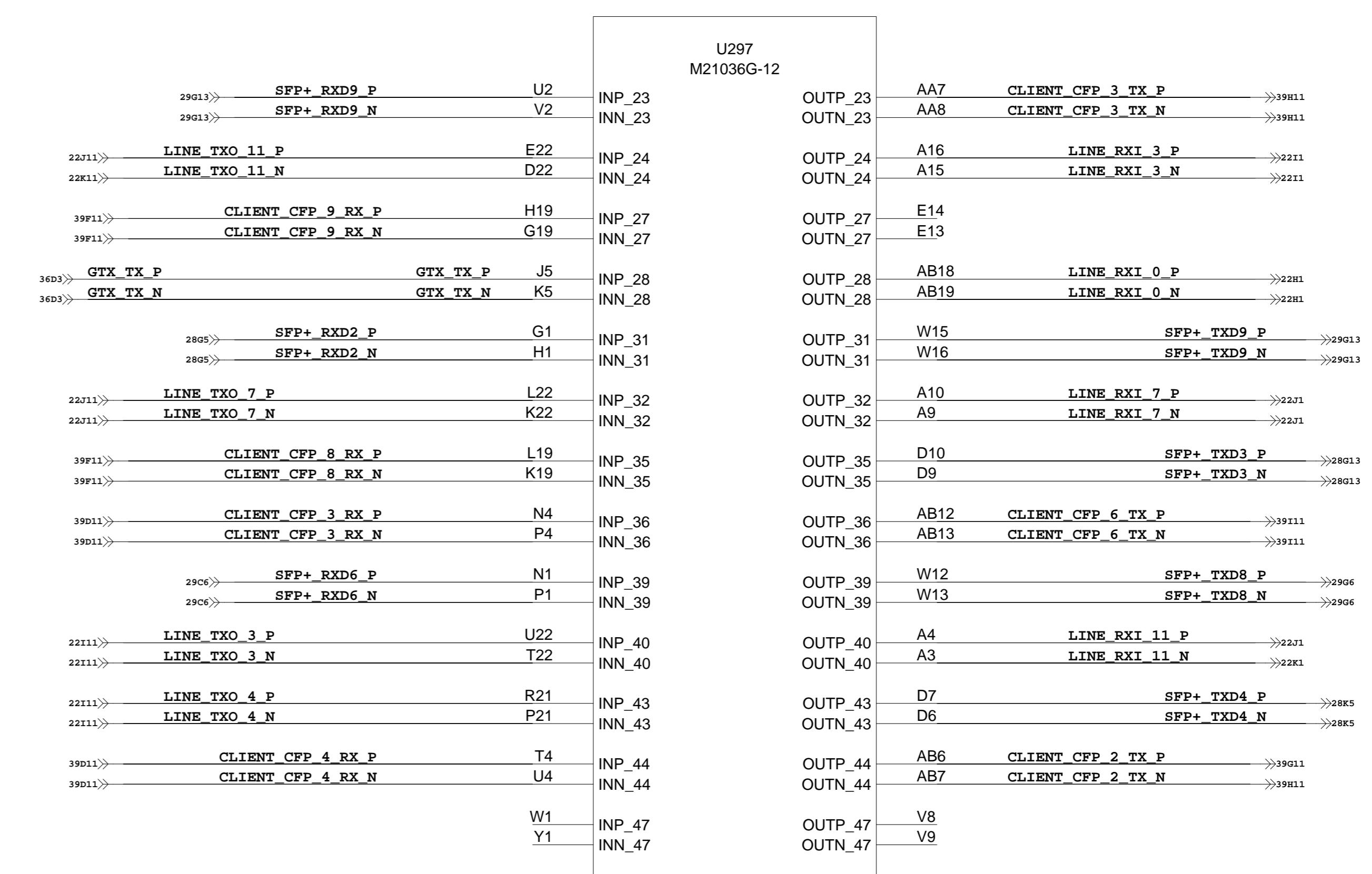
ED	01				L
				39/46	

MATRIX XAUI/SYS



RX AC COUPLING FROM PM5447

TX DC COUPLING TO PM5447

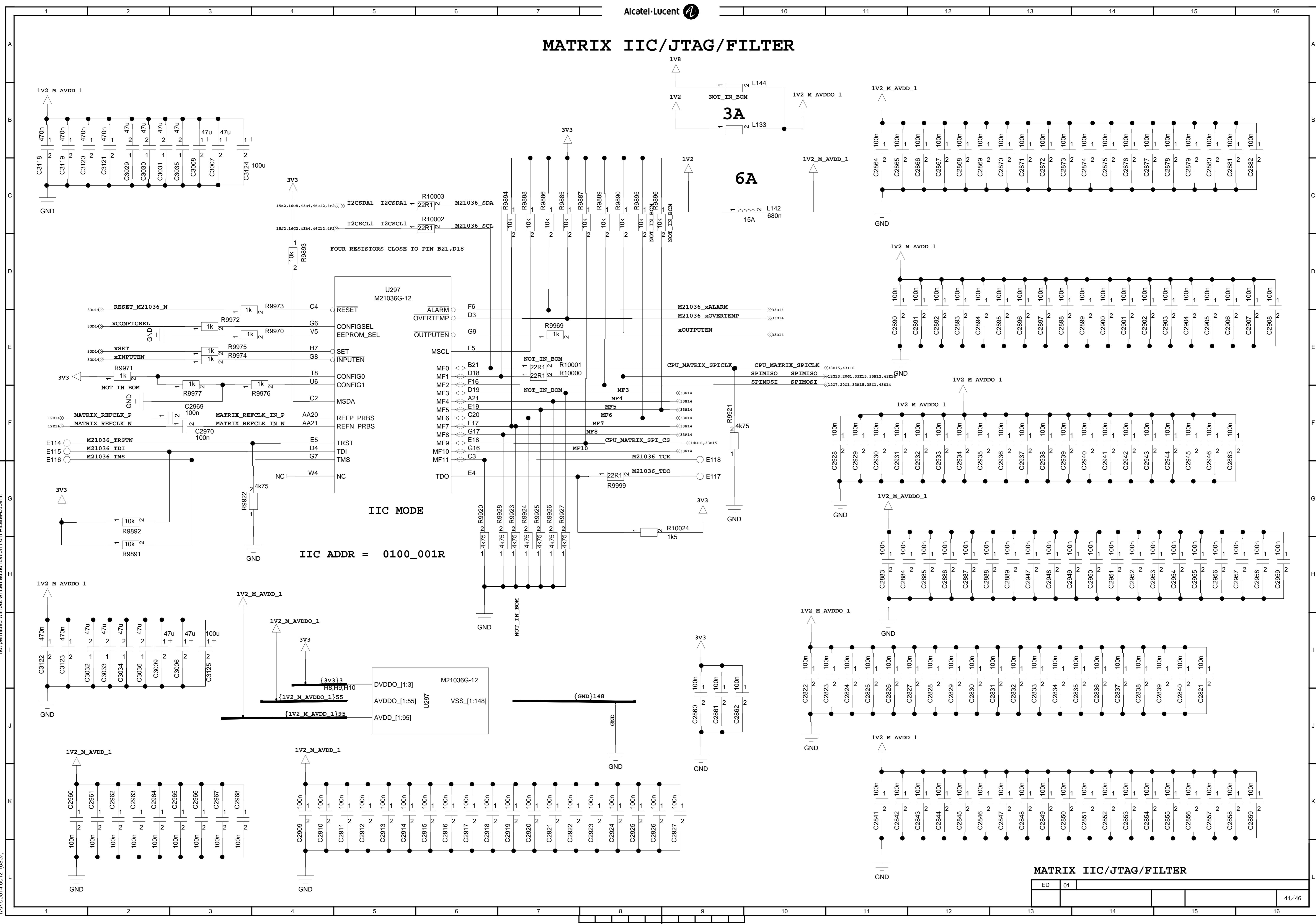


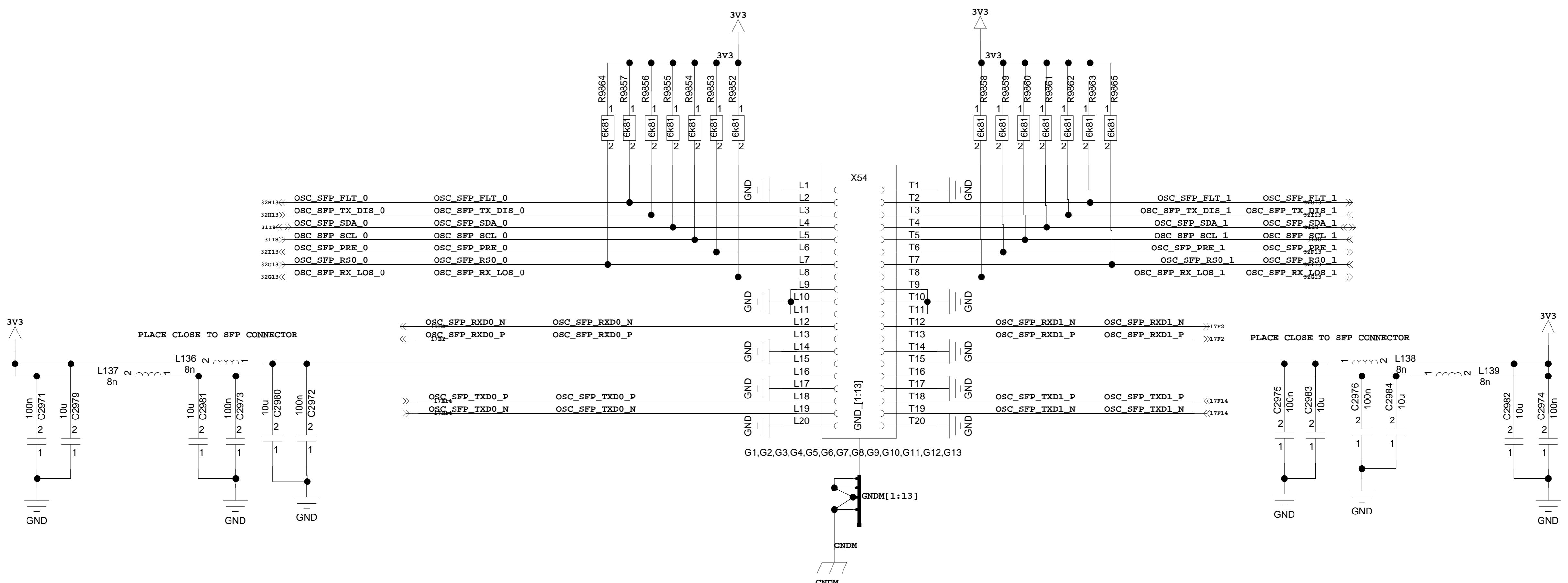
MATRIX XAUI/SYS

ED	01			
				40/46

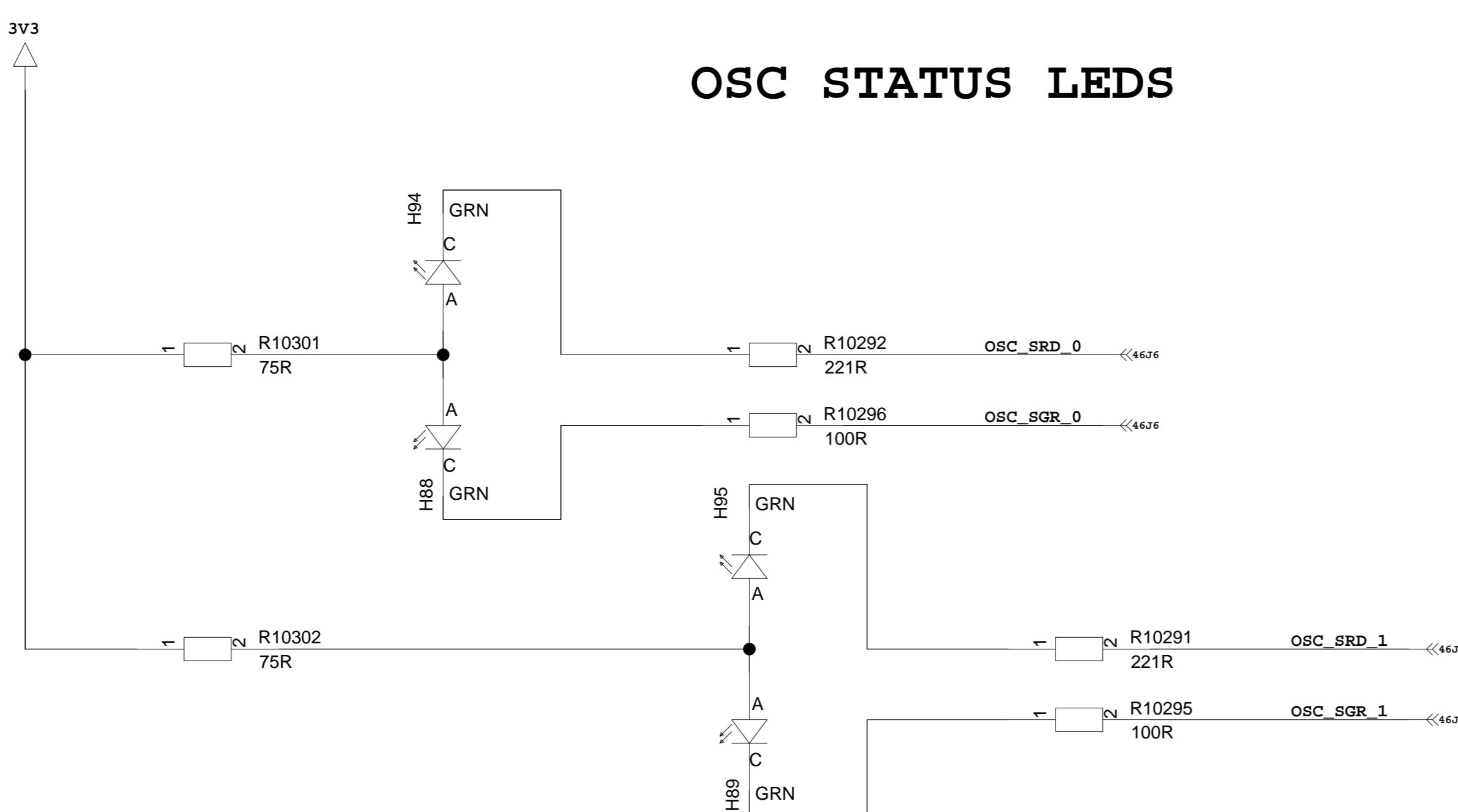
MATRIX IIC/JTAG/FILTER

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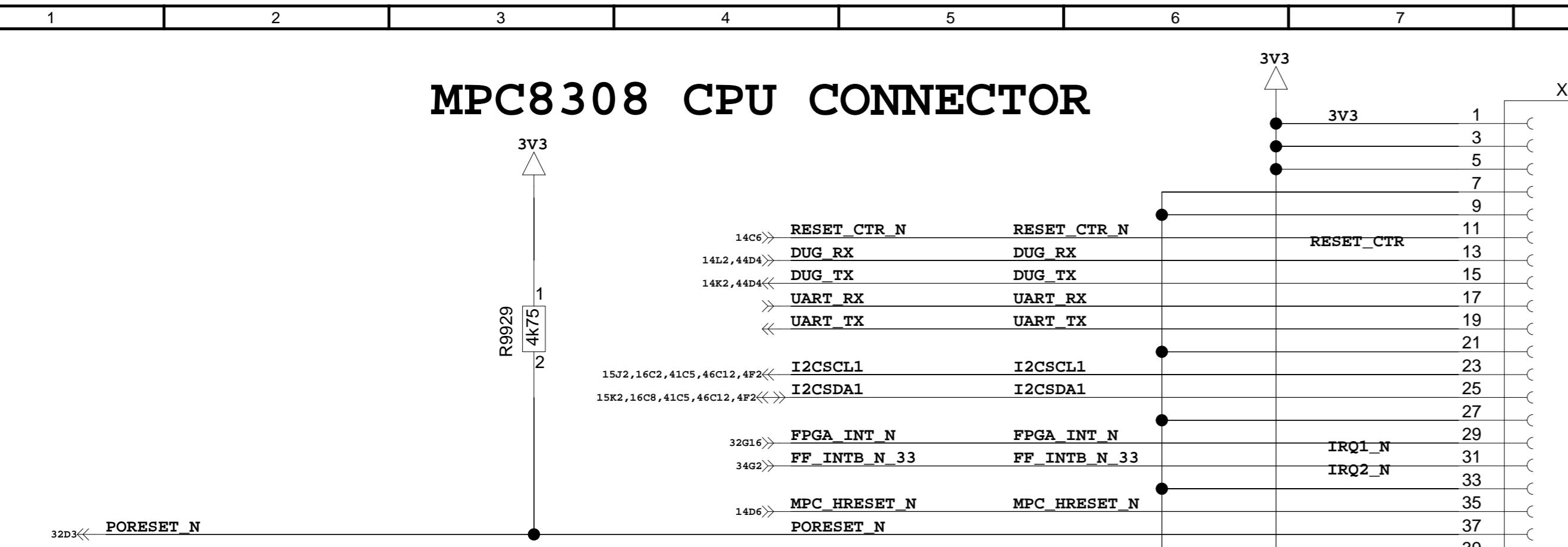


OSC STATUS LEDS



OSC : 100BASE-FX / 1000BASE-X

ED	01					42/46
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CPU with MII MAC mode

NOT USED FOR MII

BACKUP USE

13E15 TSEC2_GTX_CLK125

17E2,33D2,38F11,39F11 TSEC MDC

17H15 P5_TXD3

17H15 P5_TXD2

17H15 P5_TXD1

17G15 P5_TXD0

17G15 P5_RXCLK

17G15 P5_RXCLK

17G15 P5_OEN

17G15 P5_TXCLK

17H6 P5_RXD3

17H6 P5_RXD2

17H6 P5_RXD1

17G6 P5_RXD0

17G6 P5_RXDV

13E15 TSEC2_GTX_CLK125

13E15 CPU_LAN_RX_N

13E15 CPU_LAN_RX_P

44D15 CPU_LAN_RX_N

44D15 CPU_LAN_RX_P

2V5 2V5

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

LA30

LA28

LA26

LA24

LA22

LA20

LA18

LA16

LA14

LA12

LA10

LA8

LA6

LA14

LA12

LA10

LA8

LA6

SRAM_ZZ

SRAM_FT_N

SRAM_MODE

GPIO5

11D1,11E9 SRAM_E3_N_B

11D1,11E9 SRAM_E2_B

11D1,11E9 SRAM_E1_N_B

11C1,11C1 SRAM_E3_N_A

11C1,11C1 SRAM_E2_A

11C1,11C1 SRAM_E1_N_A

11C1,11C1 SRAM_ADV

11D1,11D9 GID0

14J15 GID1

14J15 GID2

14J15 GID3

11E15,11E7,11P7,11G15,3304 LD14

11D7,11E5,11P7,11G15,3304 LD12

11D15,11B7,11P7,11G15,3304 LD10

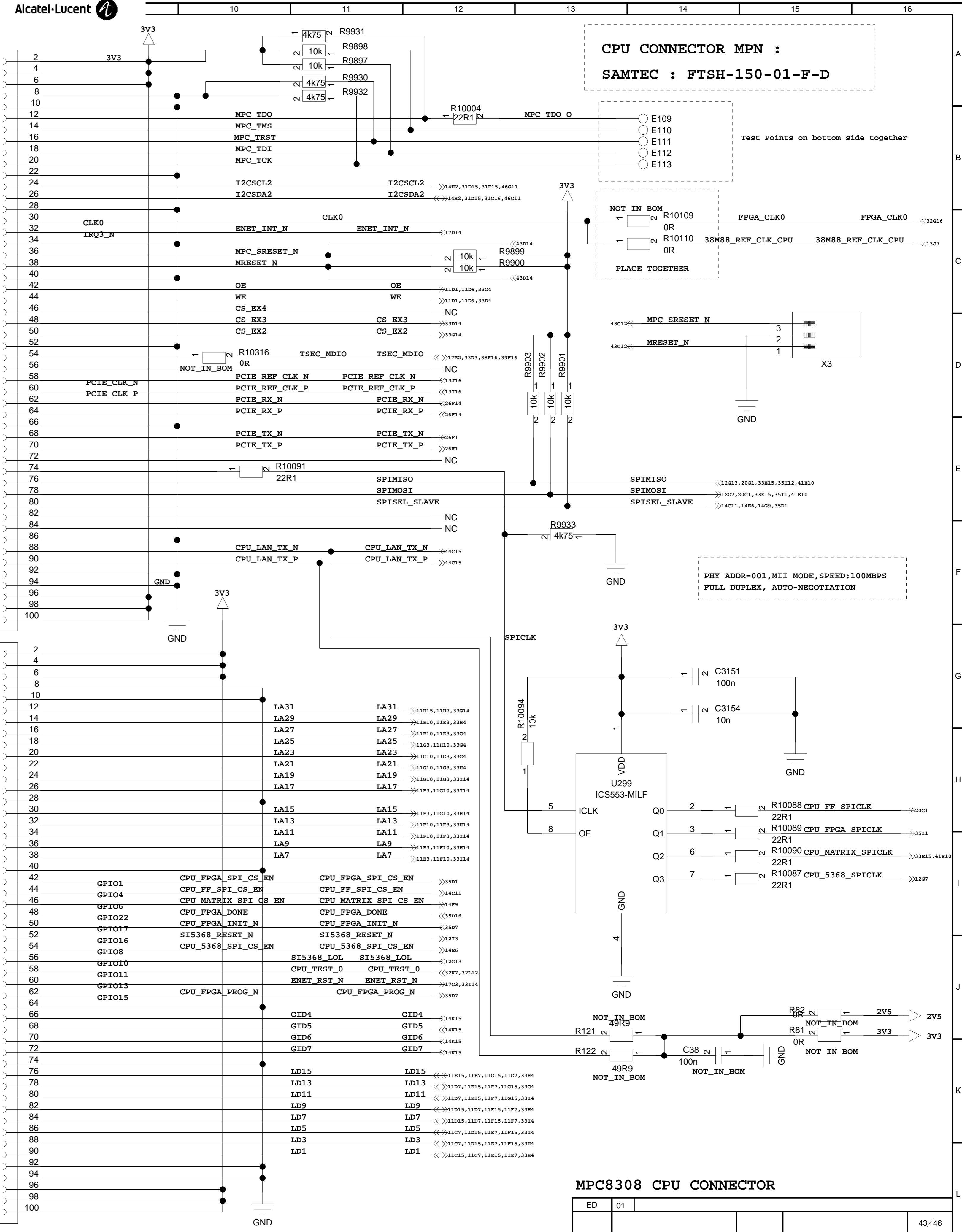
11D15,11B7,11P7,11G15,3304 LD8

11D15,11B7,11P7,11G15,3304 LD6

11C7,11D15,11B7,11P15,3304 LD4

11C15,11C7,11B15,11B7,11P15,3304 LD2

11C15,11C7,11B15,11B7,11P15,3304 LD0



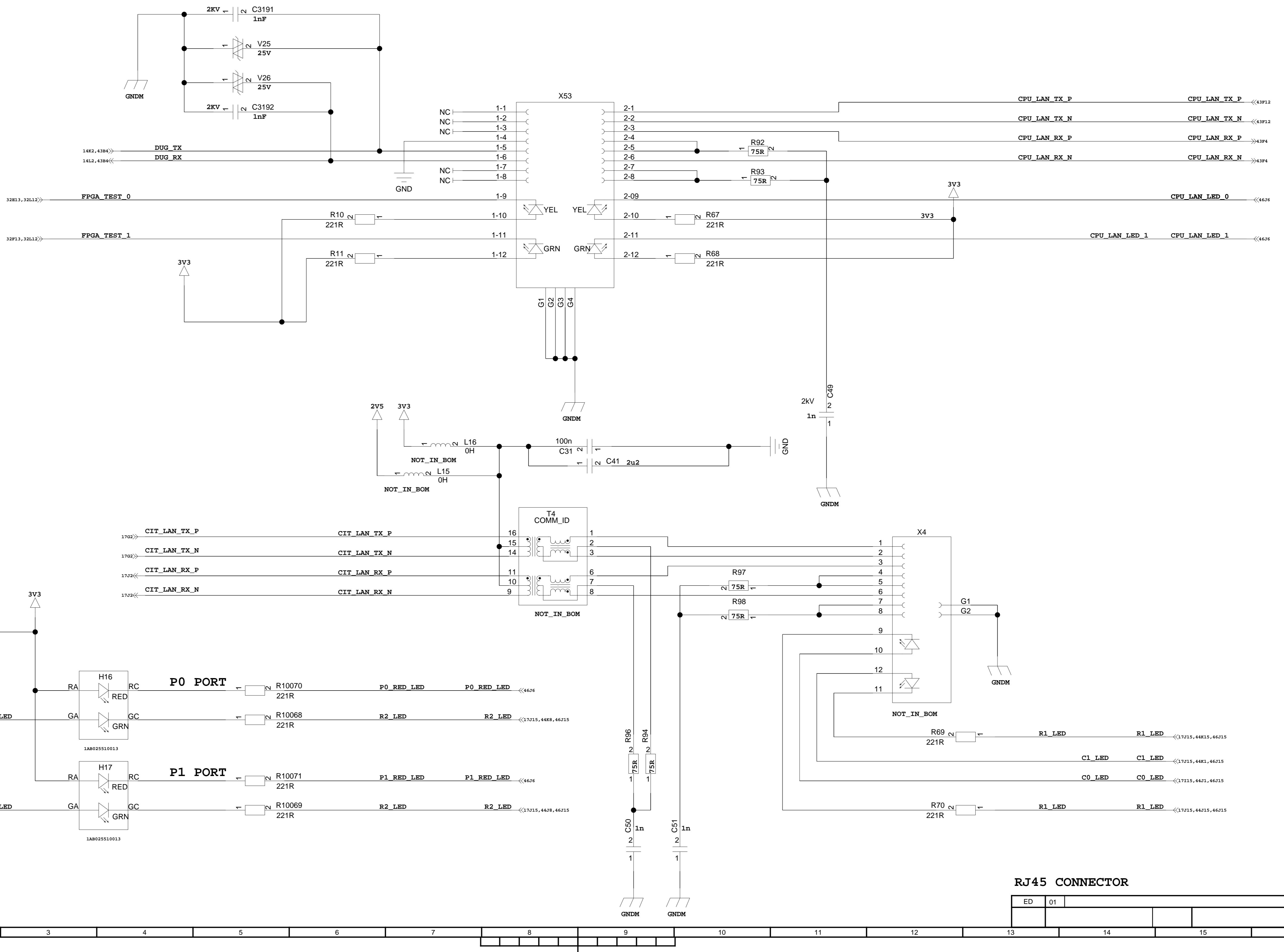
Vendor:

SAMTEC

New Schematic and Layout Lib needed

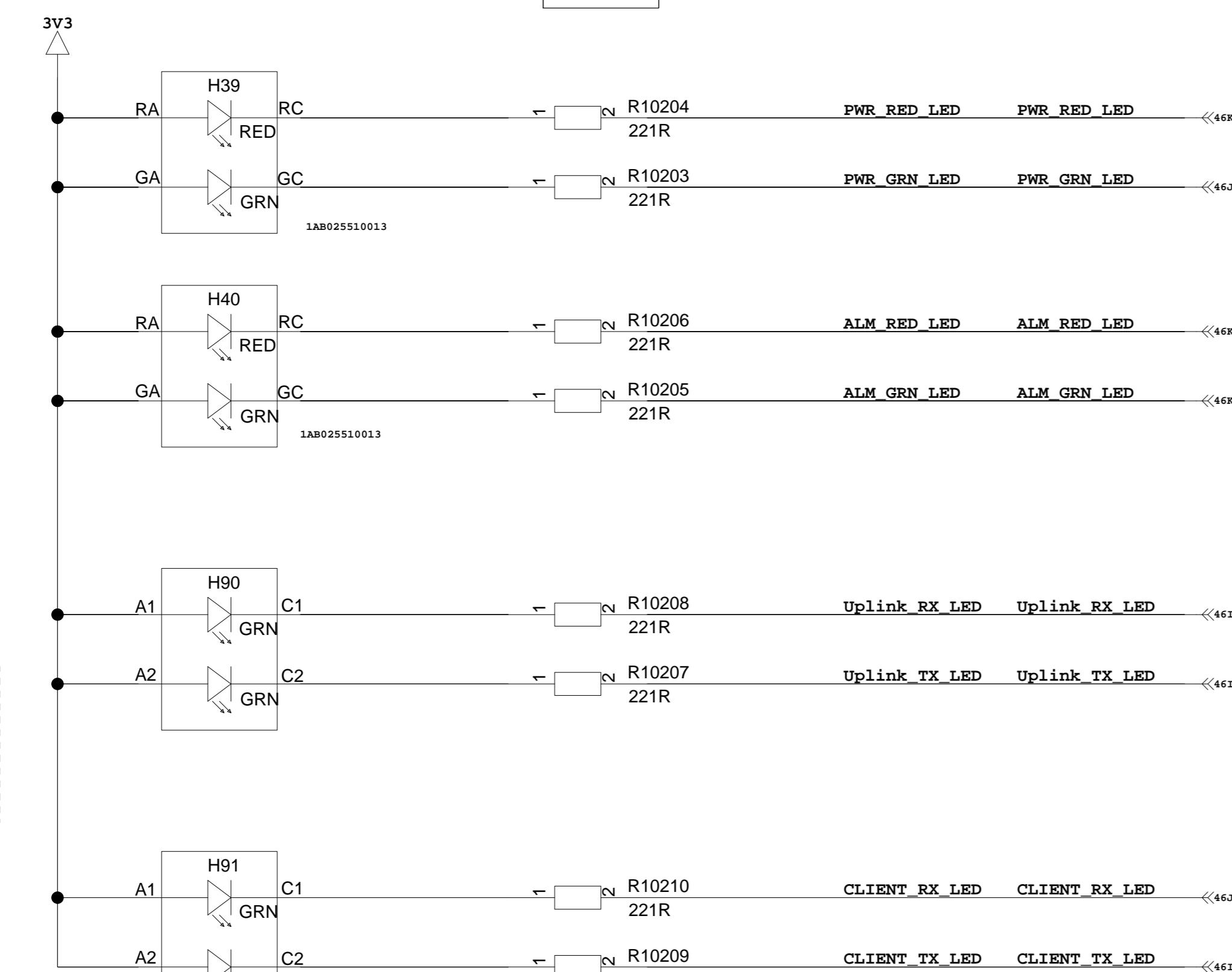
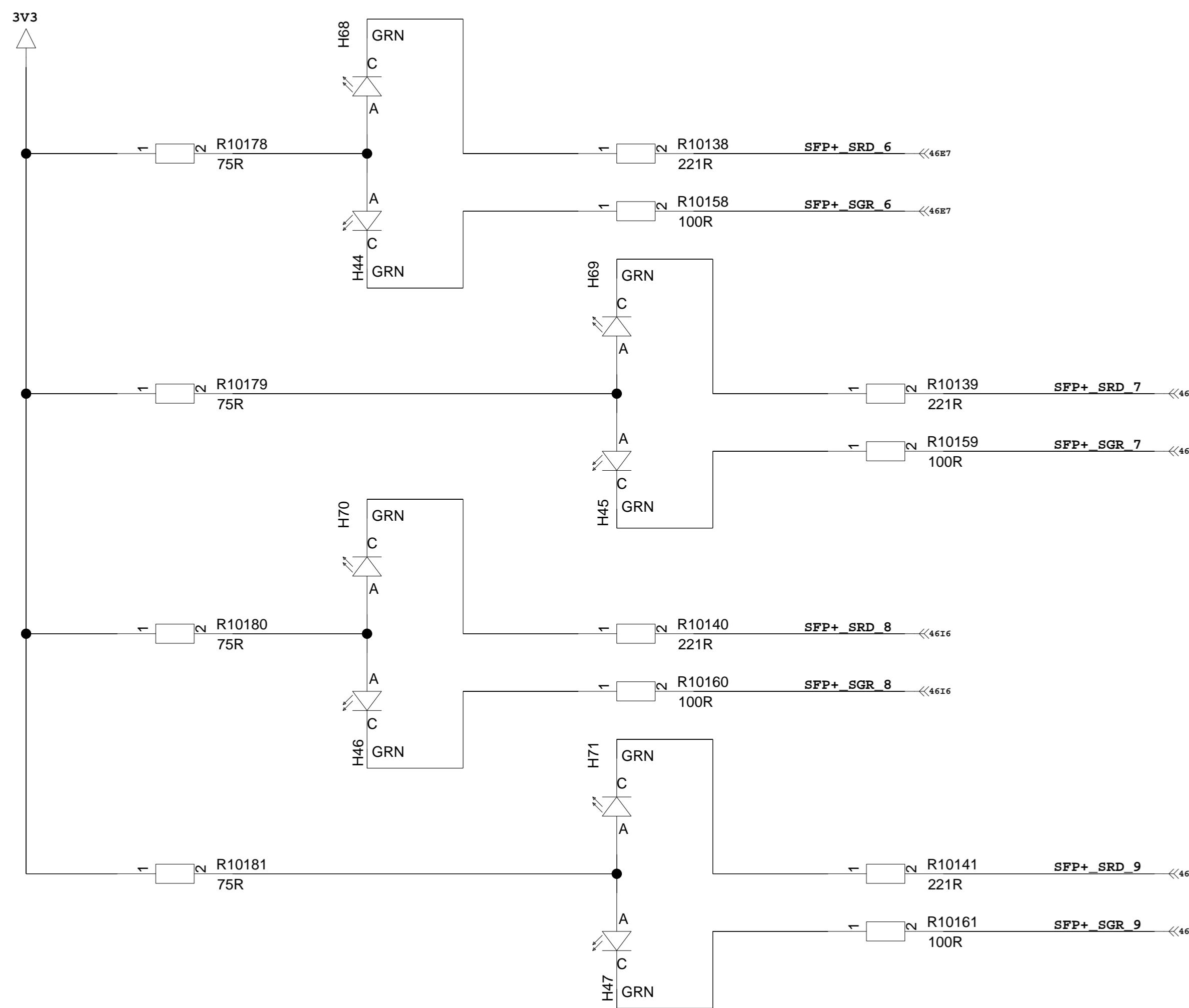
CONN MPN : FTSH-150-01-F-D

RJ45 CONNECTOR

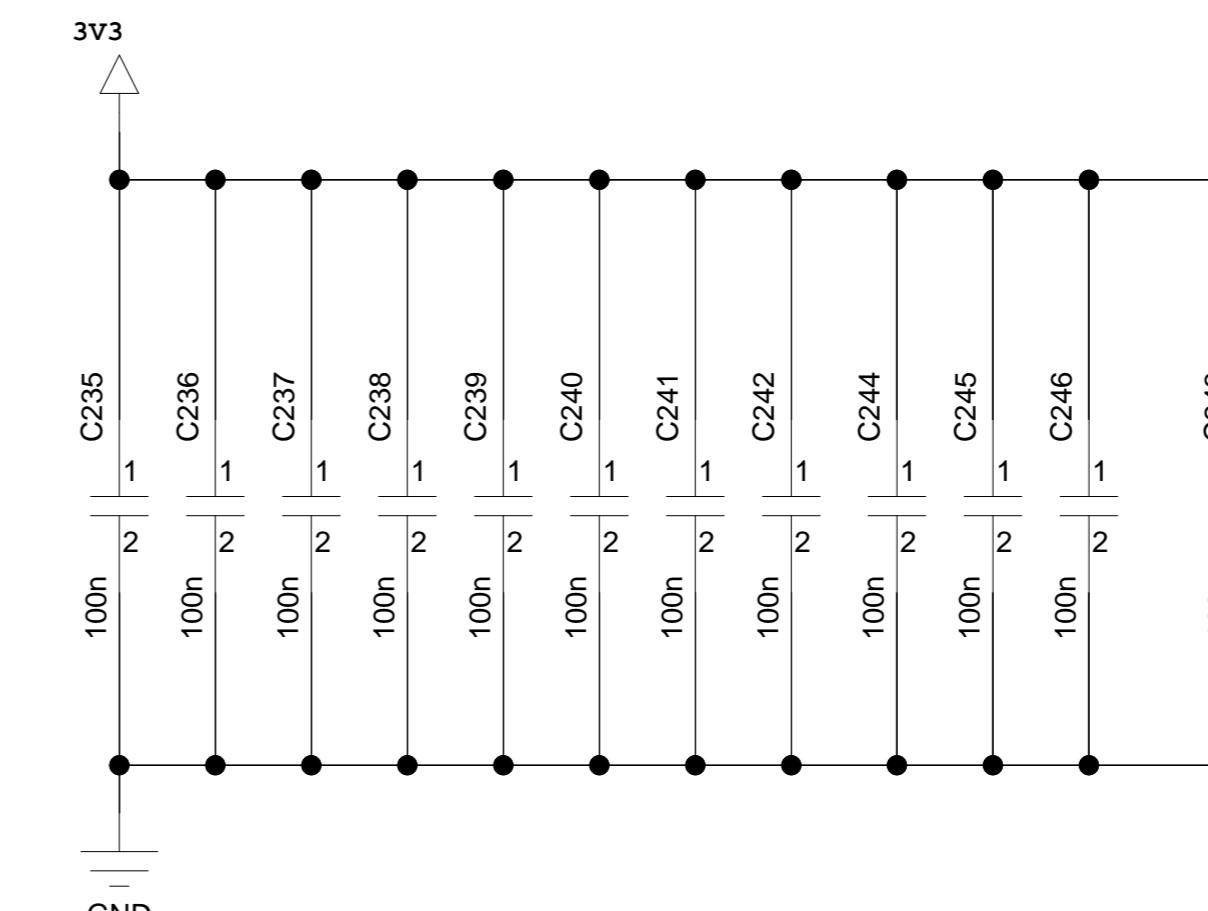
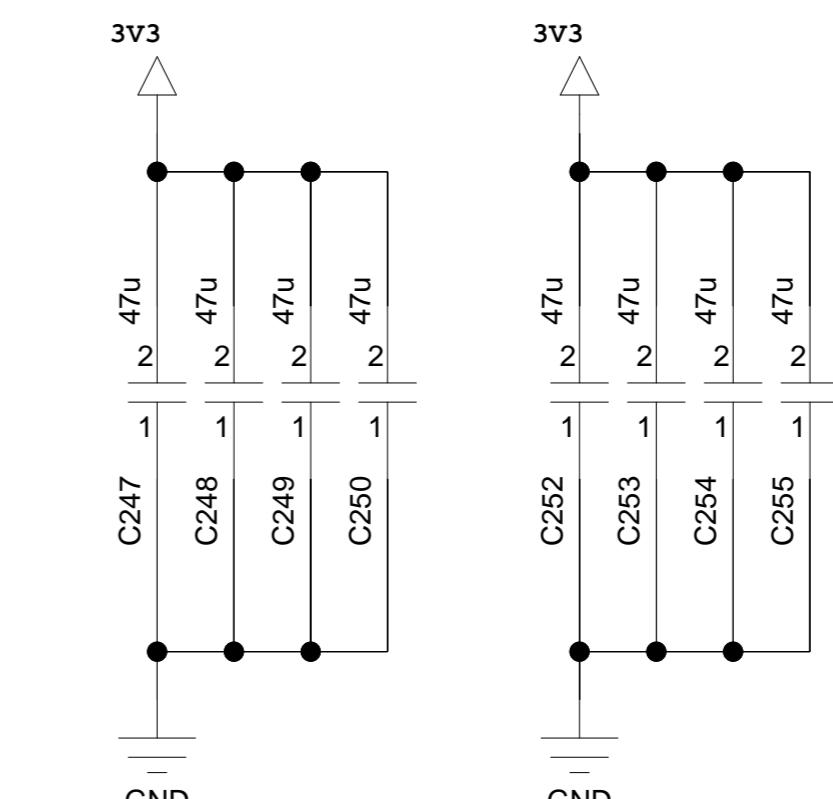


SFP+ LINK/PORT LEDS PART 2

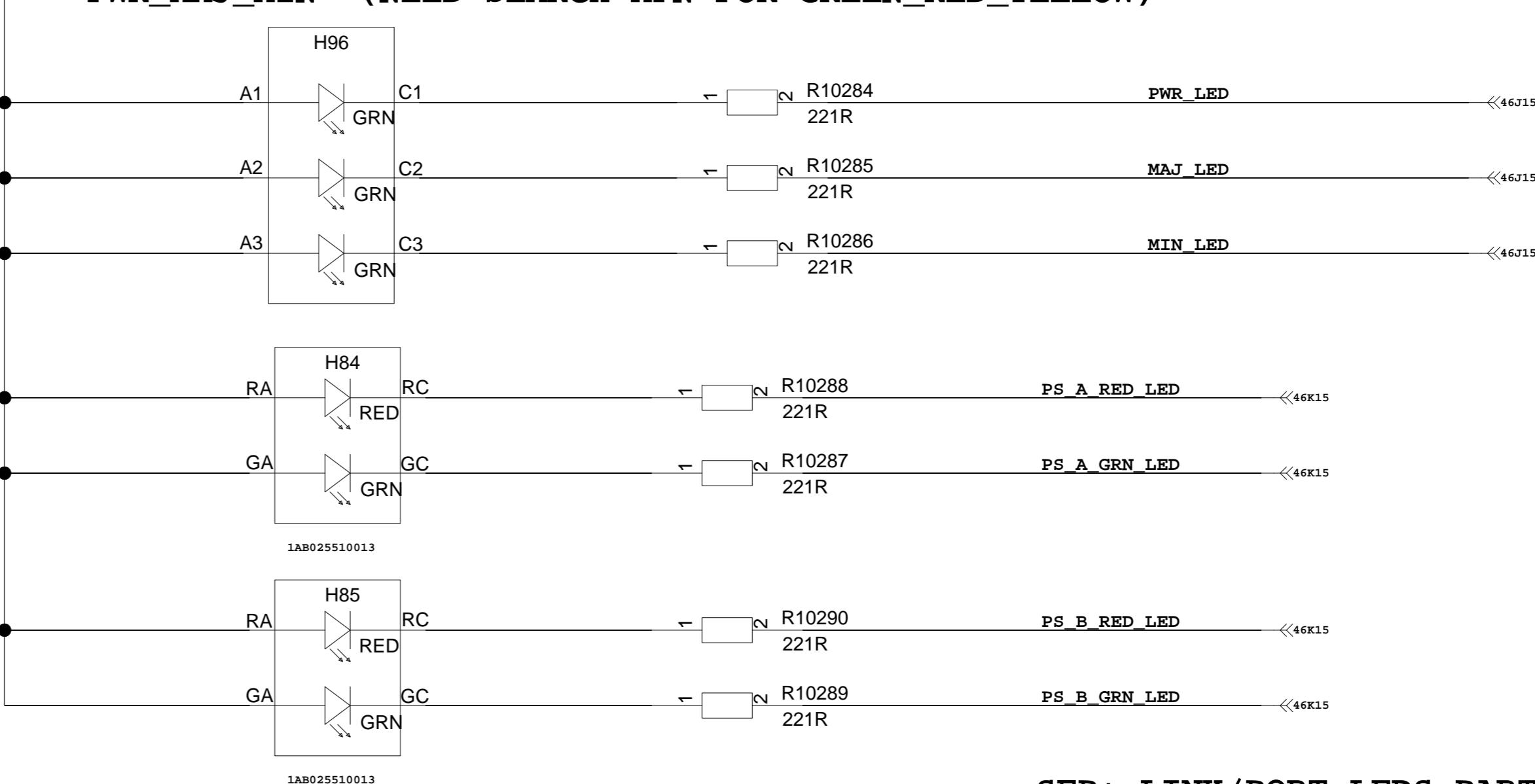
STATUS LEDS



CPU DECOUPLE CAPACITORS



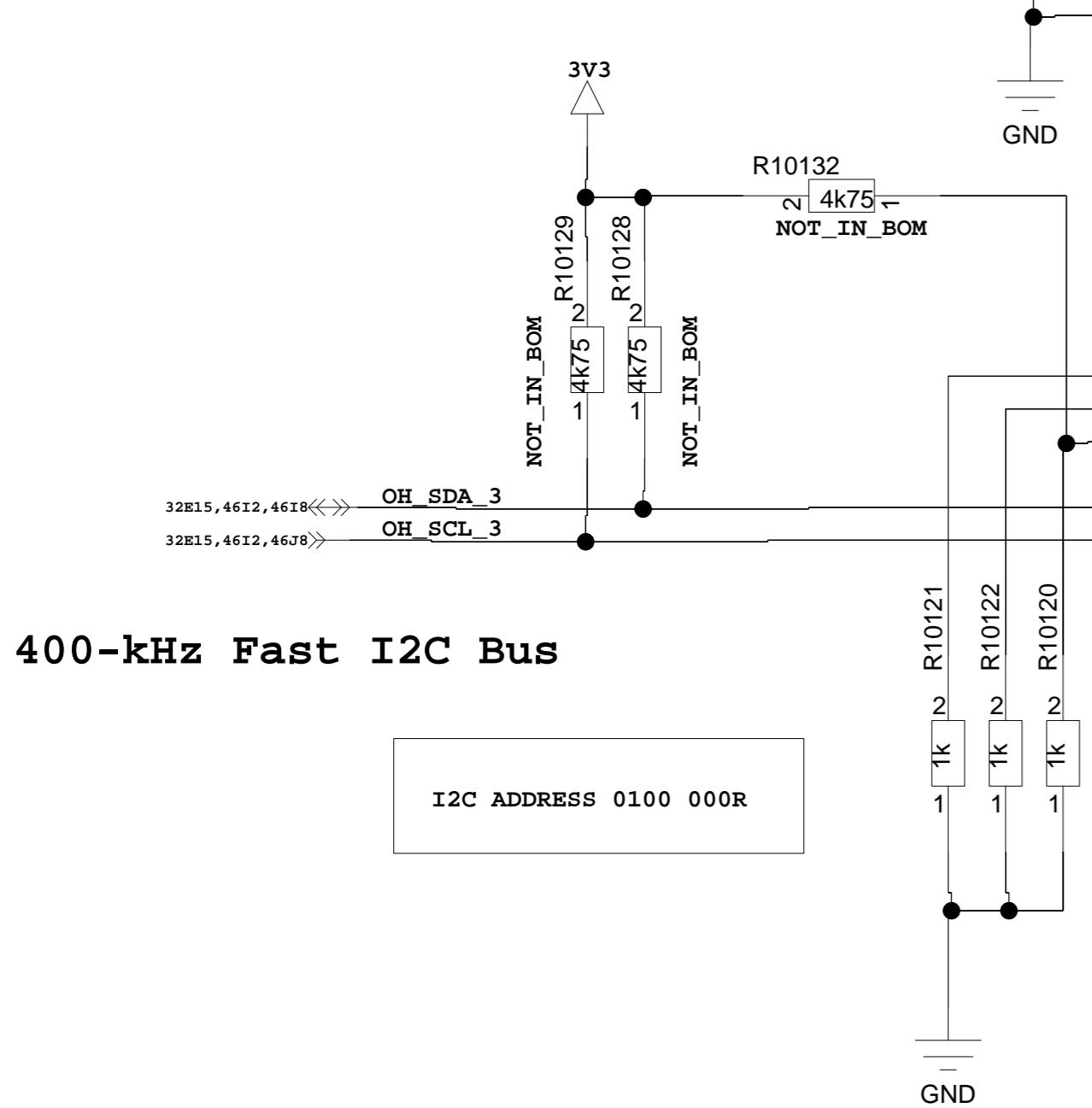
PWR_MAJ_MIN (NEED SEARCH MPN FOR GREEN_RED_YELLOW)



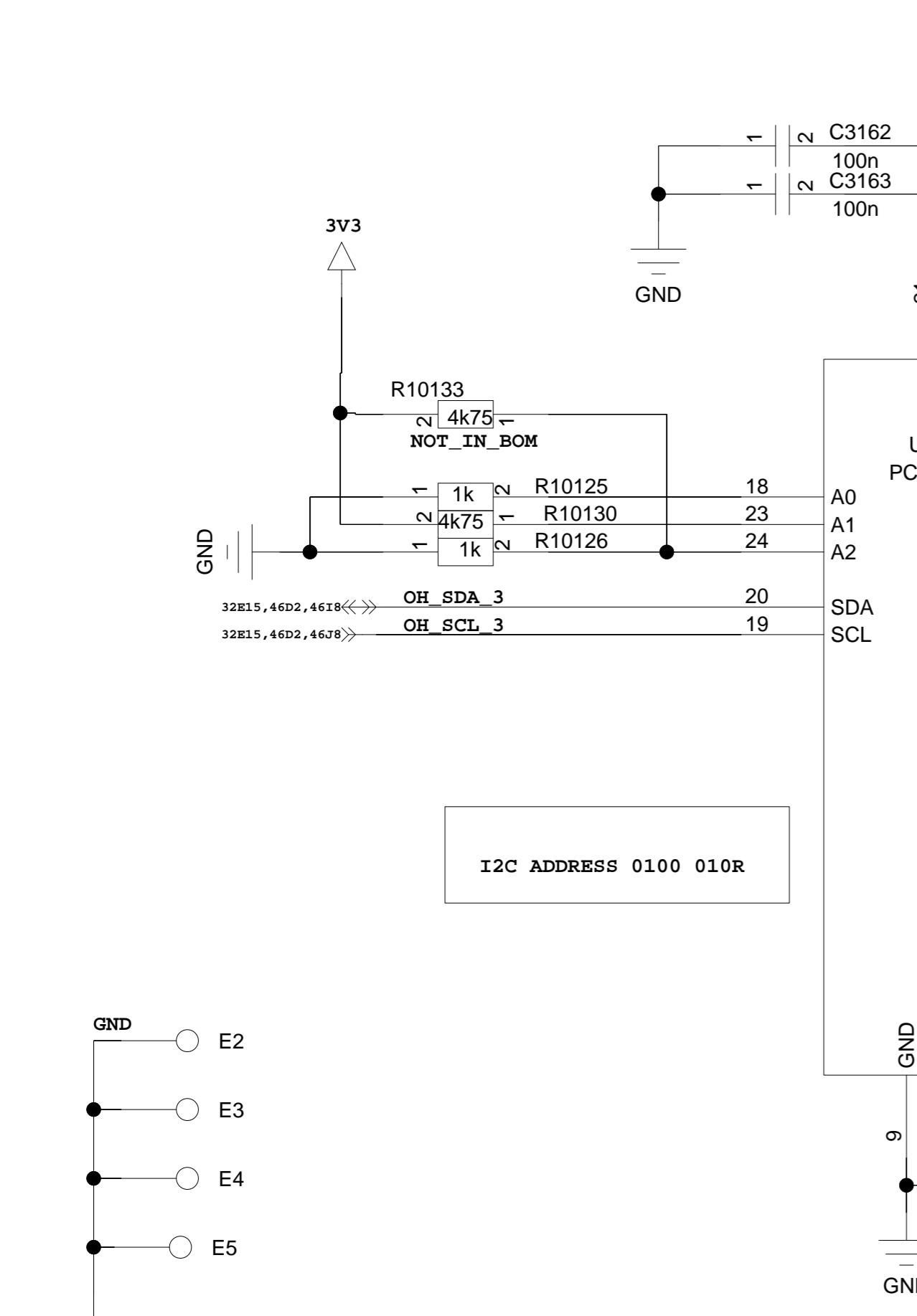
SFP+ LINK/PORT LEDS PART 2

ED	01			

I2C GPIO EXPANDERS

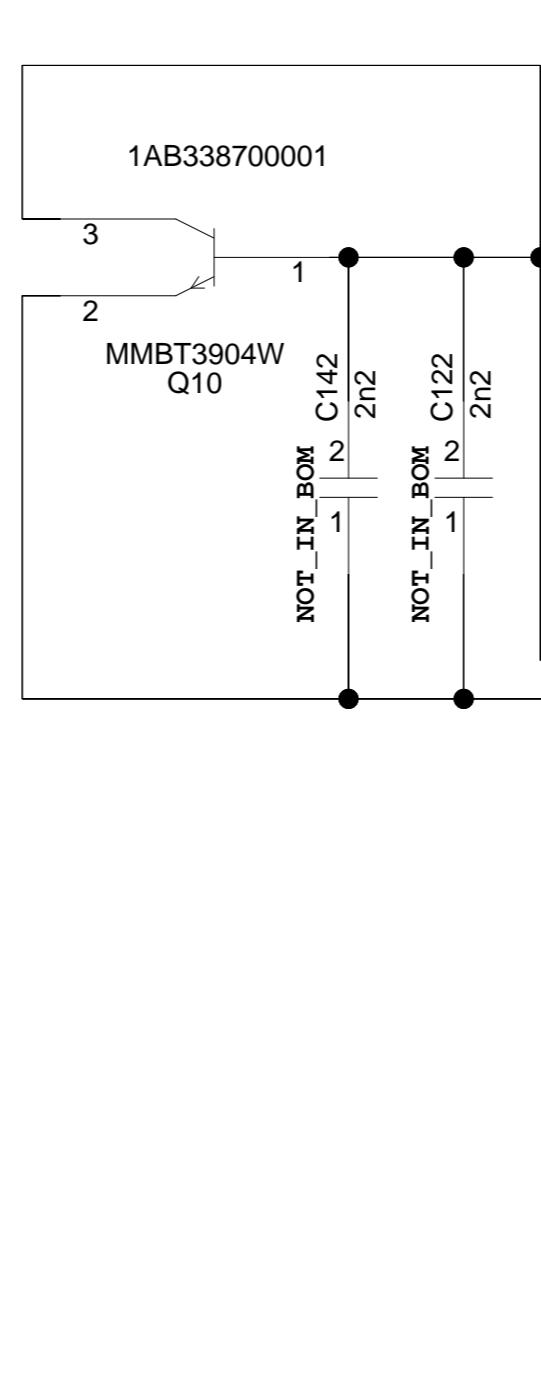


400-kHz Fast I2C Bus

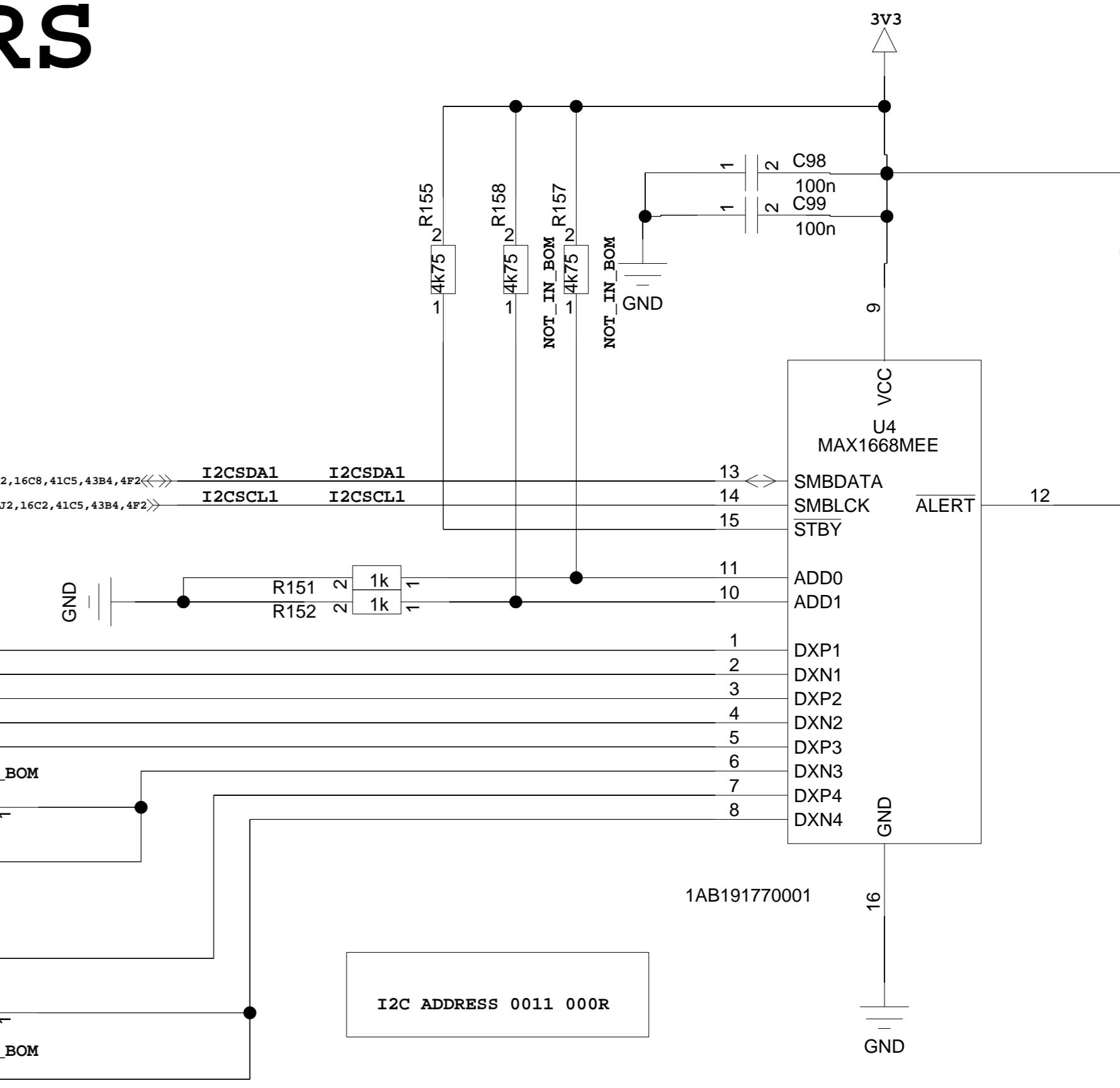
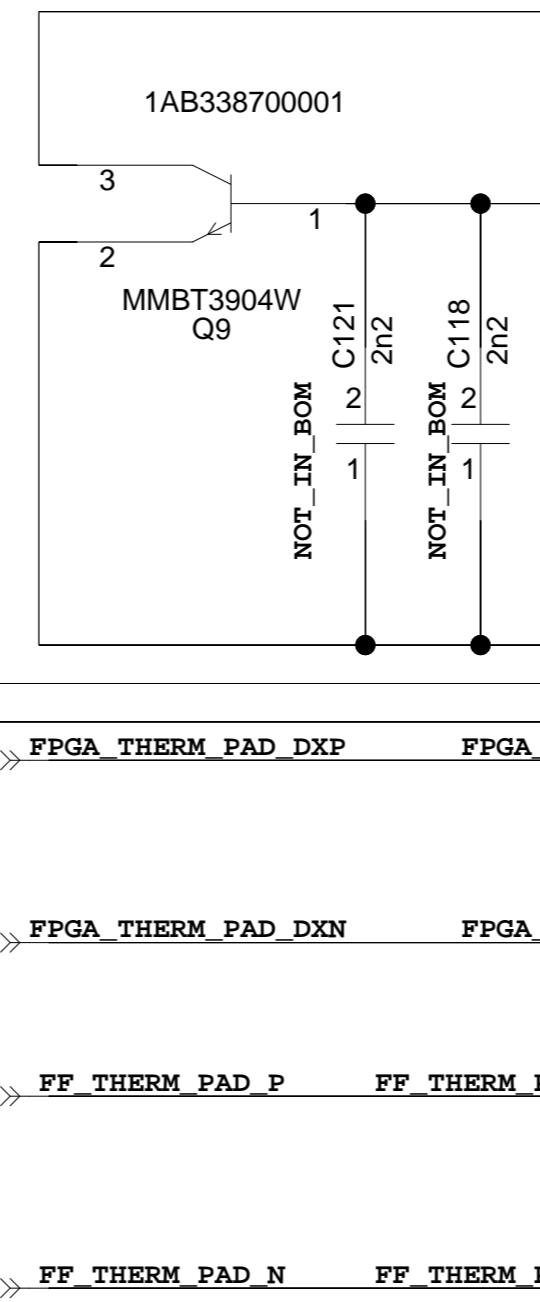


DEFUALT: OH_SCL_3 and OH_SDA_3 are CONNECTED WITH CPU
BACKUP: OH_SCL_3 and OH_SDA_3 are CONNECTED WITH FPGA

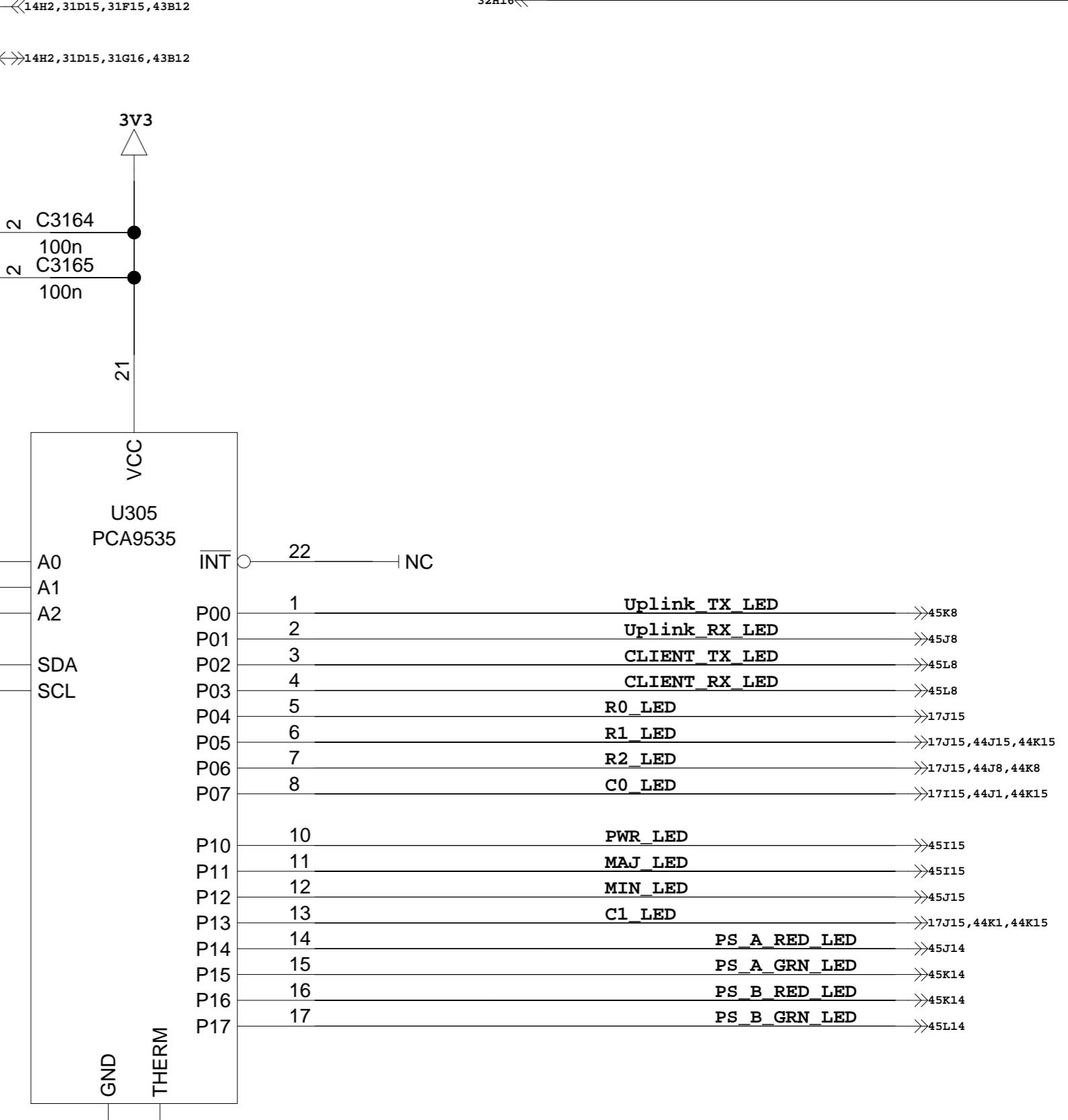
AIR IN



AIR OUT



32H16 <-- TEMP_ALERT_N TEMP_ALERT_N



I2C GPIO EXPANDERS

ED	01						
							46/46