

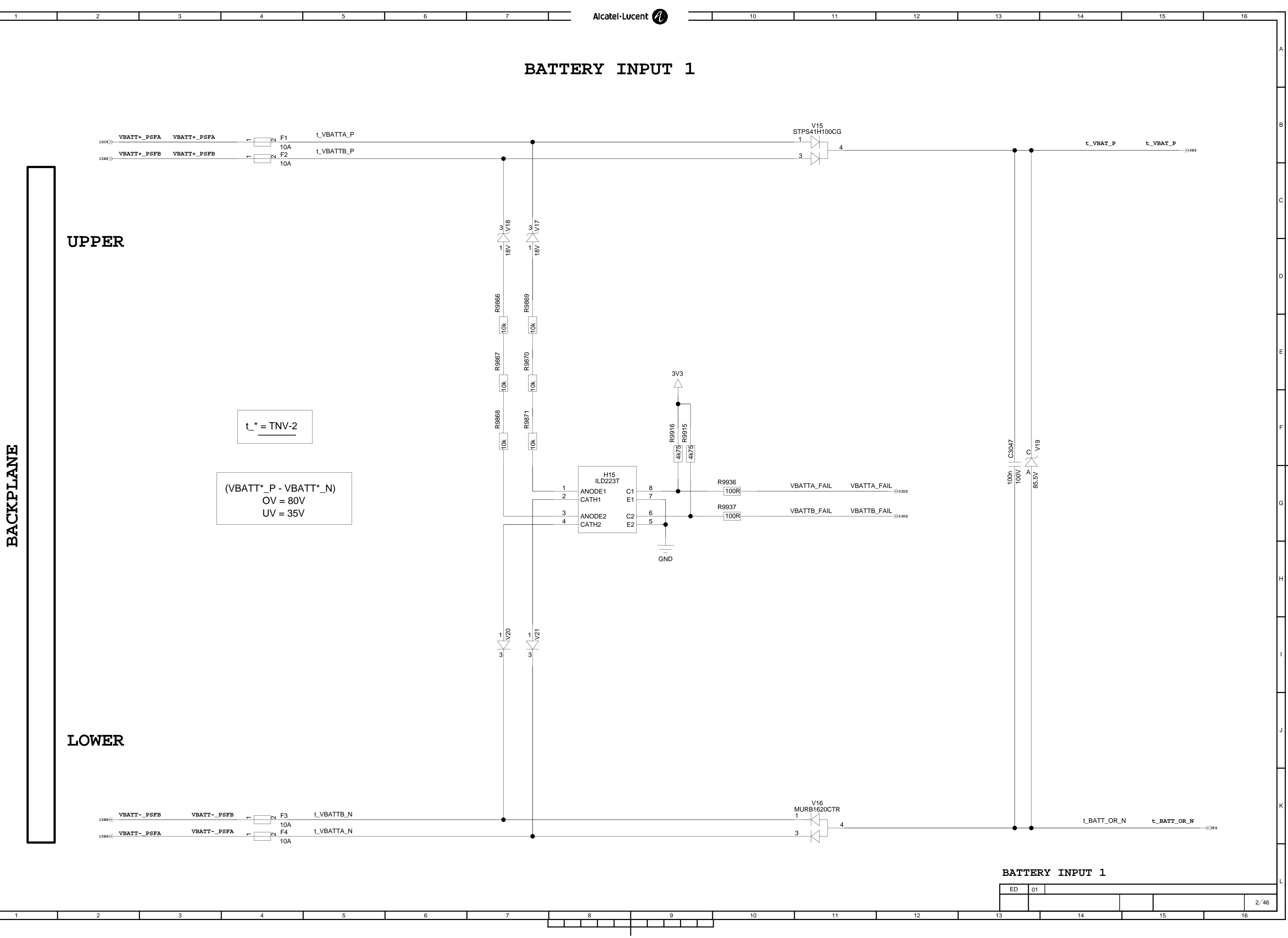
MXP-100G

SHEET	TITLE	SHEET	TITLE
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41	MATRIX IIC/JTAG/FILTER		
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43	MPC8308 CPU CONNECTOR		
44	RJ45 CONNECTOR		
45	SFP+ LINK/PORT LEDS PART 2		
46	I2C GPIO EXPANDERS		

20160610

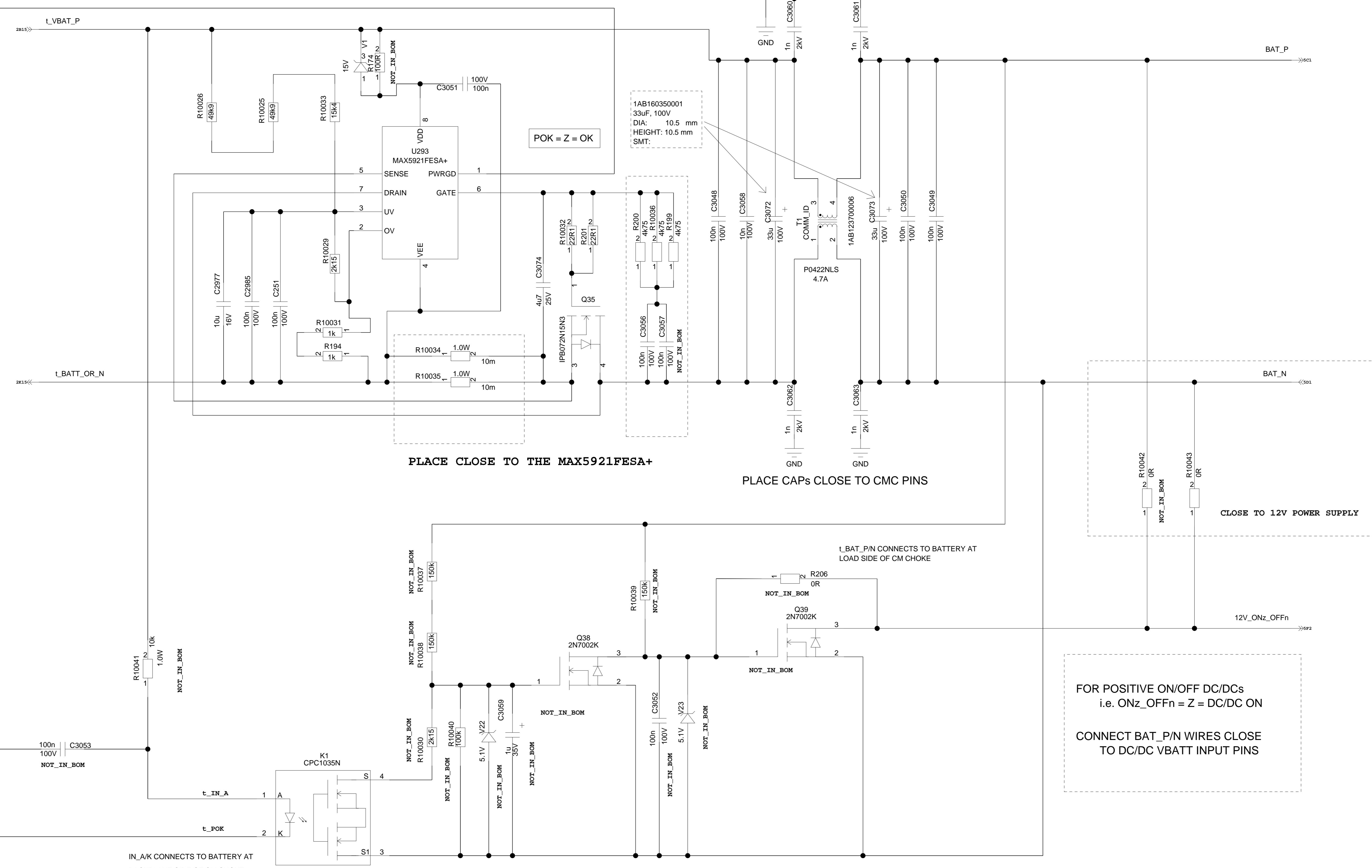
ED	DATE	01	20160101	1	01	1
CHANGE NOTE						
APPRO.AUTHO.						
ORIGINATOR						
MXP-100G						1/46

BATTERY INPUT 1



BATTERY INPUT 2

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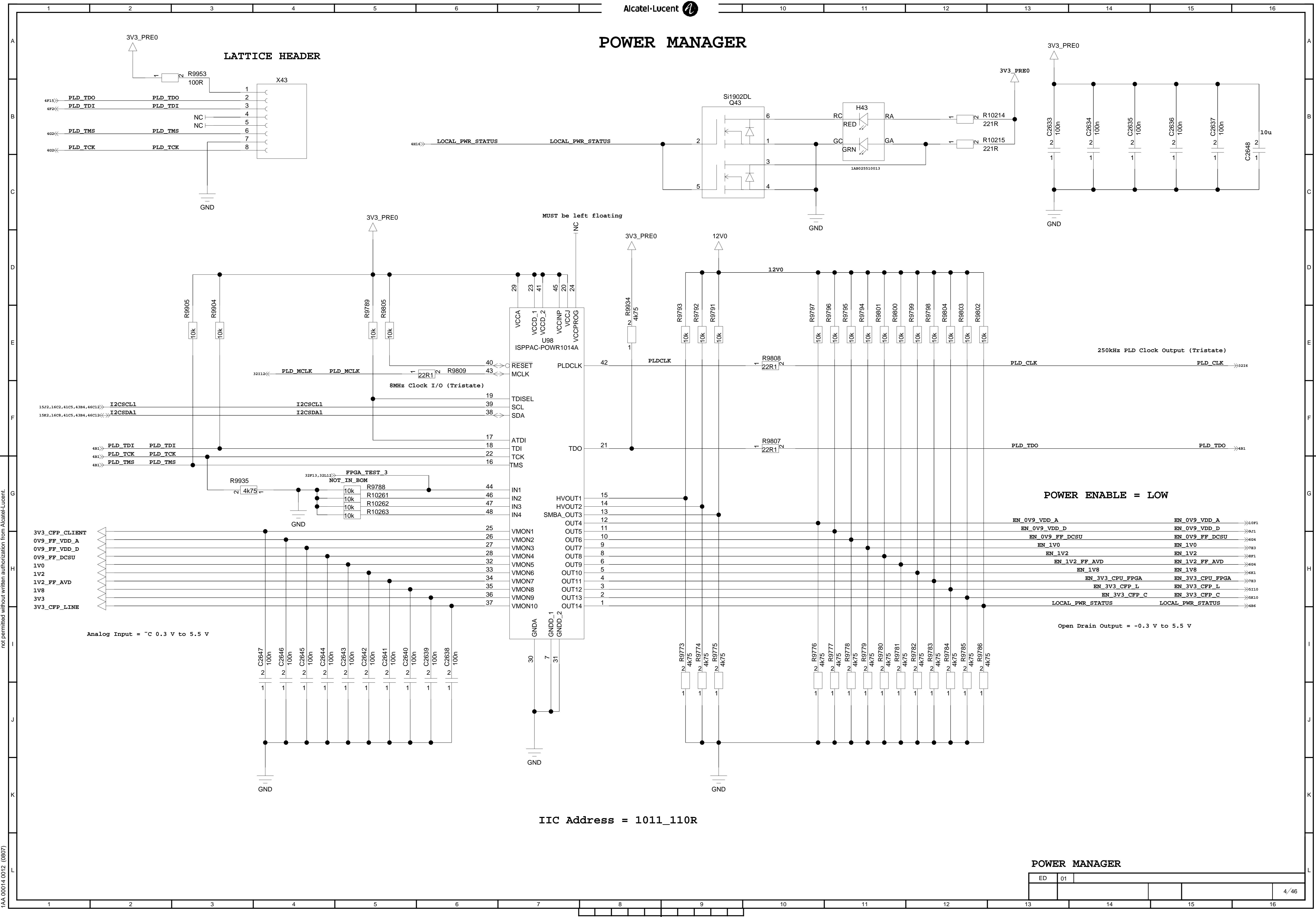


BATTERY INPUT 2

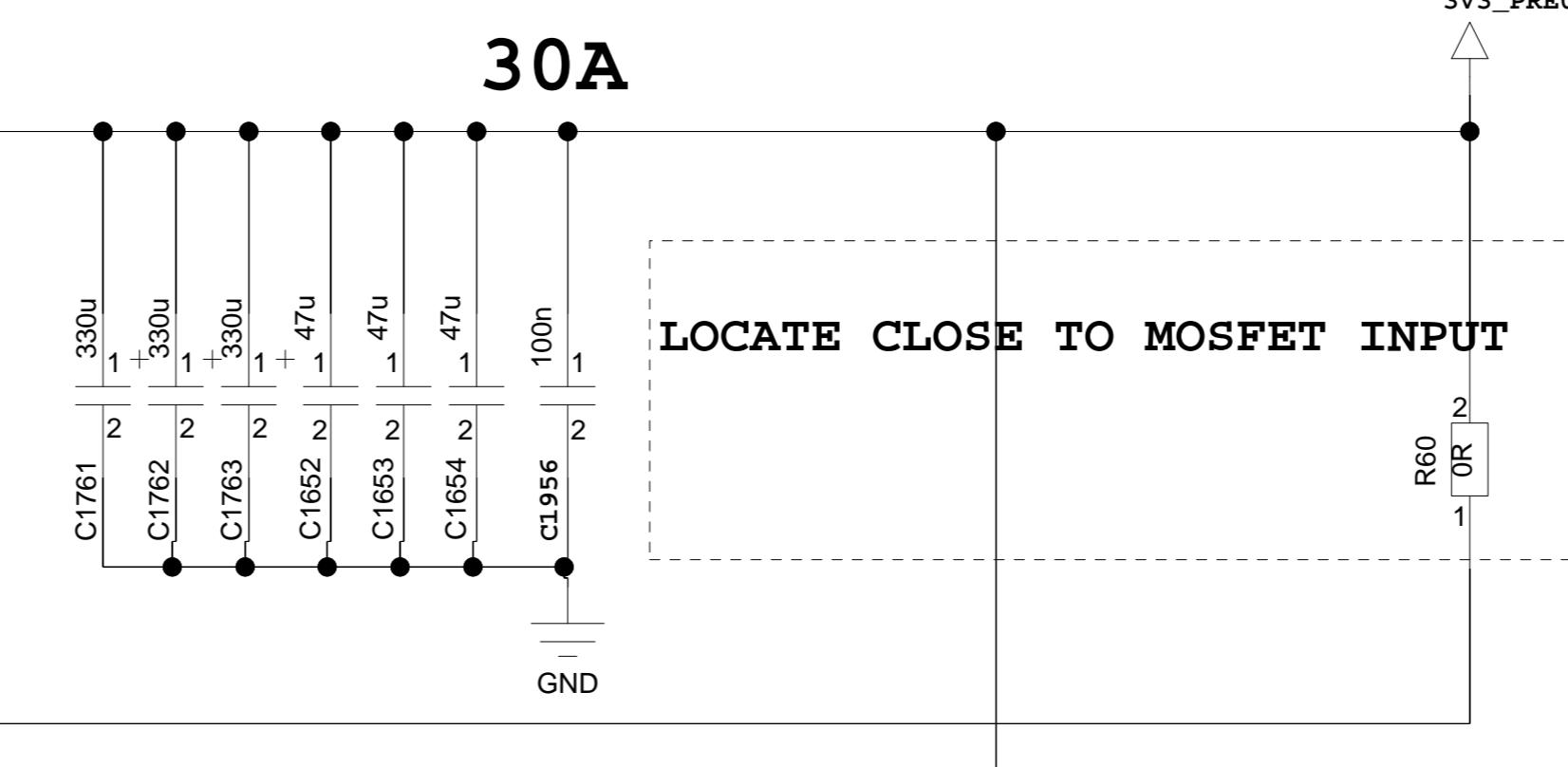
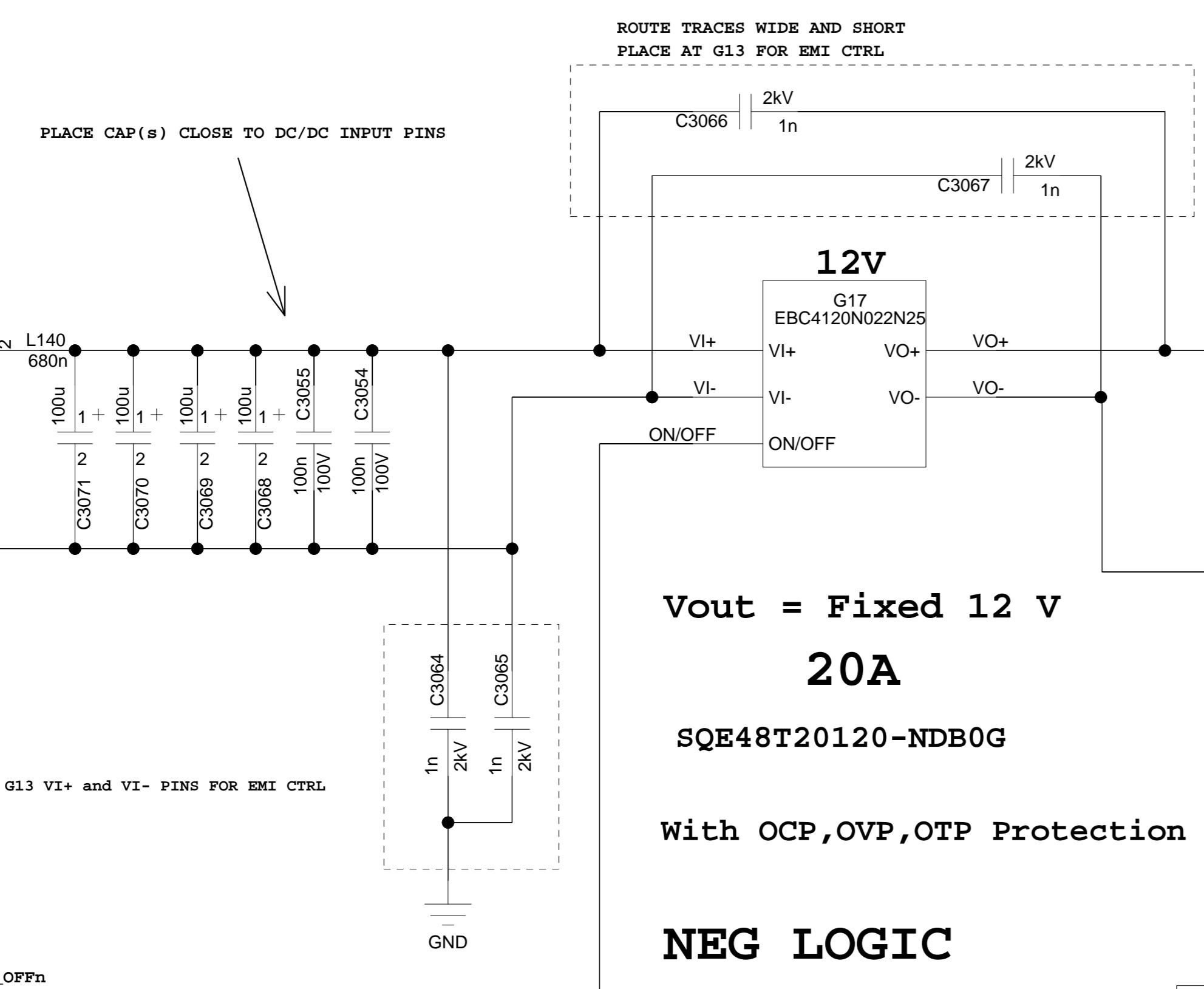
ED	01						
							3/46

POWER MANAGER

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PRIMARY POWER 12V0, 3V3



LOCATE CLOSE TO MODULE

Rtrim = 3.2 k VO = 3.3V

LOCATE CLOSE TO MODULE

With OCP, OTP Protection

NOT IN BOM

R1005
22k1R9960
1k

1

2

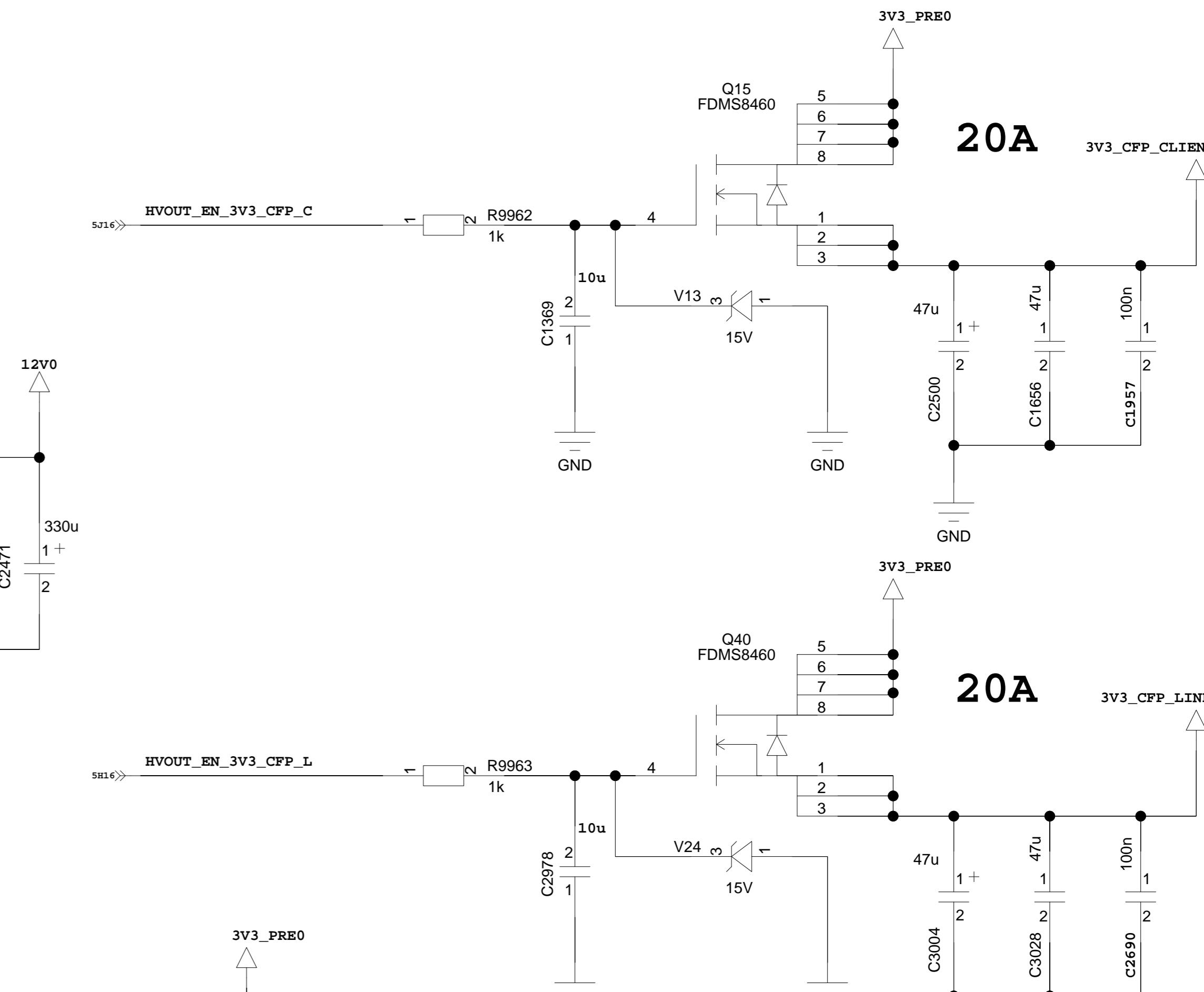
GND

Vout = 8000/R+0.8 = 3.467V

APTS030A0X3-SRPHZ

SLIN-30E1AL

1/AA 00014 0012 (0807)



PRIMARY POWER 12V0, 3V3

ED 01

5/46

POS LOGIC

PRIMARY POWER 1V8,1V2_FF,0V9_DCSU

LOCATE CLOSE TO MODULE

$$V_{out} = (1184/R) + 0.592 = 1.814V$$

With OCP,OTP Protection

EN_1V2_FF_AVD (4H16) → R9980 (1k) → Pin 2 → Pin 6 (via R9982, 1k)

EN_0V9_FF_DCSU (4H16) → R9981 (1k) → Pin 2 → Pin 6 (via R9983, 1k)

Pin 1 → GND

Pin 3 → GND

Pin 4 → GND

Pin 5 → Pin 6 (via R9982, 1k)

Pin 6 → GND (via R9983, 1k)

Si1902DL Q37

POS LOGIC

U291 MAX8556

1V8_PRE

1V2_FF_AVD

1V2_FF_AVD_POK

34G5

Vout = 0.5 * (1 + R2/R3) = 1.2V

$$V_{out} = 0.5 * (1 + R2/R3) = 1.2V$$

POSITIVE LOGIC

MAX8556 (U296) Pinout and Components:

- Pin 1: IN1
- Pin 2: IN2
- Pin 3: IN3
- Pin 4: IN4
- Pin 5: IN5
- Pin 6: IN6
- Pin 7: OUT1
- Pin 8: OUT2
- Pin 9: OUT3
- Pin 10: OUT4
- Pin 11: OUT5
- Pin 12: POK
- Pin 13: FB
- Pin 14: GND
- Pin 17: THERM
- NC=15

Capacitors and Components:

- 47uF capacitor C3013 connected between Pin 12 and ground.
- 10uF capacitor C3020 connected between Pin 13 and ground.
- 10nF capacitor C3002 connected between Pin 13 and ground.
- 10uF capacitor C3021 connected between Pin 14 and ground.
- 10nF capacitor C3002 connected between Pin 17 and ground.
- 0V9_FF_DCSU_POK bus connected to Pin 12, Pin 13, Pin 14, and Pin 17.
- 0V9_FF_DCSU_POK bus connected to Pin 13 and Pin 17.
- 34F5 component connected to Pin 13 and Pin 17.

$$V_{out} = 0.5 * (1 + R2/R3)$$

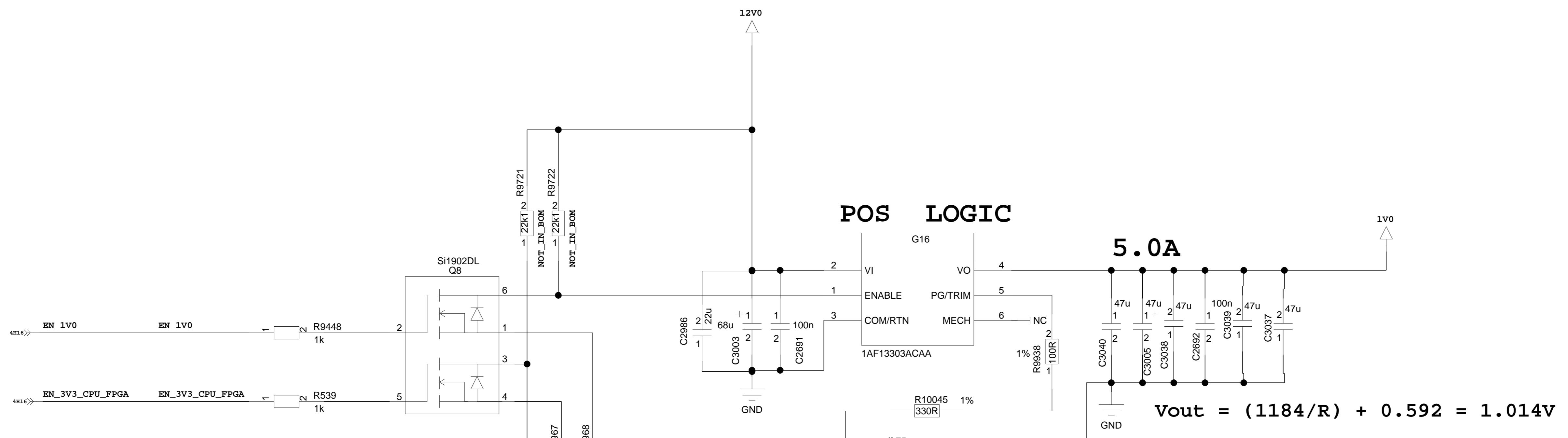
SET ≡ LOW ≡ Core SLOW v ≡ 0.925V

SET ≡ HIGH ≡ Core FAST v ≡ 0.875V

CLOSE TO U296

CLOSE TO U296

PRIMARY POWER 1V0, 3V3

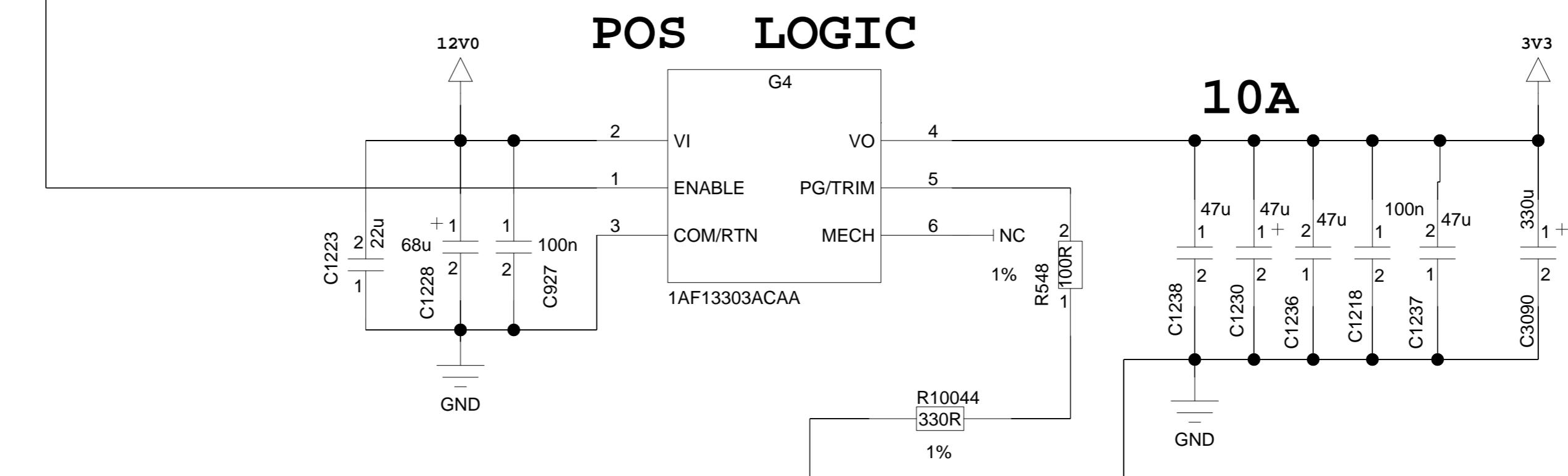


5.0A

$$V_{out} = (1184/R) + 0.592 = 1.014V$$

With OCP,OTP Protection

POS LOGIC



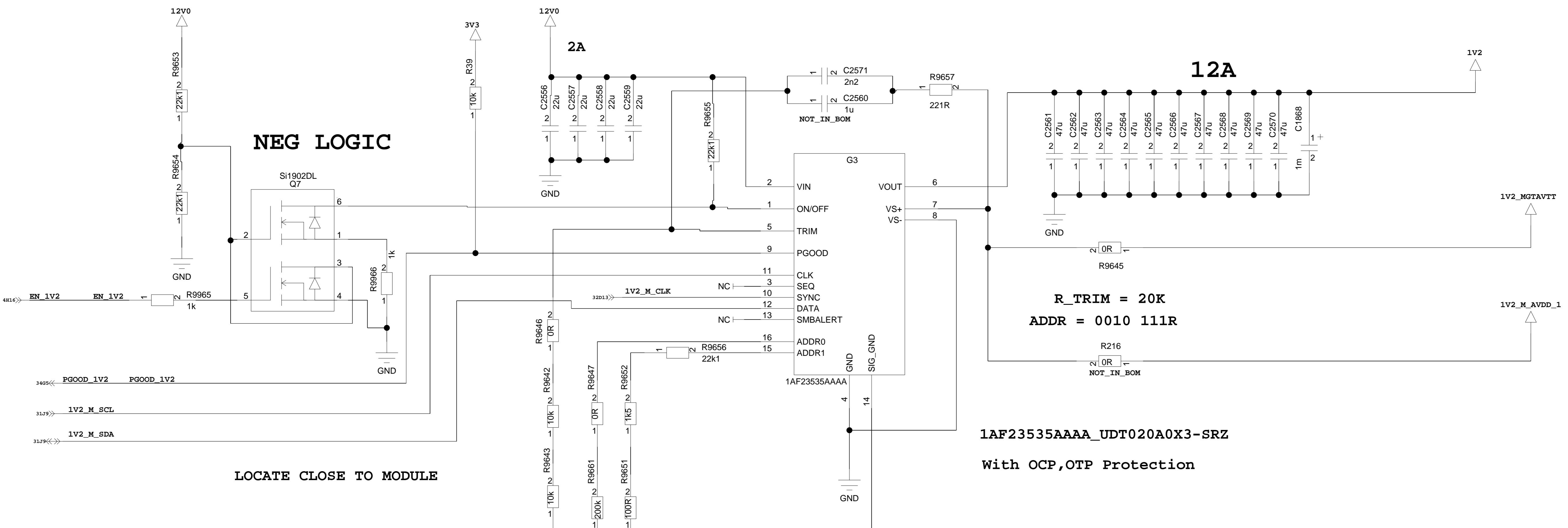
LOCATE CLOSE TO MODULE
With OCP,OTP Protection

$$V_{out} = (1184/R) + 0.592 = 3.345V$$

PRIMARY POWER 1V0,3V3

ED	01				7/46
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PRIMARY POWER 1V2



FLEXFRAMER POWER SUPPLY 1

Sense Path if FF is not assembled

GND

NEARLY
CLOSE TO MODULE

HIGH = GOOD

SET = LOW = Core SLOW V = 0.925V
SET = HIGH = Core FAST V = 0.875V

FLEXFRAMER POWER SUPPLY 1

ED 01

With OCP,OTP Protection
MDT040A0X3-SRPHZ SYNC Min 510k, typ k, 720k
SLDN-40E1AL SYNC Min 320k, typ k, Max 480k

NEG LOGIC

ADDR = 0010 000R

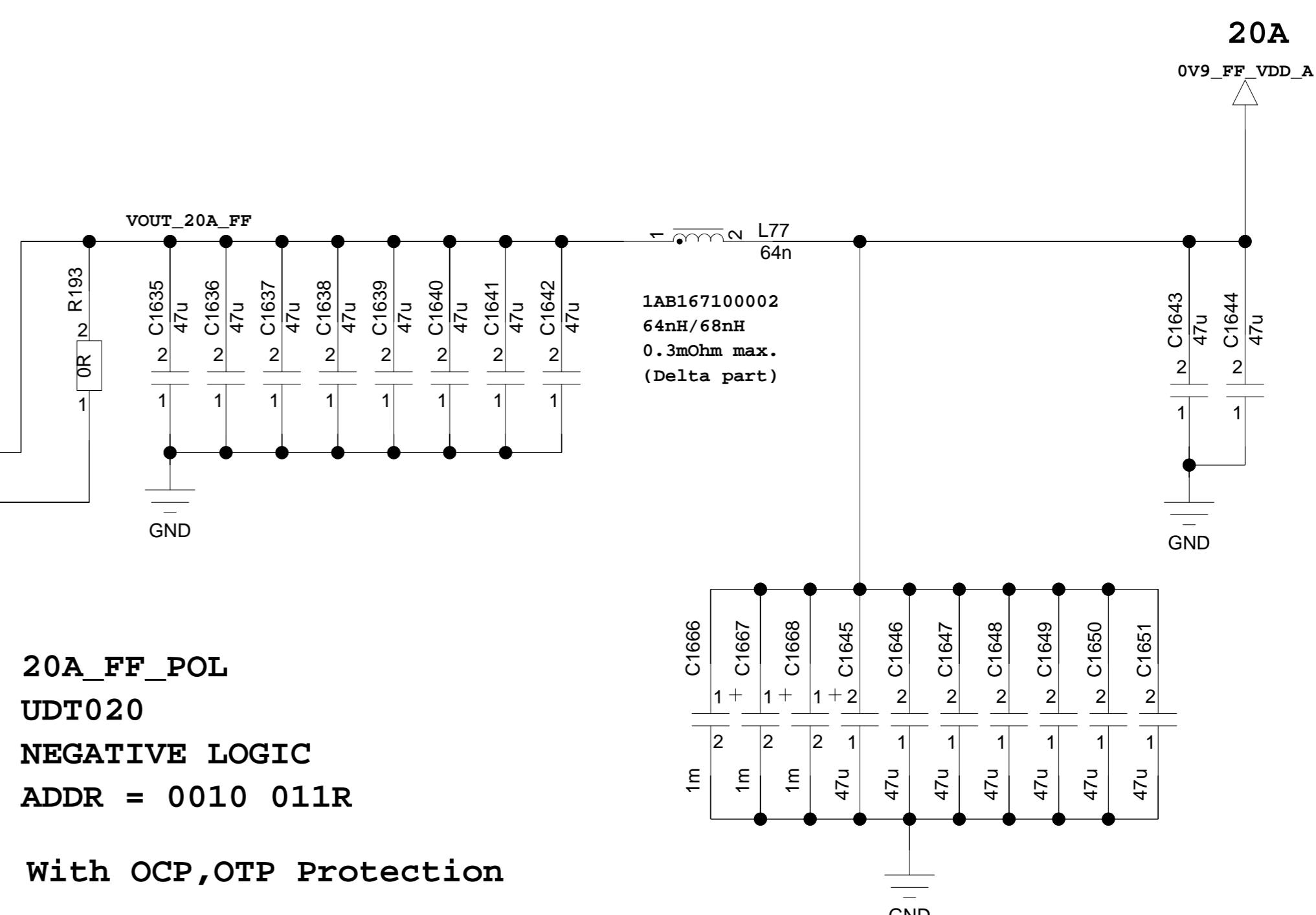
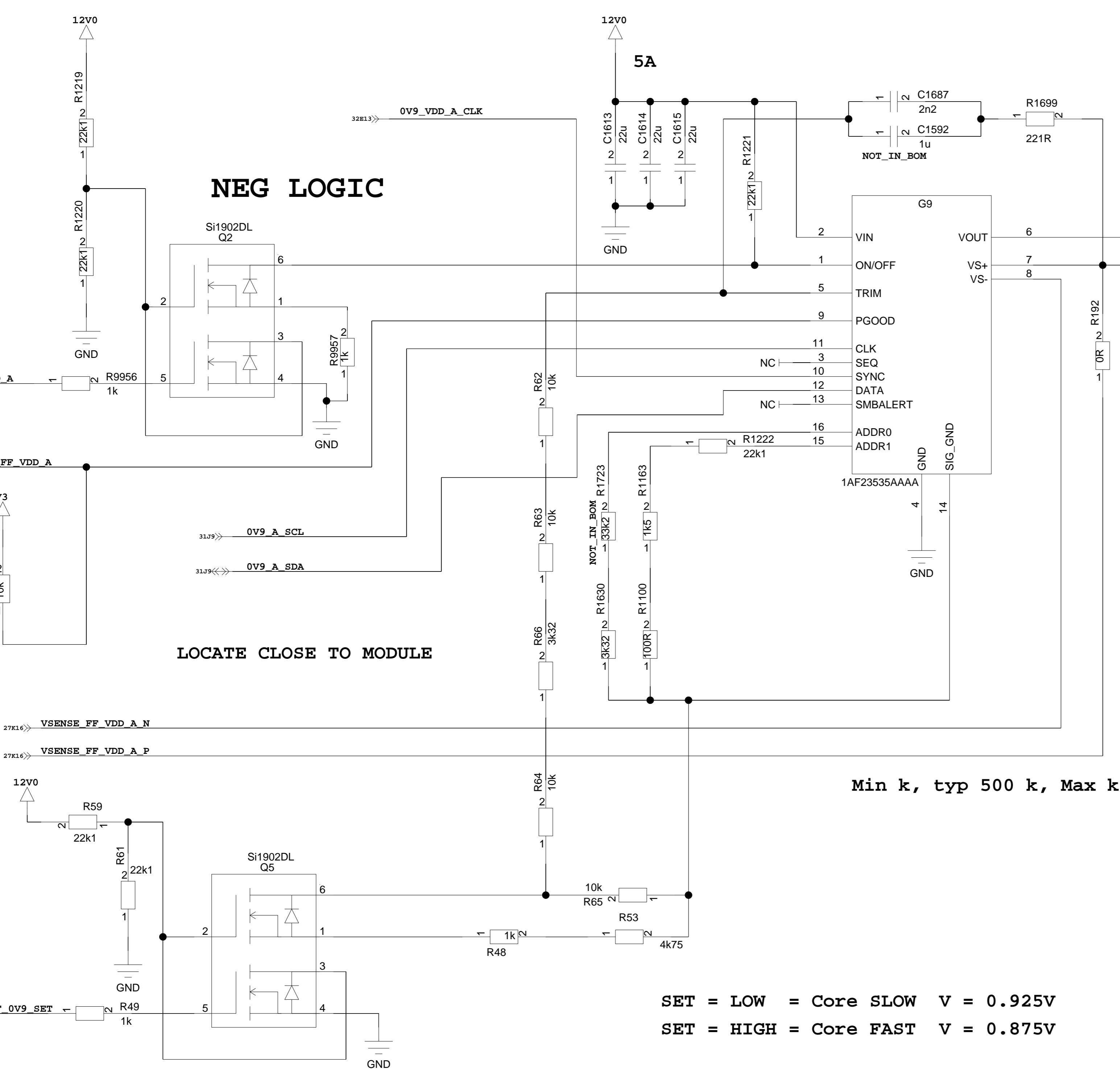
LOCATE CLOSE TO MODULE

HIGH = GOOD

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111 00011 0012 (0802)

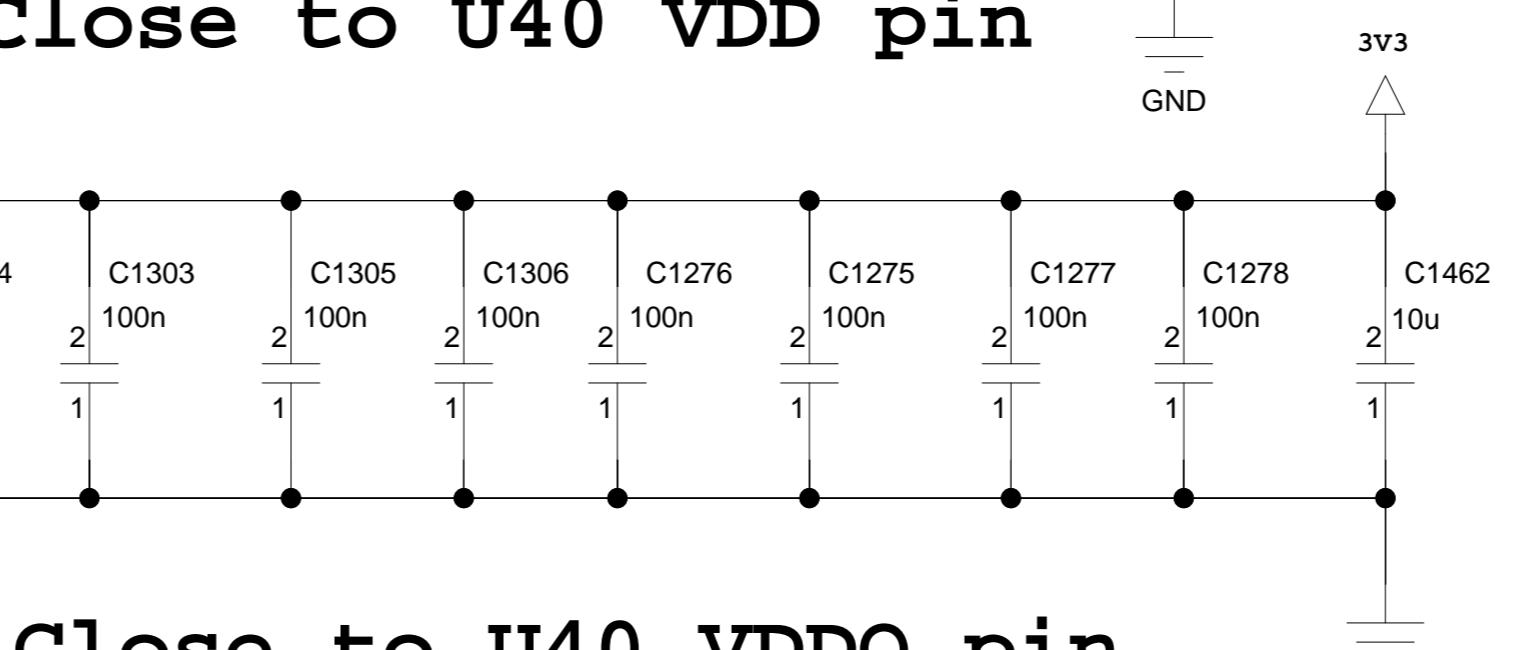
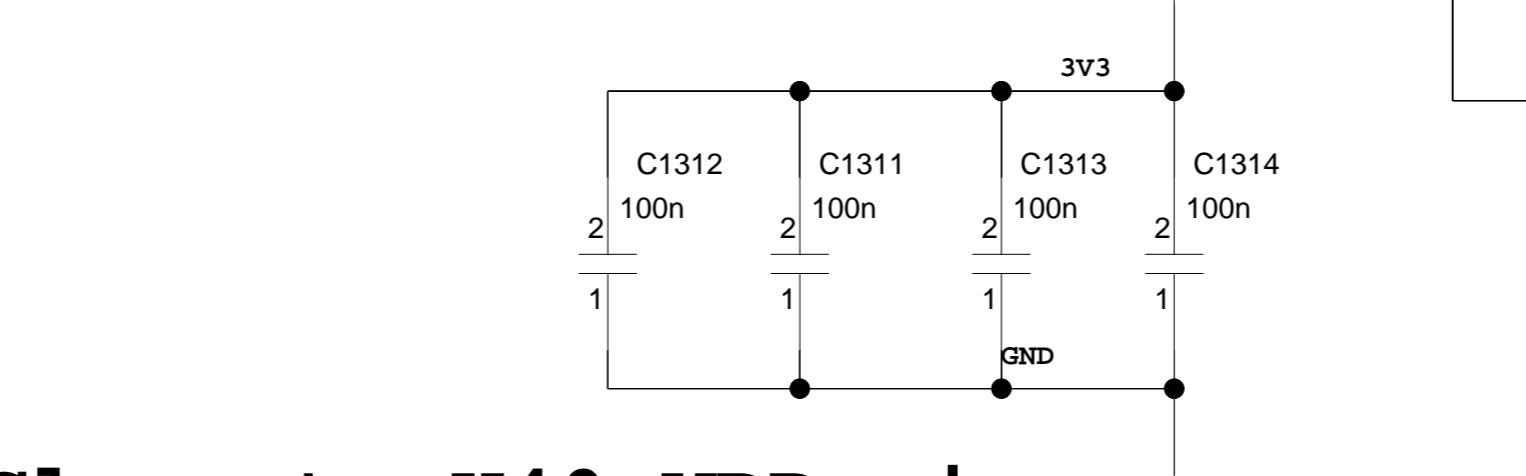
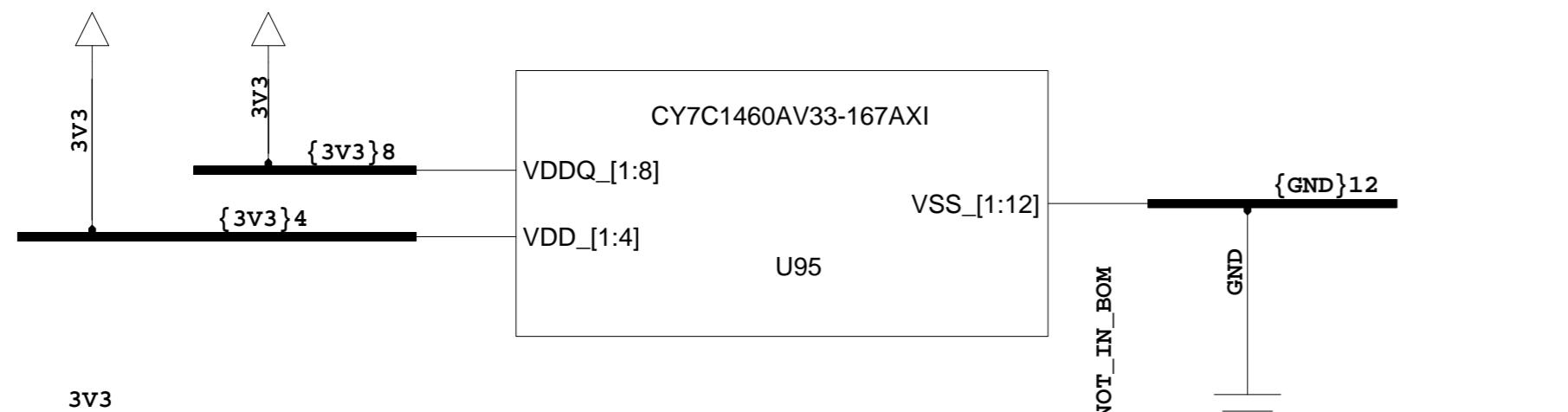
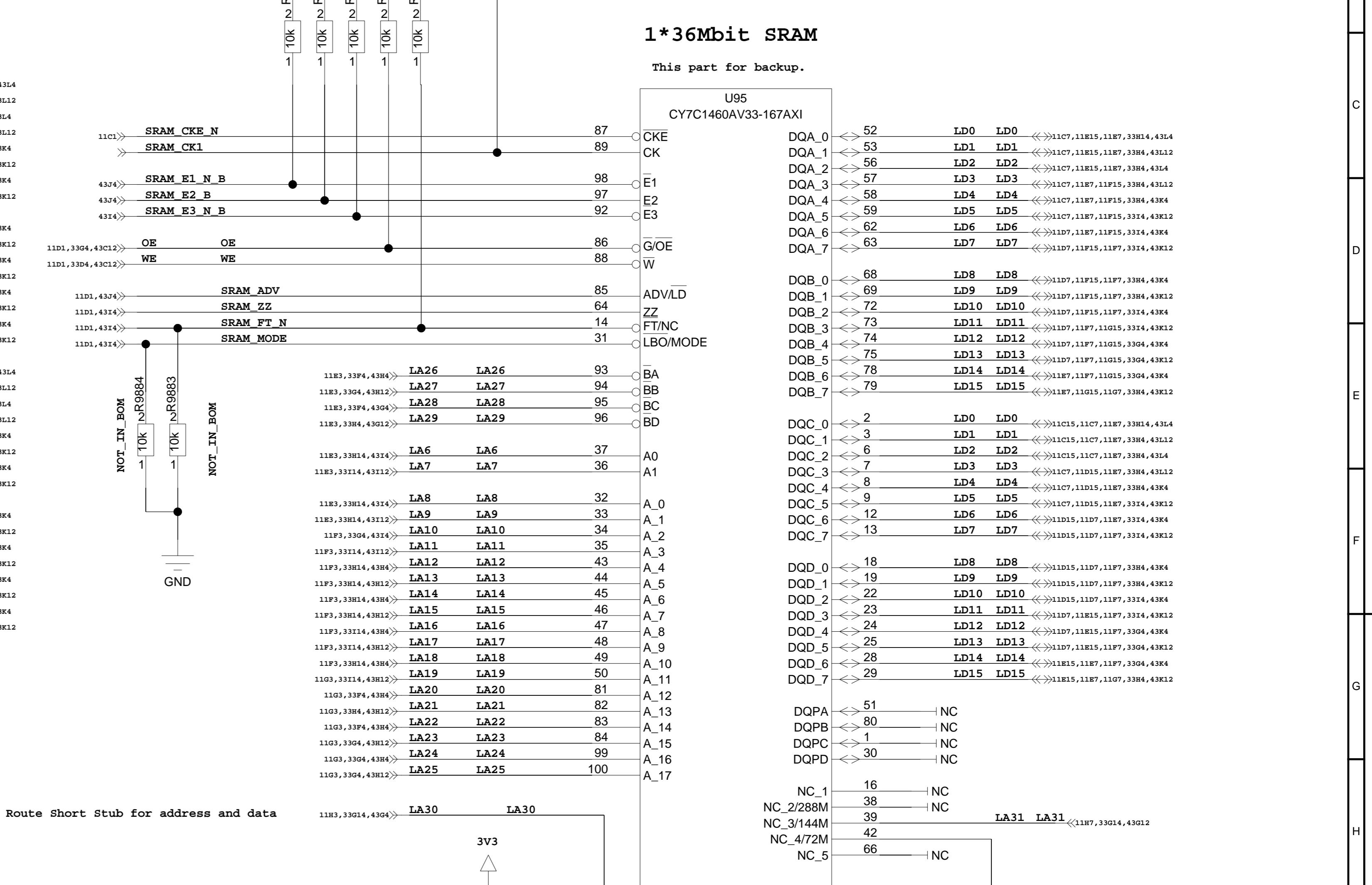
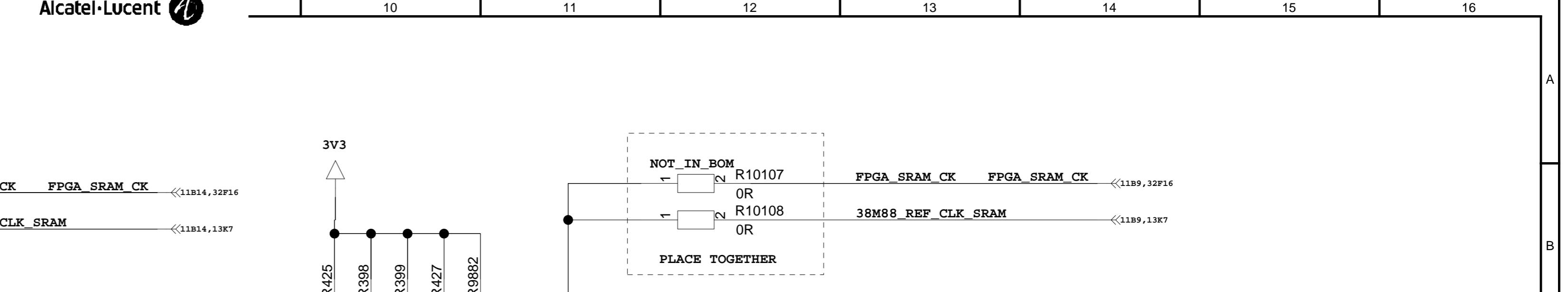
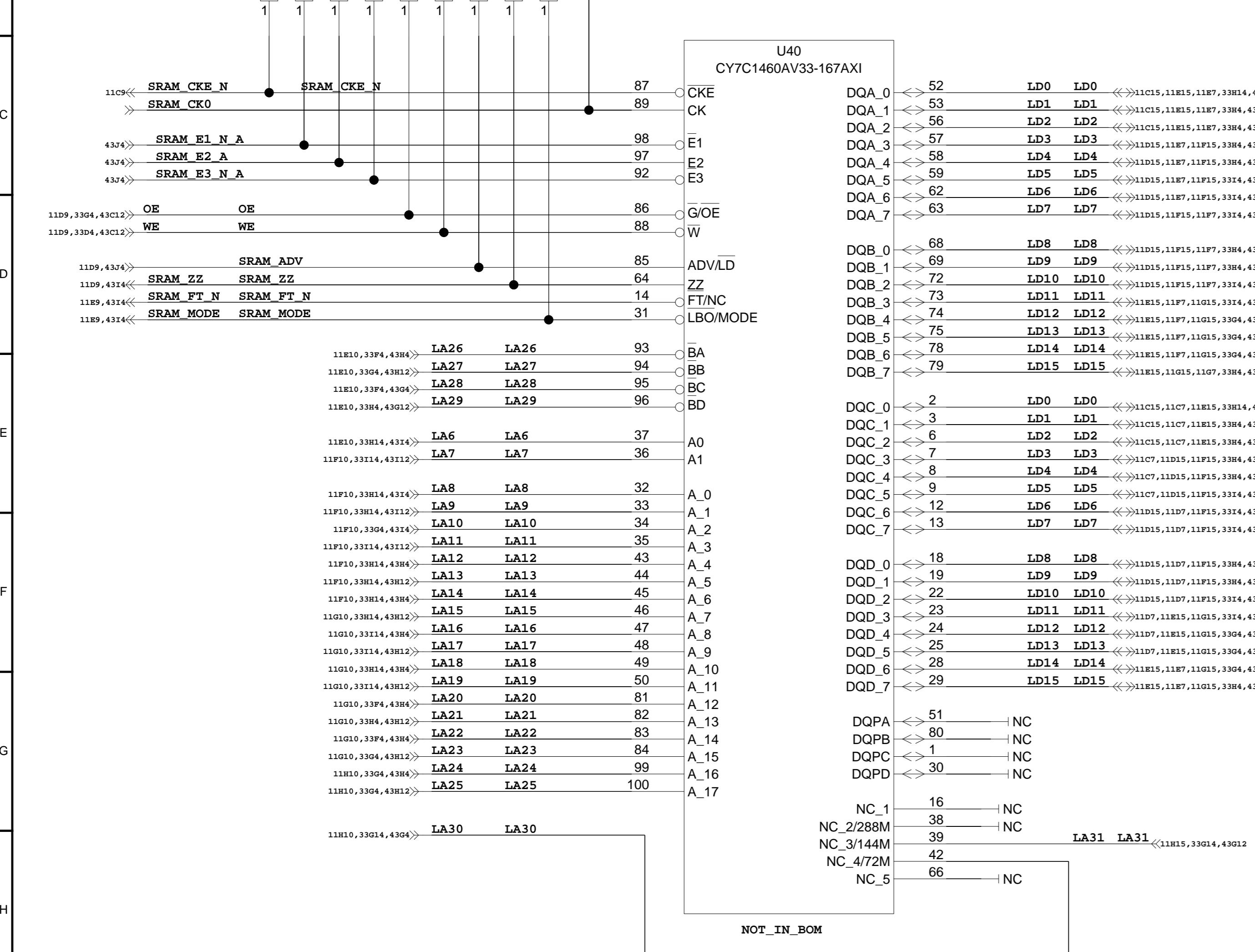
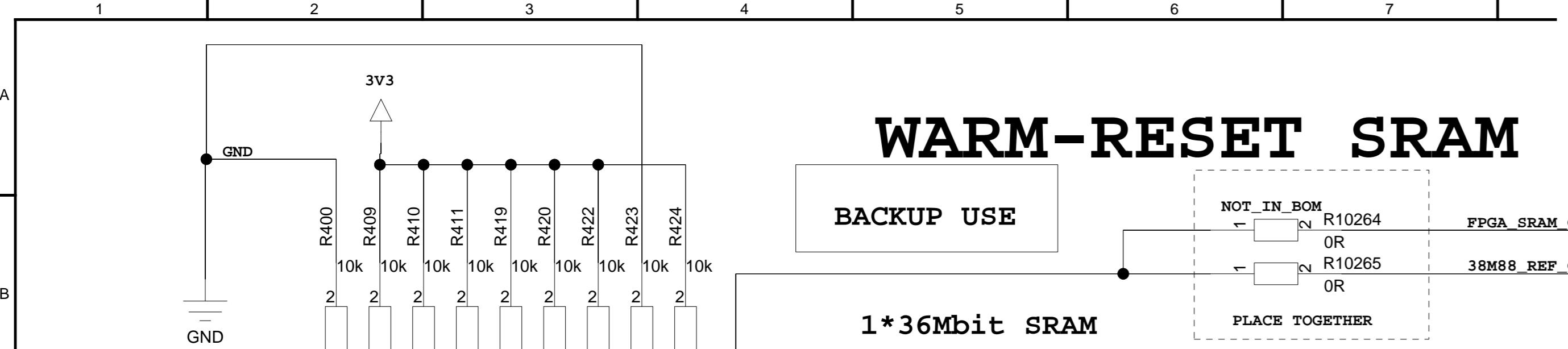
FLEXFRAMER POWER SUPPLY 2



NOTE for G9 (UDT020):

Sensitive, high-impedance, analog pins
 TRIM and SIG_GND on the one hand side
 and digital traces CLK, DATA and SMBALERT
 on the other hand side, have to be separated
 as good/far as possible in the layout!

R1723 IS JUST FOR IIC TEST USAGE



Close to U40 VDDQ pin

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U95

NOT_IN_BOM

GND

3V3

{3V3}8

{3V3}4

VDDQ_[1:8] VSS_[1:12]

U40

NOT_IN_BOM

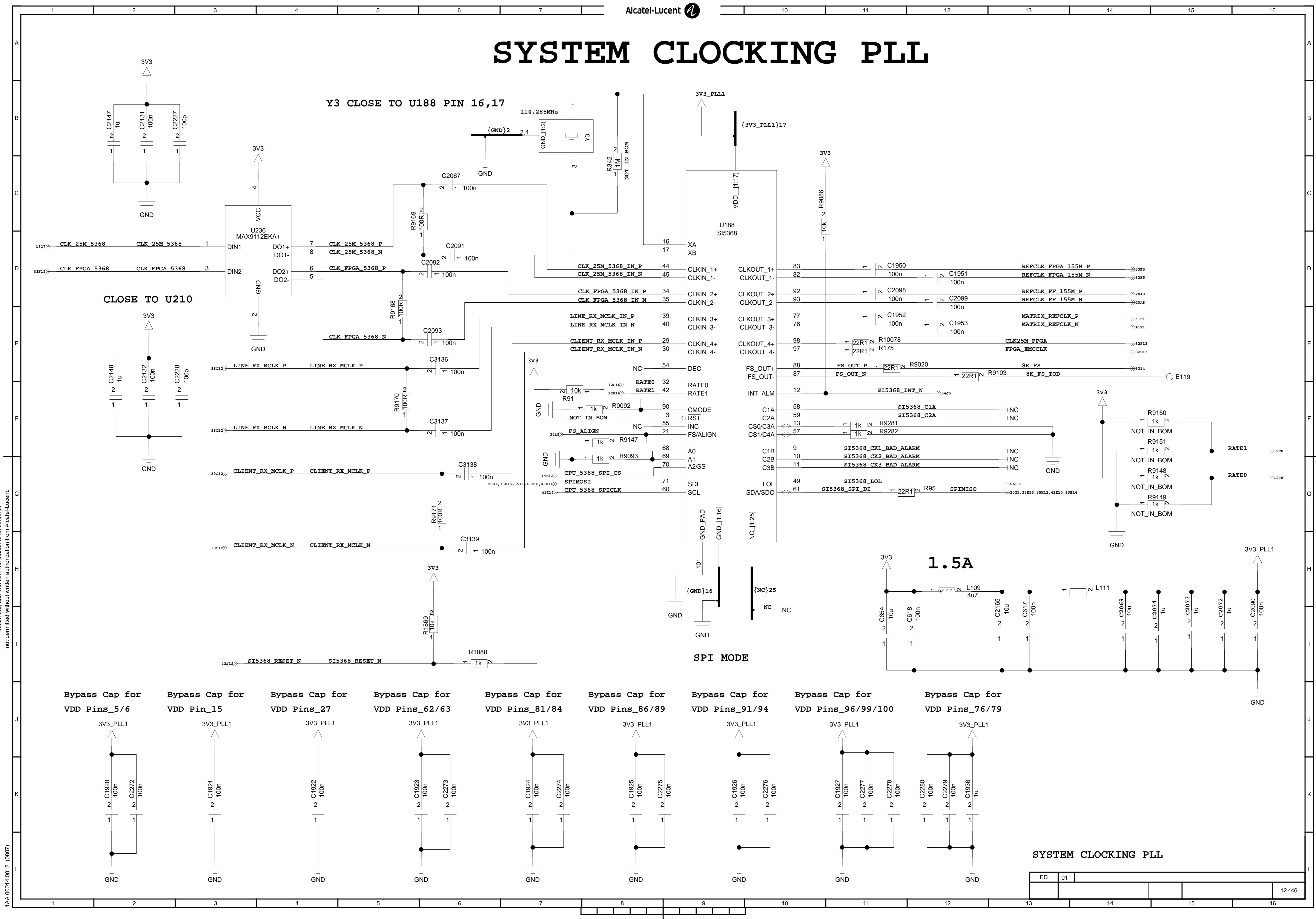
GND

3V3

{3V3}8

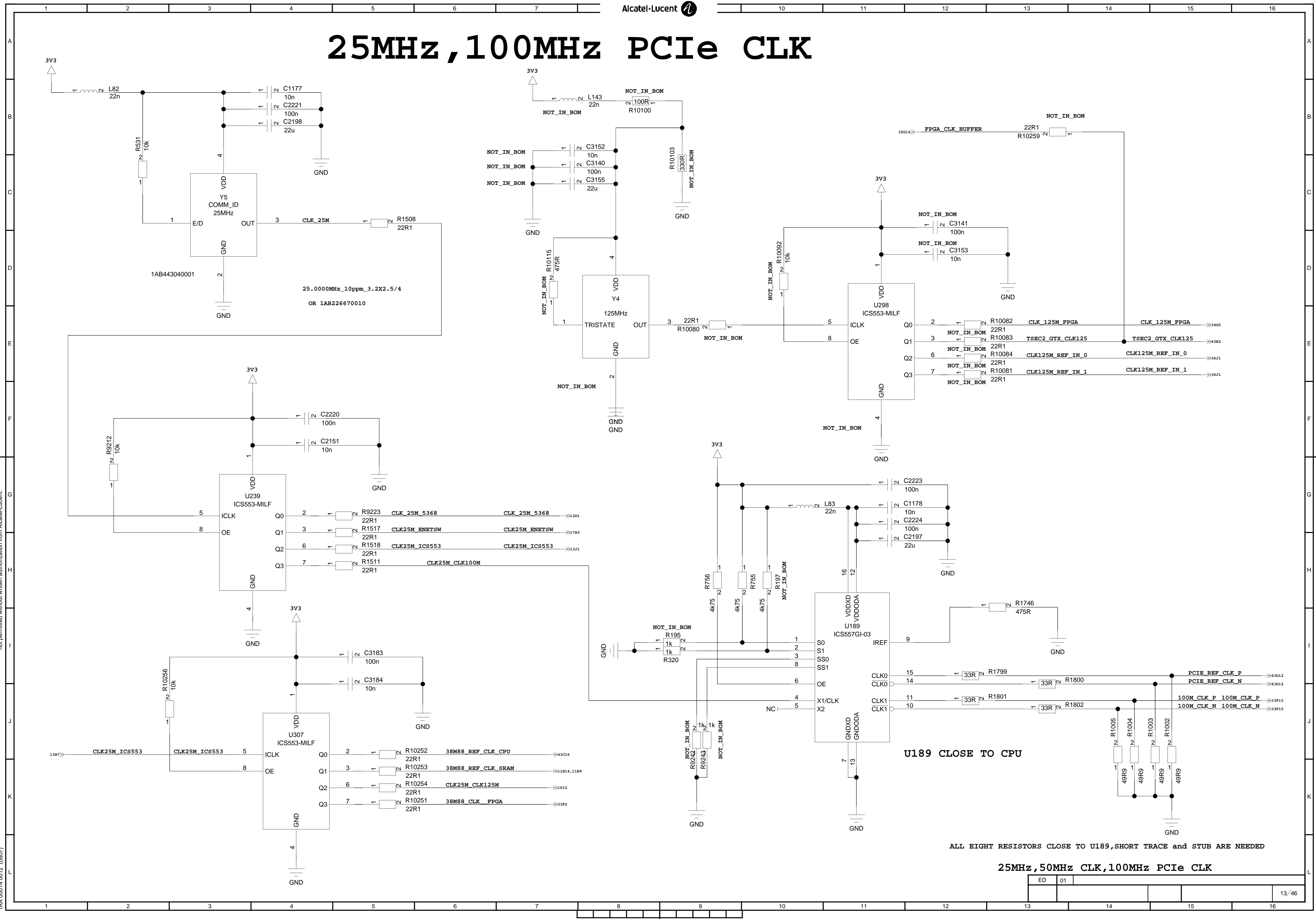
SYSTEM CLOCKING PLL

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25MHz, 100MHz PCIe CLK

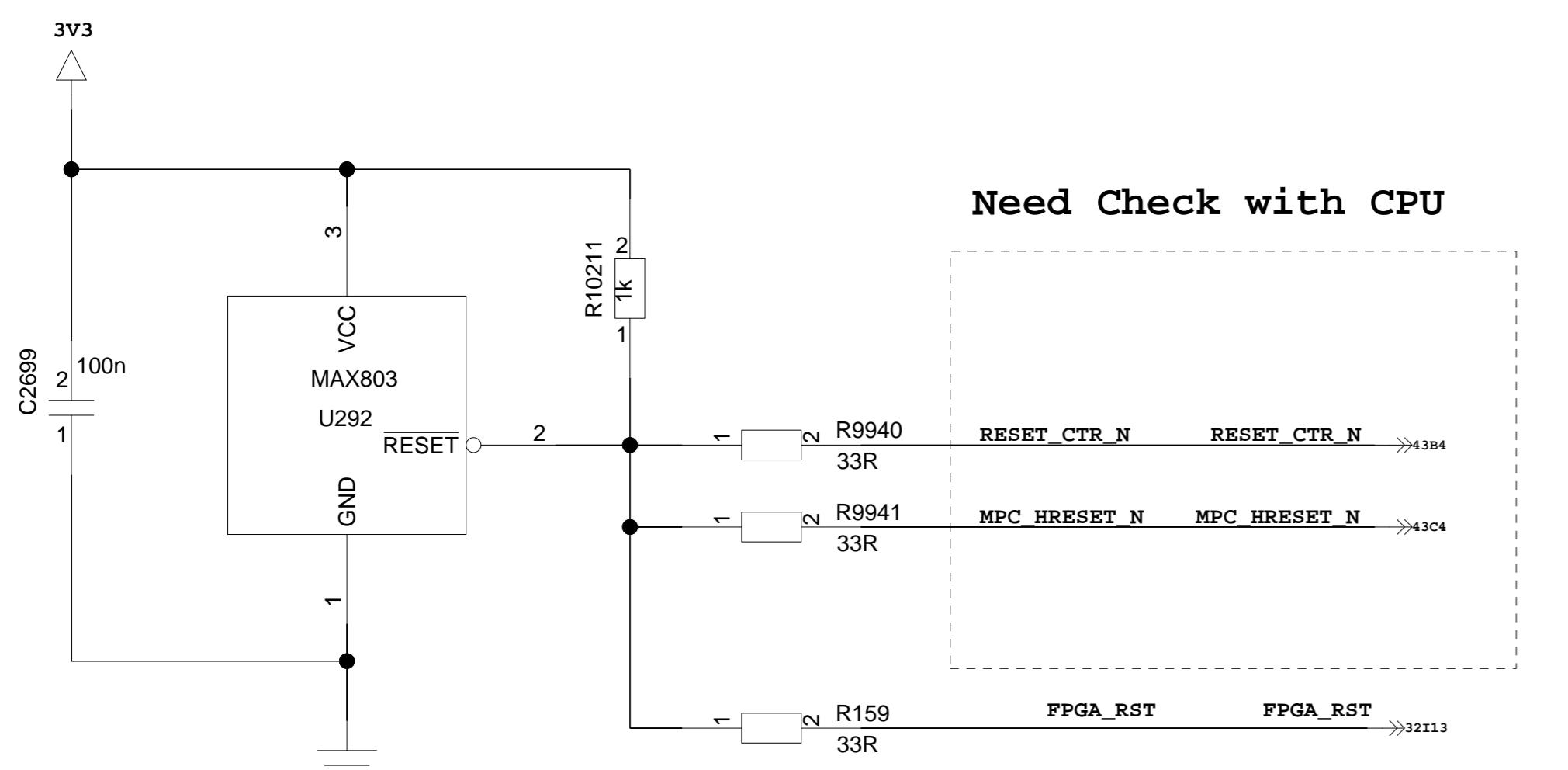
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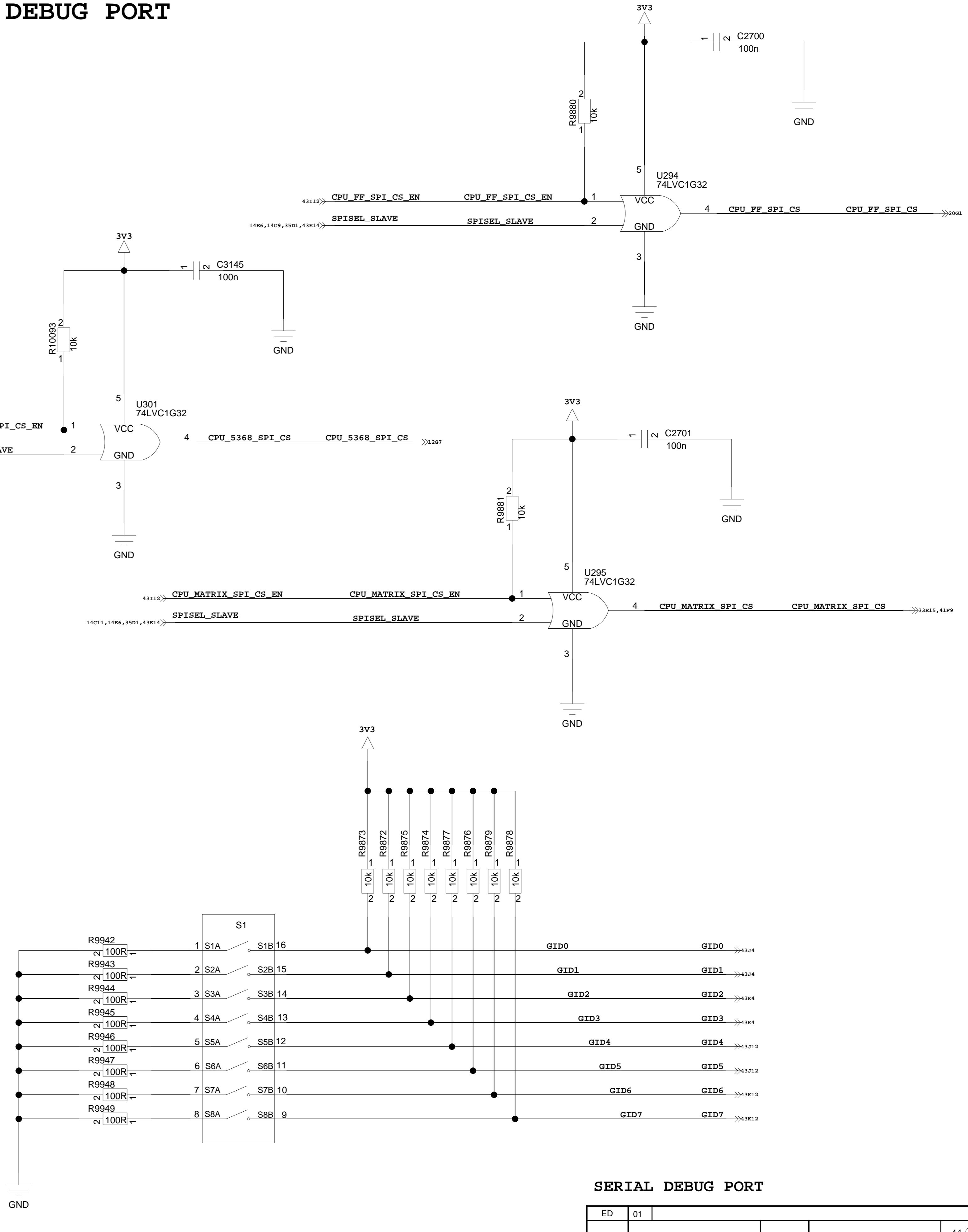
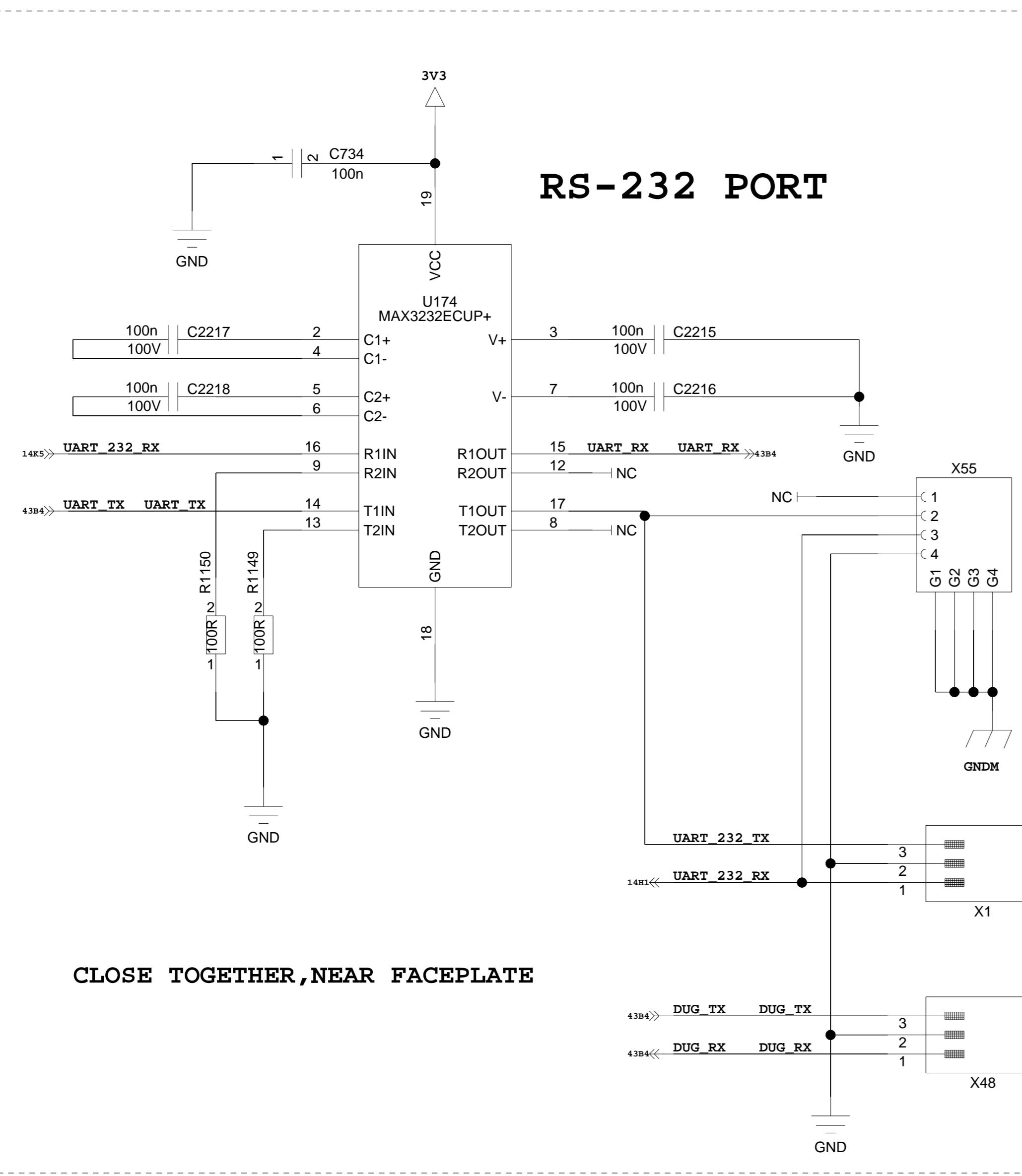
SERIAL DEBUG PORT

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CLOSE TOGETHER, NEAR FACEPLATE

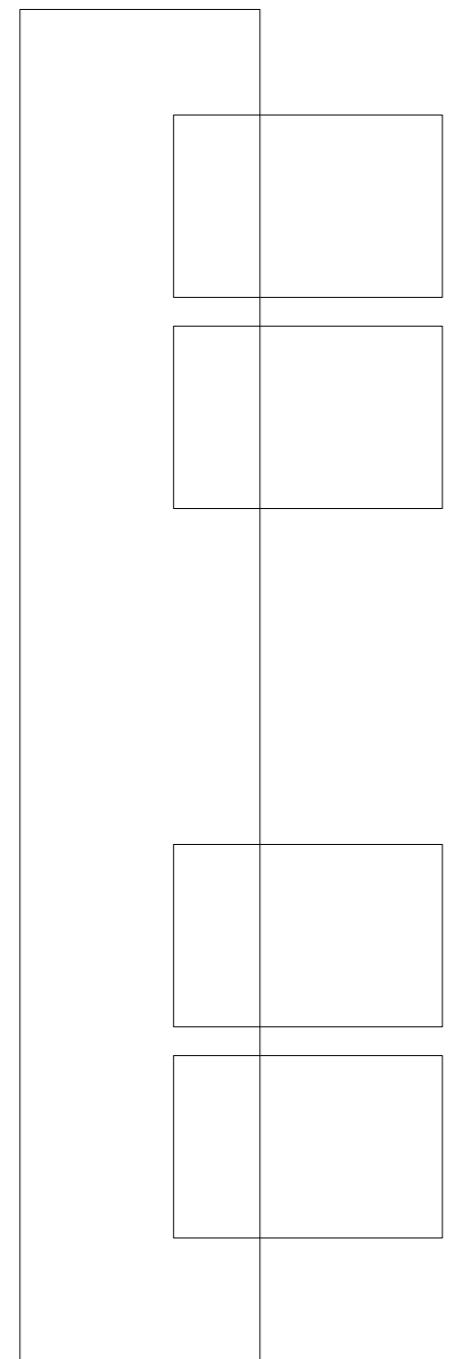


RS-232 PORT



New Schematic and Layout Lib needed

MAIN BOARD BACKPLANE CONNECTOR LOCATION



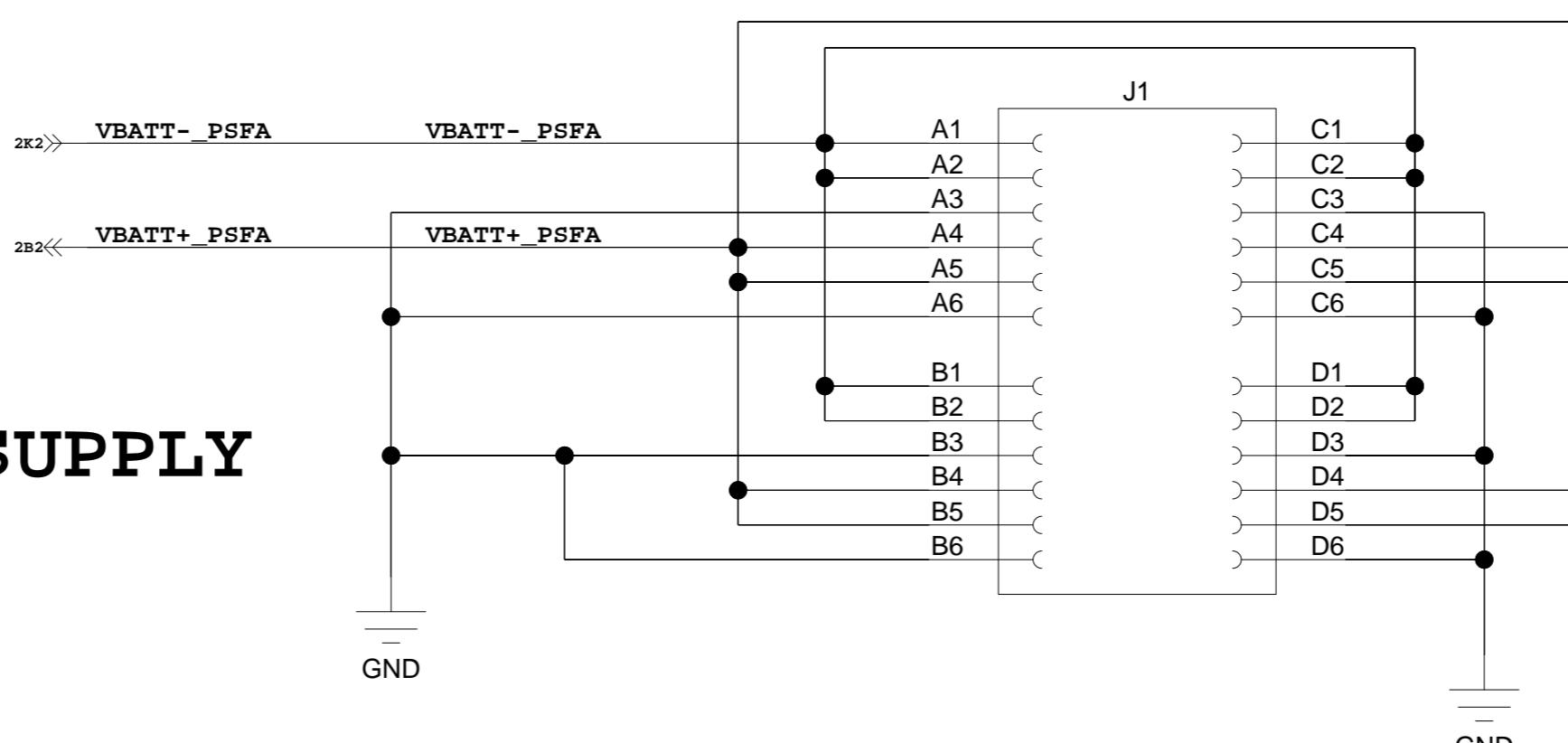
J1

J2

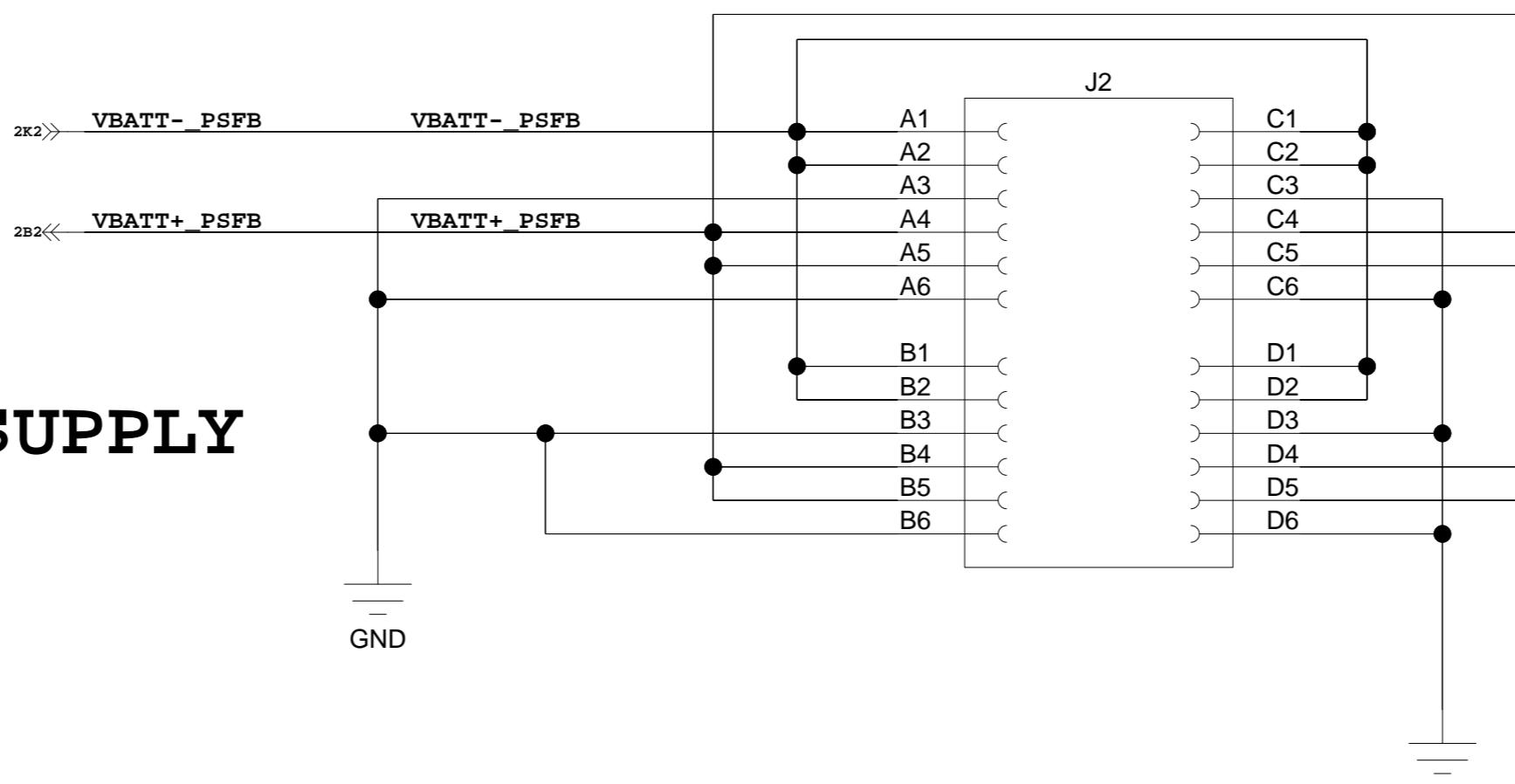
J3

J4

POWER A SUPPLY



POWER B SUPPLY



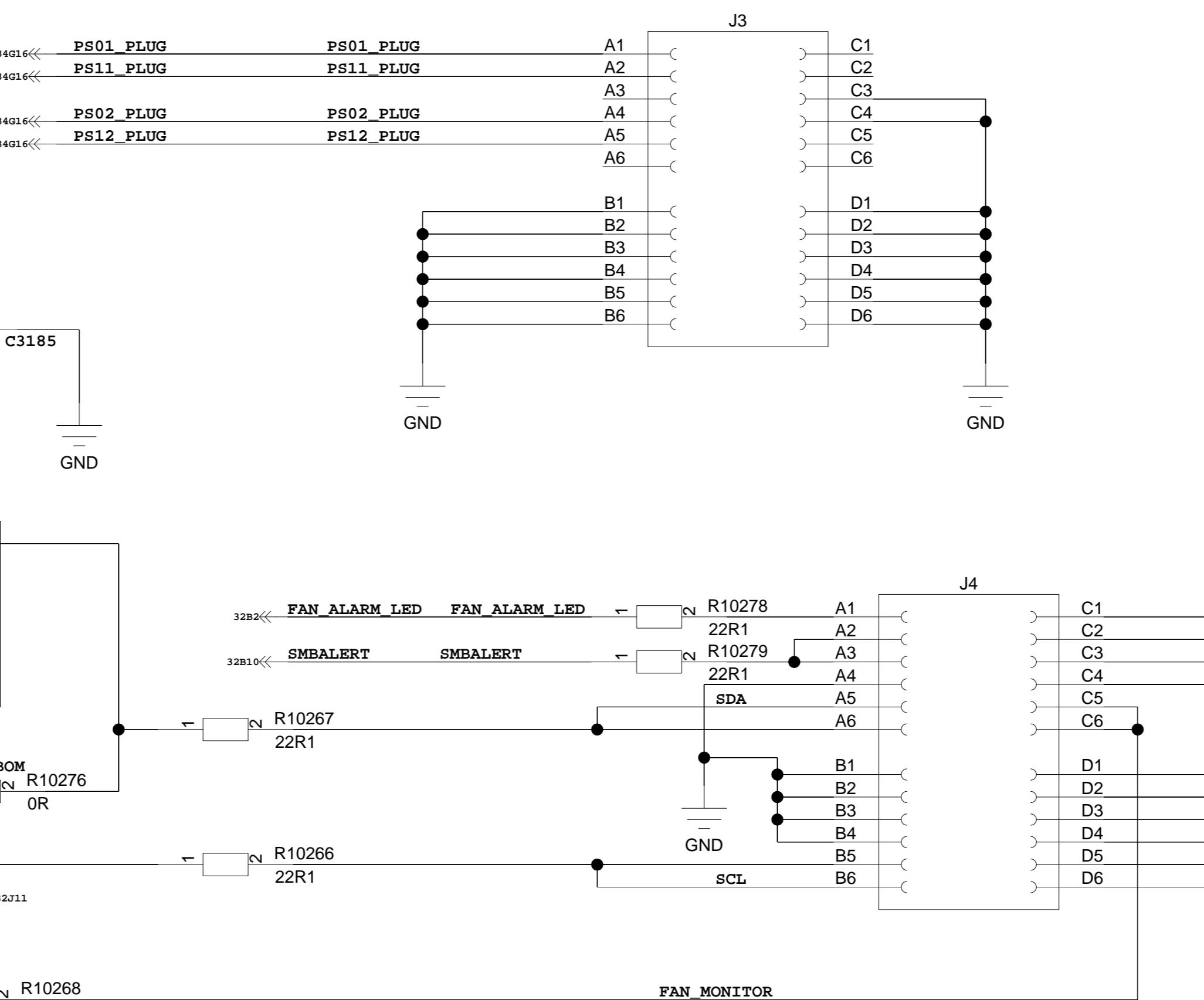
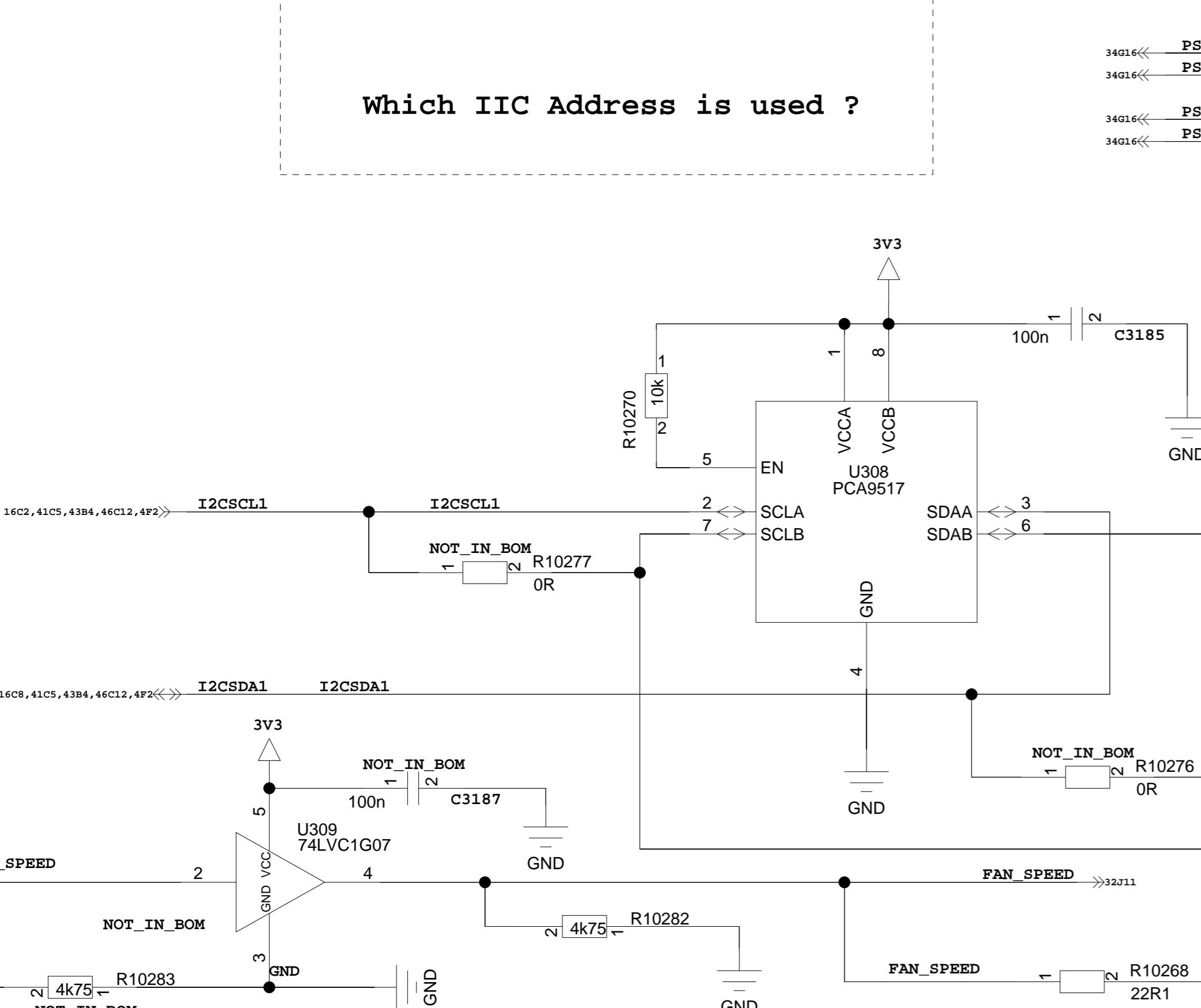
Need check with BP Connector

VENDOR : OUPIN

BACKPLANE : 9111-4124BC10PU

MAIN BOARD : 9111-42241G10PU

Which IIC Address is used ?



BATTERY POWER CONNECTOR

ED	01						
							15/46

REMOTE INVENTORY, I2C BUS TRANSLATOR & TEST HEADER

1AB195600005

I2C ADDRESS = 1010 010R

$$V_{out} = 0.5 * (1 + R2/R3) = 2.5V$$

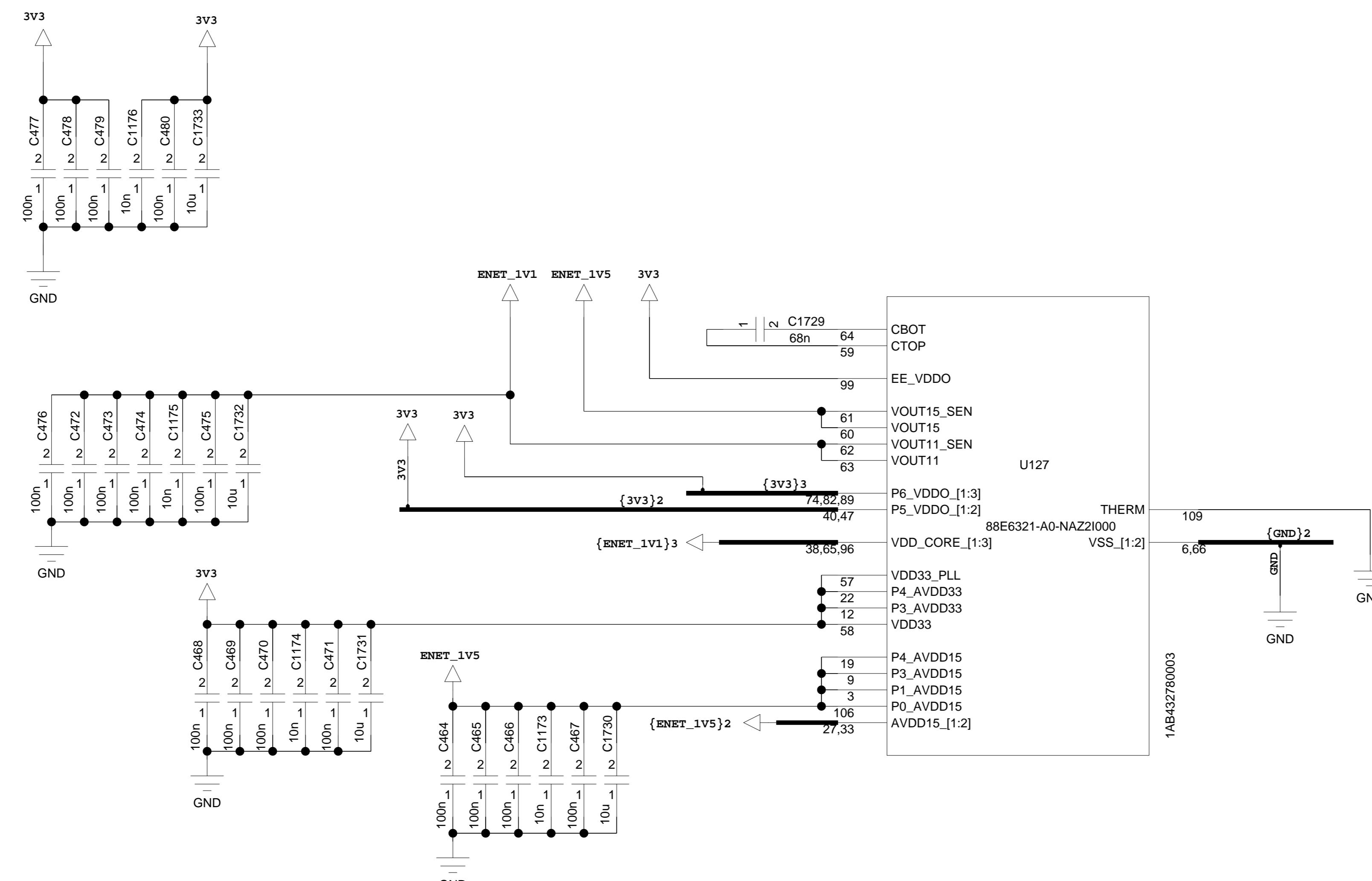
U5 FOR FPGA GTP REFERENCE

REMOTE INVENTORY

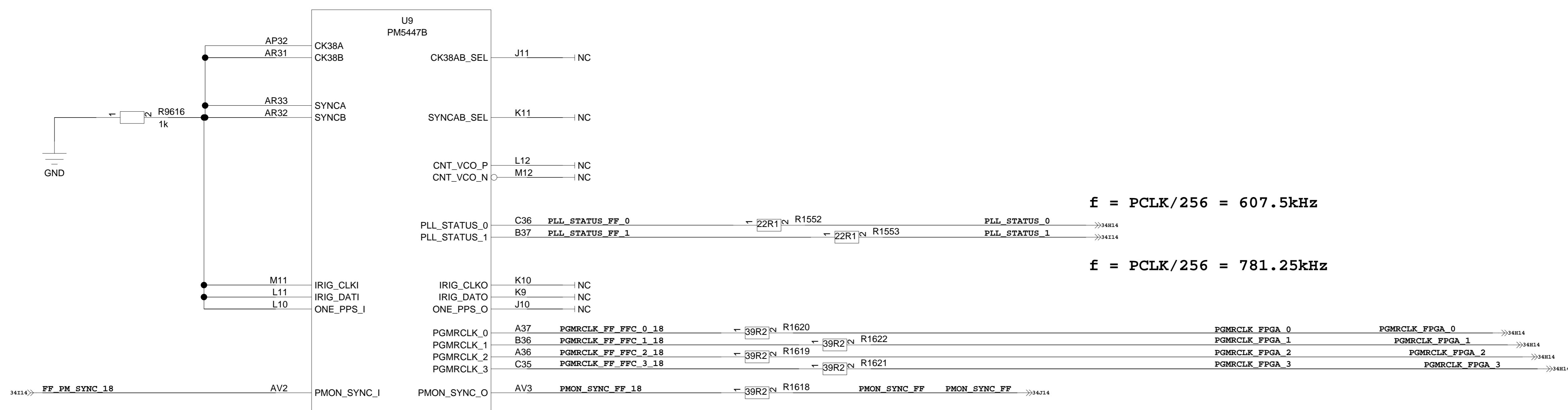
ETHERNET SWITCH POWER

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111 00011 0012 (0802)

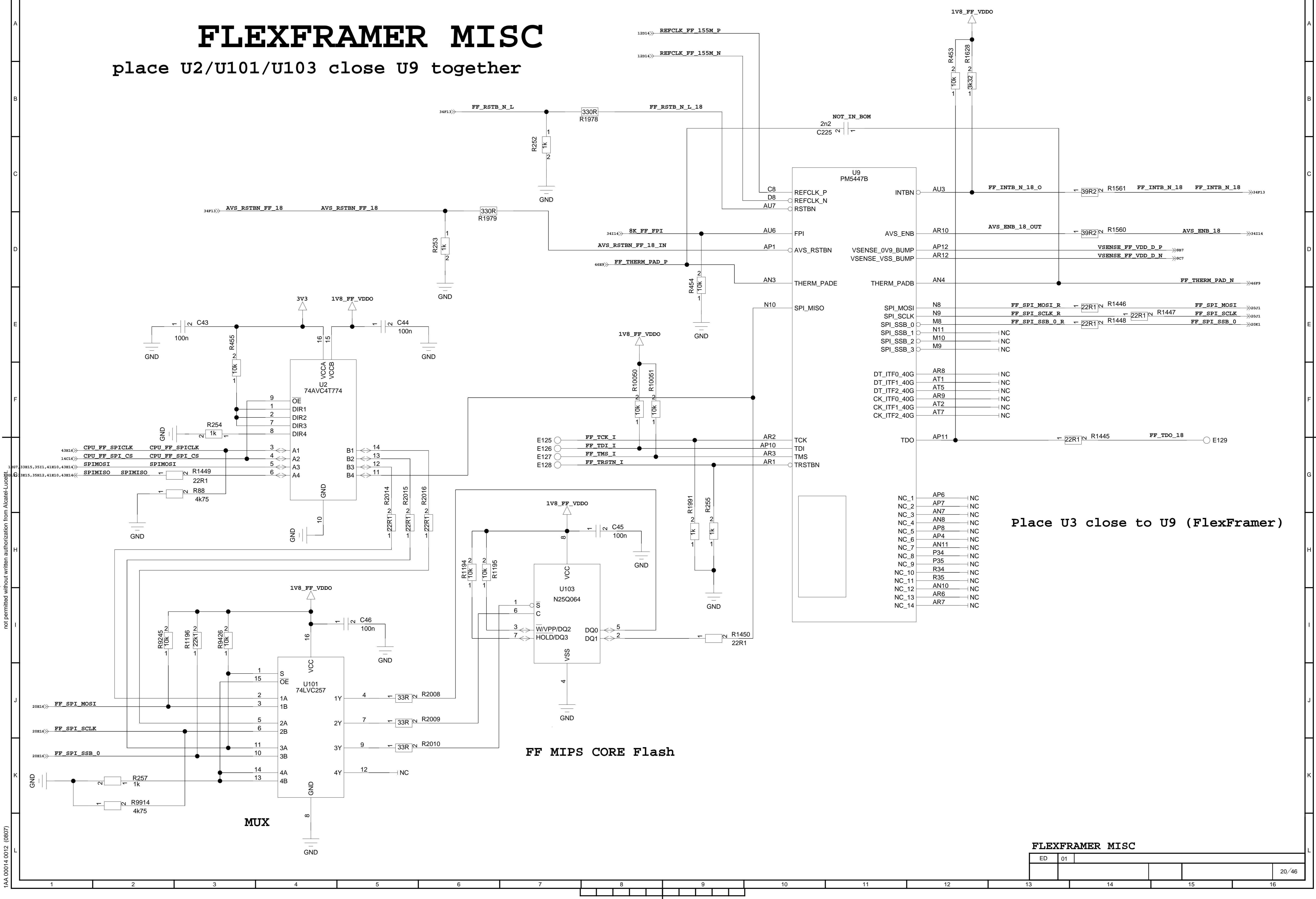


FLEXFRAMER CLK/SYNC/PTP



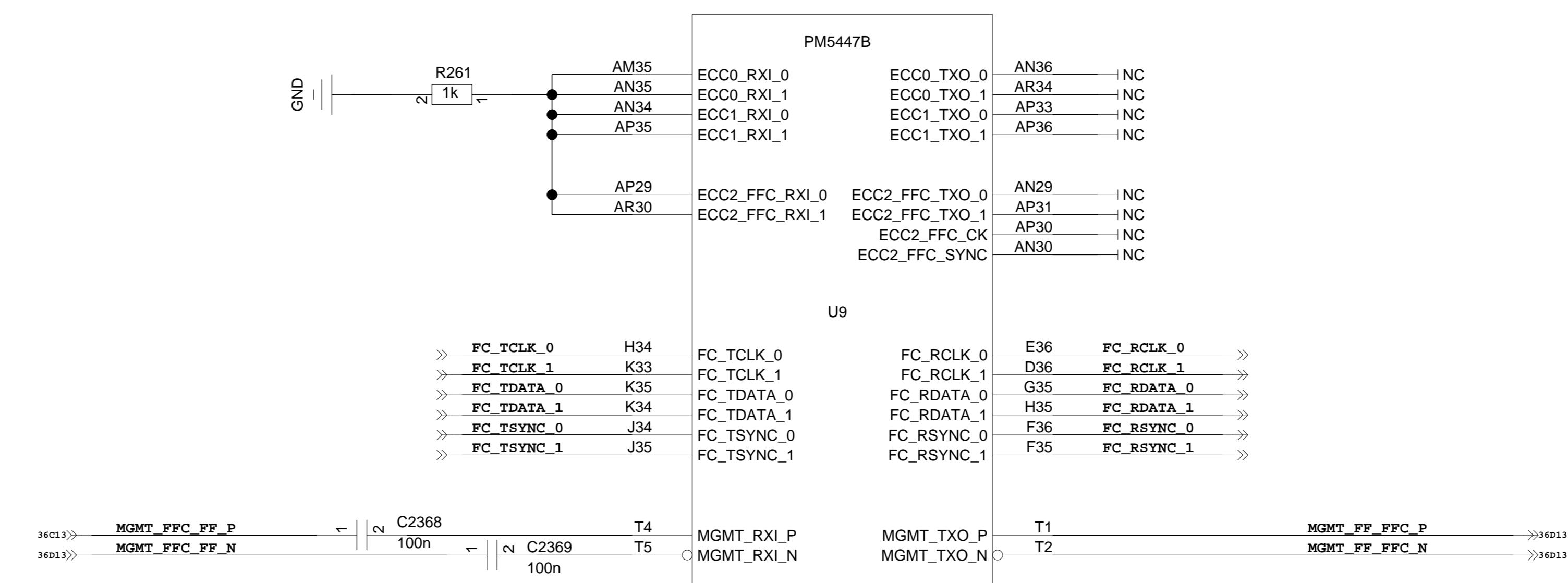
FLEXFRAMER MISCELLANEOUS

place U2/U101/U103 close U9 together



Place U3 close to U9 (FlexFramer)

FLEXFRAMER ECC/FC/MGMT



FLEXFRAMER LINE

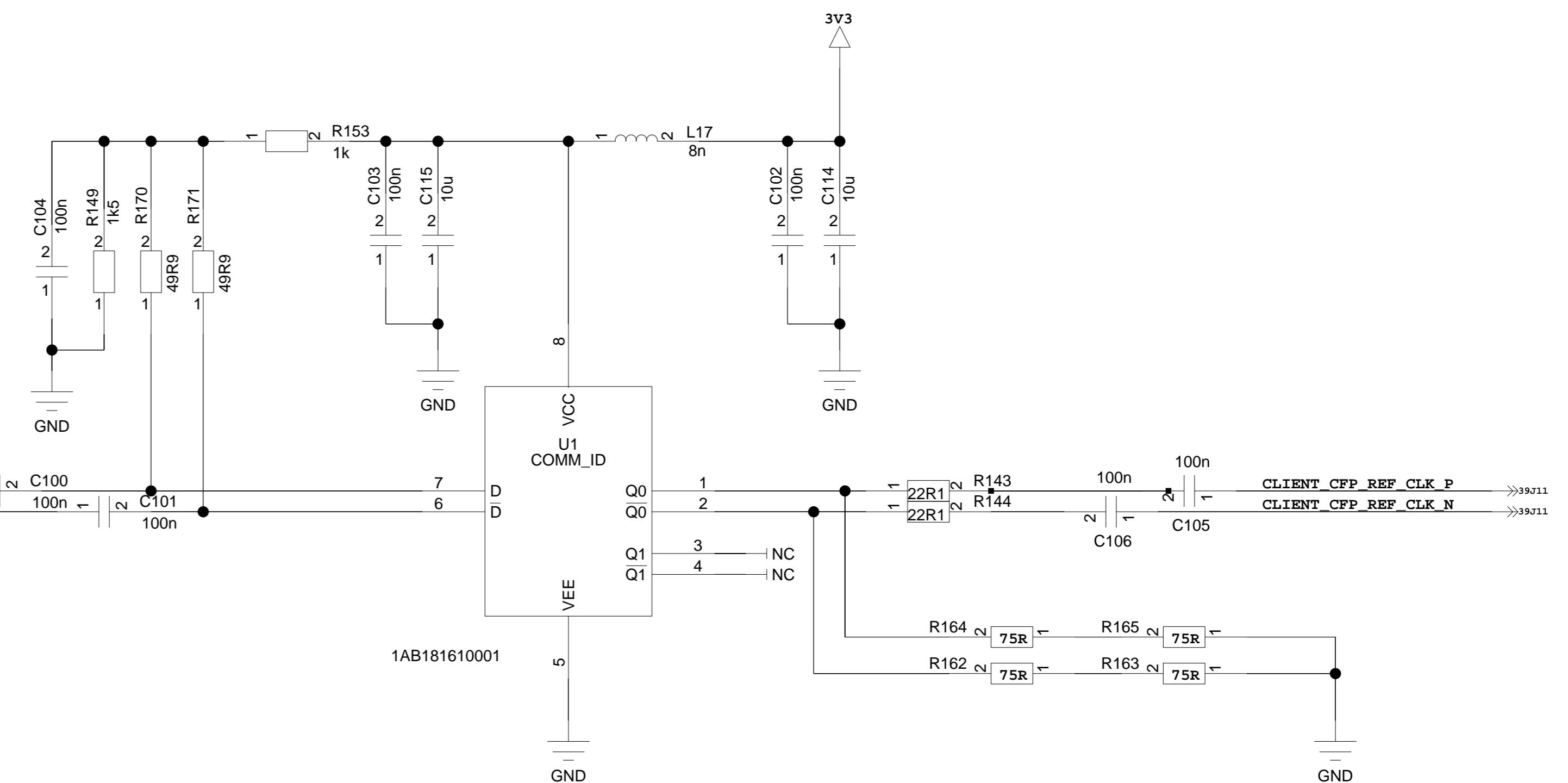
RX DC COUPLING FROM M21036 TX AC COUPLING TO M21036

34D13>>	RX_LOS_SFP+_FF_0	RX_LOS_SFP+_FF_0	U10
34D13>>	RX_LOS_SFP+_FF_1	RX_LOS_SFP+_FF_1	T9
34E13>>	RX_LOS_SFP+_FF_2	RX_LOS_SFP+_FF_2	U11
34E13>>	RX_LOS_SFP+_FF_3	RX_LOS_SFP+_FF_3	T11
34E13>>	RX_LOS_SFP+_FF_4	RX_LOS_SFP+_FF_4	T10
34E13>>	RX_LOS_SFP+_FF_5	RX_LOS_SFP+_FF_5	R8
34E13>>	RX_LOS_SFP+_FF_6	RX_LOS_SFP+_FF_6	R10
34E13>>	RX_LOS_SFP+_FF_7	RX_LOS_SFP+_FF_7	R9
34E13>>	RX_LOS_SFP+_FF_8	RX_LOS_SFP+_FF_8	P8
34E13>>	RX_LOS_SFP+_FF_9	RX_LOS_SFP+_FF_9	R11
34E13>>	RX_LOS_SFP+_FF_10	RX_LOS_SFP+_FF_10	P10
34E13>>	RX_LOS_SFP+_FF_11	RX_LOS_SFP+_FF_11	P11

U9 PM5447B	
LINE_LOS_0	LINE_REFCLK_0_P
LINE_LOS_1	LINE_REFCLK_0_N
LINE_LOS_2	LINE_REFCLK_1_P
LINE_LOS_3	LINE_REFCLK_1_N
LINE_LOS_4	LINE_REFCLK_2_P
LINE_LOS_5	LINE_REFCLK_2_N
LINE_LOS_6	LINE_REFCLK_3_P
LINE_LOS_7	LINE_REFCLK_3_N
LINE_LOS_8	LINE_REFCLK_4_P
LINE_LOS_9	LINE_REFCLK_4_N
LINE_LOS_10	LINE_REFCLK_5_P
LINE_LOS_11	LINE_REFCLK_5_N
	LINE_REFCLK_6_P
	LINE_REFCLK_6_N
	LINE_REFCLK_7_P
	LINE_REFCLK_7_N
	LINE_REFCLK_8_P
	LINE_REFCLK_8_N
	LINE_REFCLK_9_P
	LINE_REFCLK_9_N
	LINE_REFCLK_10_P
	LINE_REFCLK_10_N
	LINE_REFCLK_11_P
	LINE_REFCLK_11_N

40F15>>	LINE_RXI_0_P	AM5	LINE_RXI_0_P
40F15>>	LINE_RXI_0_N	AM6	LINE_RXI_0_N
40C15>>	LINE_RXI_1_P	AL6	LINE_RXI_1_P
40C15>>	LINE_RXI_1_N	AL7	LINE_RXI_1_N
40D15>>	LINE_RXI_2_P	AK5	LINE_RXI_2_P
40D15>>	LINE_RXI_2_N	AK6	LINE_RXI_2_N
40F15>>	LINE_RXI_3_P	AJ6	LINE_RXI_3_P
40F15>>	LINE_RXI_3_N	AJ7	LINE_RXI_3_N
40D15>>	LINE_RXI_4_P	AH5	LINE_RXI_4_P
40D15>>	LINE_RXI_4_N	AH6	LINE_RXI_4_N
40F15>>	LINE_RXI_5_P	AG6	LINE_RXI_5_P
40F15>>	LINE_RXI_5_N	AG7	LINE_RXI_5_N
40G15>>	LINE_RXI_6_P	AE5	LINE_RXI_6_P
40G15>>	LINE_RXI_6_N	AE6	LINE_RXI_6_N
40G15>>	LINE_RXI_7_P	AD6	LINE_RXI_7_P
40G15>>	LINE_RXI_7_N	AD7	LINE_RXI_7_N
40I15>>	LINE_RXI_8_P	AC5	LINE_RXI_8_P
40I15>>	LINE_RXI_8_N	AC6	LINE_RXI_8_N
40I15>>	LINE_RXI_9_P	AB6	LINE_RXI_9_P
40I15>>	LINE_RXI_9_N	AB7	LINE_RXI_9_N
40I15>>	LINE_RXI_10_P	AA5	LINE_RXI_10_P
40I15>>	LINE_RXI_10_N	AA6	LINE_RXI_10_N
40H15>>	LINE_RXI_11_P	Y6	LINE_RXI_11_P
40H15>>	LINE_RXI_11_N	Y7	LINE_RXI_11_N

AM1	AM2	1	2	C2664	LINE_RXO_0_P	40I2
LINE_RXO_0_P	LINE_RXO_0_N	1	2	C2665	LINE_RXO_0_N	40I2
LINE_RXO_1_P	LINE_RXO_1_N	100n	1	C2666	LINE_RXO_1_P	40I2
LINE_RXO_1_N	LINE_RXO_1_P	1	2	C2667	LINE_RXO_1_N	40I2
LINE_RXO_2_P	LINE_RXO_2_N	100n	1	C2668	LINE_RXO_2_P	40I2
LINE_RXO_2_N	LINE_RXO_2_P	1	2	C2669	LINE_RXO_2_N	40I2
LINE_RXO_3_P	LINE_RXO_3_N	100n	1	C2670	LINE_RXO_3_P	40H9
LINE_RXO_3_N	LINE_RXO_3_P	1	2	C2671	LINE_RXO_3_N	40H9
LINE_RXO_4_P	LINE_RXO_4_N	100n	1	C2672	LINE_RXO_4_P	40I9
LINE_RXO_4_N	LINE_RXO_4_P	1	2	C2673	LINE_RXO_4_N	40I9
LINE_RXO_5_P	LINE_RXO_5_N	100n	1	C2674	LINE_RXO_5_P	40G2
LINE_RXO_5_N	LINE_RXO_5_P	1	2	C2675	LINE_RXO_5_N	40G2
LINE_RXO_6_P	LINE_RXO_6_N	100n	1	C2676	LINE_RXO_6_P	40P2
LINE_RXO_6_N	LINE_RXO_6_P	1	2	C2677	LINE_RXO_6_N	40P2
LINE_RXO_7_P	LINE_RXO_7_N	100n	1	C2678	LINE_RXO_7_P	40G9
LINE_RXO_7_N	LINE_RXO_7_P	1	2	C2679	LINE_RXO_7_N	40G9
LINE_RXO_8_P	LINE_RXO_8_N	100n	1	C2680	LINE_RXO_8_P	40D2
LINE_RXO_8_N	LINE_RXO_8_P	1	2	C2681	LINE_RXO_8_N	40D2
LINE_RXO_9_P	LINE_RXO_9_N	100n	1	C2682	LINE_RXO_9_P	40D2
LINE_RXO_9_N	LINE_RXO_9_P	1	2	C2683	LINE_RXO_9_N	40D2
LINE_RXO_10_P	LINE_RXO_10_N	100n	1	C2684	LINE_RXO_10_P	40C2
LINE_RXO_10_N	LINE_RXO_10_P	1	2	C2685	LINE_RXO_10_N	40C2
LINE_RXO_11_P	LINE_RXO_11_N	100n	1	C2686	LINE_RXO_11_P	40F9
LINE_RXO_11_N	LINE_RXO_11_P	1	2	C2687	LINE_RXO_11_N	40F9
		100n				



FLEXFRAMER LINE

ED	01			

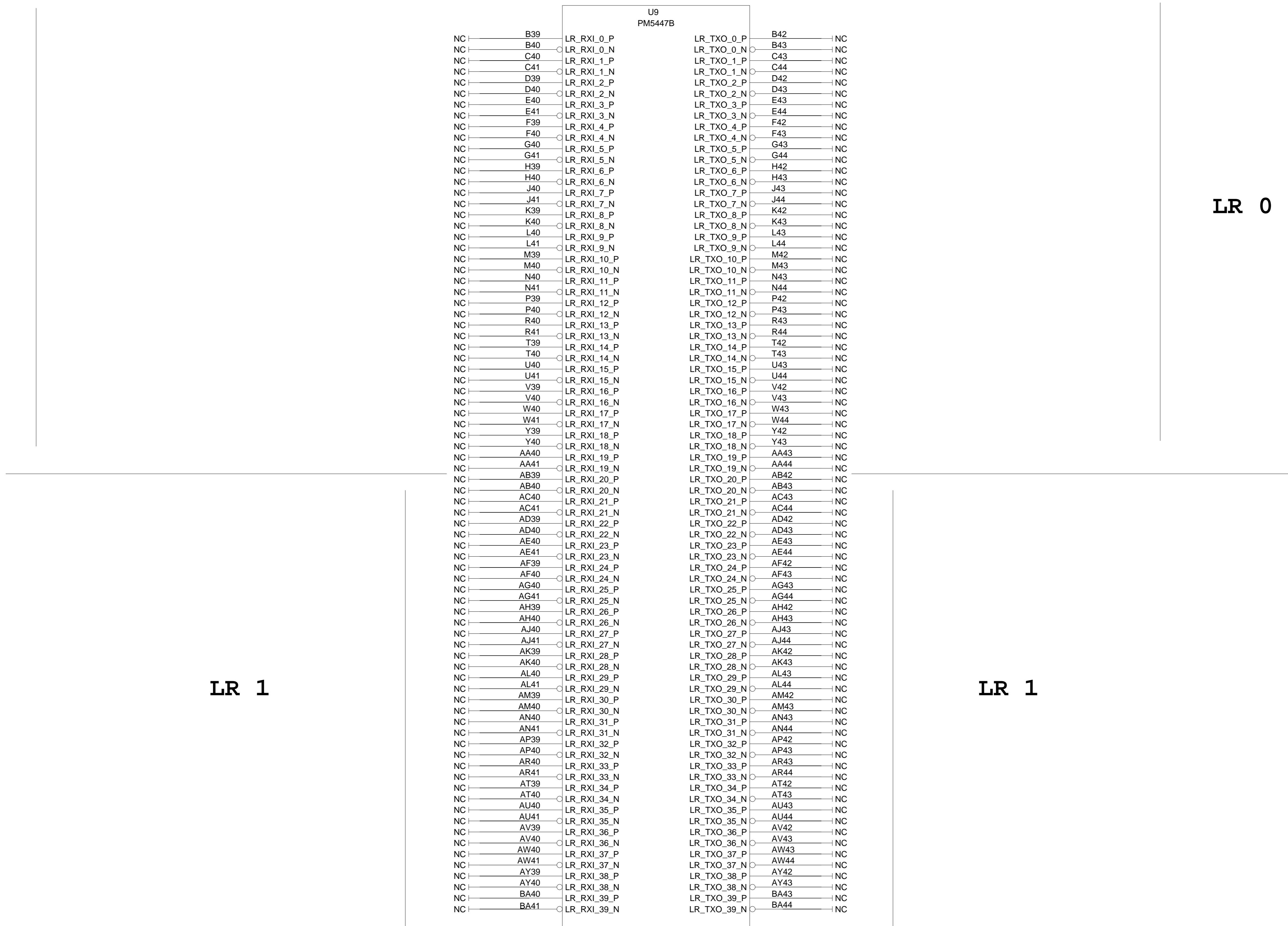
FLEXFRAMER BACKPLANE LR

LR 0

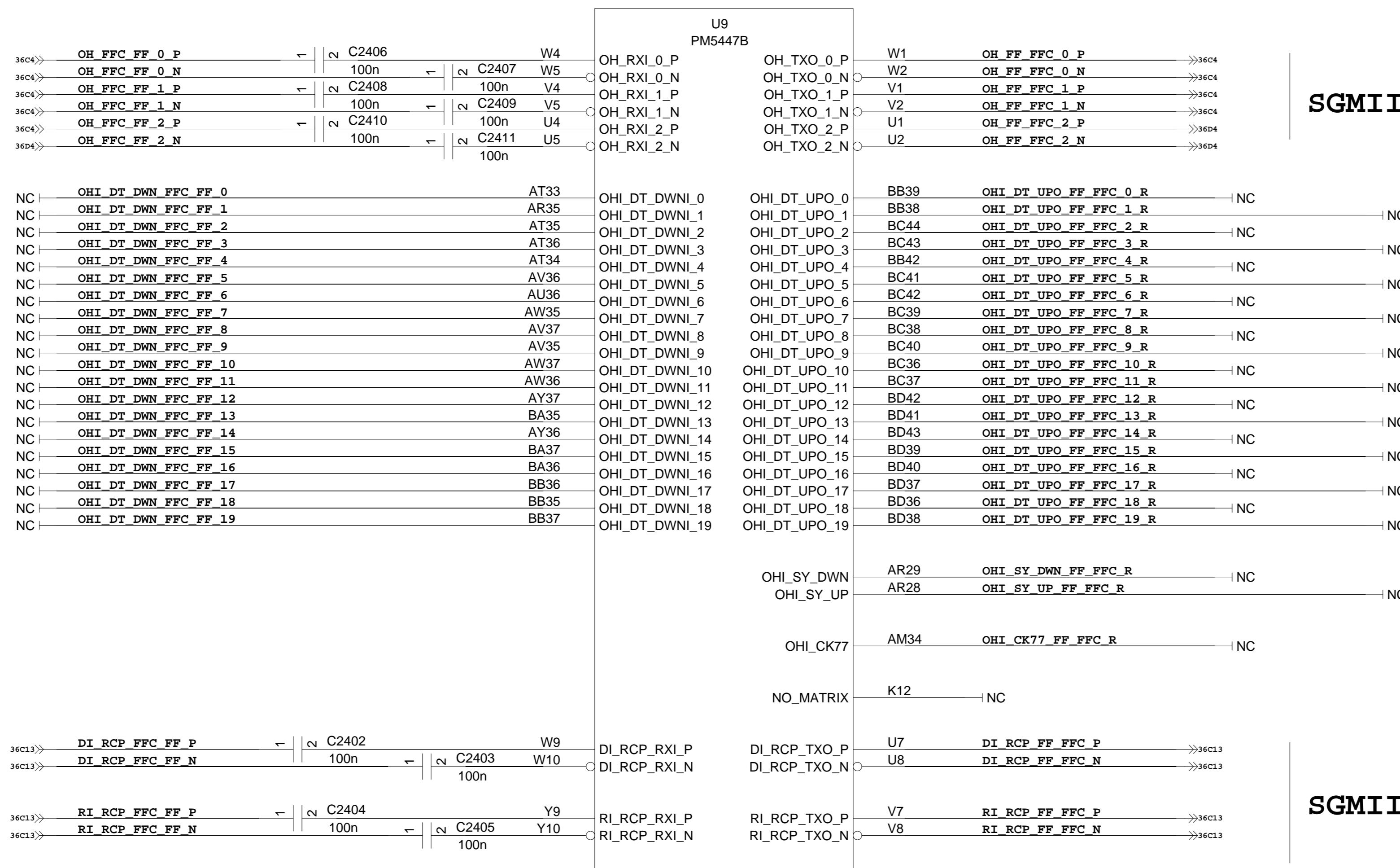
LR 0

LR 1

LR 1



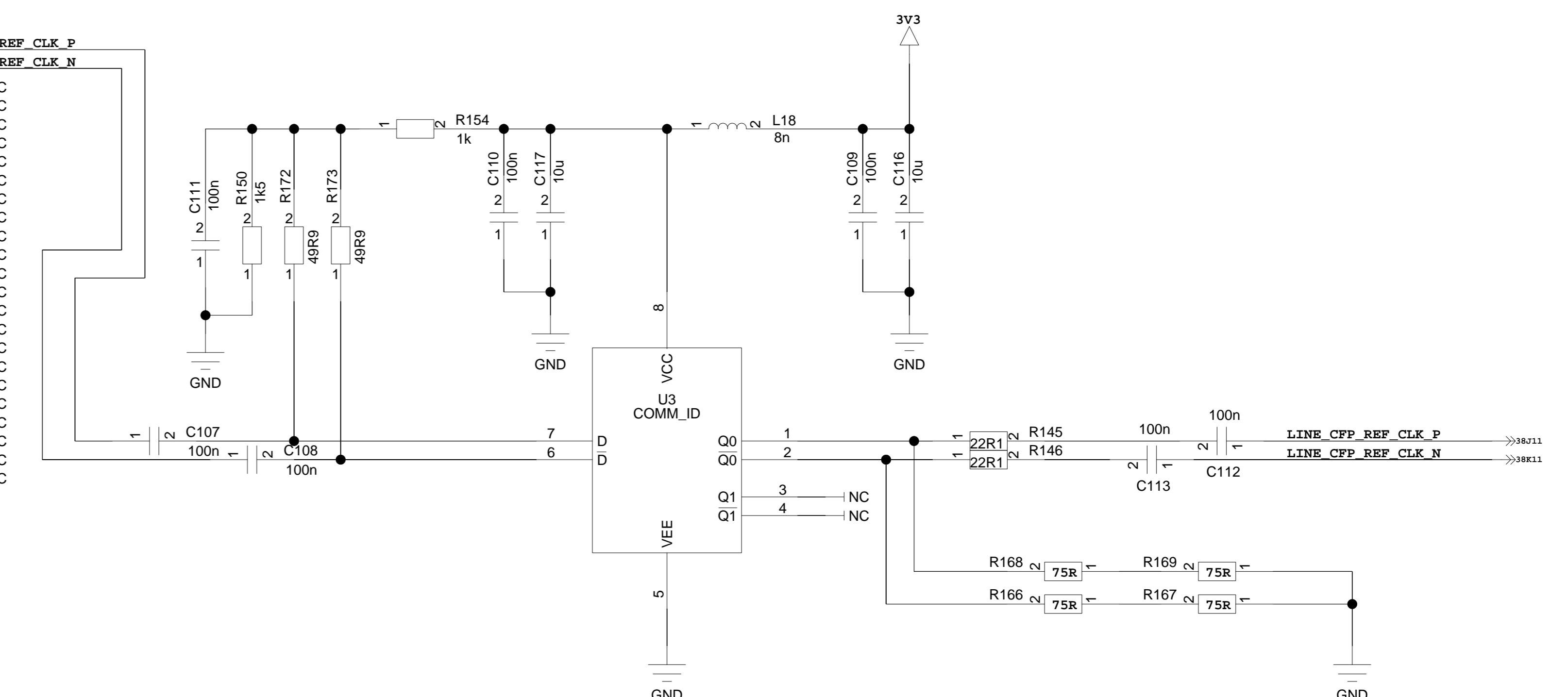
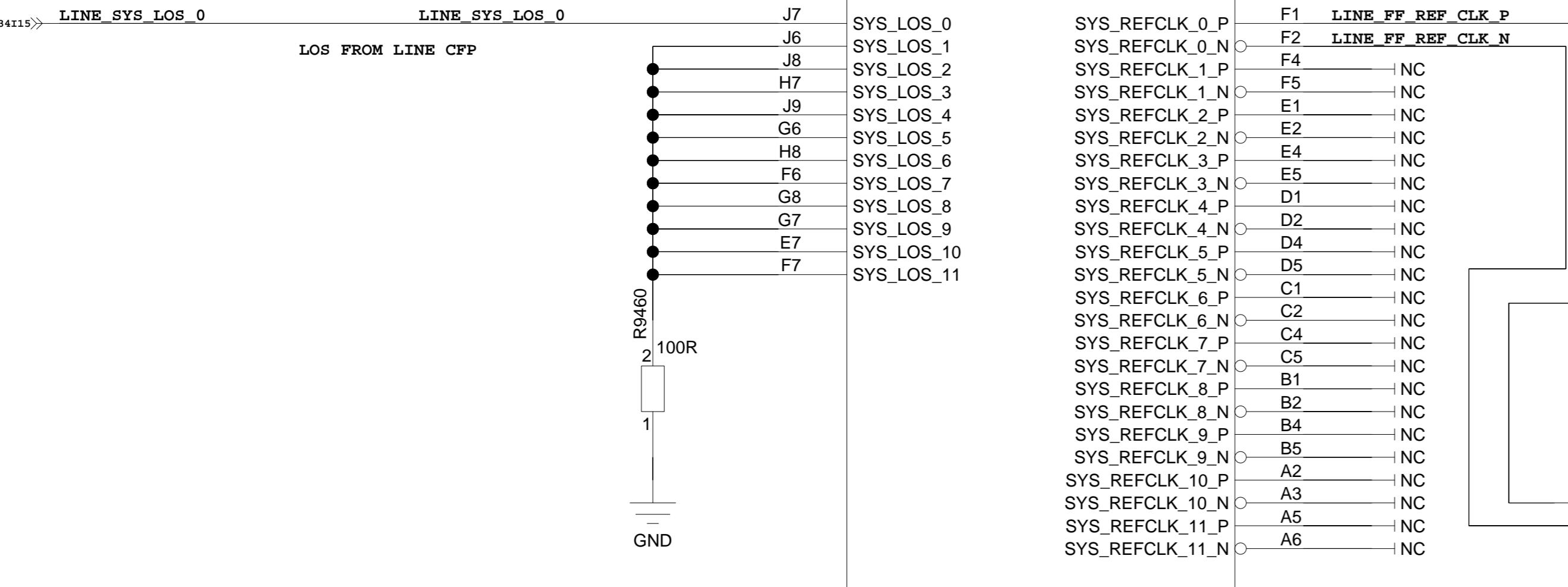
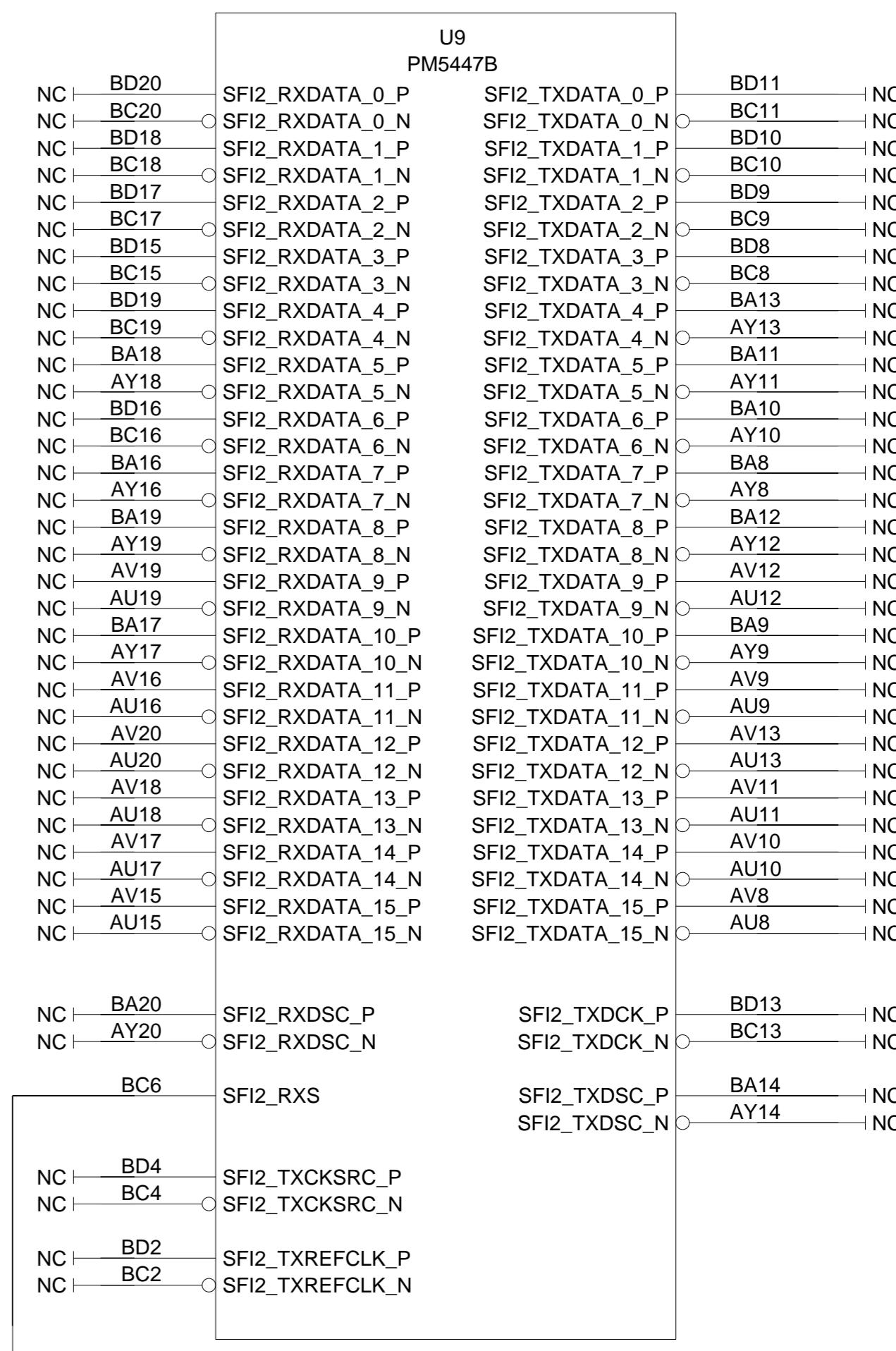
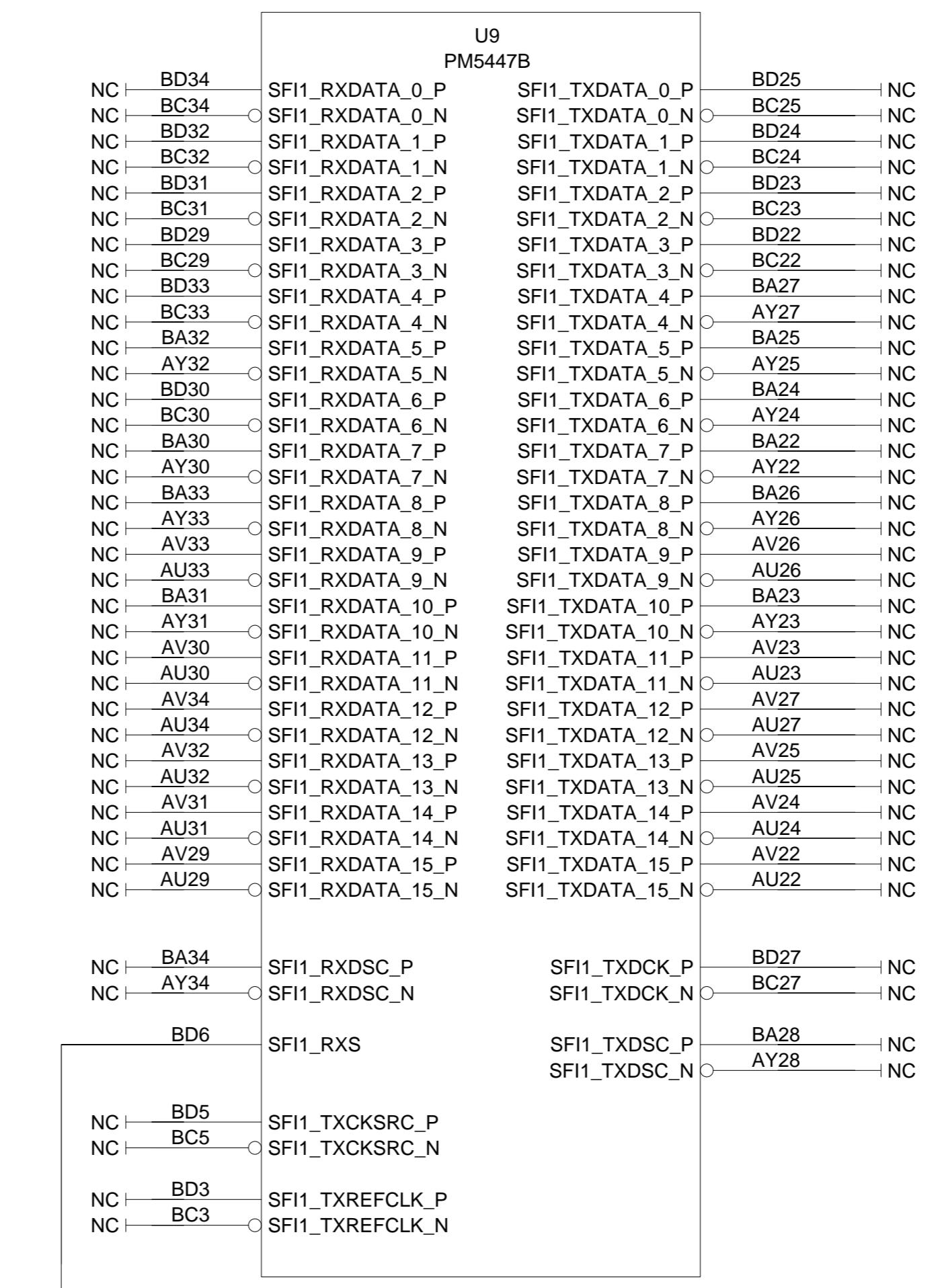
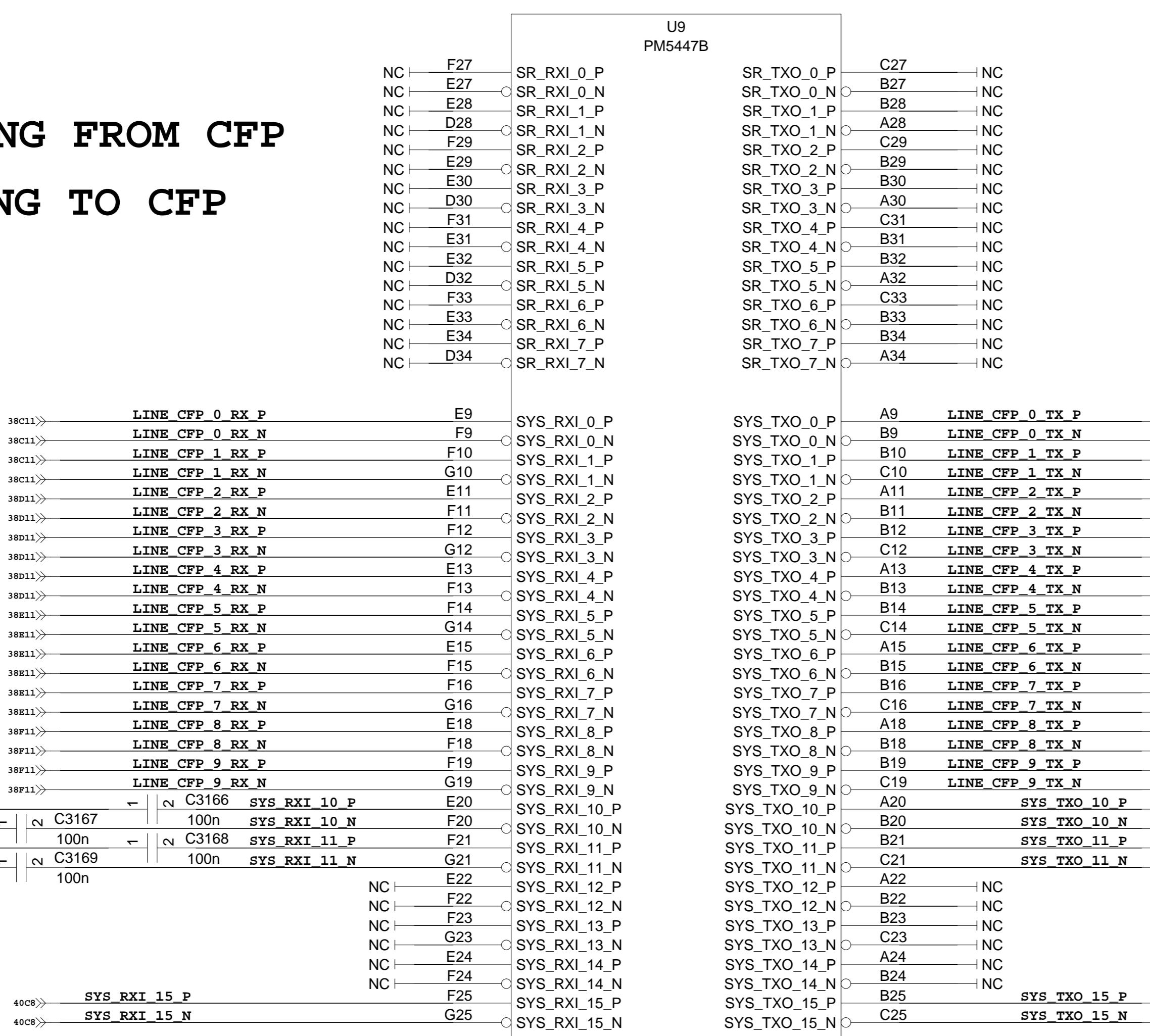
FLEXFRAMER OH/OHI



FLEXFRAMER SFI-5.1/SYS/SR

RX AC COUPLING FROM CFP

TX AC COUPLING TO CFP

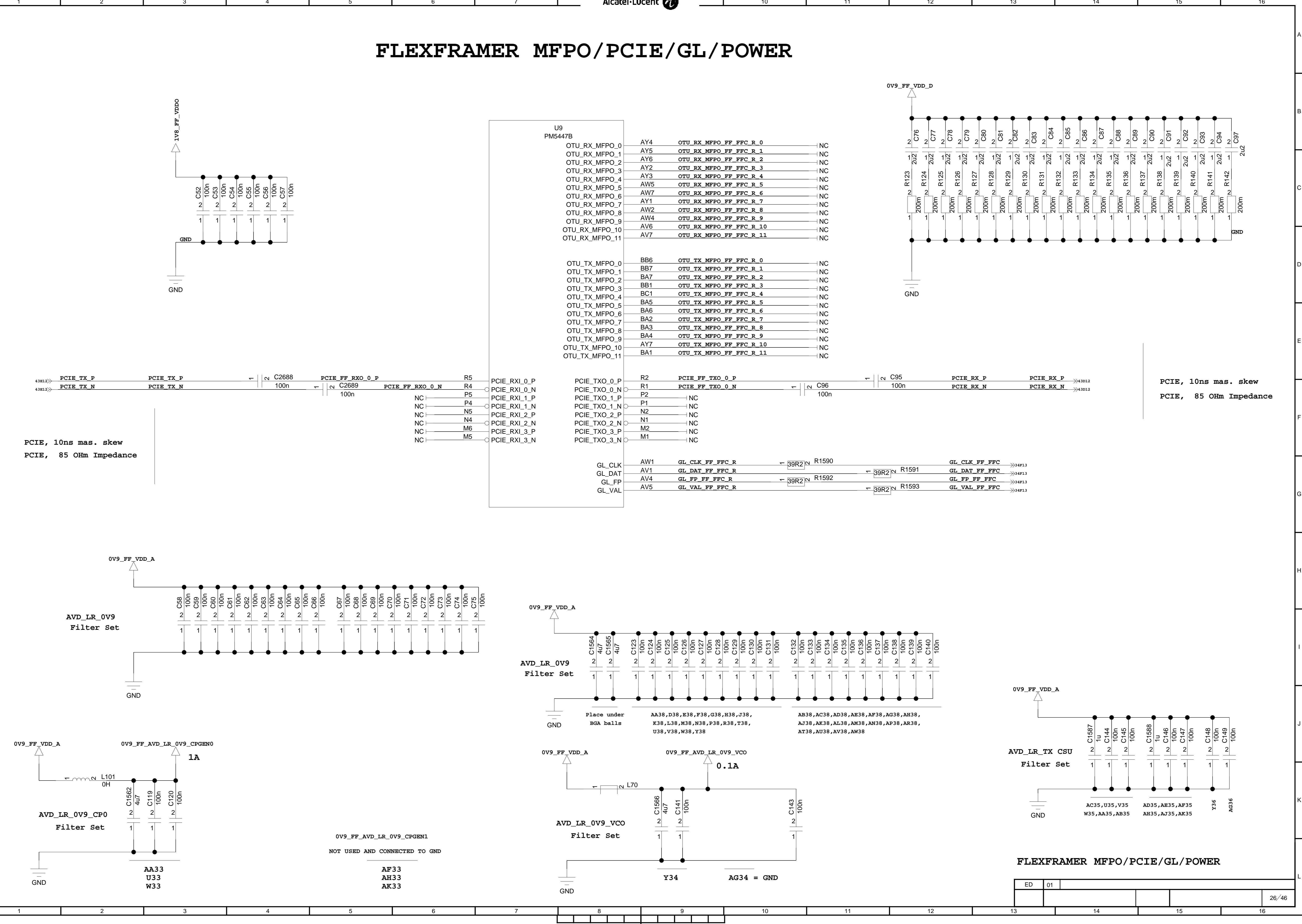


FLEXFRAMER SFI-5.1/SYS/SR

ED 01 | 25/

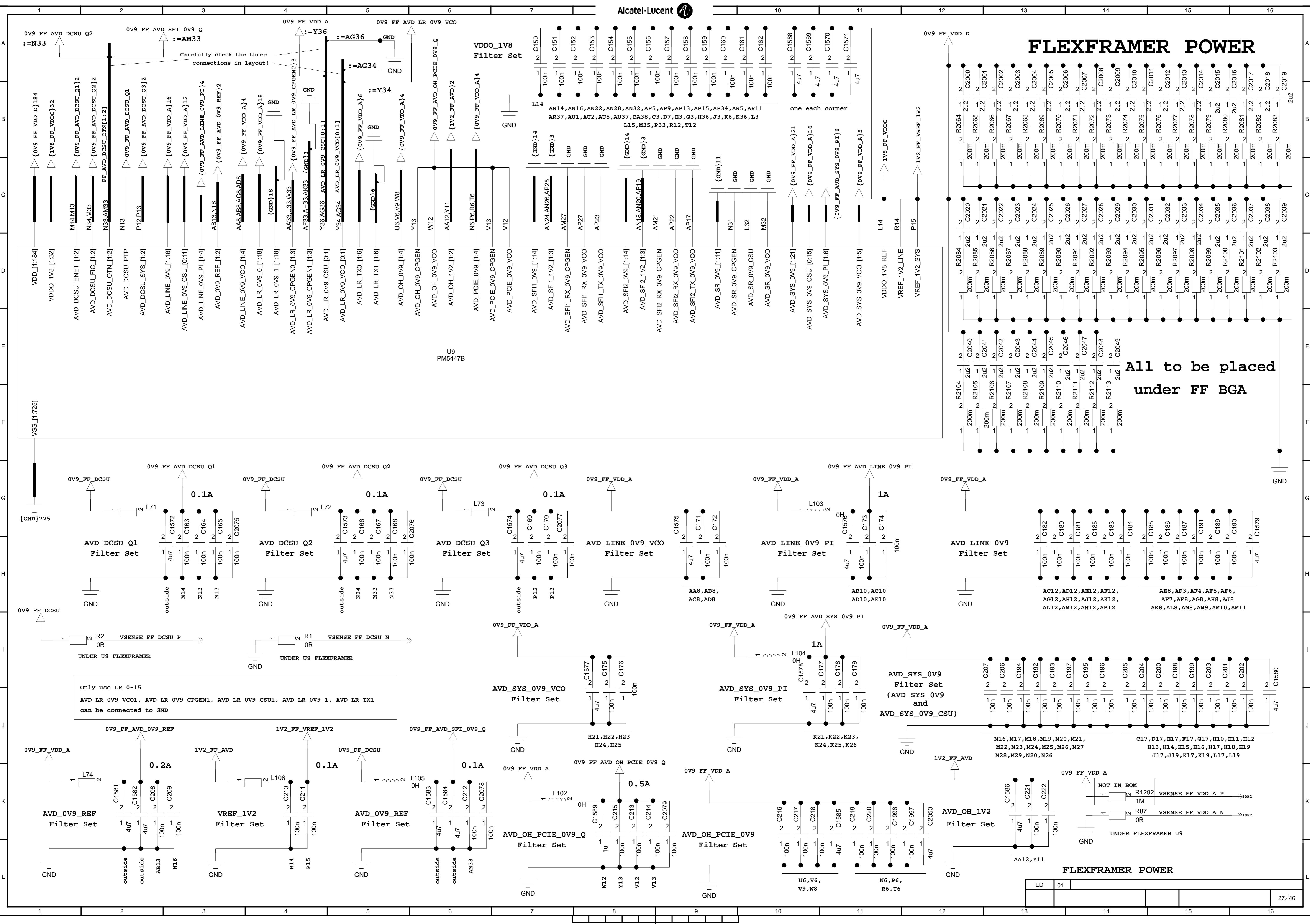
FLEXFRAMER MFPO/PCIE/GL/POWER

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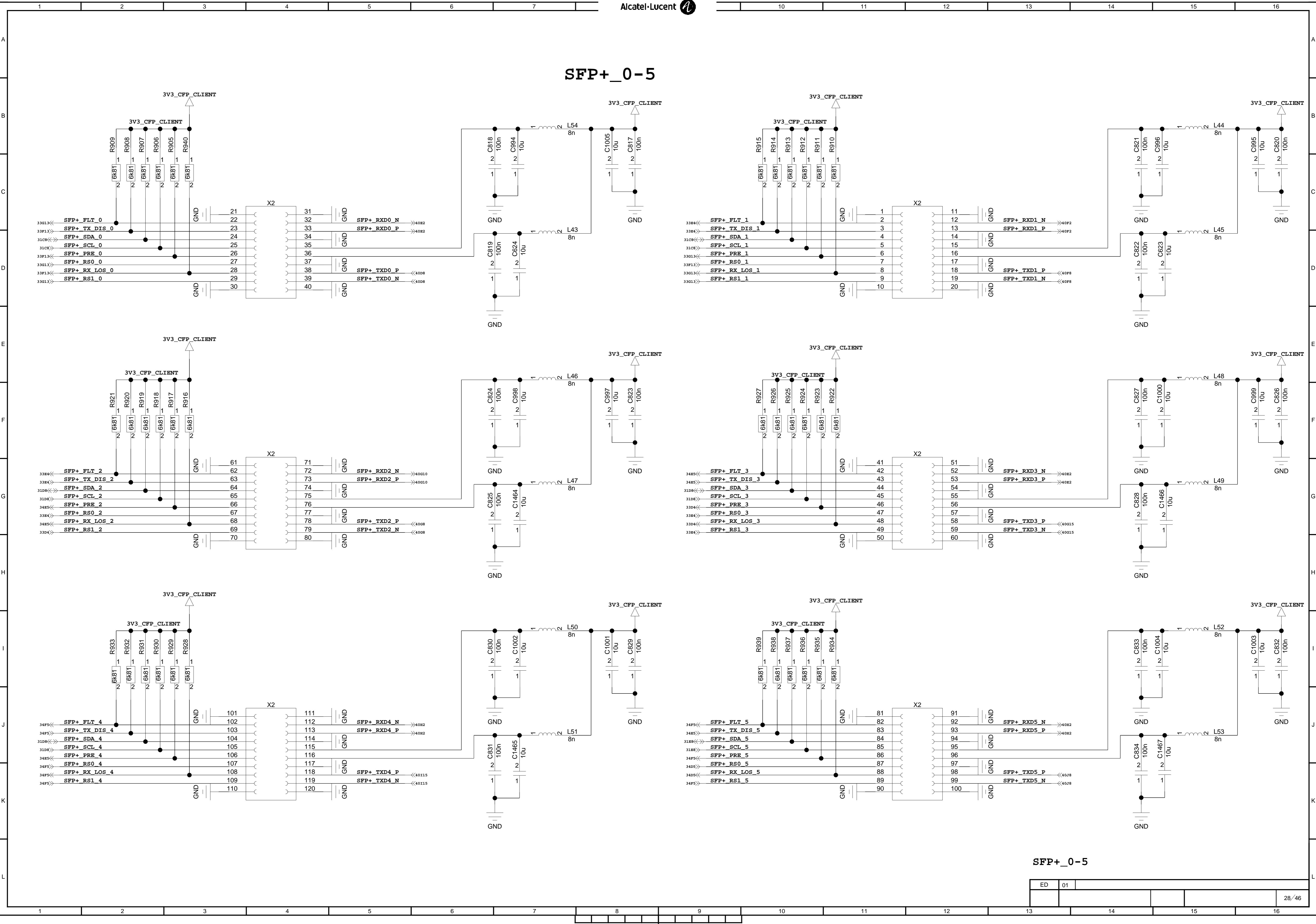
All to be placed
under FF BGA

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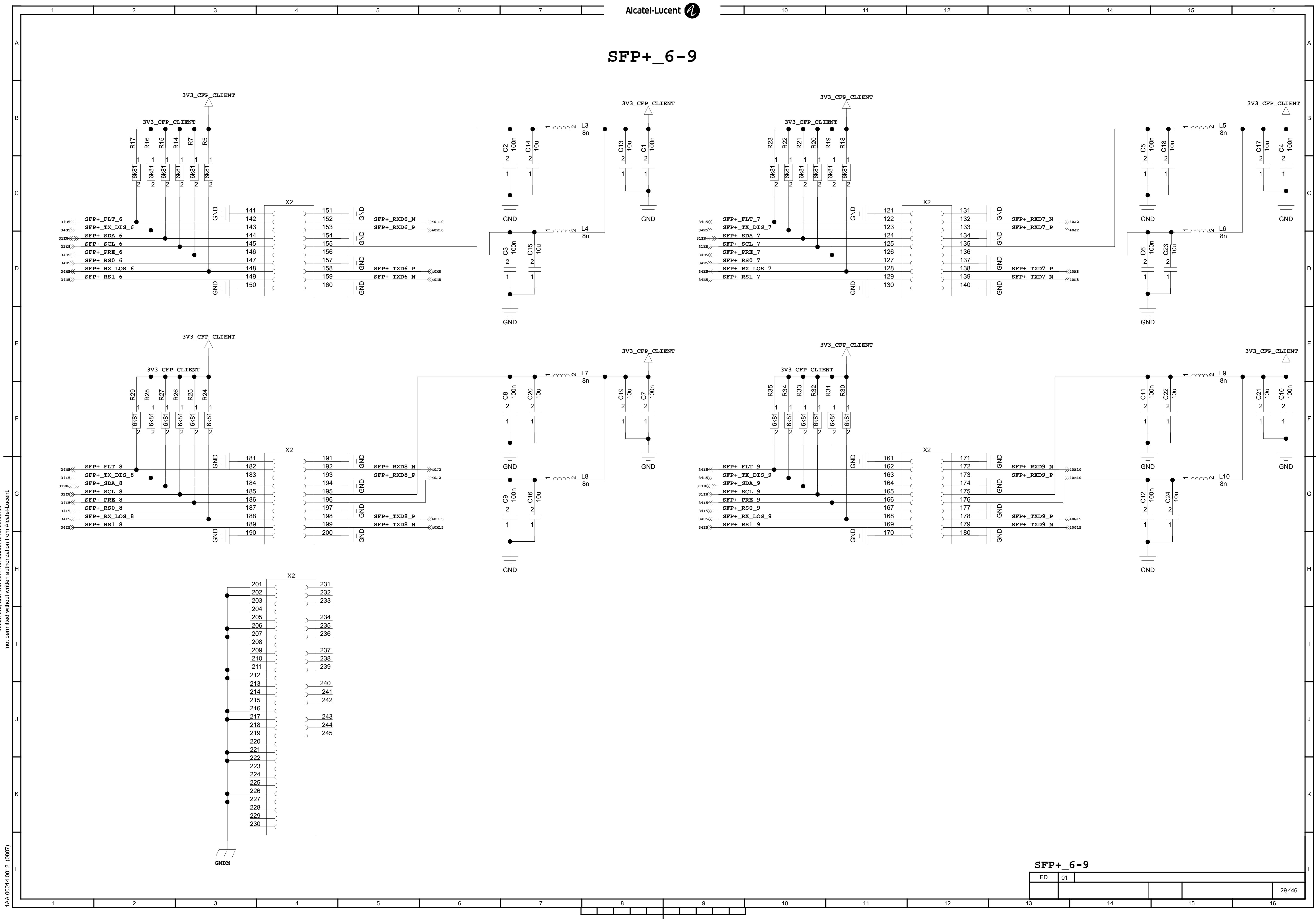
SFP+_0-5

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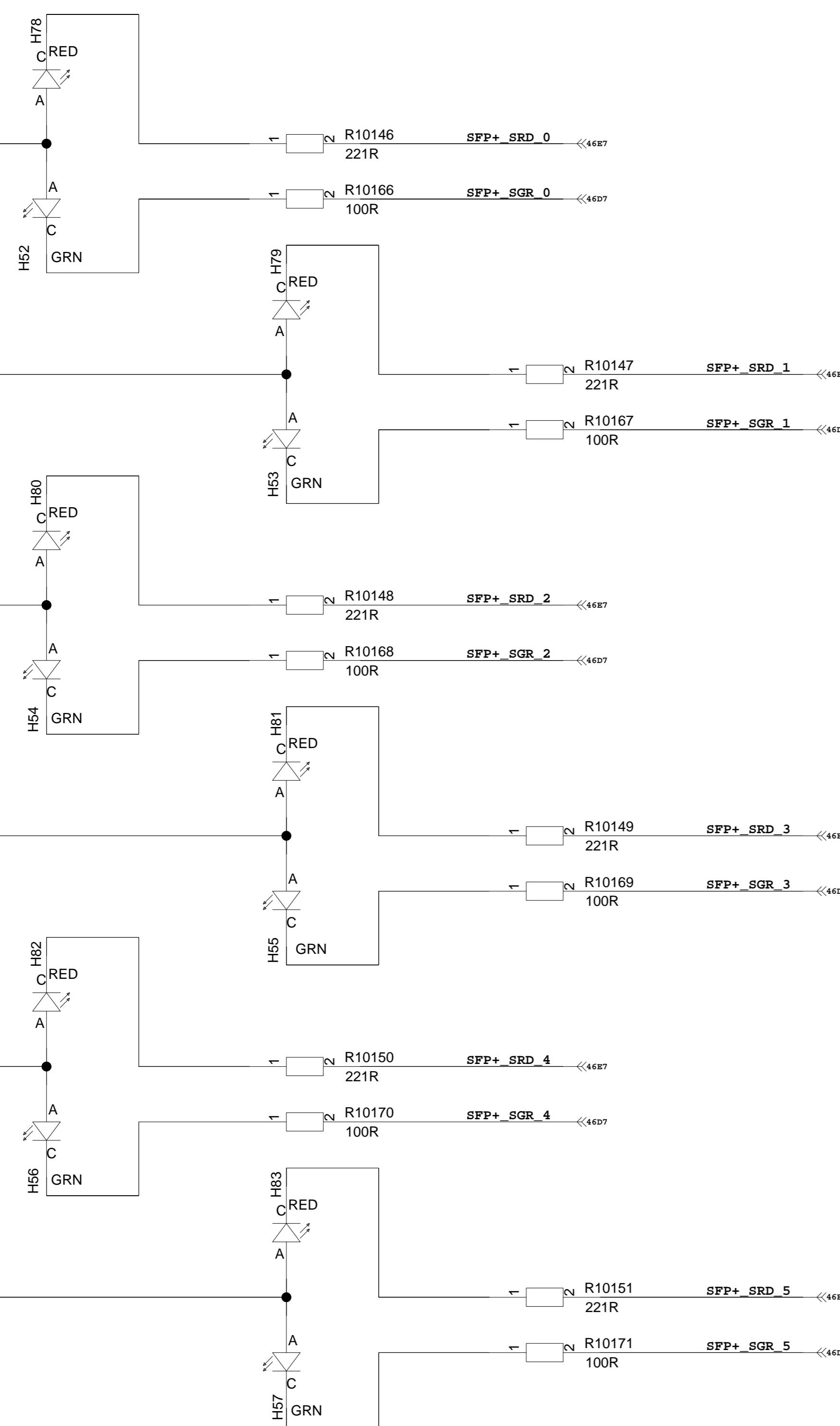
SFP+_0-5

SFP+_6-9

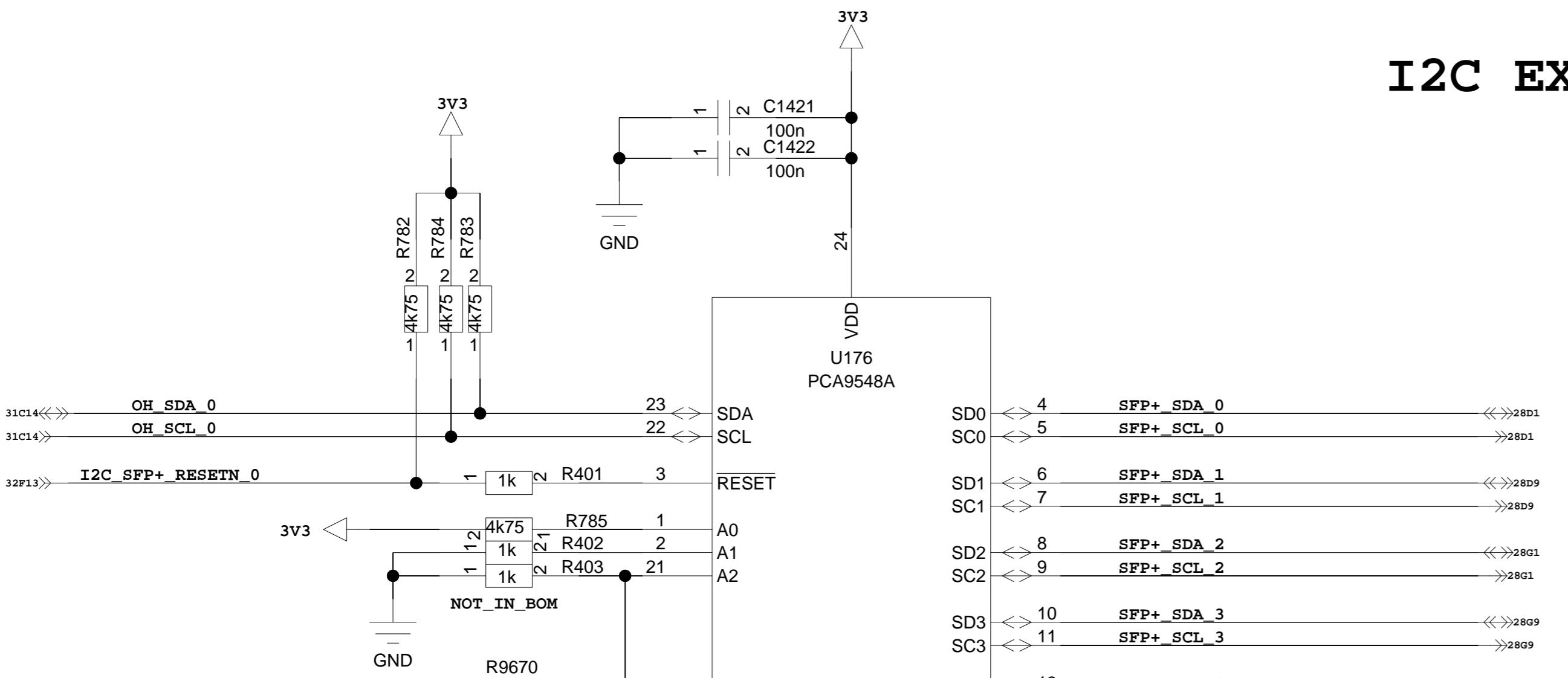


SFP+ LINK/PORT LEDs PART 1

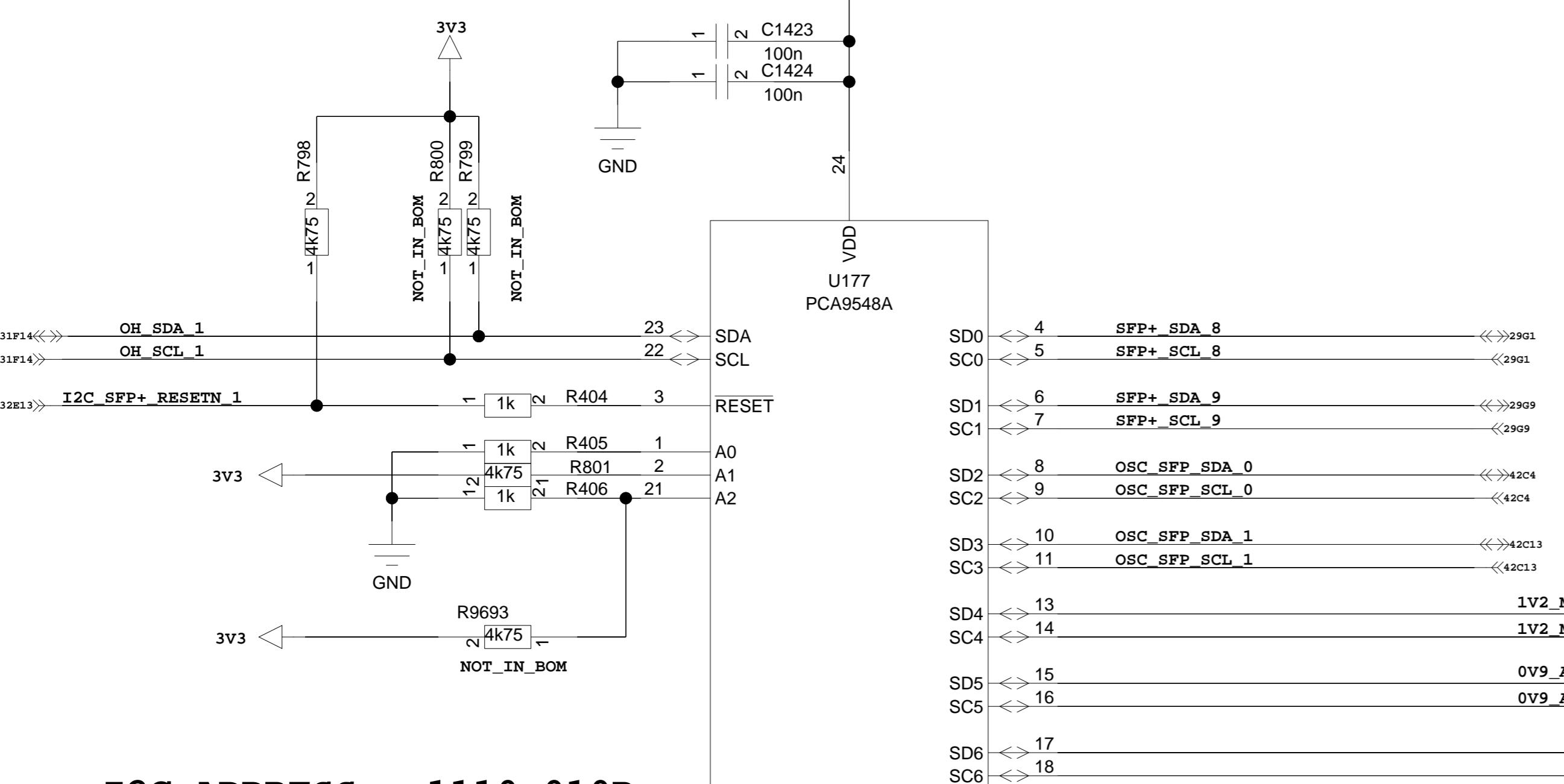
STATUS LEDs



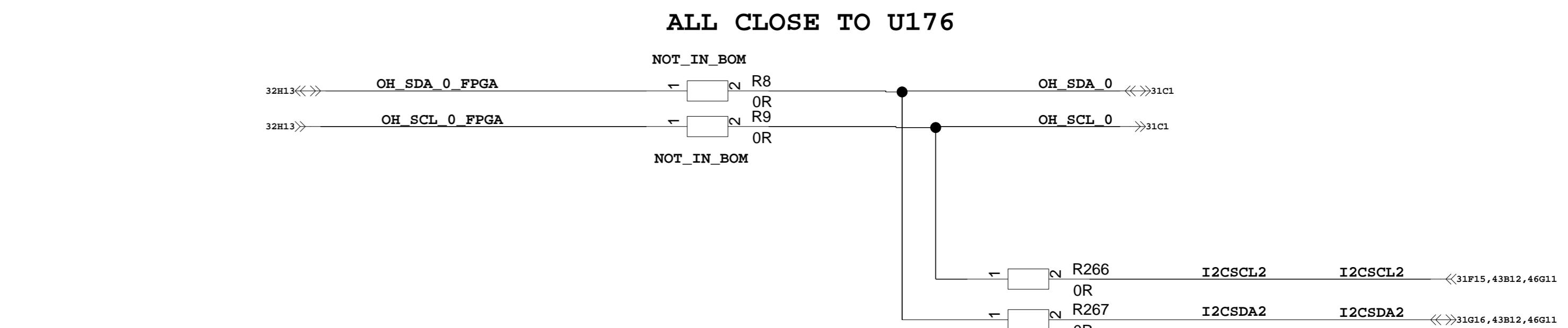
I2C EXPANDERS



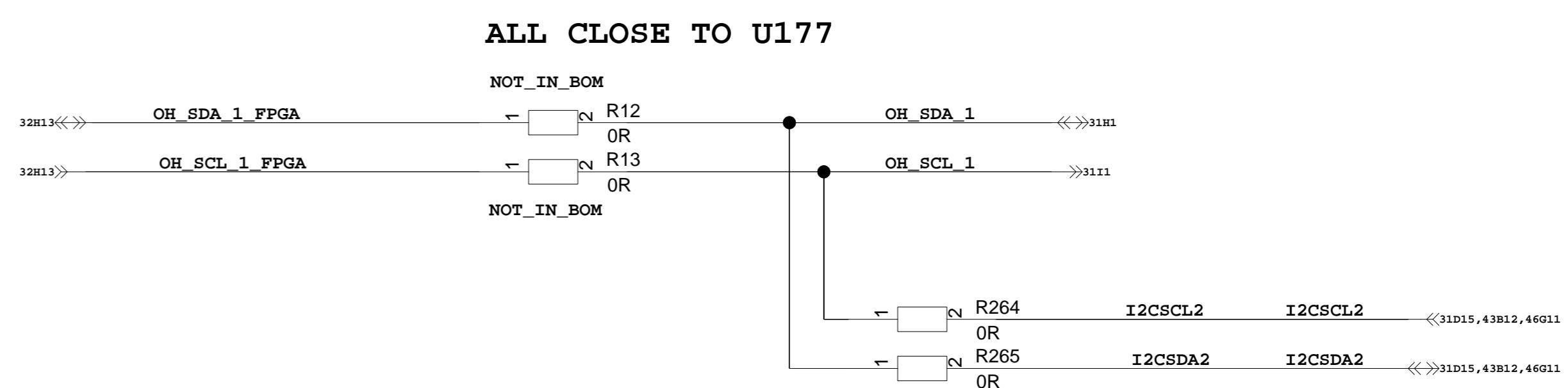
I2C ADDRESS = 1110 101R



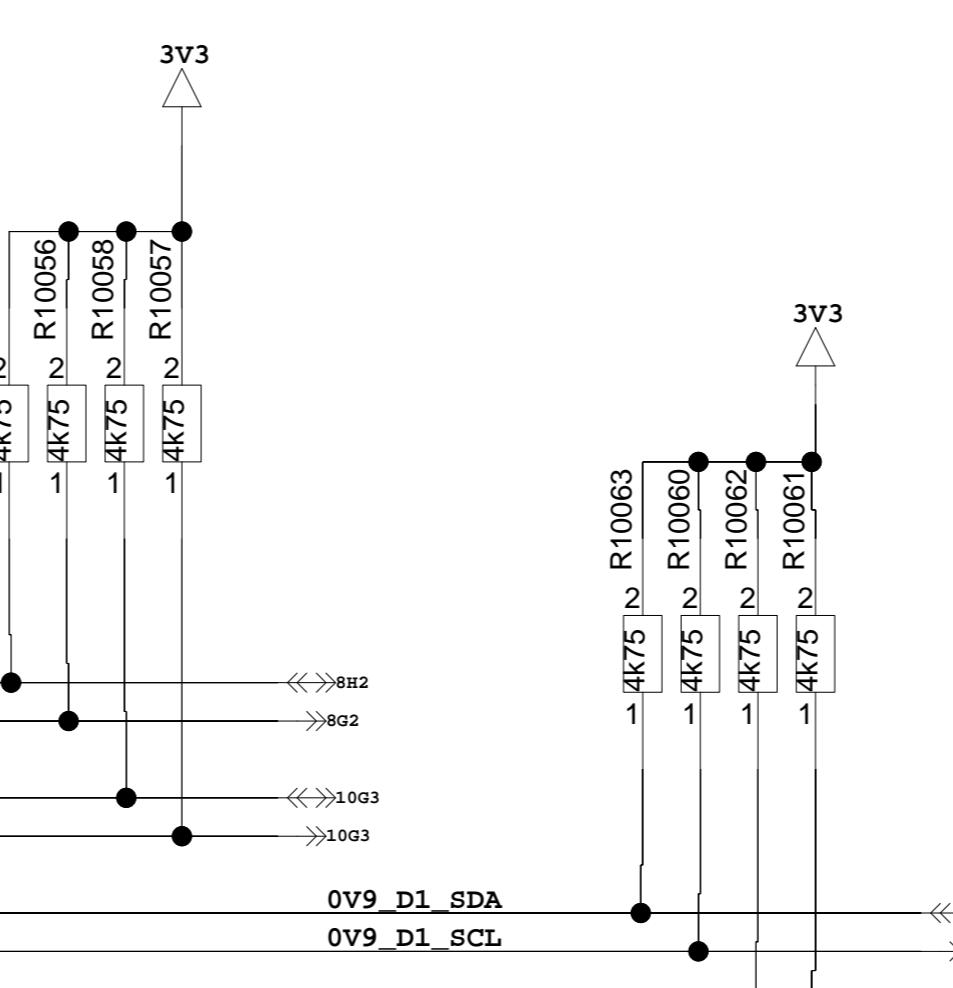
I2C ADDRESS = 1110 010R



ALL CLOSE TO U176



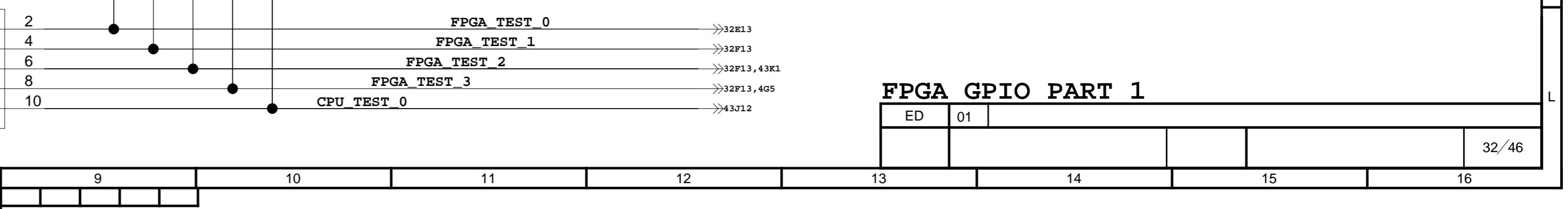
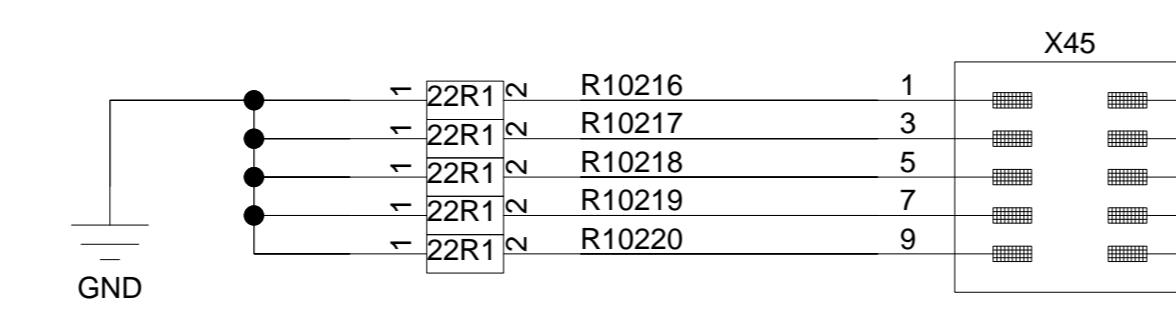
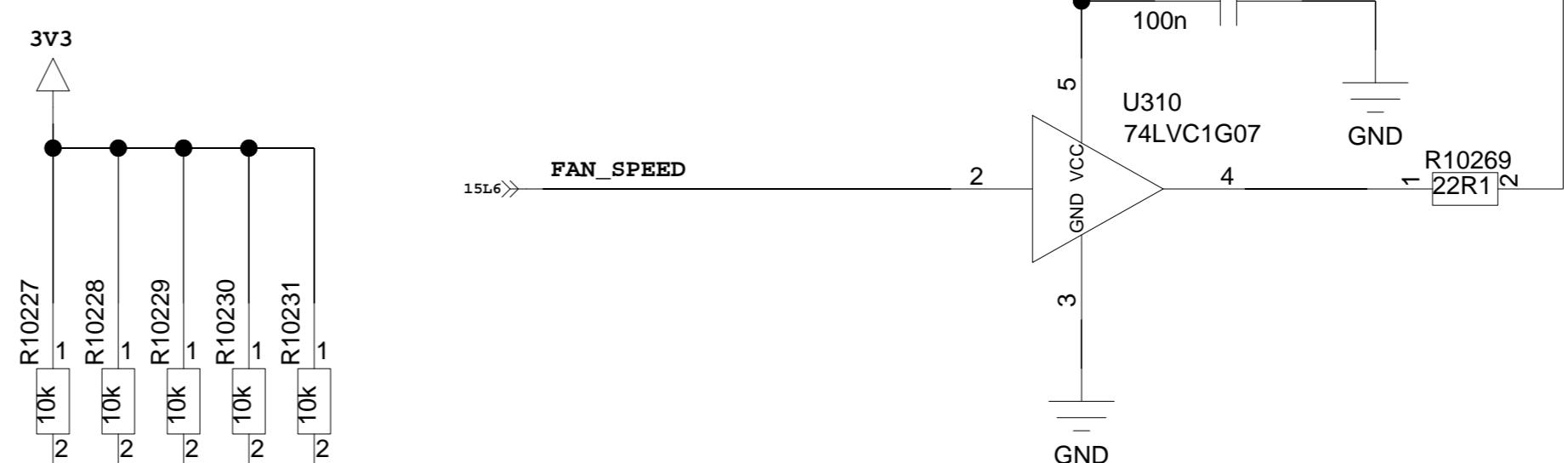
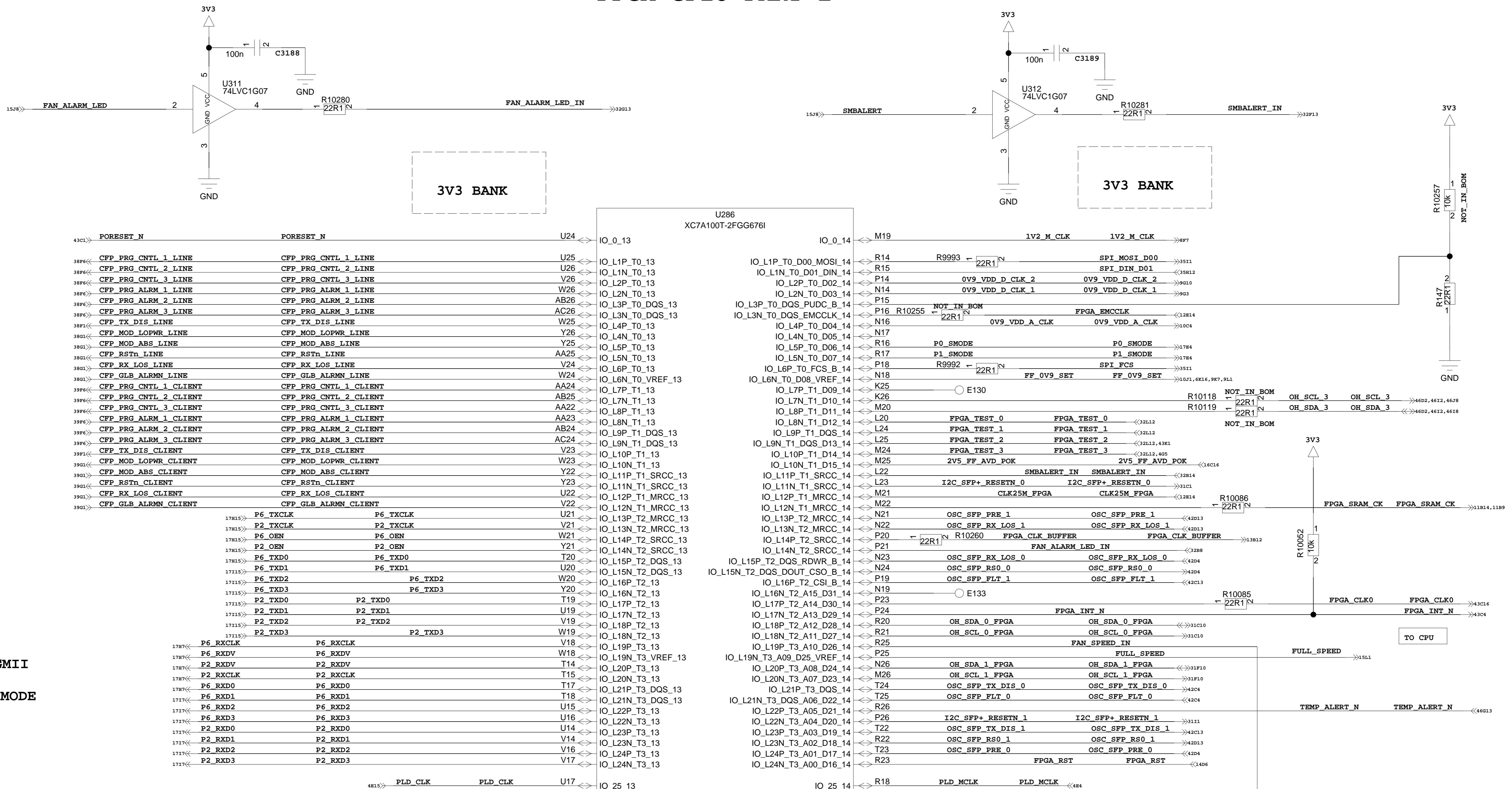
ALL CLOSE TO U177

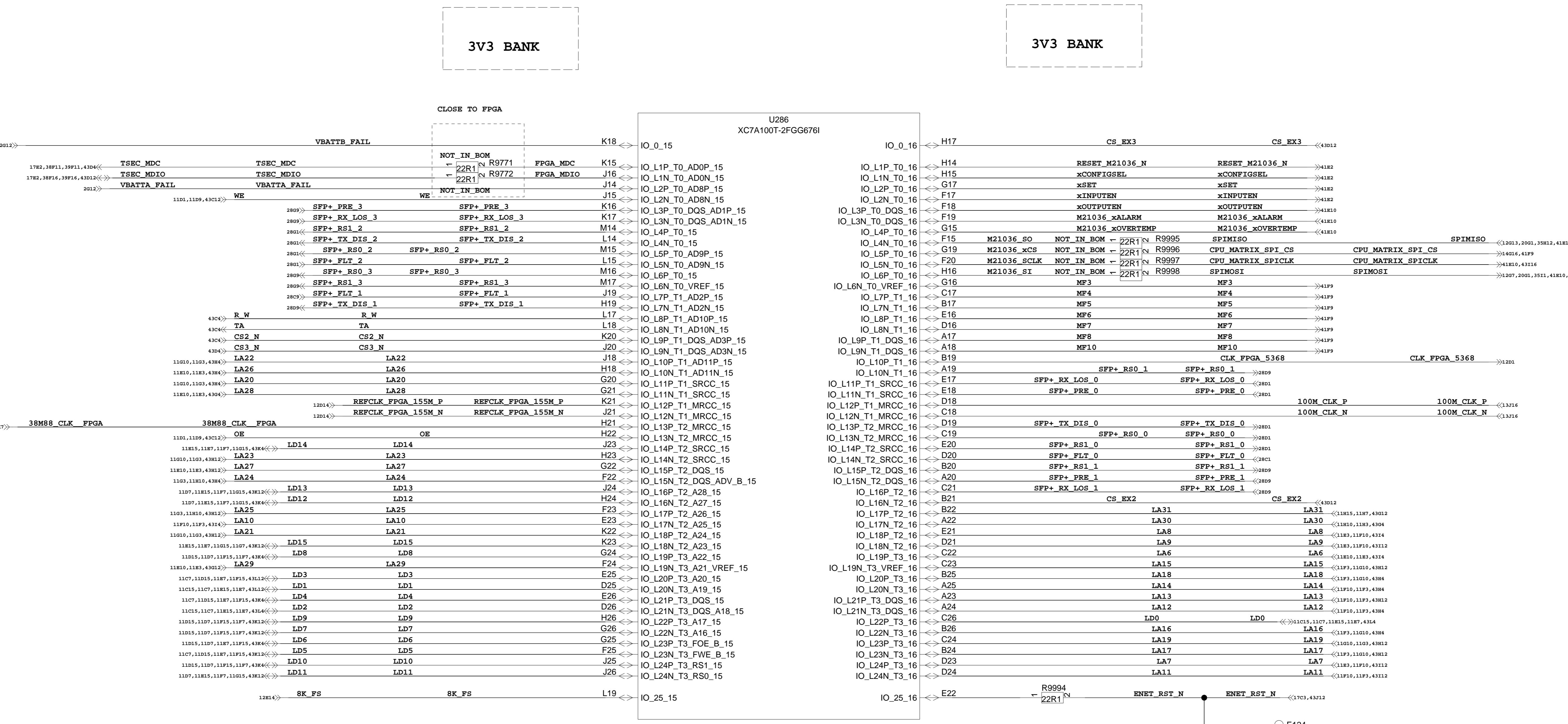


I2C EXPANDERS

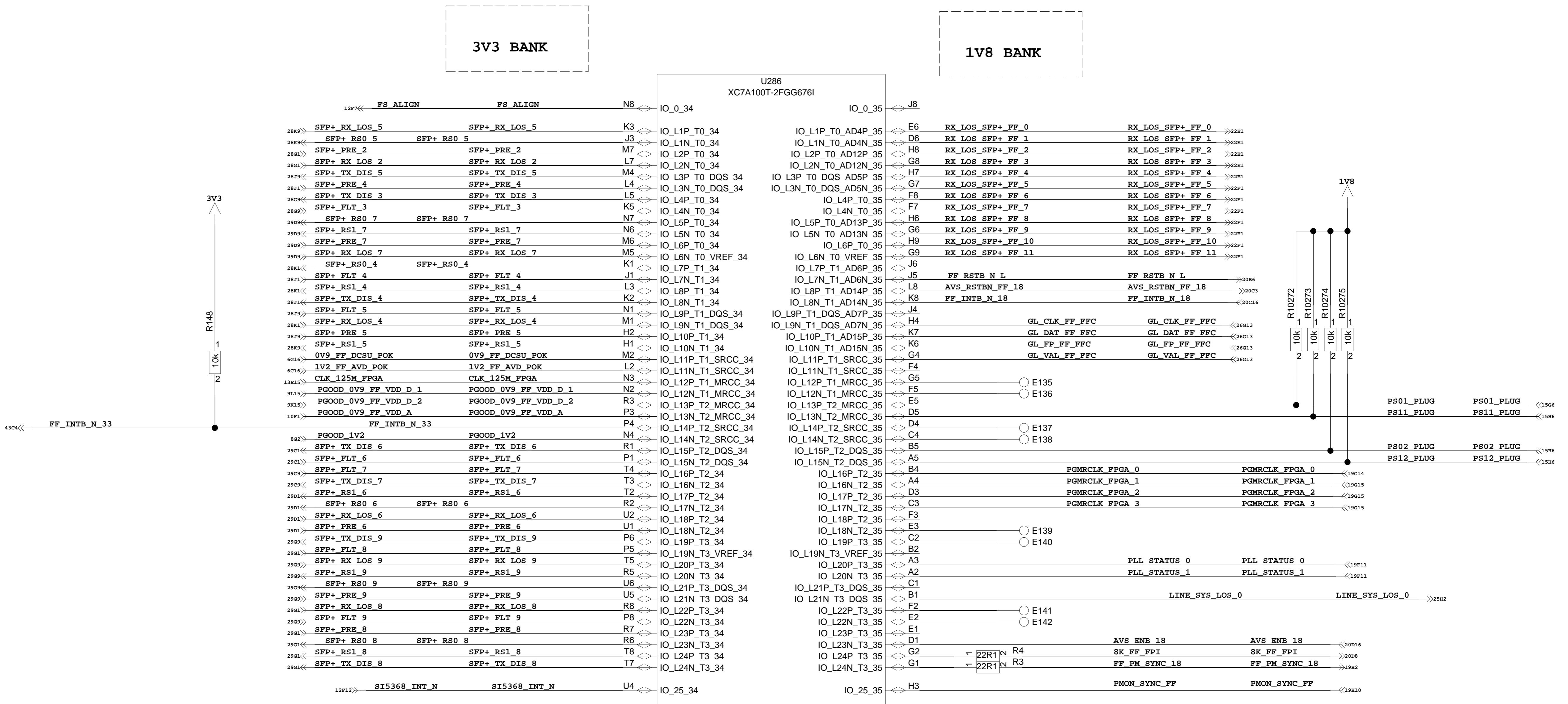
ED	01			
				31/46

FPGA GPIO PART 1

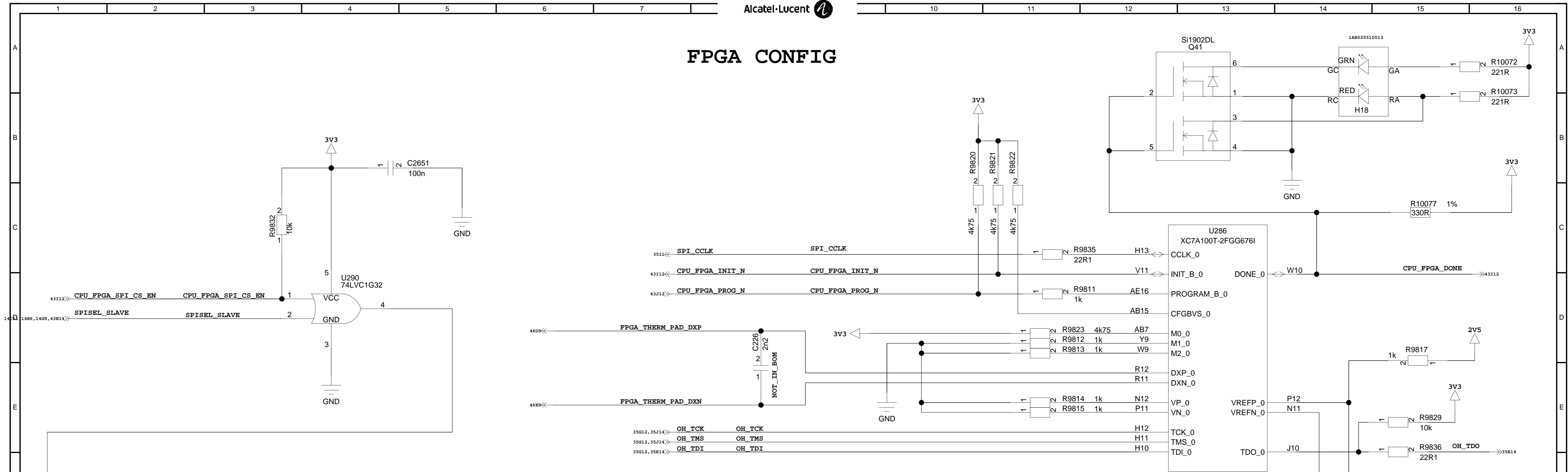




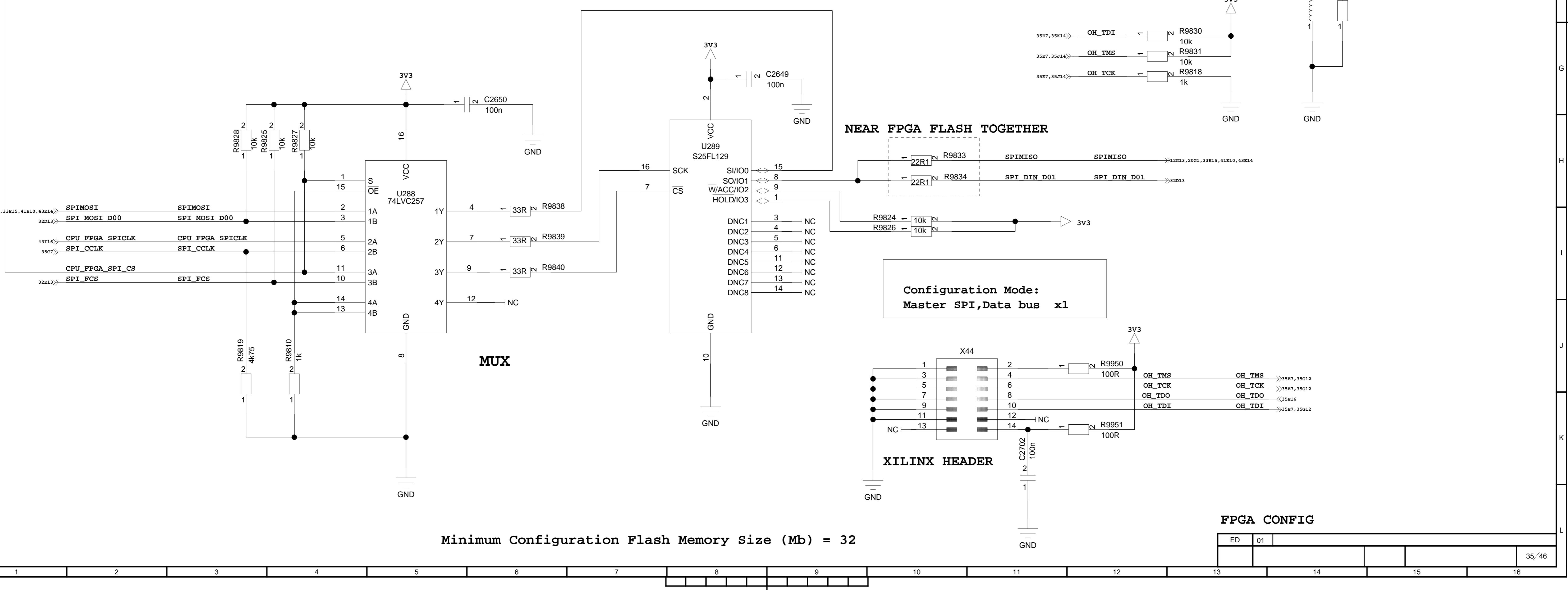
FPGA GPIO PART 3



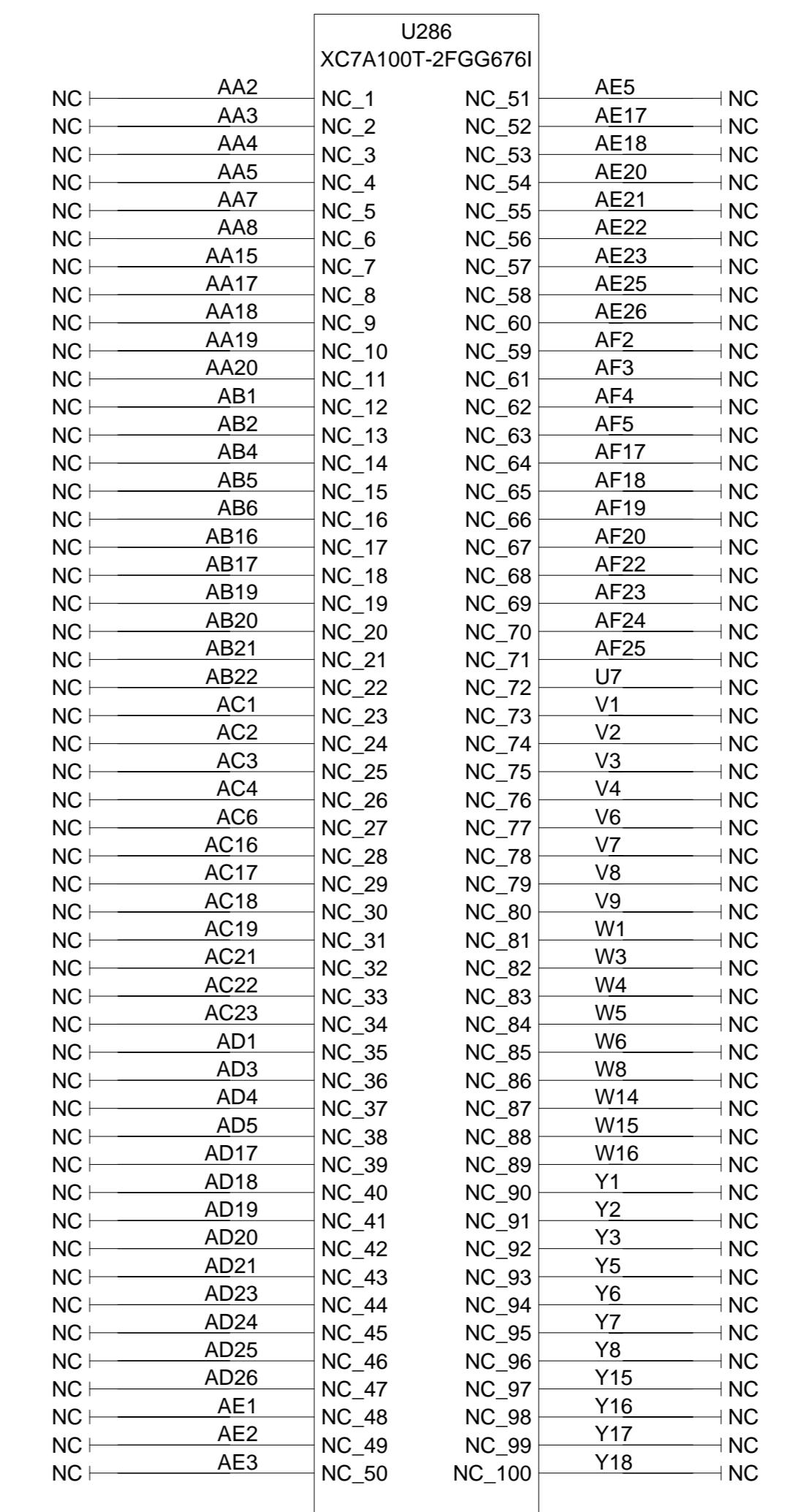
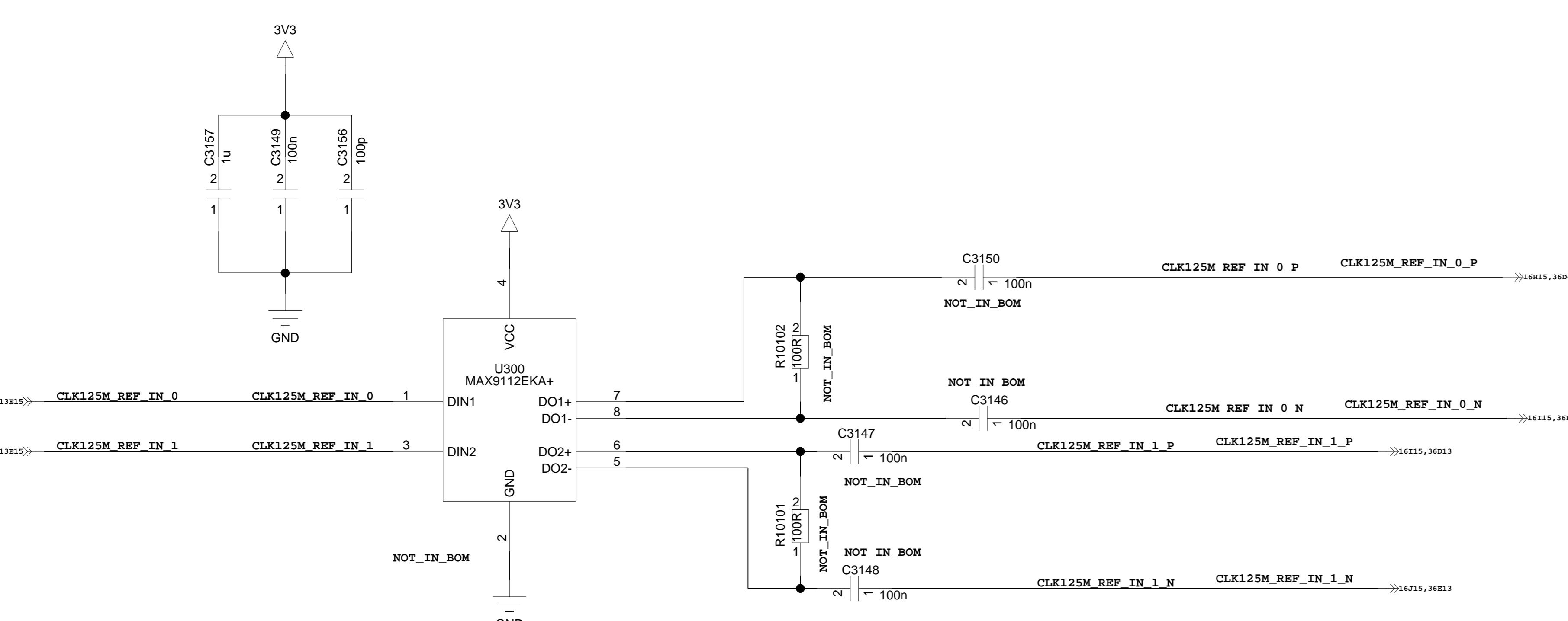
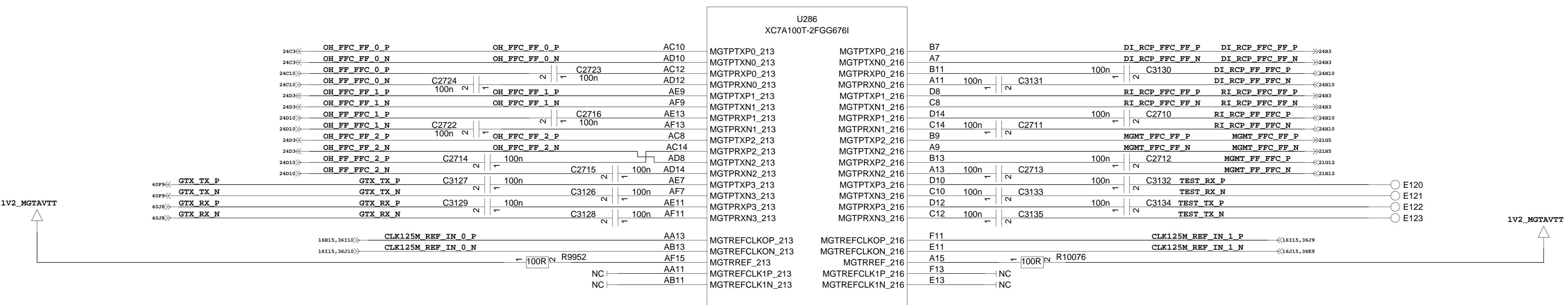
FPGA CONFIG

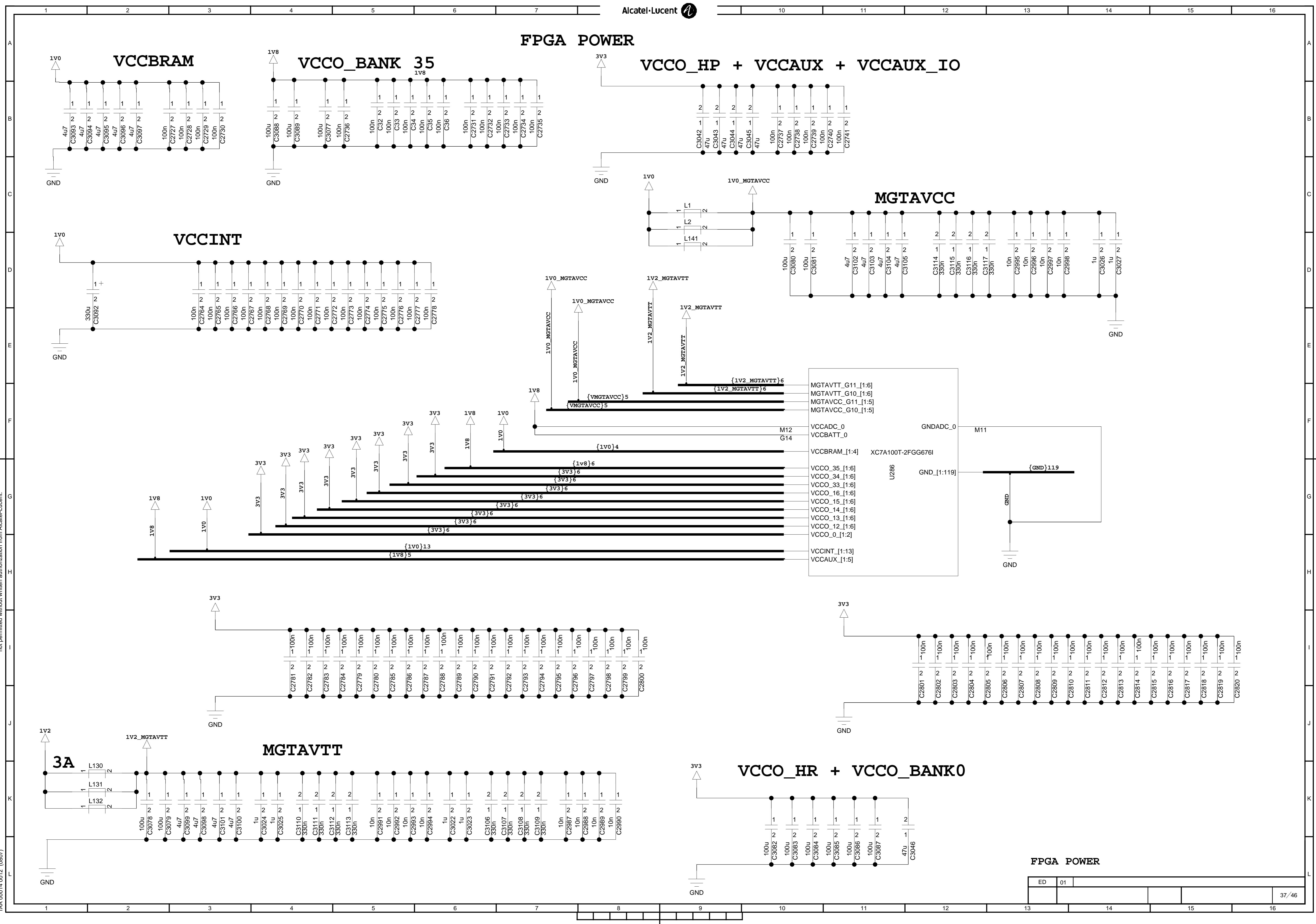


place U288, U289 and U290 close together near U286



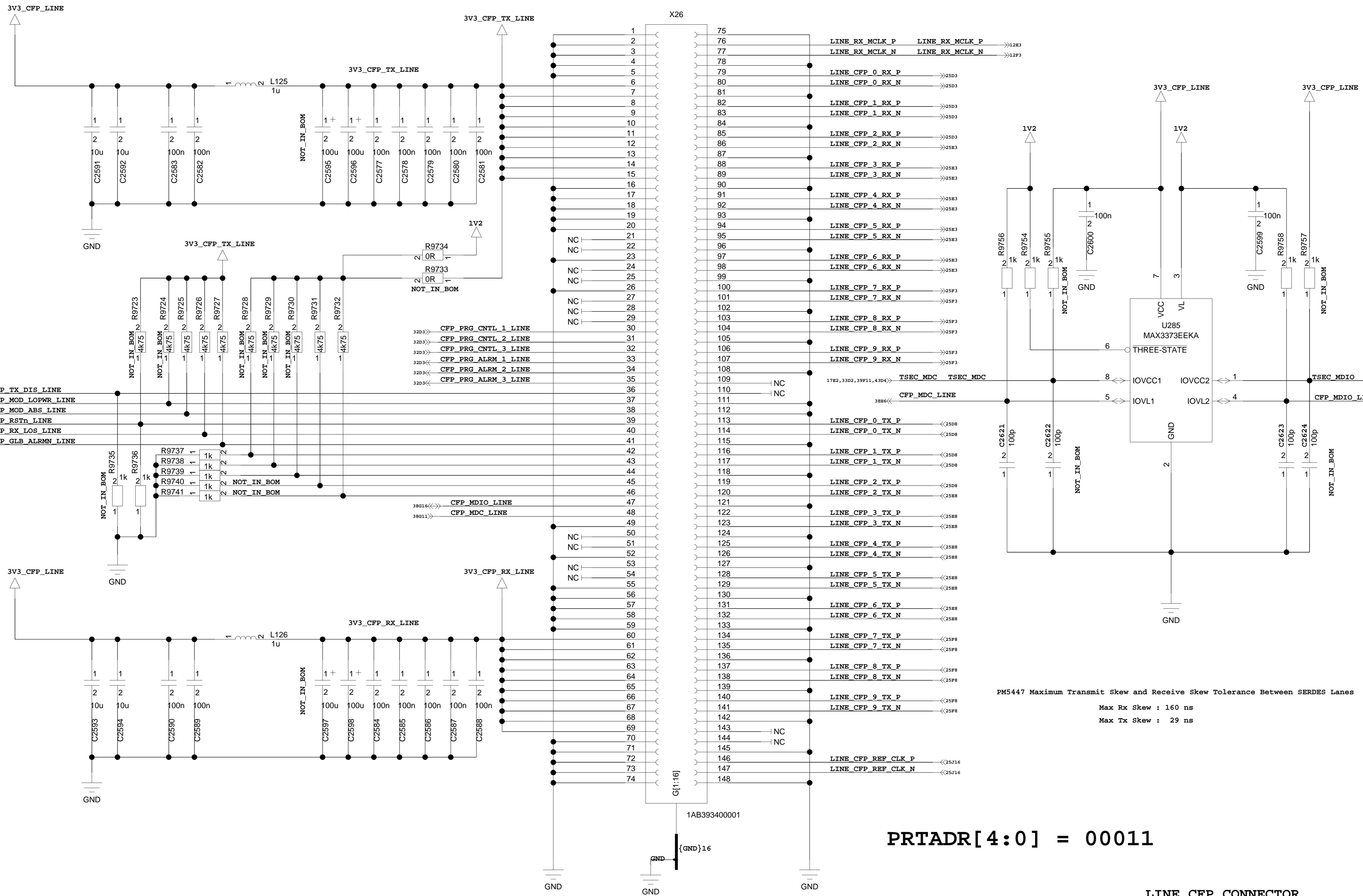
FPGA GTX PORTS





LINE CFP CONNECTOR

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PM5447 Maximum Transmit Skew and Receive Skew Tolerance Between SERDES Lanes

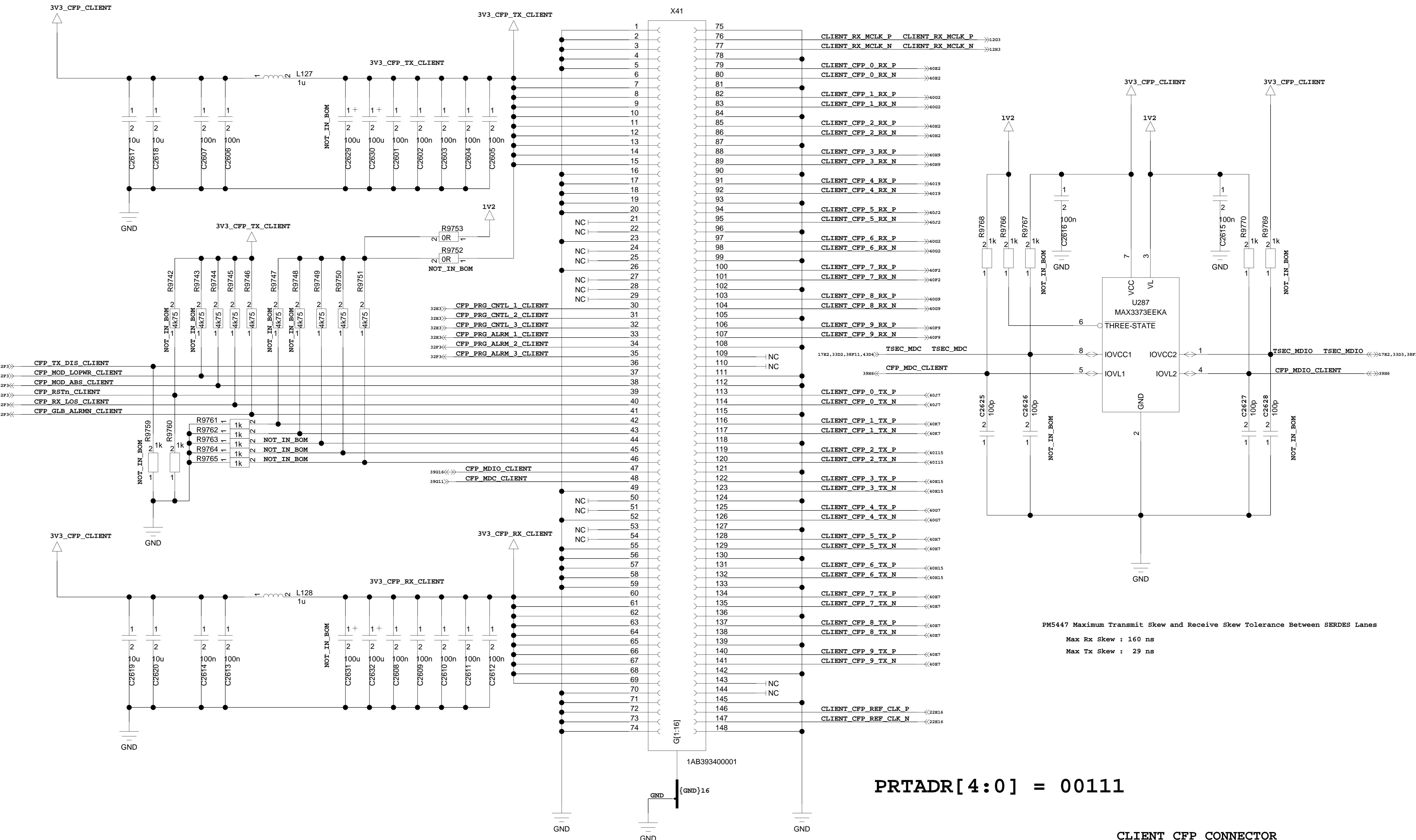
Max Rx Skew : 160 ns
Max Tx Skew : 29 ns

PRTADR[4:0] = 00011

LINE CFP CONNECTOR

CLIENT CFP CONNECTOR

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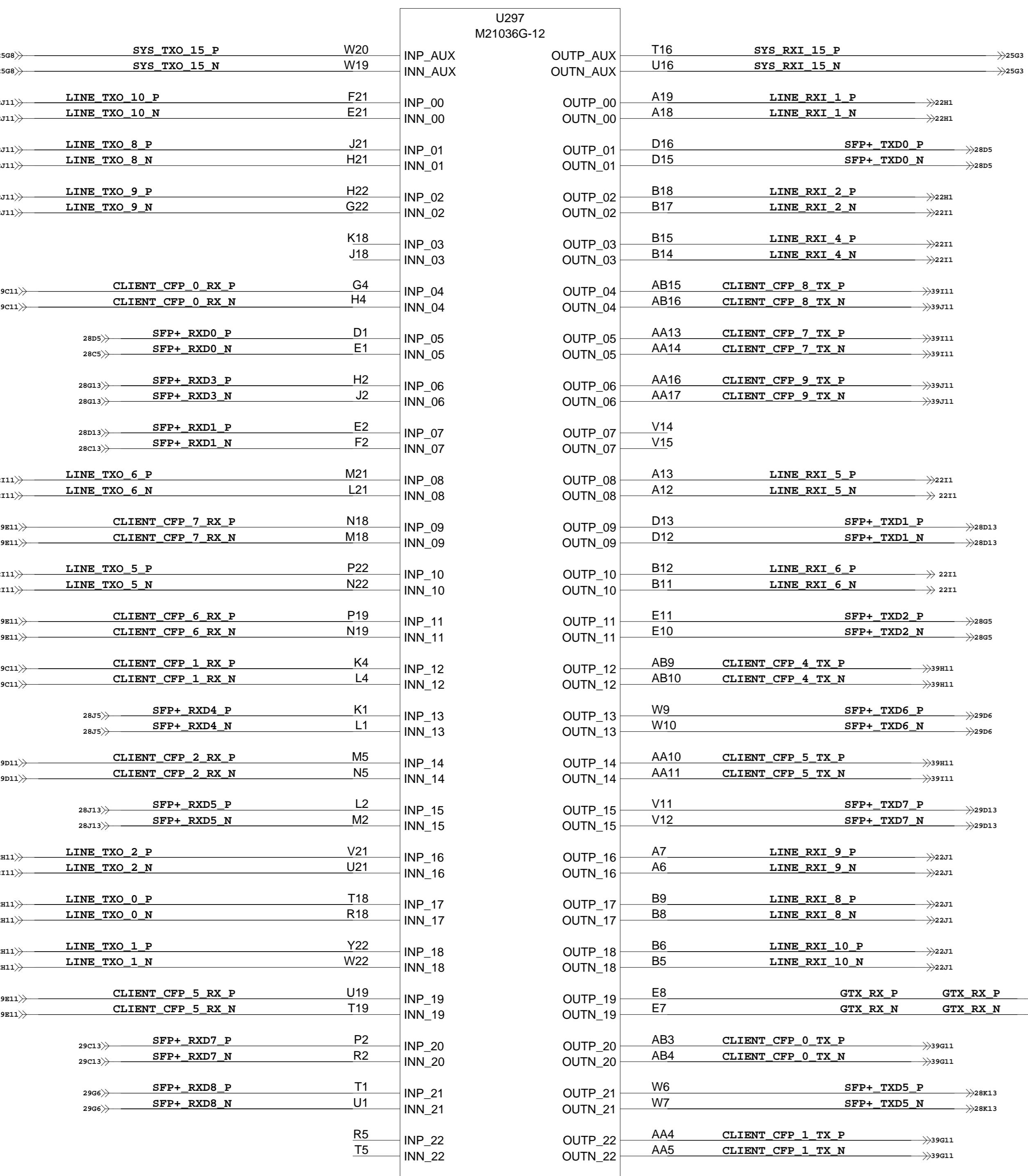


PRTADR[4 : 0] = 00111

CLIENT CFP CONNECTOR

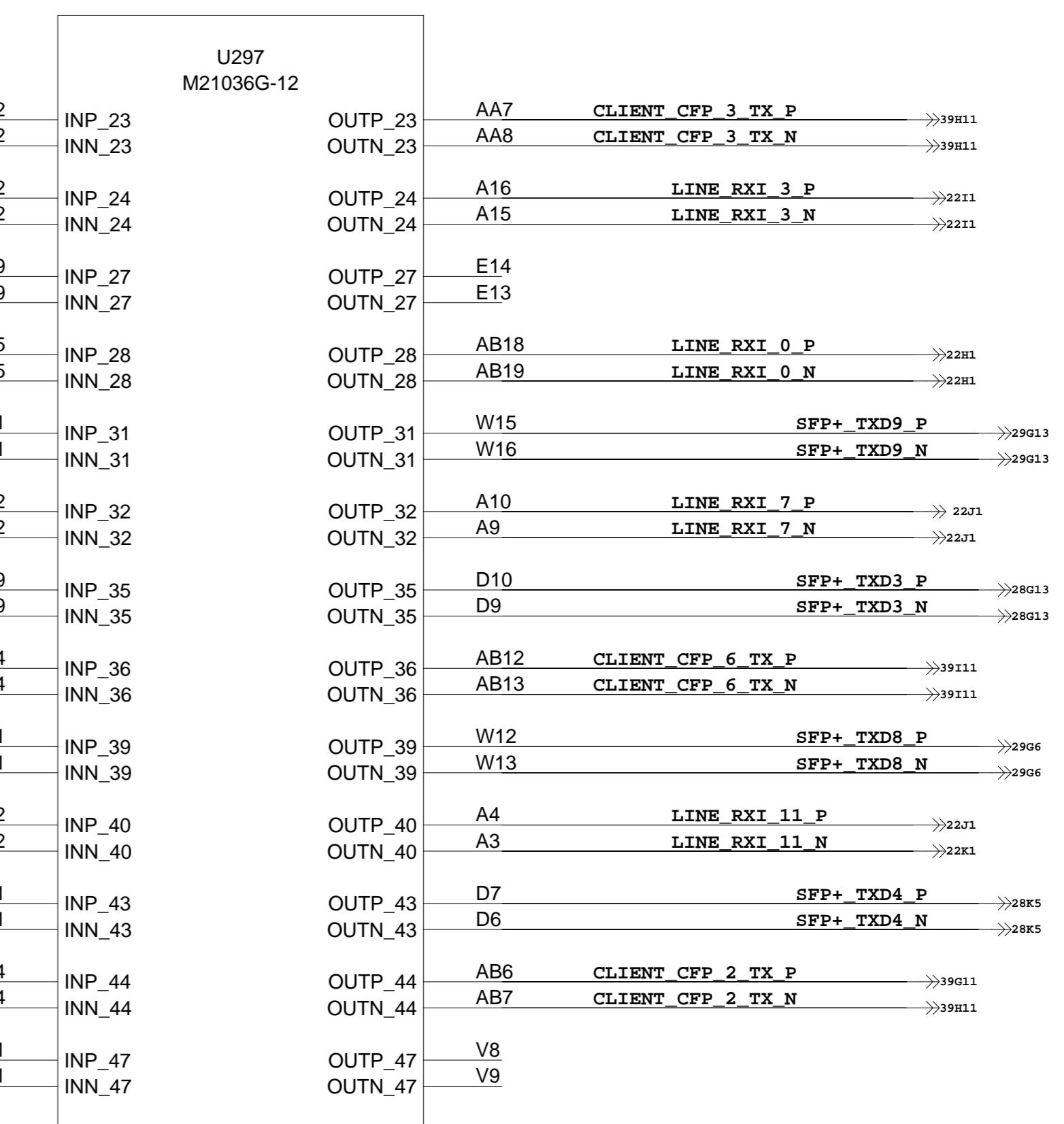
ED	01				39/46

MATRIX XAUI/SYS



RX AC COUPLING FROM PM5447

TX DC COUPLING TO PM5447

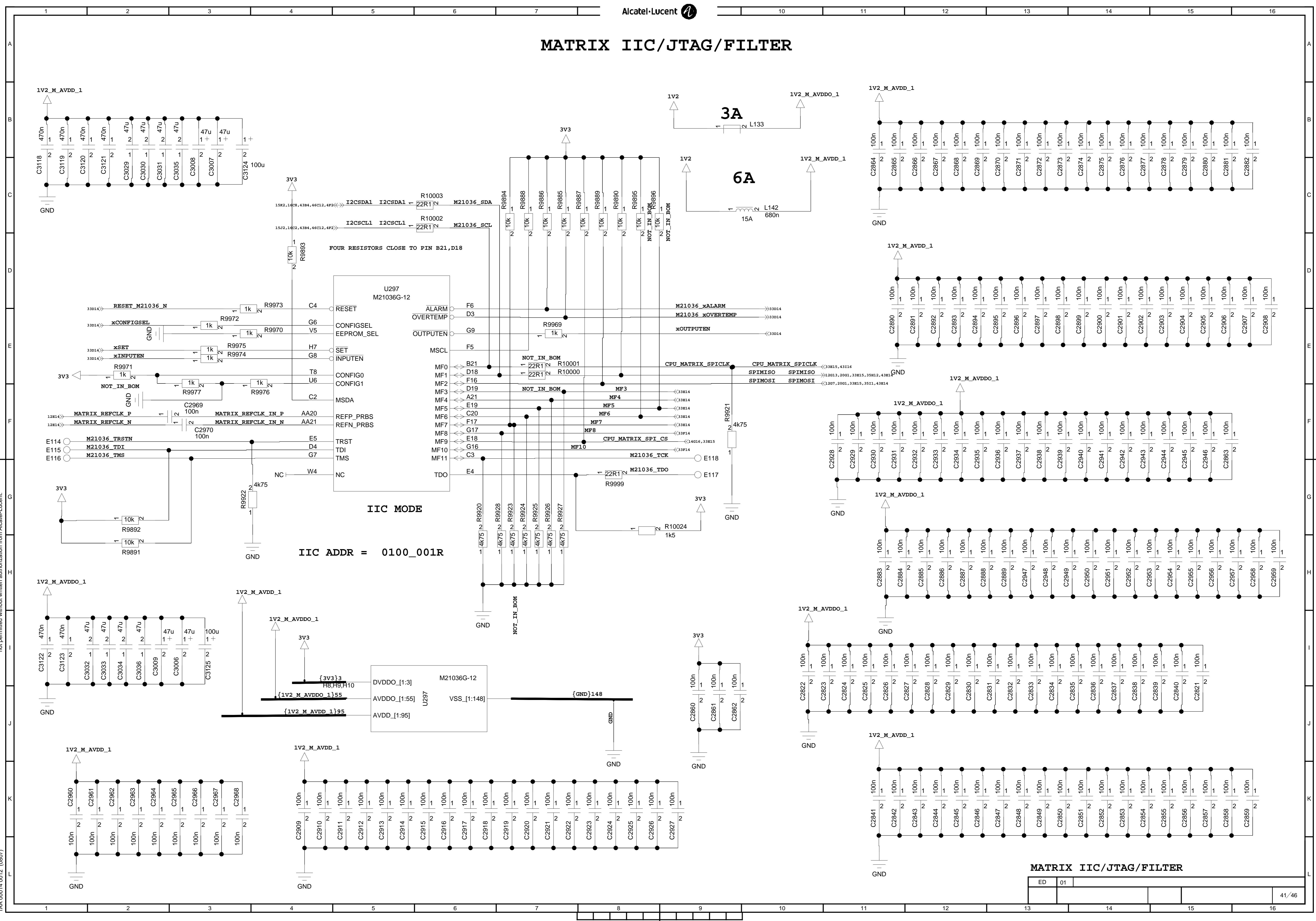


MATRIX XAUI/SYS

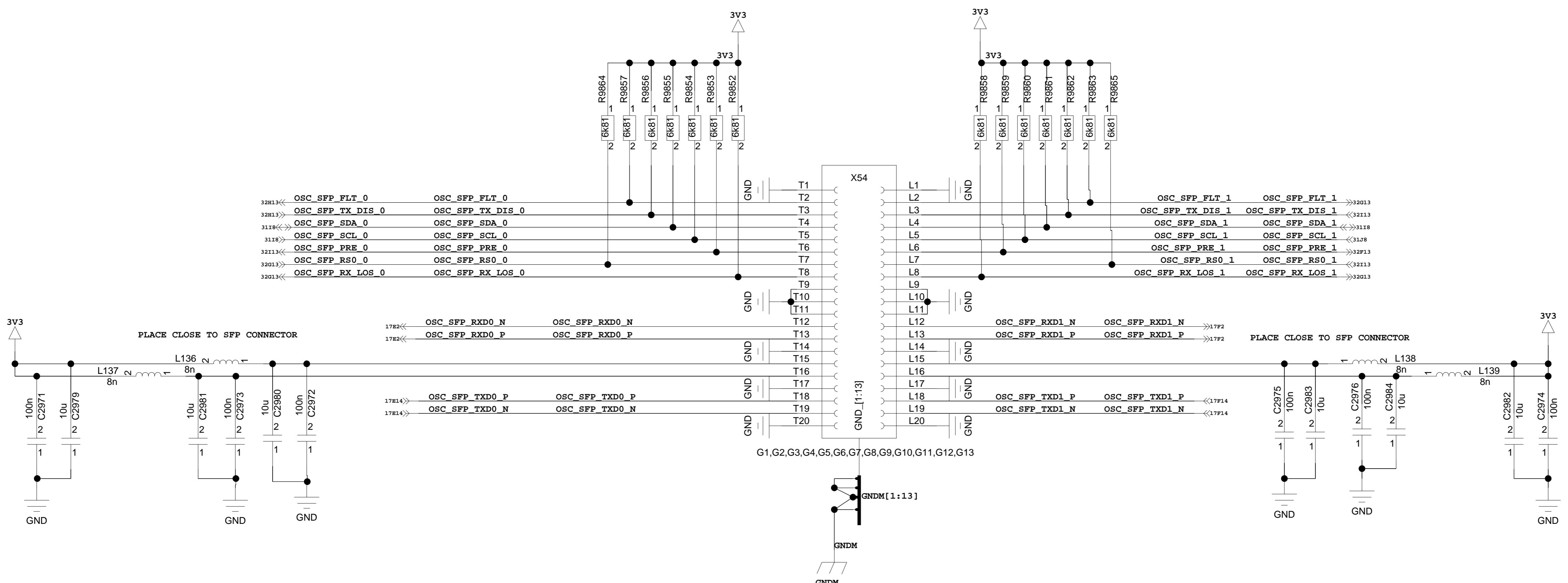
ED	01			
				40/46

MATRIX IIC/JTAG/FILTER

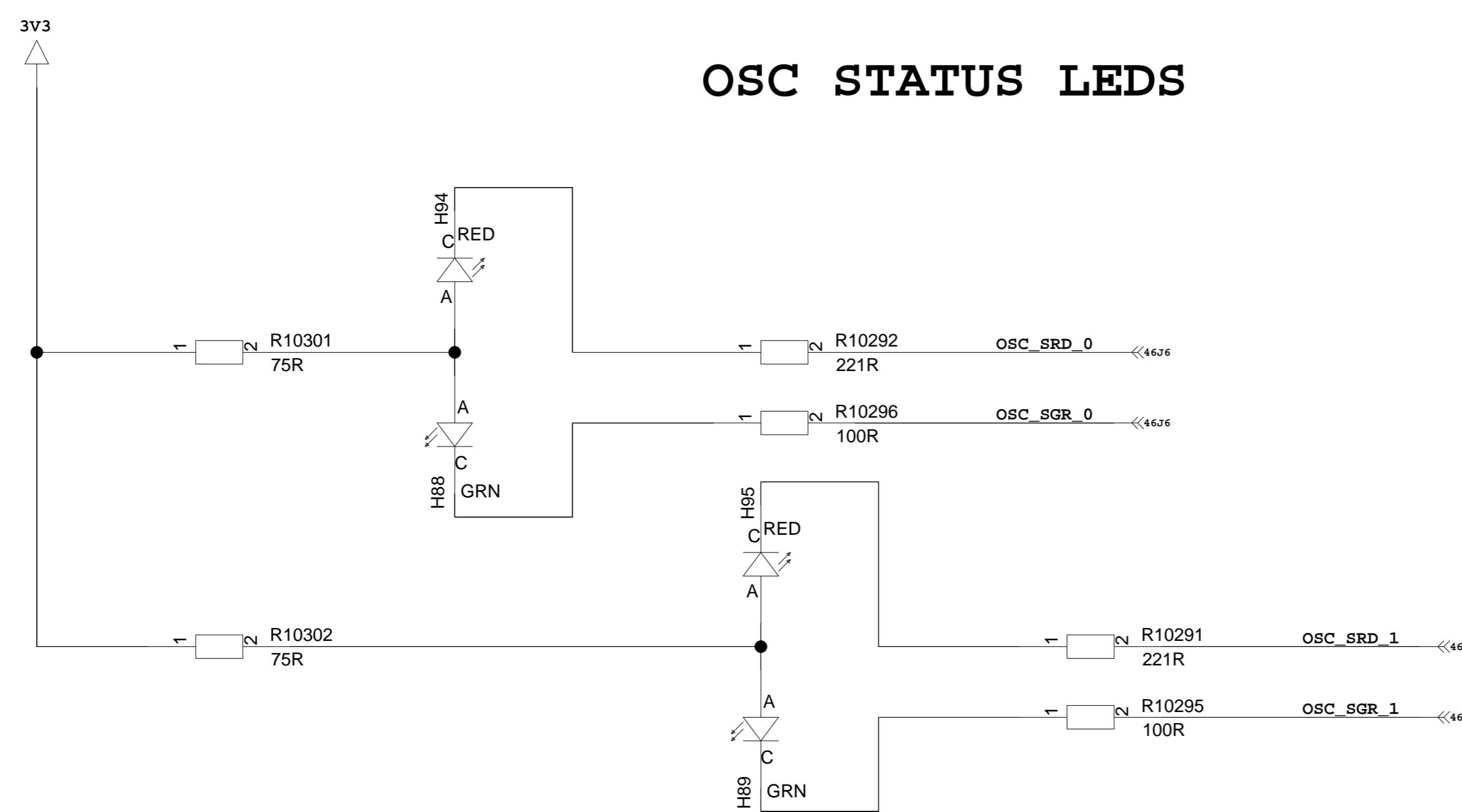
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OSC : 100BASE-FX / 1000BASE-X



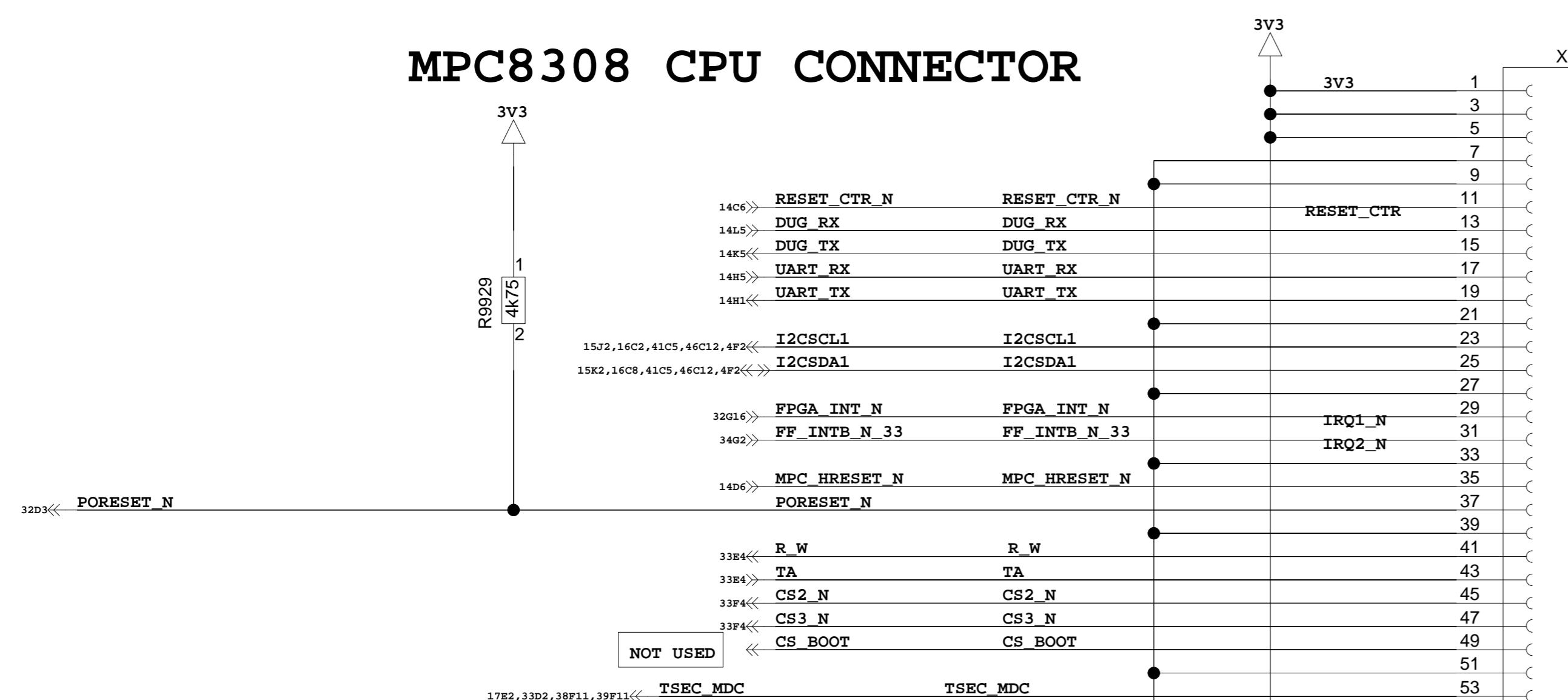
OSC STATUS LEDs



OSC : 100BASE-FX / 1000BASE-X

ED	01			
				42/46

MPC8308 CPU CONNECTOR



CPU with MII MAC mode

NOT USED FOR MII

BACKUP USE

13E15 TSEC2_GTX_CLK125

17E2,33D2,38F11,39F11 P5_TXD3

17H15 P5_TXD2

17H15 P5_TXD1

17G15 P5_TXD0

17G15 P5_RXCLK

17G15 P5_RXCLK

44D15 CPU_LAN_RX_N

44D15 CPU_LAN_RX_P

44D15 CPU_LAN_RX_N

44D15 CPU_LAN_RX_P

2V5 2V5

R80 OR

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

GND GND

3V3 3V3

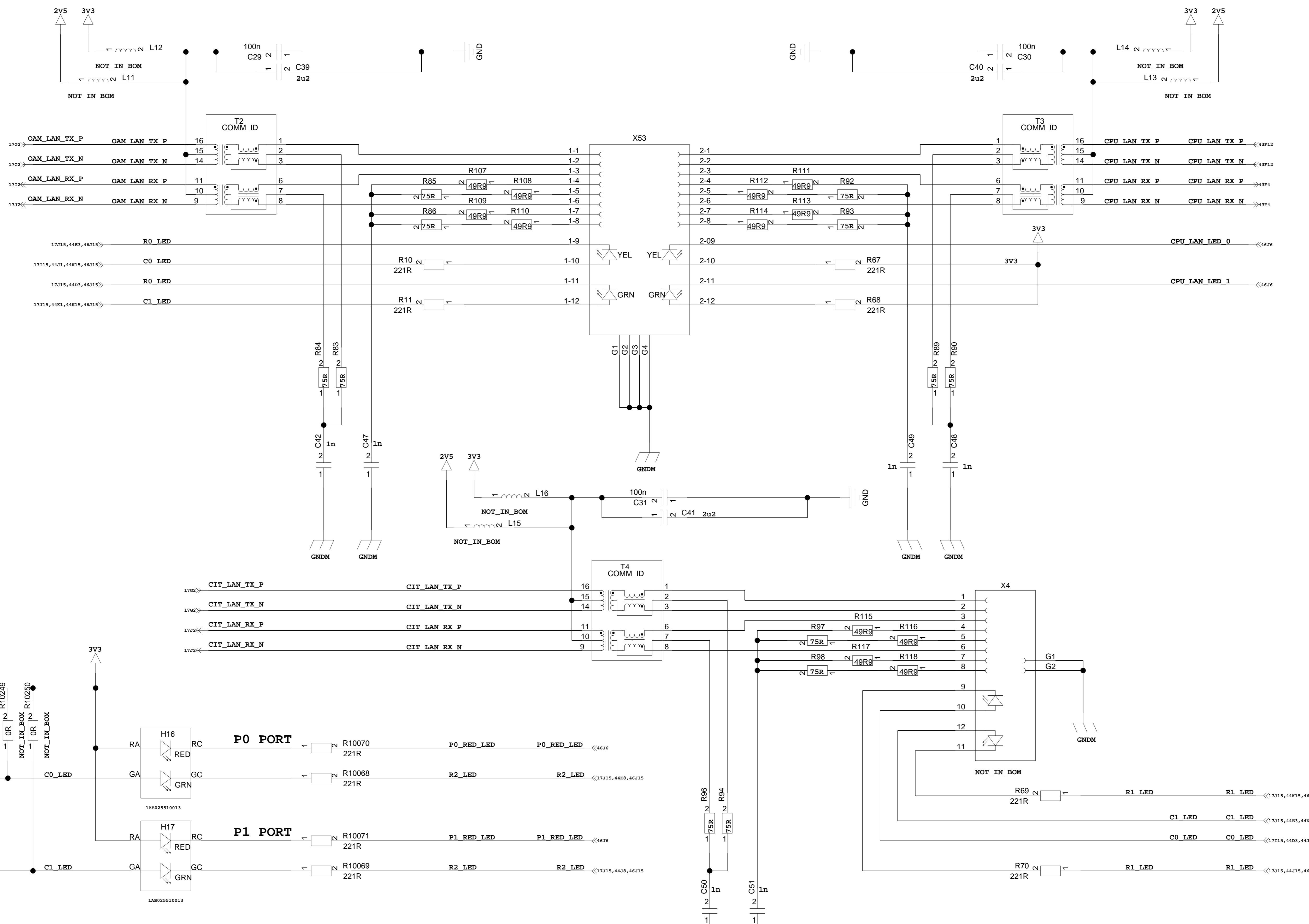
NOT_IN_BOM NOT_IN_BOM

GND GND

100n 100n

NOT_IN_BOM NOT_IN_BOM

RJ45 CONNECTOR

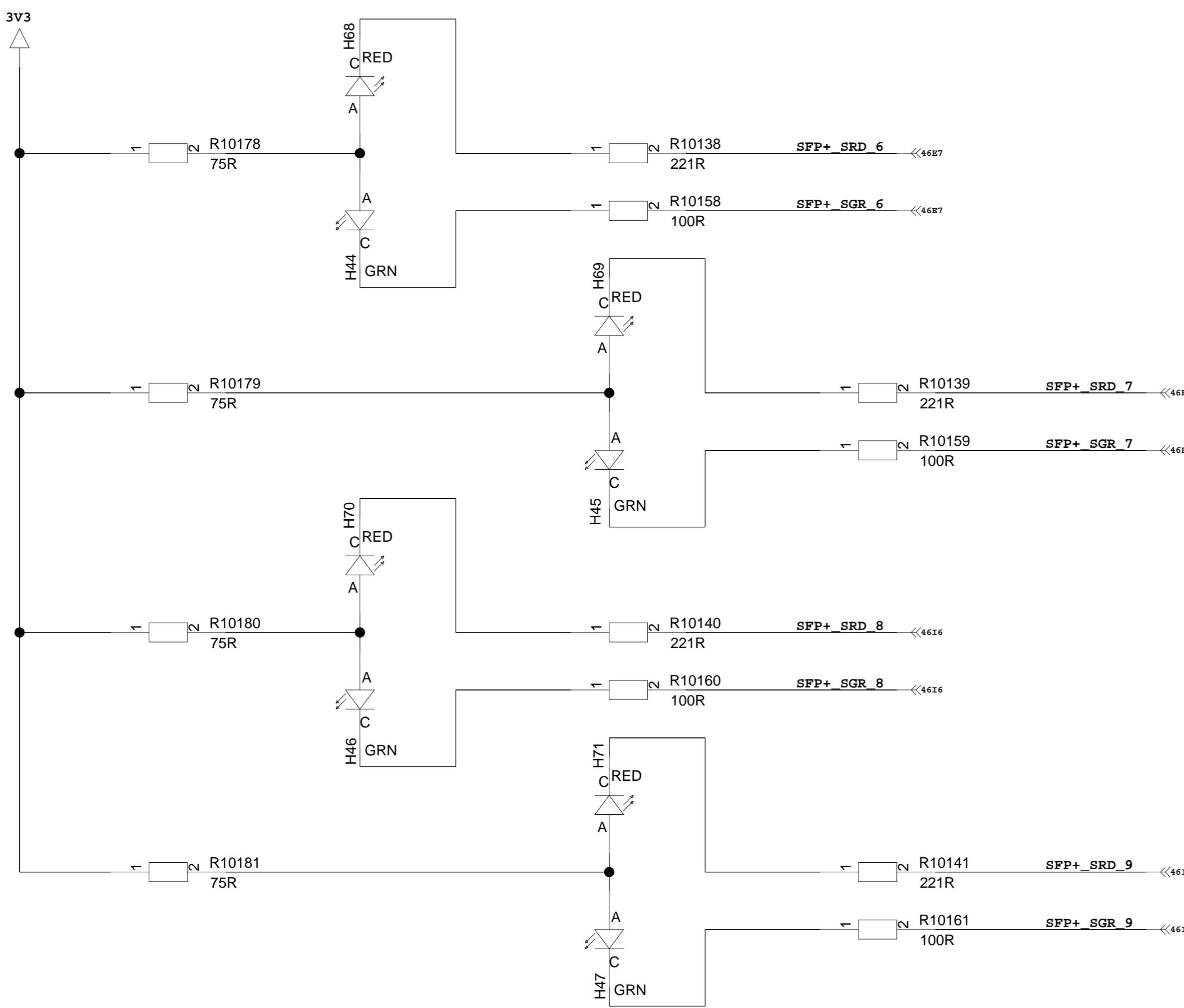


RJ45 CONNECTOR

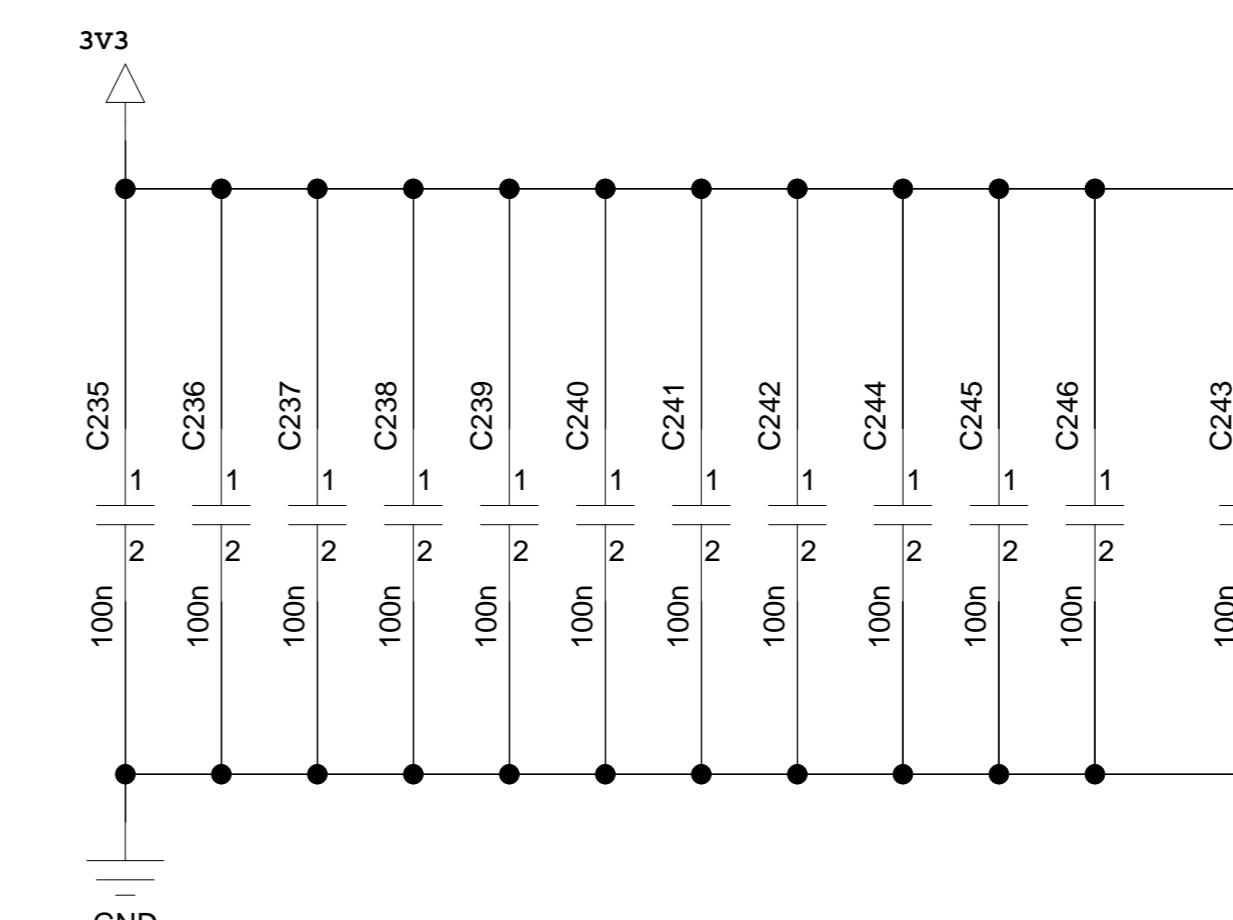
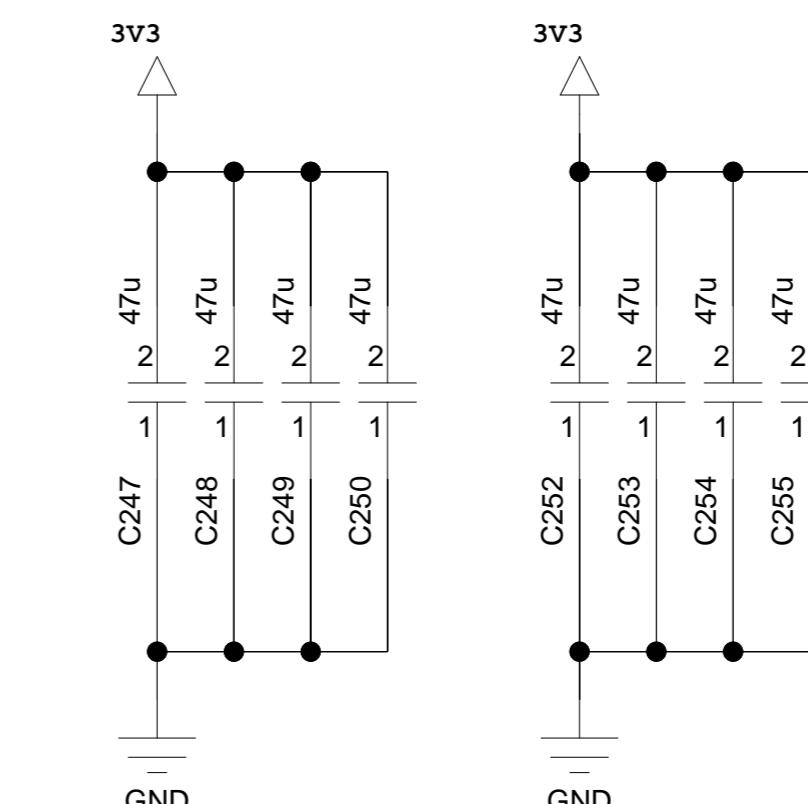
ED 01 | 44/46 L

SFP+ LINK/PORT LEDS PART 2

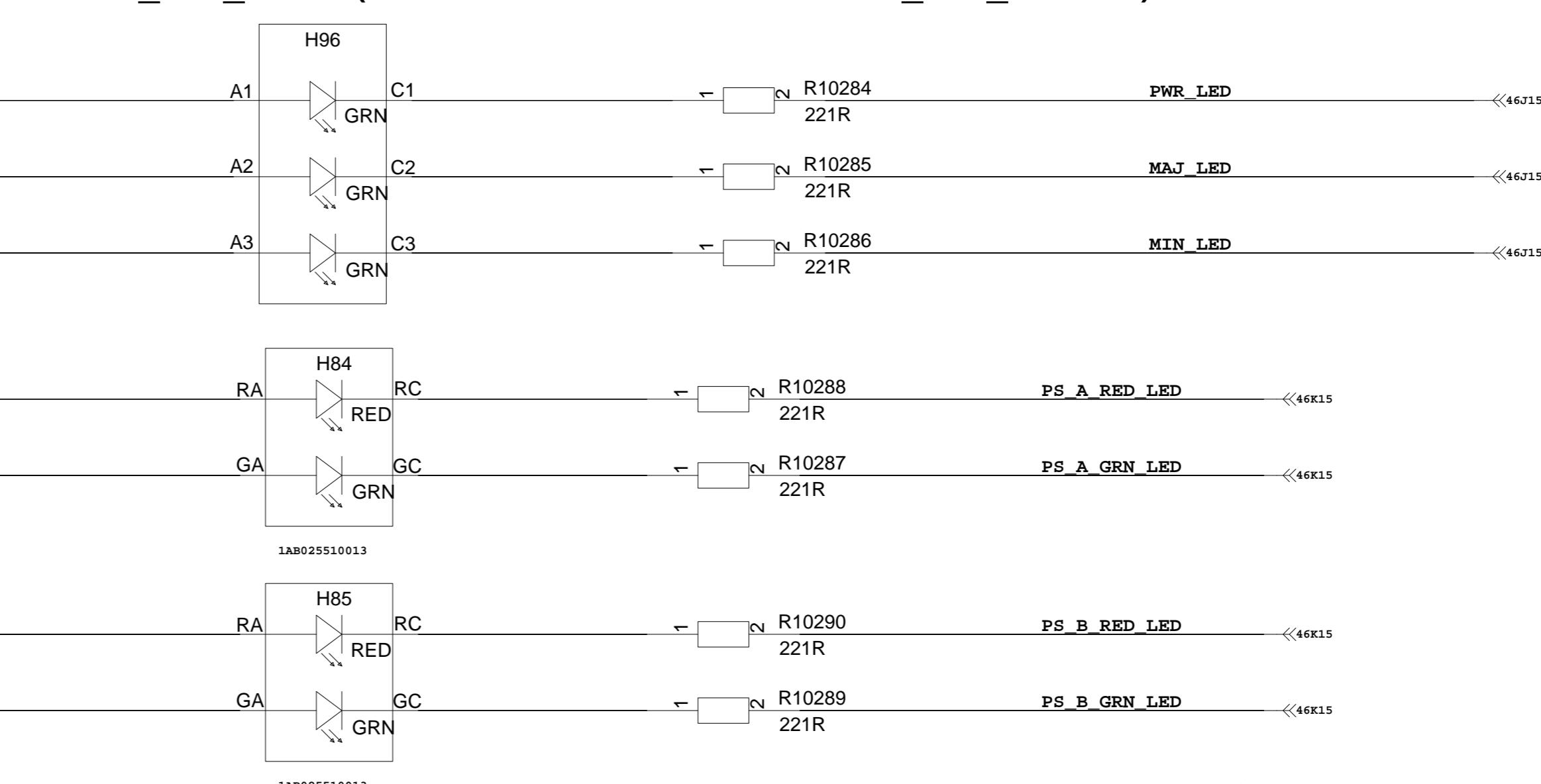
STATUS LEDS



CPU DECOUPLE CAPACITORS



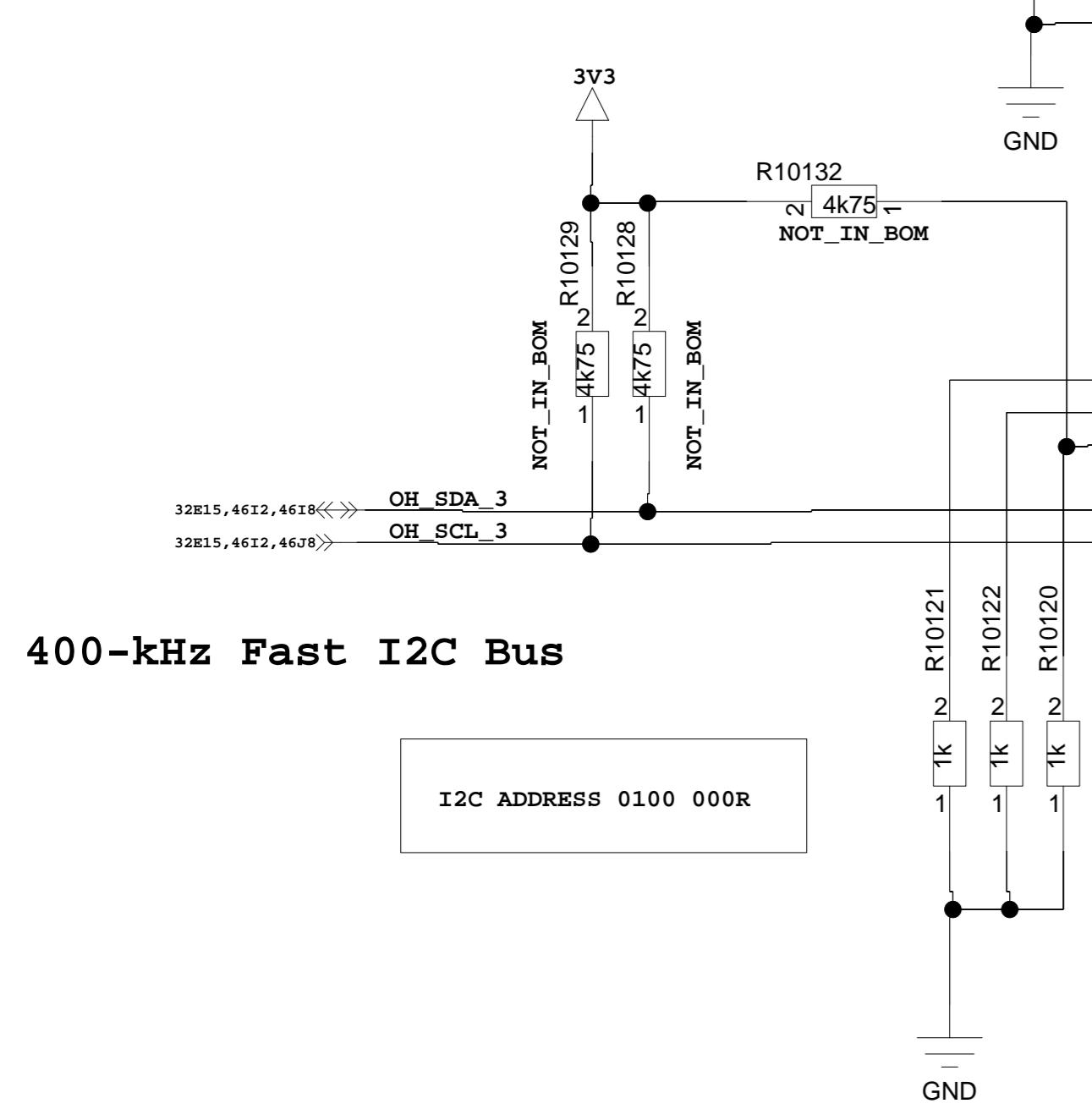
PWR_MAJ_MIN (NEED SEARCH MPN FOR GREEN_RED_YELLOW)



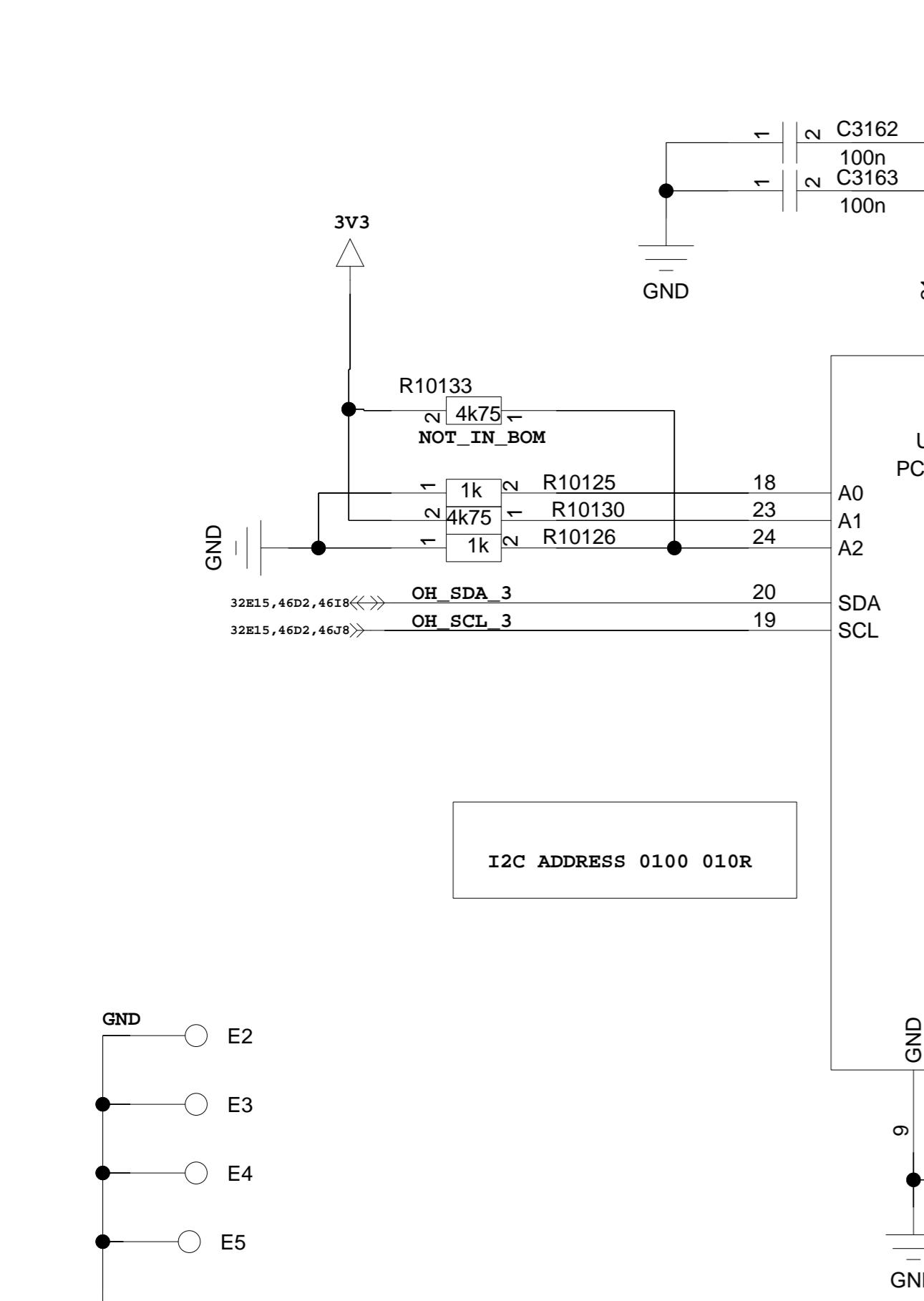
SFP+ LINK/PORT LEDS PART 2

ED	01			

I2C GPIO EXPANDERS

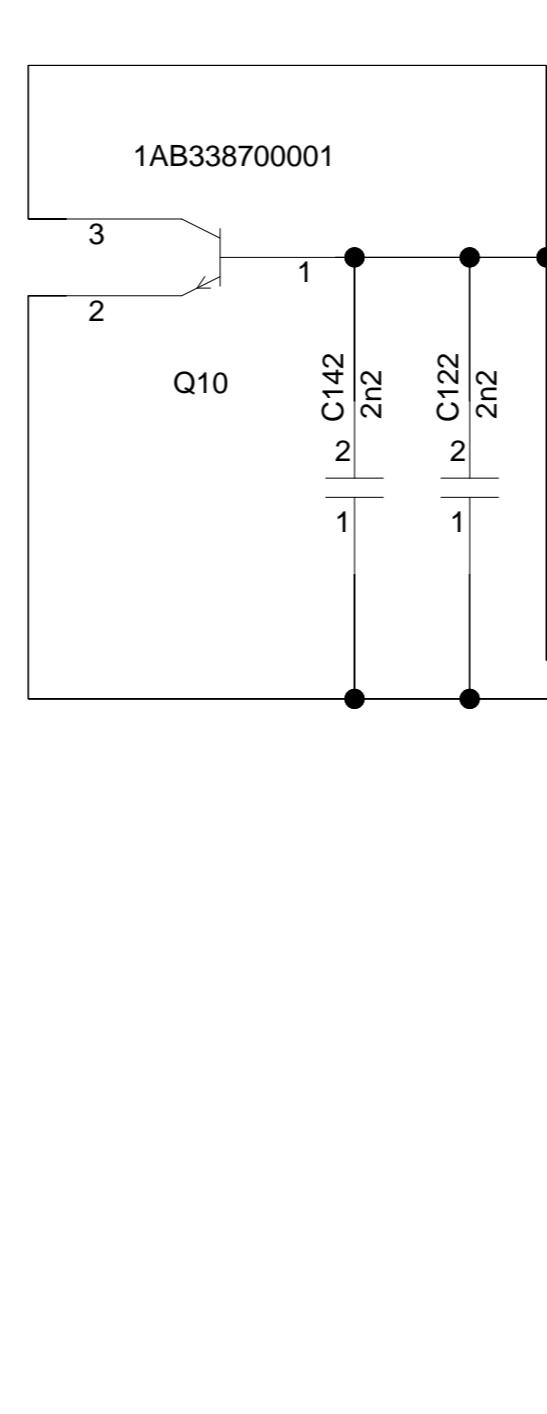


400-kHz Fast I2C Bus

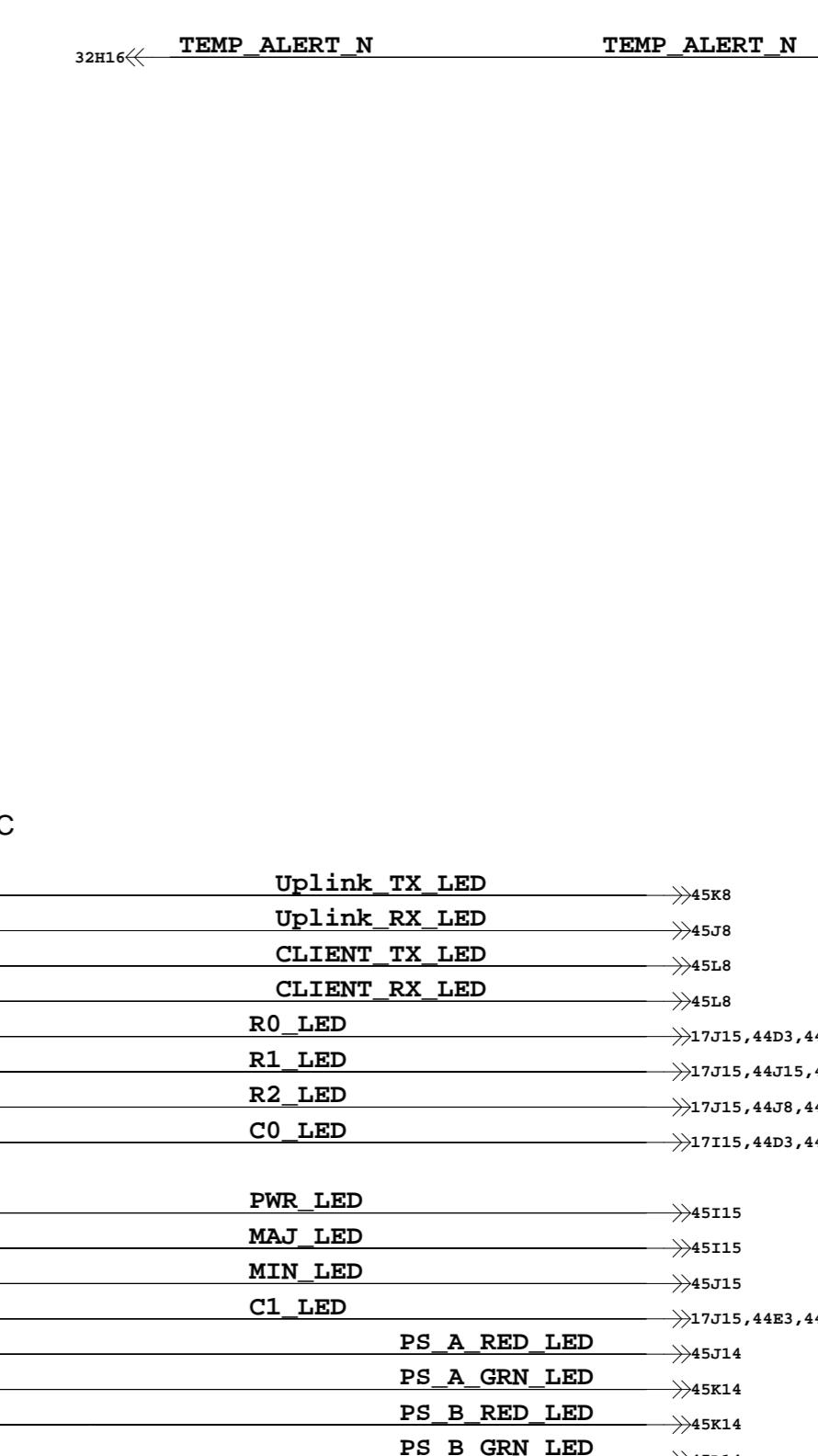
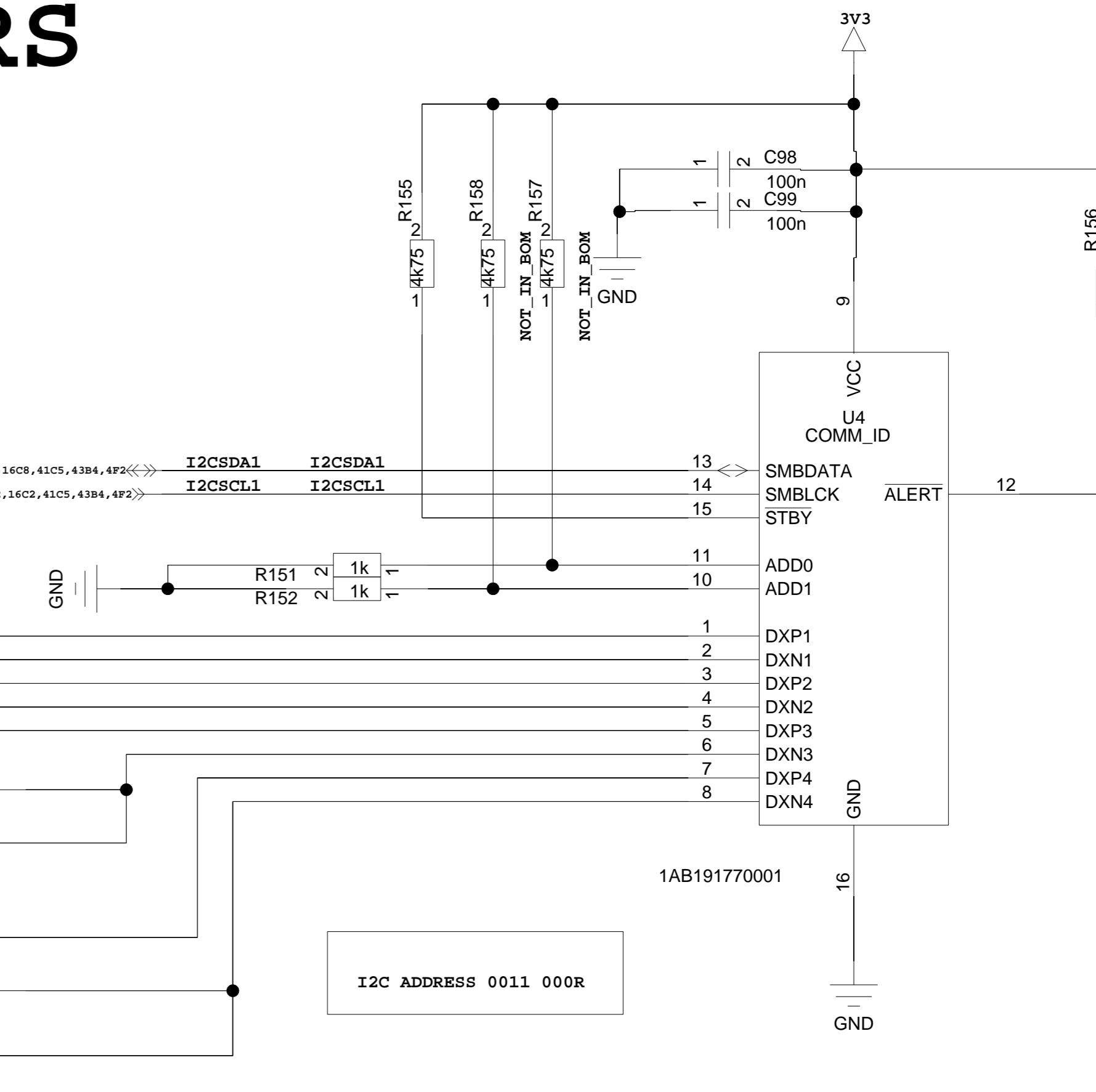
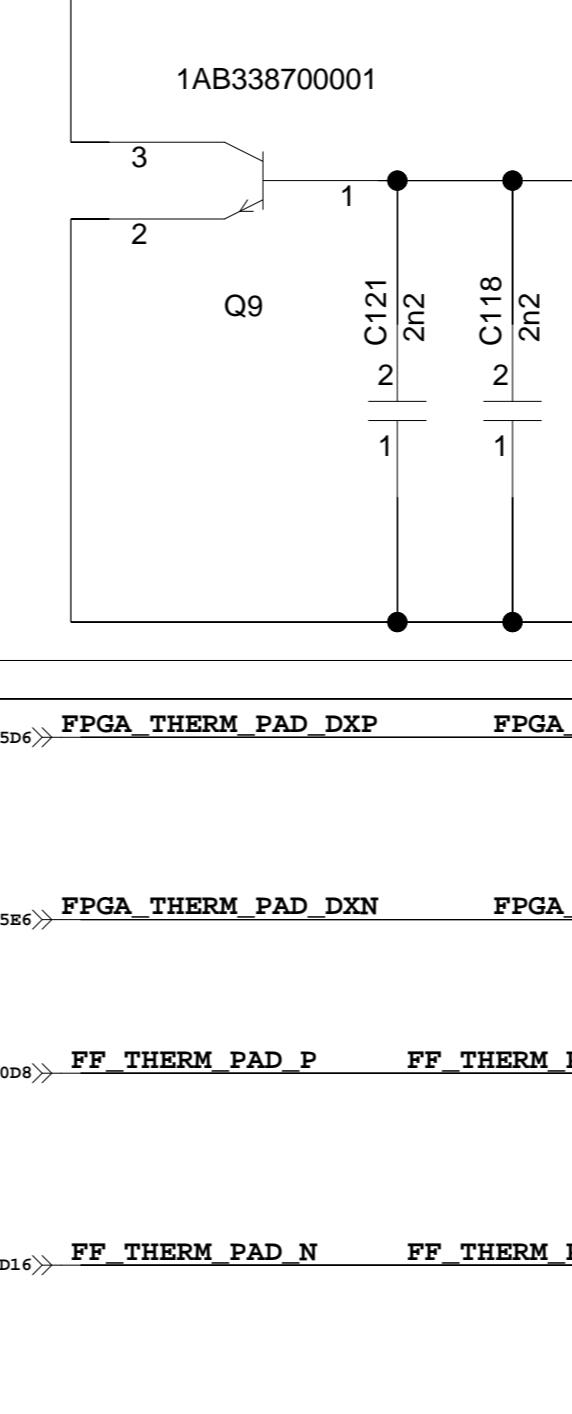


DEFAULT: OH_SCL_3 and OH_SDA_3 are CONNECTED WITH CPU
BACKUP: OH_SCL_3 and OH_SDA_3 are CONNECTED WITH FPGA

AIR IN



AIR OUT



I2C GPIO EXPANDERS

ED	01			
				46/46