

MXP-100G

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CHANGE NOTE						
APPRO.AUTHO.						
ORIGINATOR						
MXP-100G						1/46

BATTERY INPUT 1

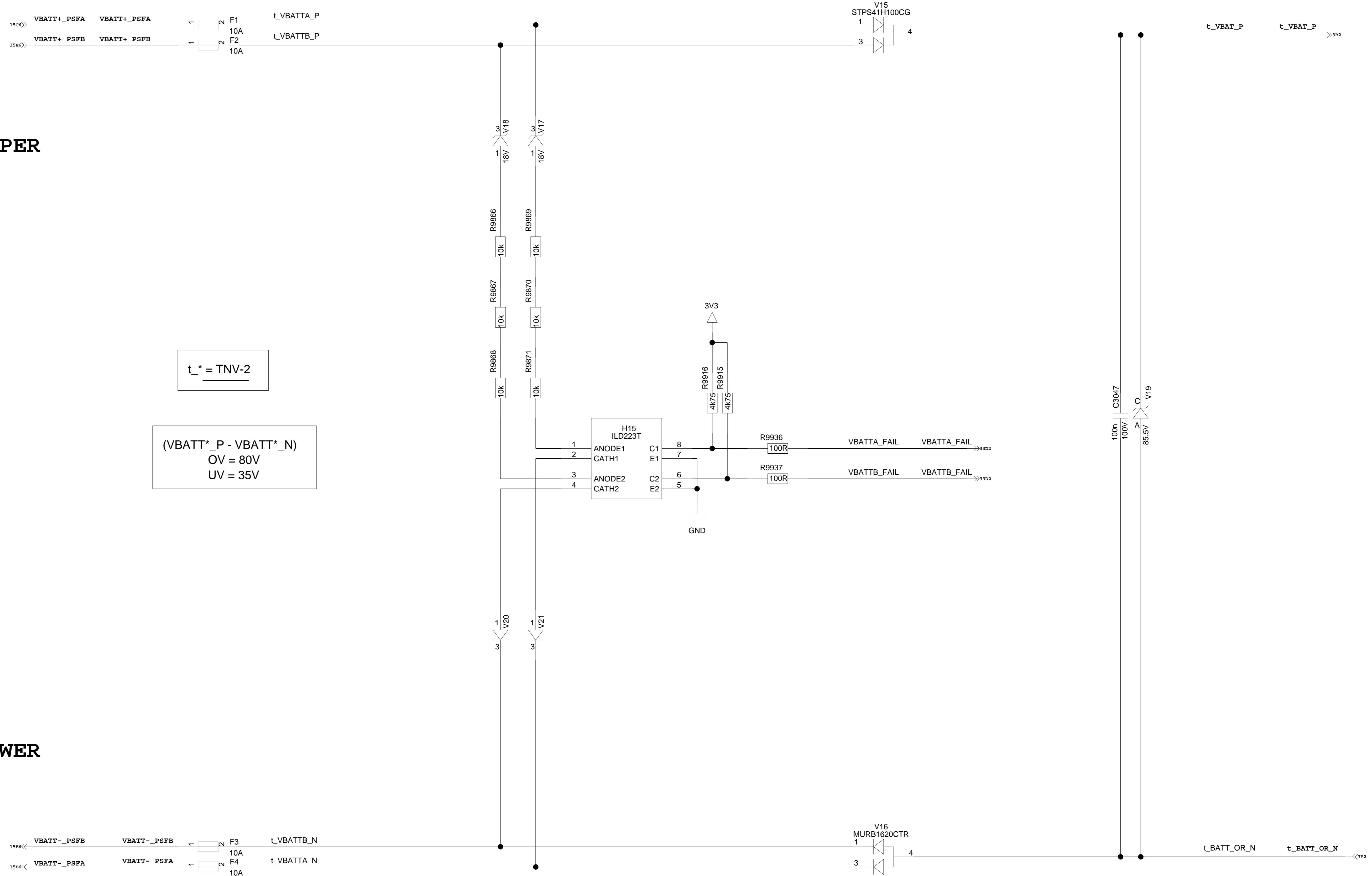
UPPER

BACKPLANE

LOWER

/BATT*_P - VBATT*_N
OV = 80V
UV = 35V

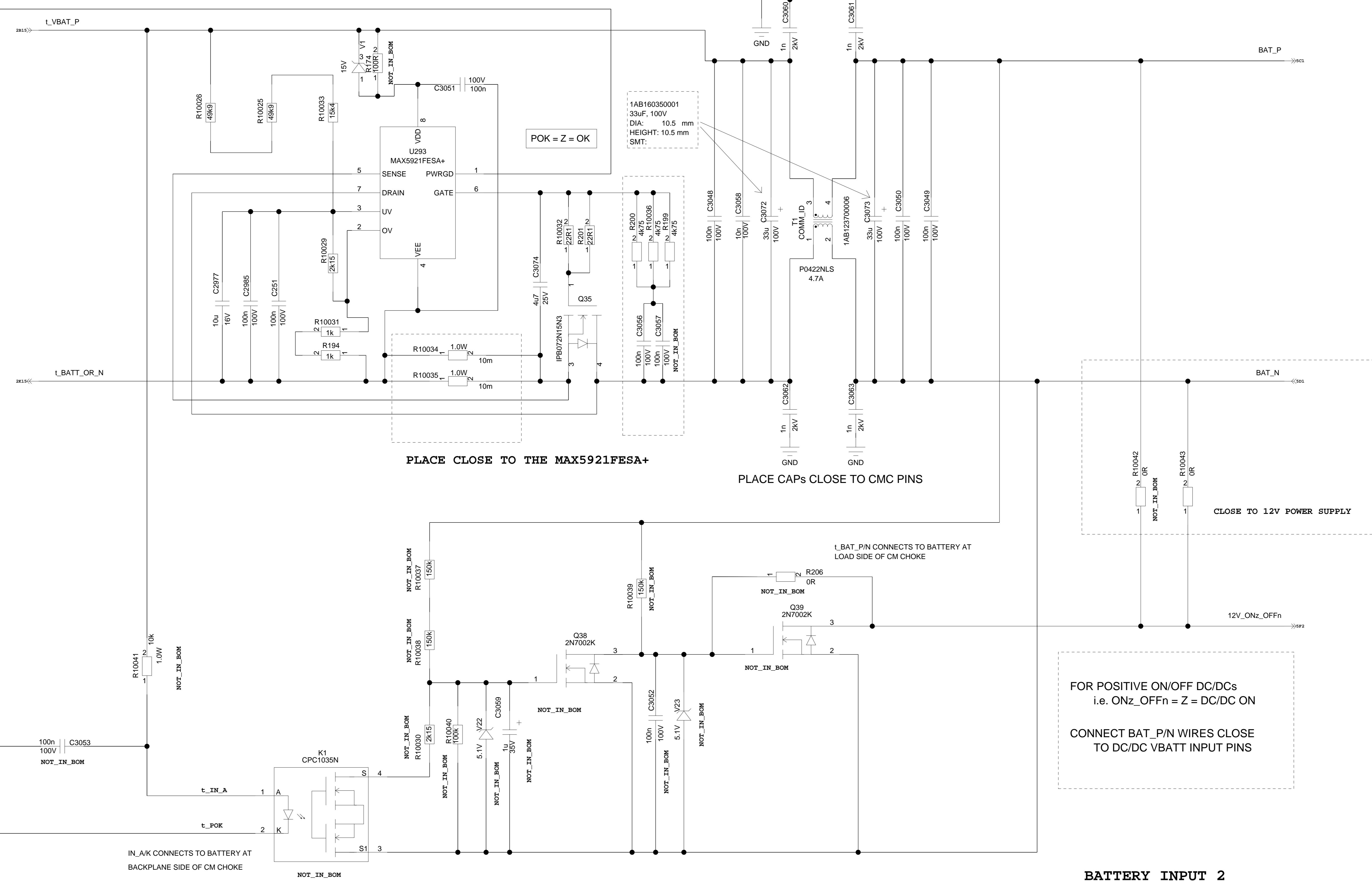
$$t_{-}^{*} = \frac{TNV-2}{2}$$



BATTERY INPUT 1

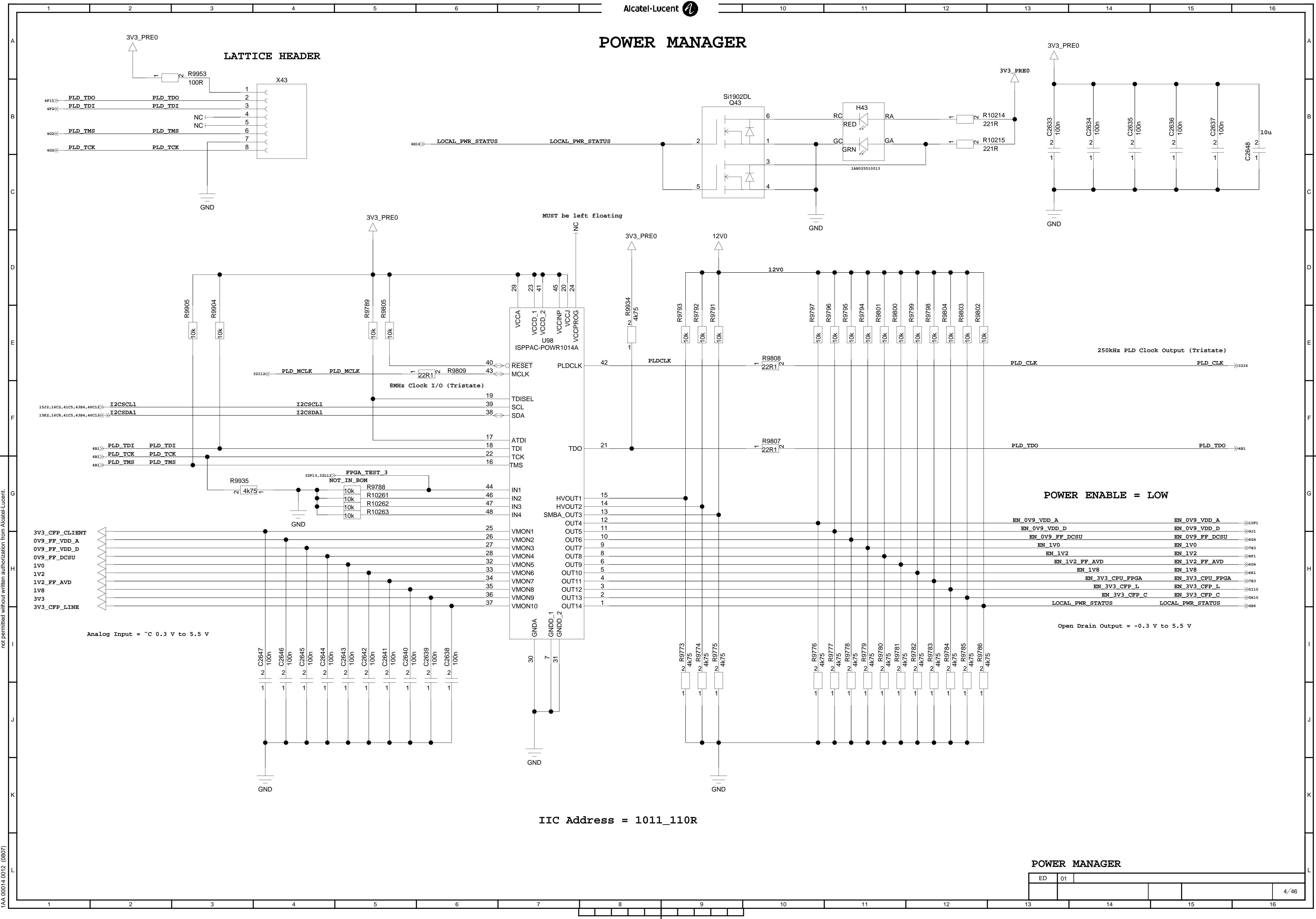
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BATTERY INPUT 2

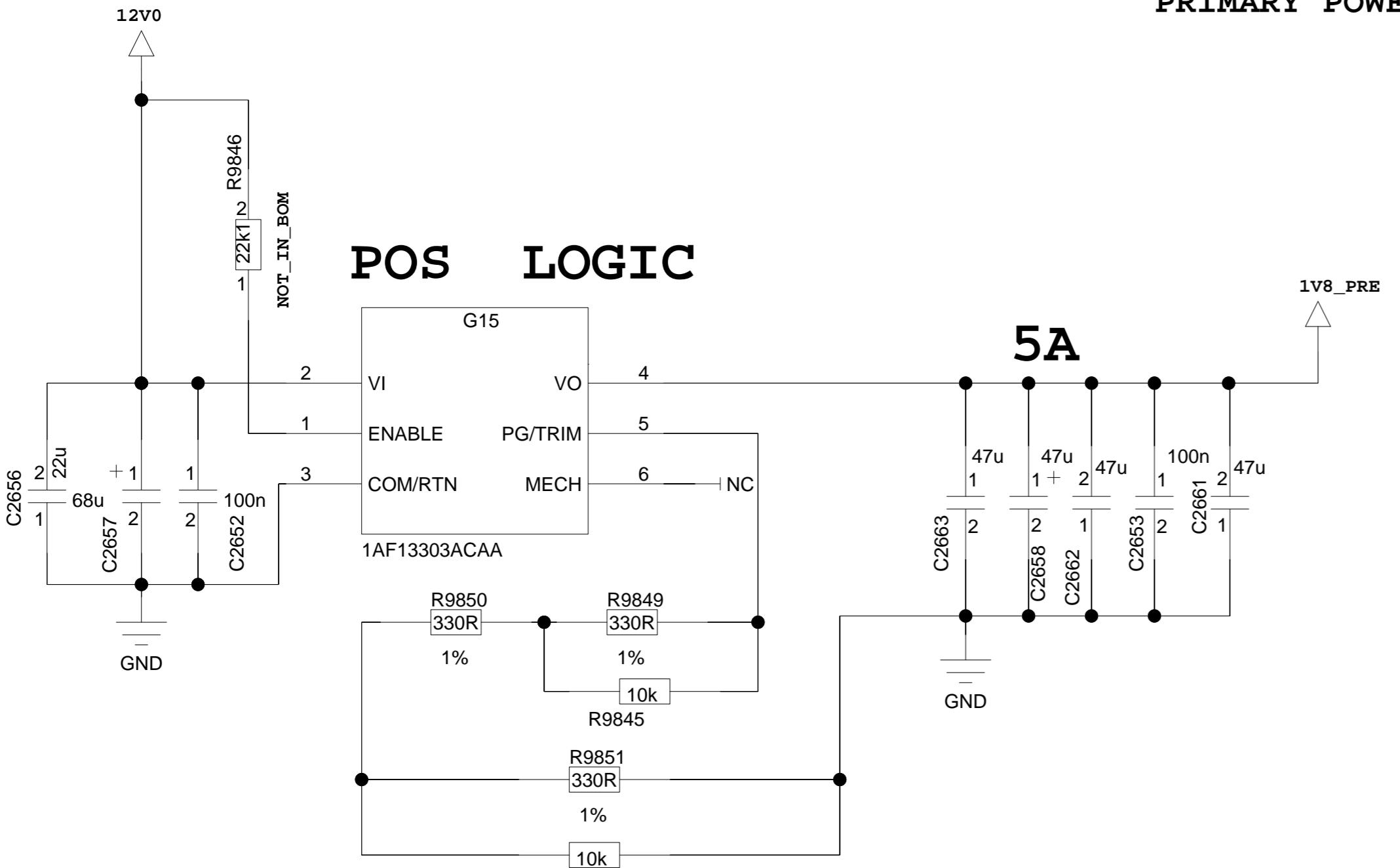


POWER MANAGER

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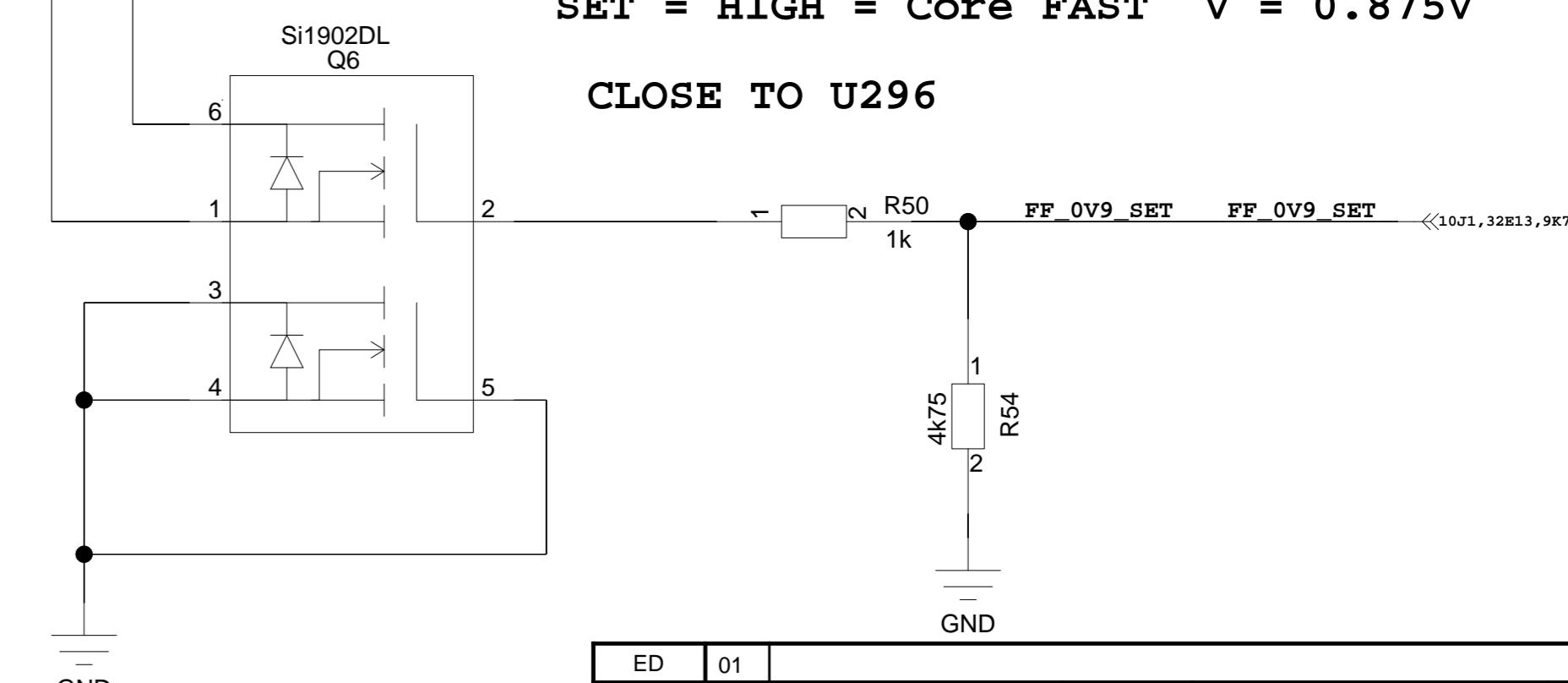
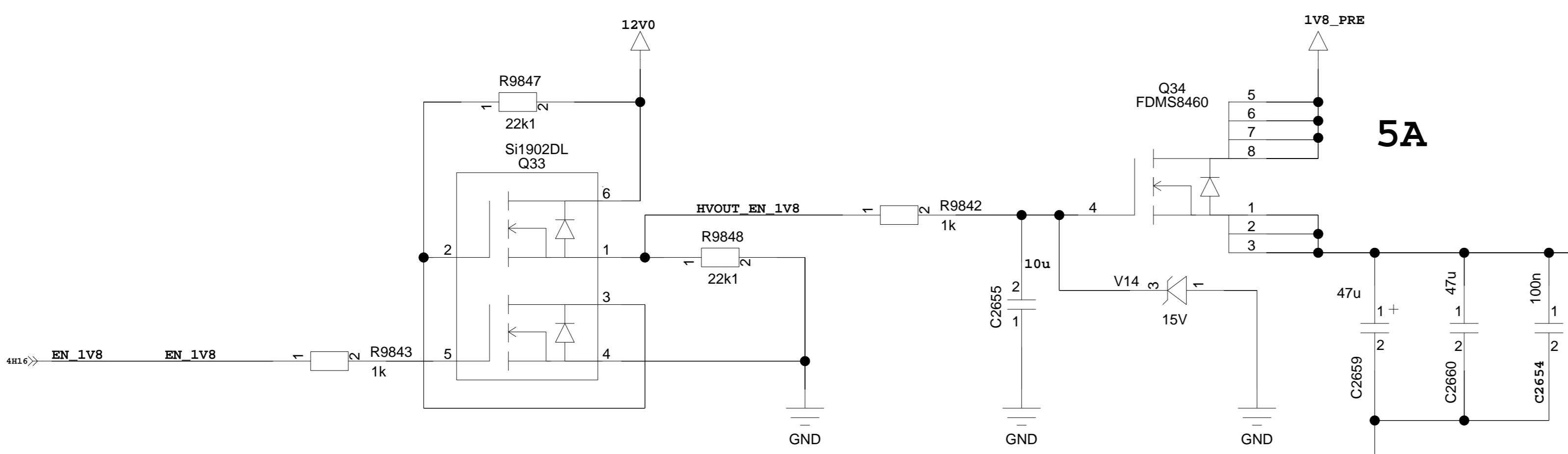
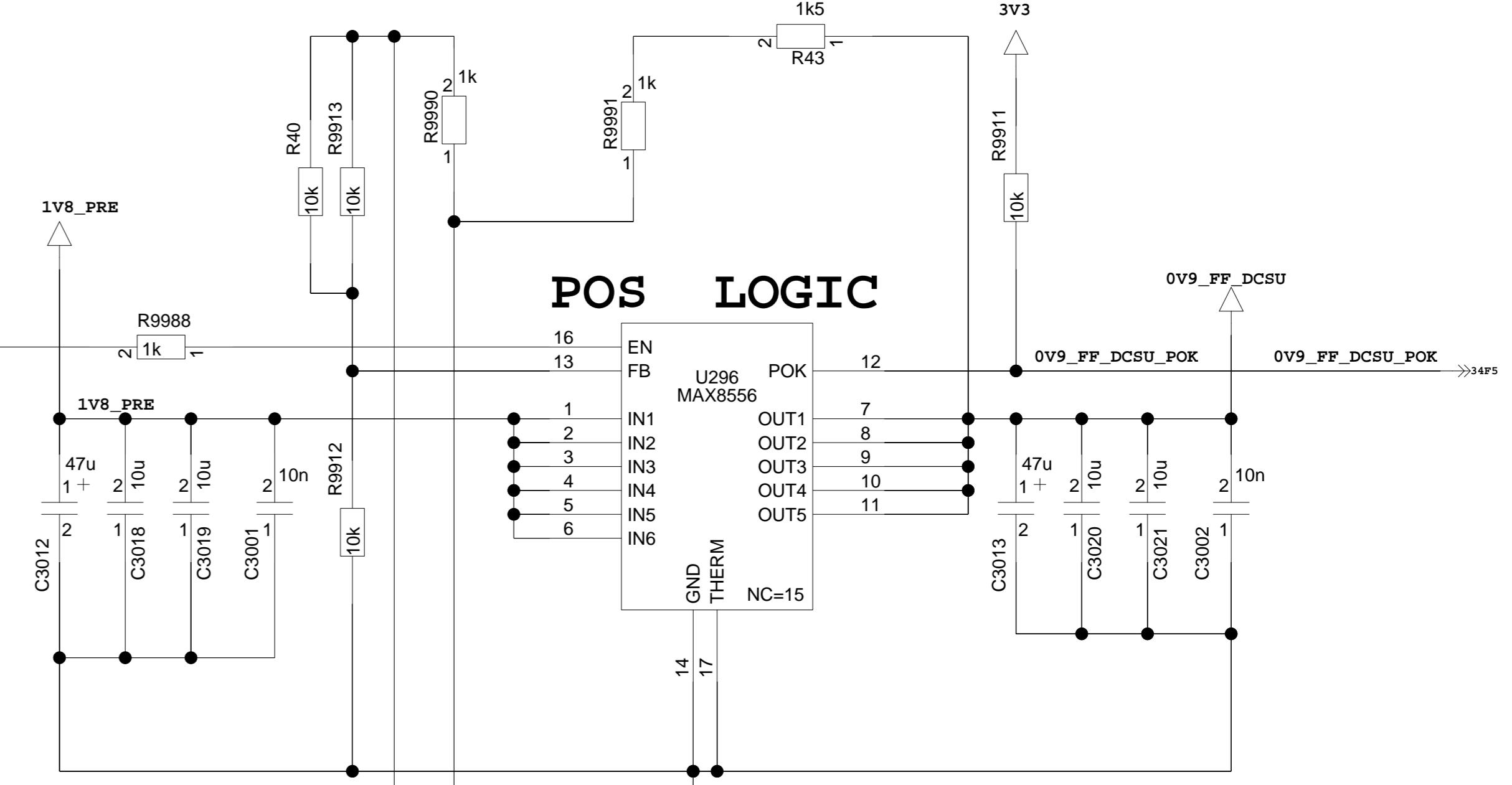
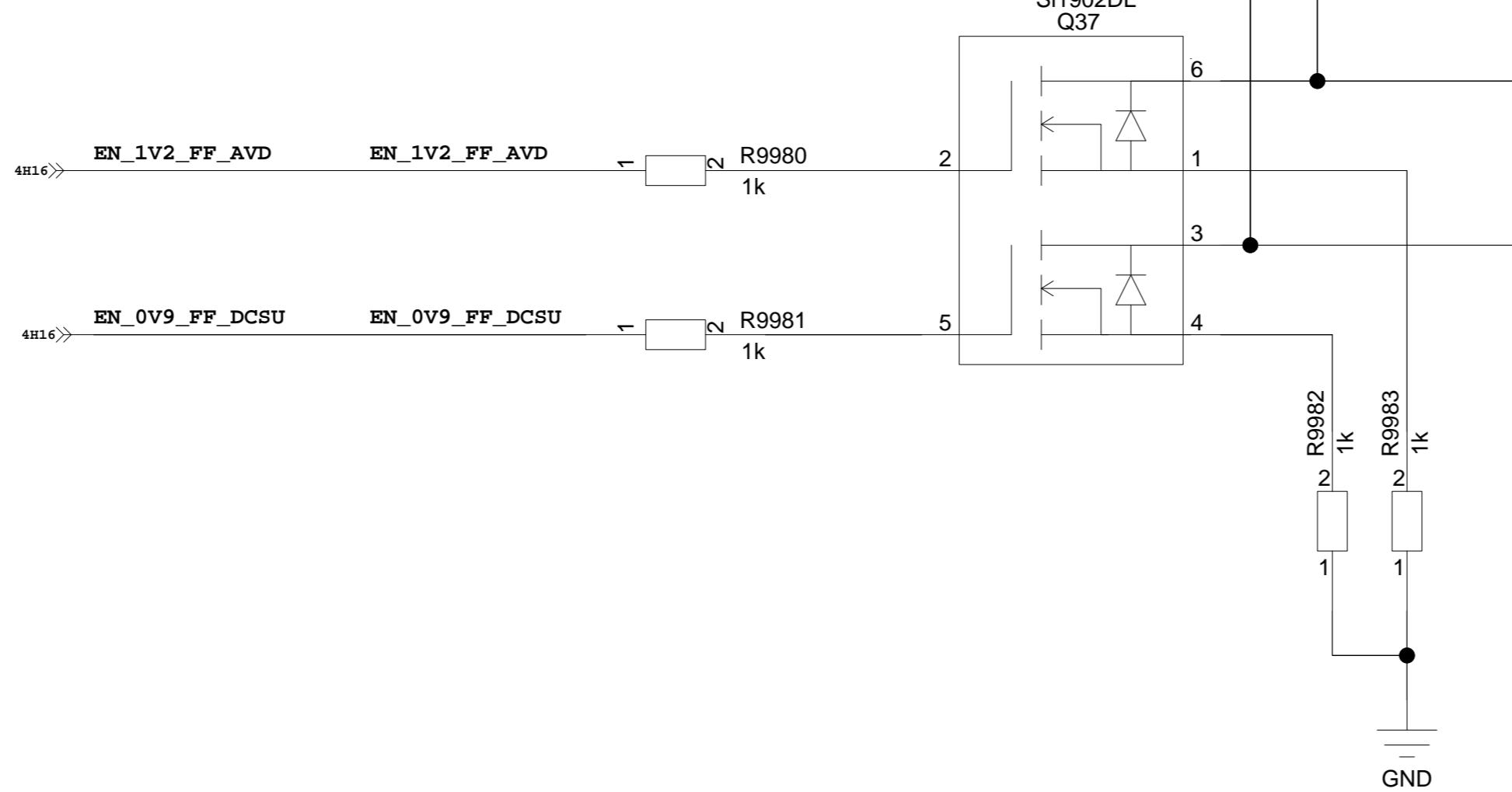
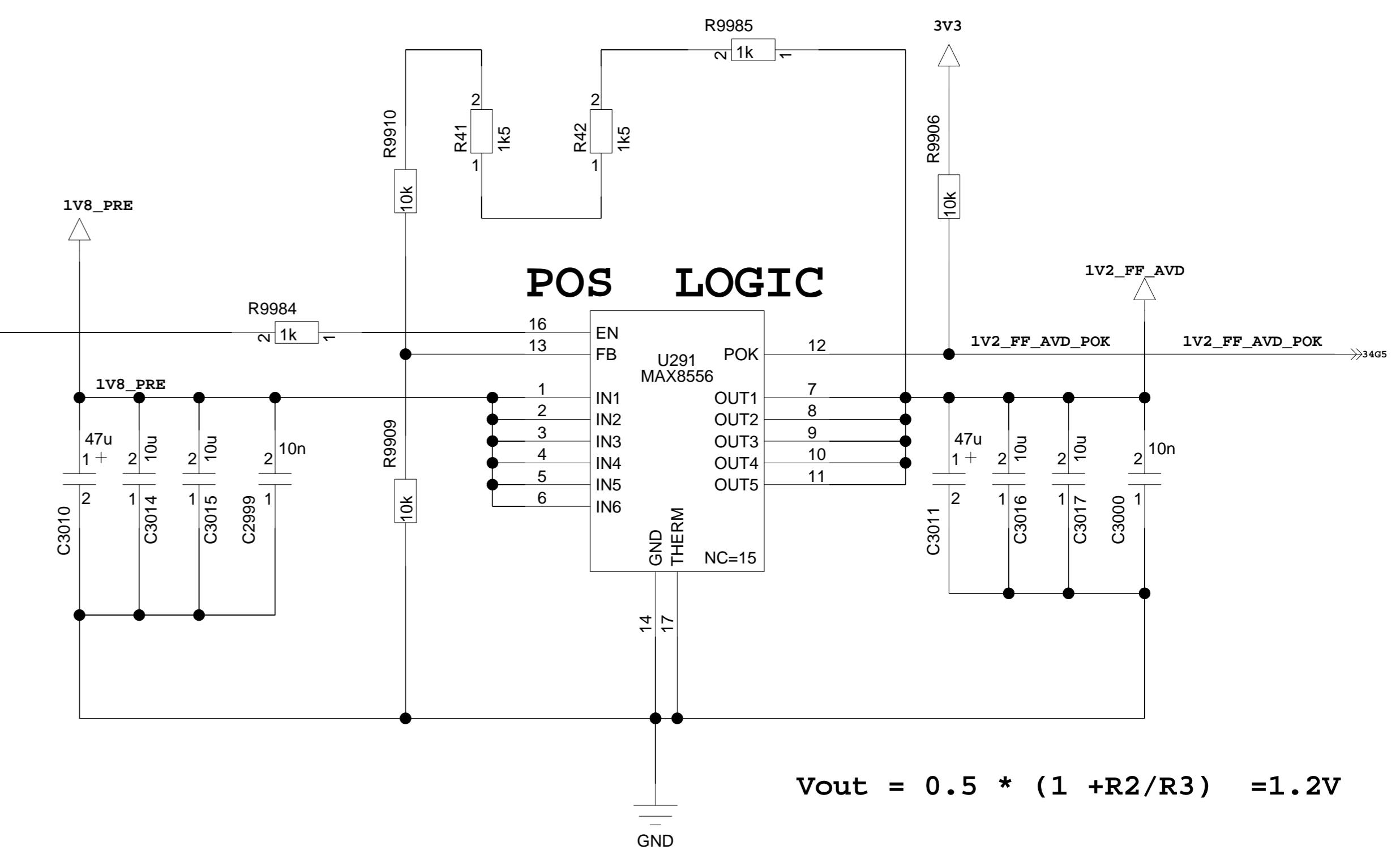
PRIMARY POWER 1V8,1V2_FF,0V9_DCSU



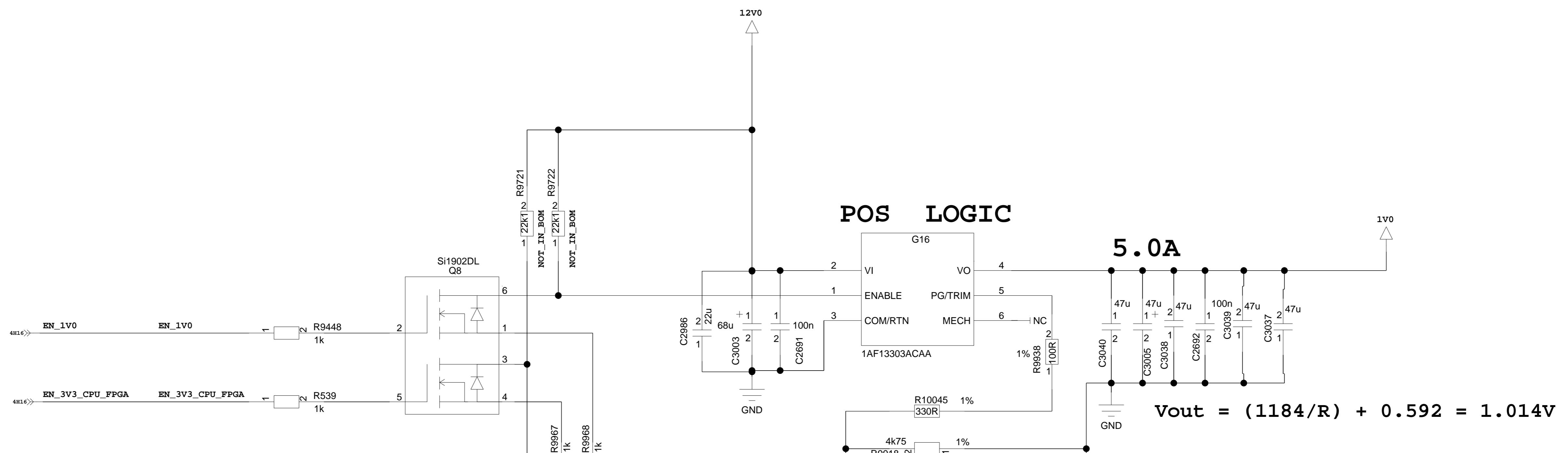
LOCATE CLOSE TO MODULE

$$V_{out} = (1184/R) + 0.592 = 1.814V$$

With OCP,OTP Protection



PRIMARY POWER 1V0 , 3V3



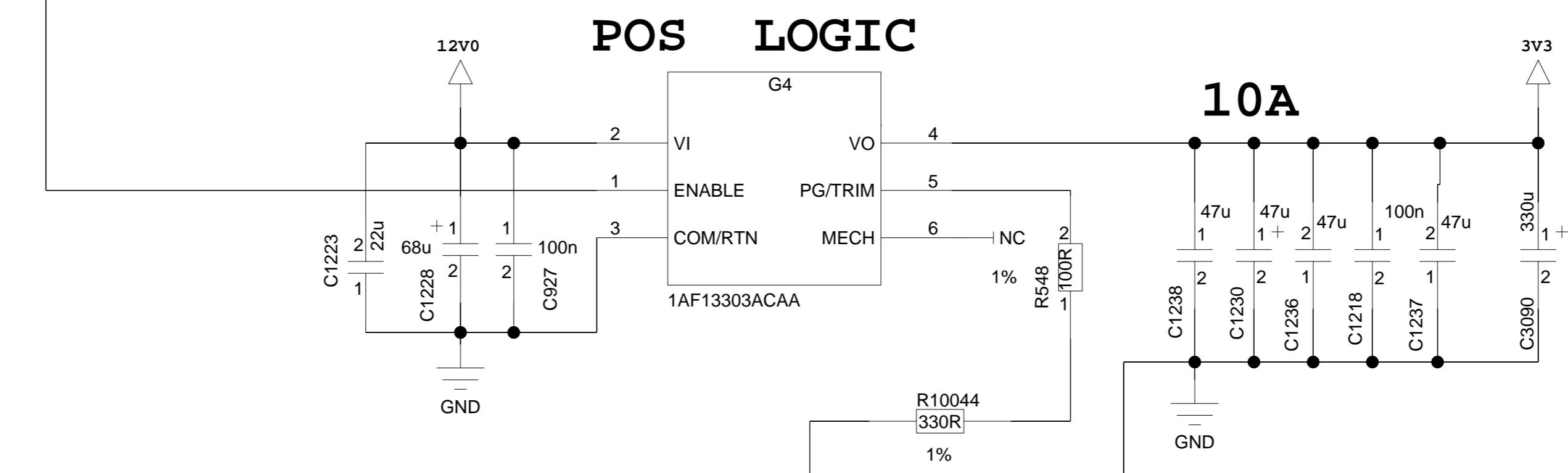
POS LOGIC

5.0A

$$V_{out} = (1184/R) + 0.592 = 1.014V$$

With OCP,OTP Protection

POS LOGIC



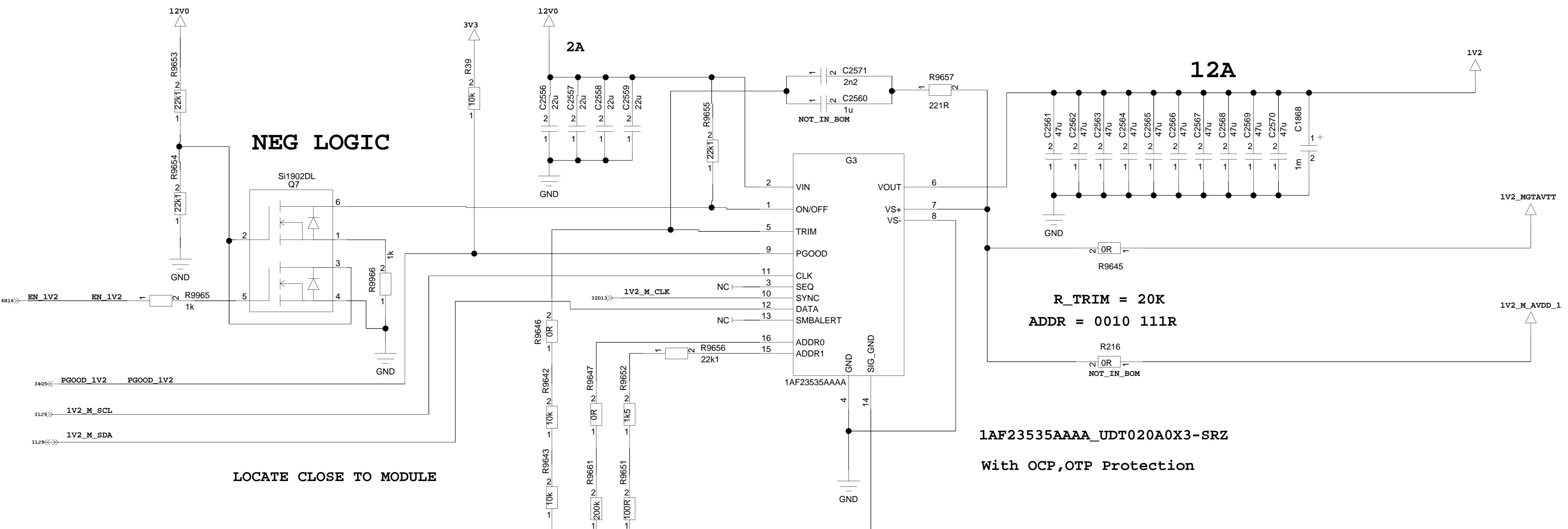
LOCATE CLOSE TO MODULE With OCP,OTP Protection

$$V_{out} = (1184/R) + 0.592 = 3.345V$$

PRIMARY POWER 1V0, 3V3

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PRIMARY POWER 1V2



R9661 IS JUST FOR IIC TEST USAGE

PRIMARY POWER 1V2

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FLEXFRAMER POWER SUPPLY 1

Sense Path if FF is not assembled

GND

CP,OTP Protection

IGH = GOOD

SET = LOW = Core SLOW V = 0.925V
SET = HIGH = Core FAST V = 0.875V

FLEXFRAMER POWER SUPPLY 1

With OCP,OTP Protection
MDT040A0X3-SRPHZ SYNC Min 510k, typ k, 720k
SLDN-40E1AL SYNC Min 320k, typ k, Max 480k

NEG LOGIC

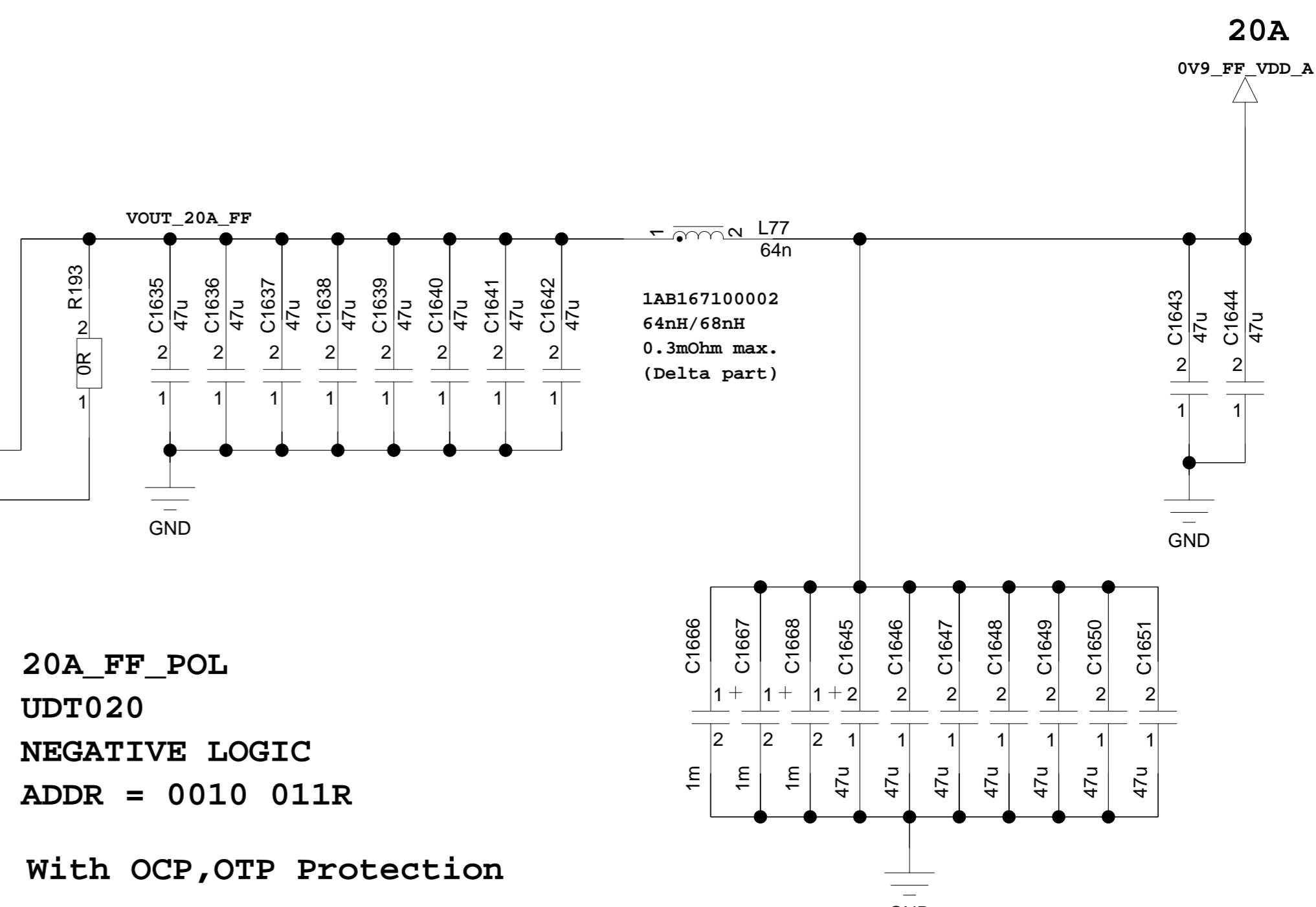
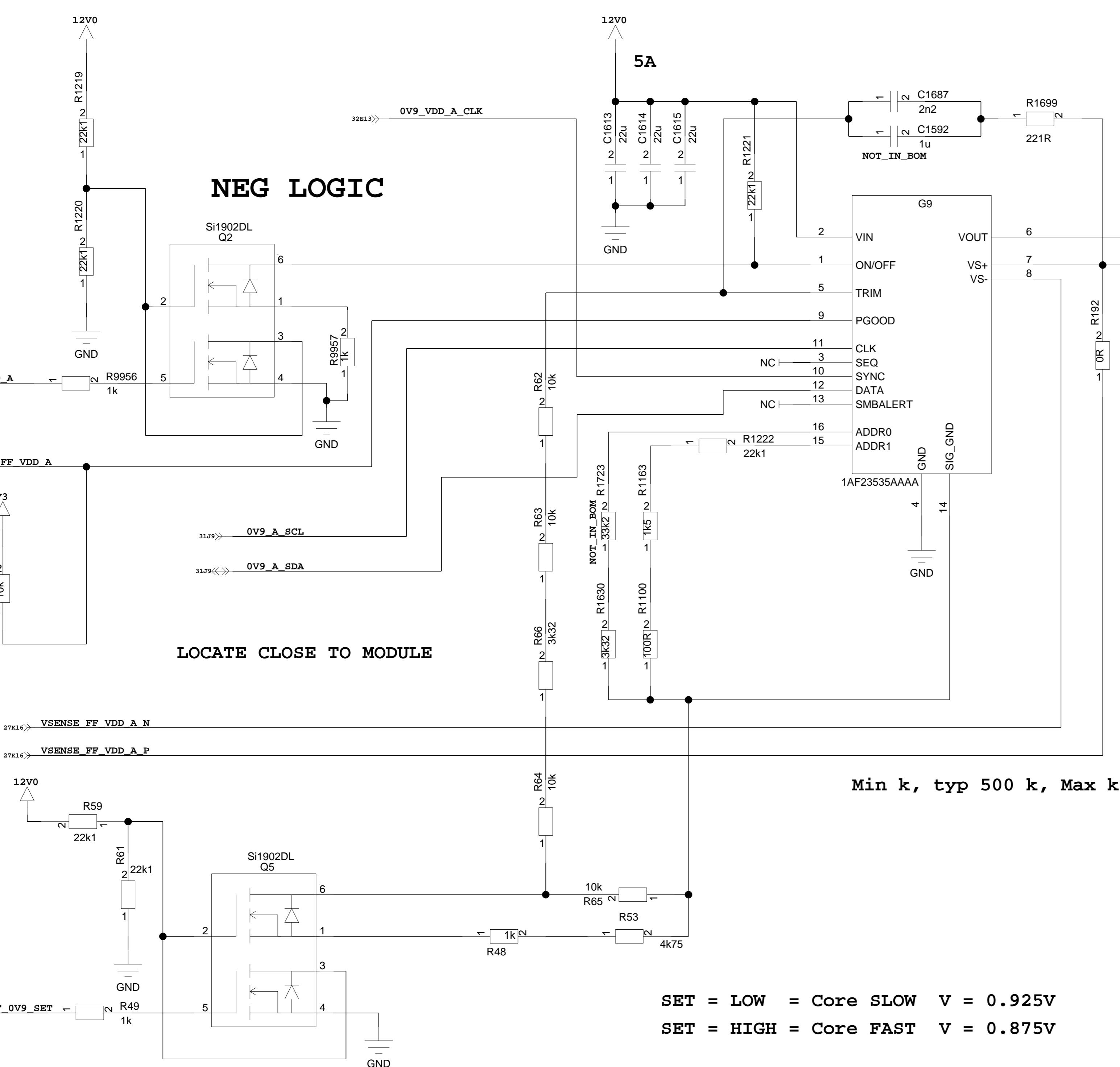
ADDR = 0010 000R

LOCATE CLOSE TO MODULE

HIGH = GOOD

D_0V9_FF_VDD_D_2 → 34G5
D_0V9_FF_VDD_D_1 → 34G5

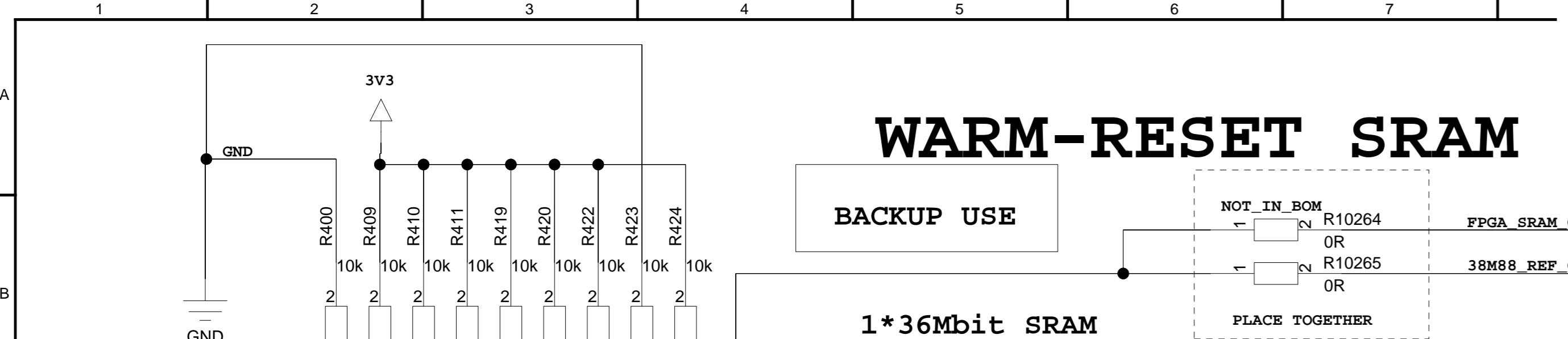
FLEXFRAMER POWER SUPPLY 2



NOTE for G9 (UDT020):

Sensitive, high-impedance, analog pins
TRIM and SIG_GND on the one hand side
and digital traces CLK, DATA and SMBALERT
on the other hand side, have to be separated
as good/far as possible in the layout!

R1723 IS JUST FOR IIC TEST USAGE

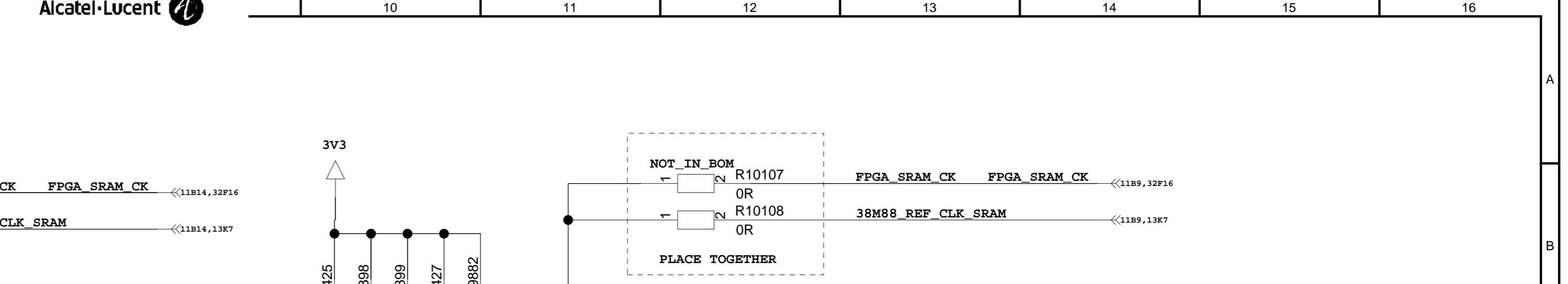


WARM-RESET SRAM

BACKUP USE

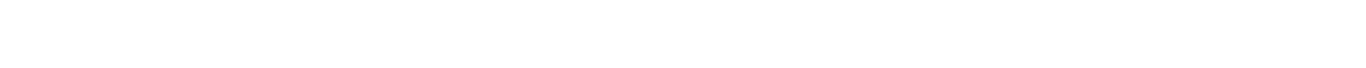
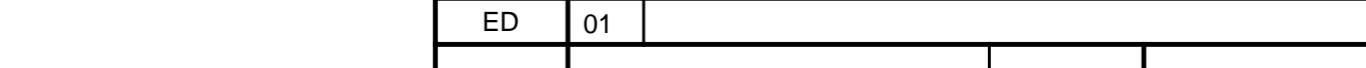
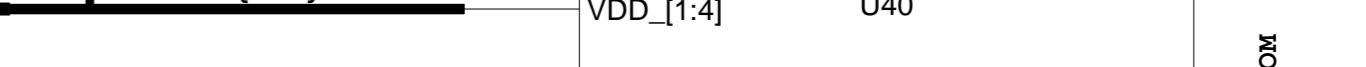
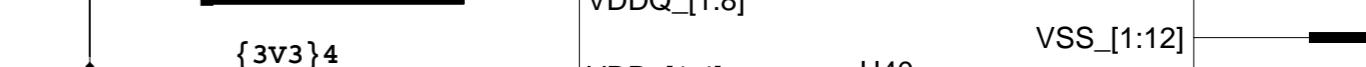
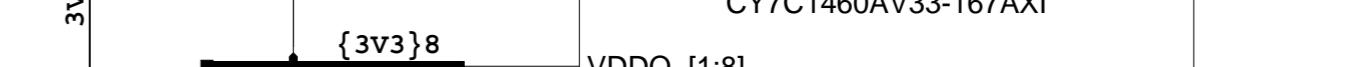
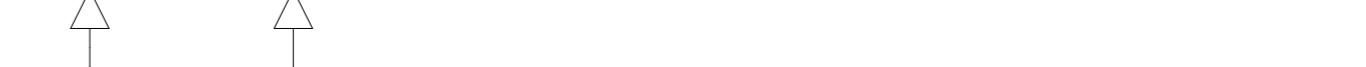
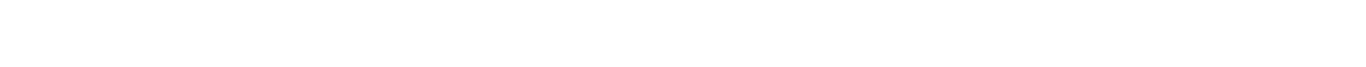
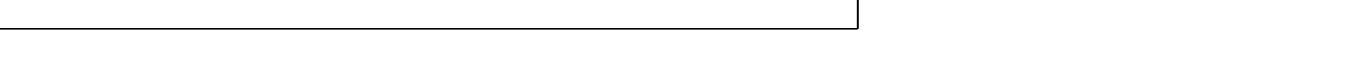
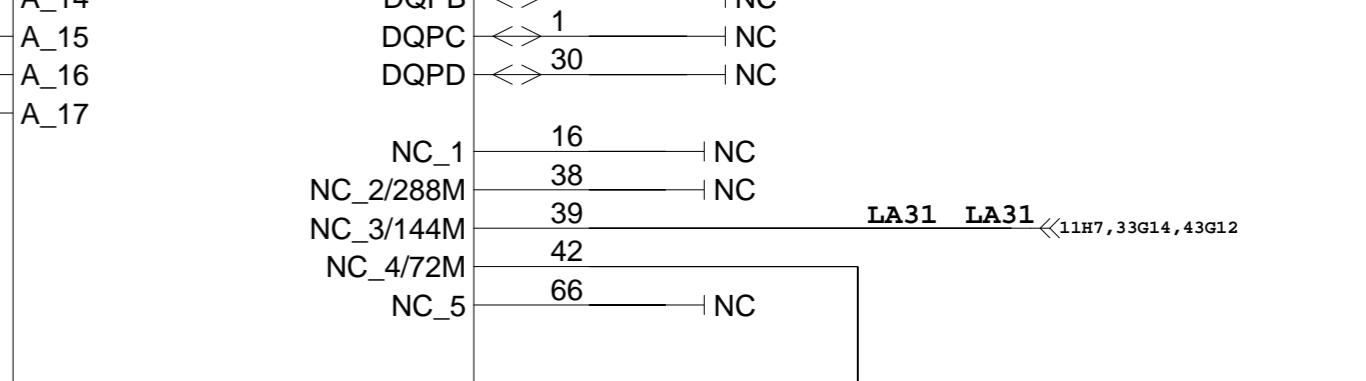
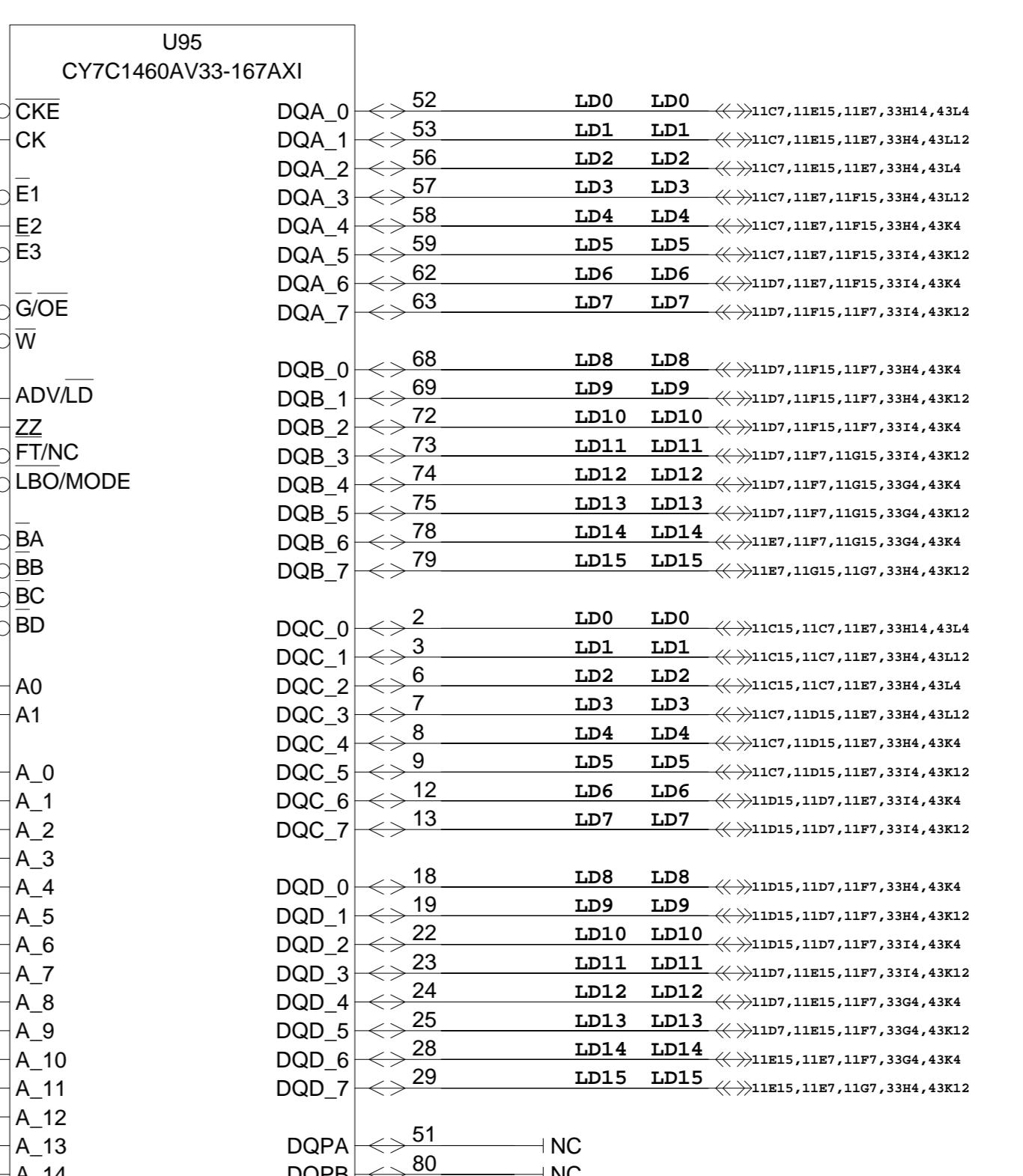
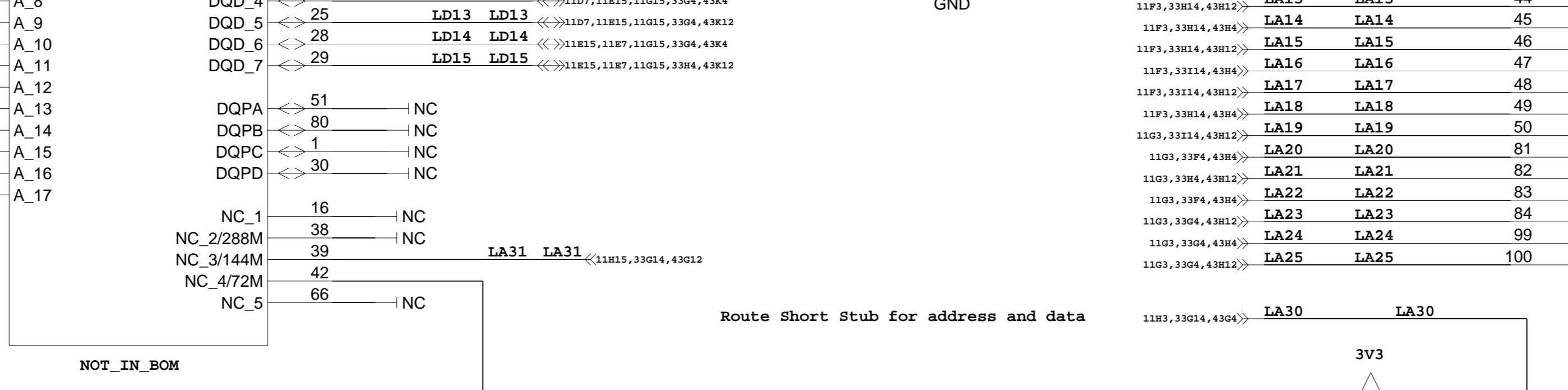
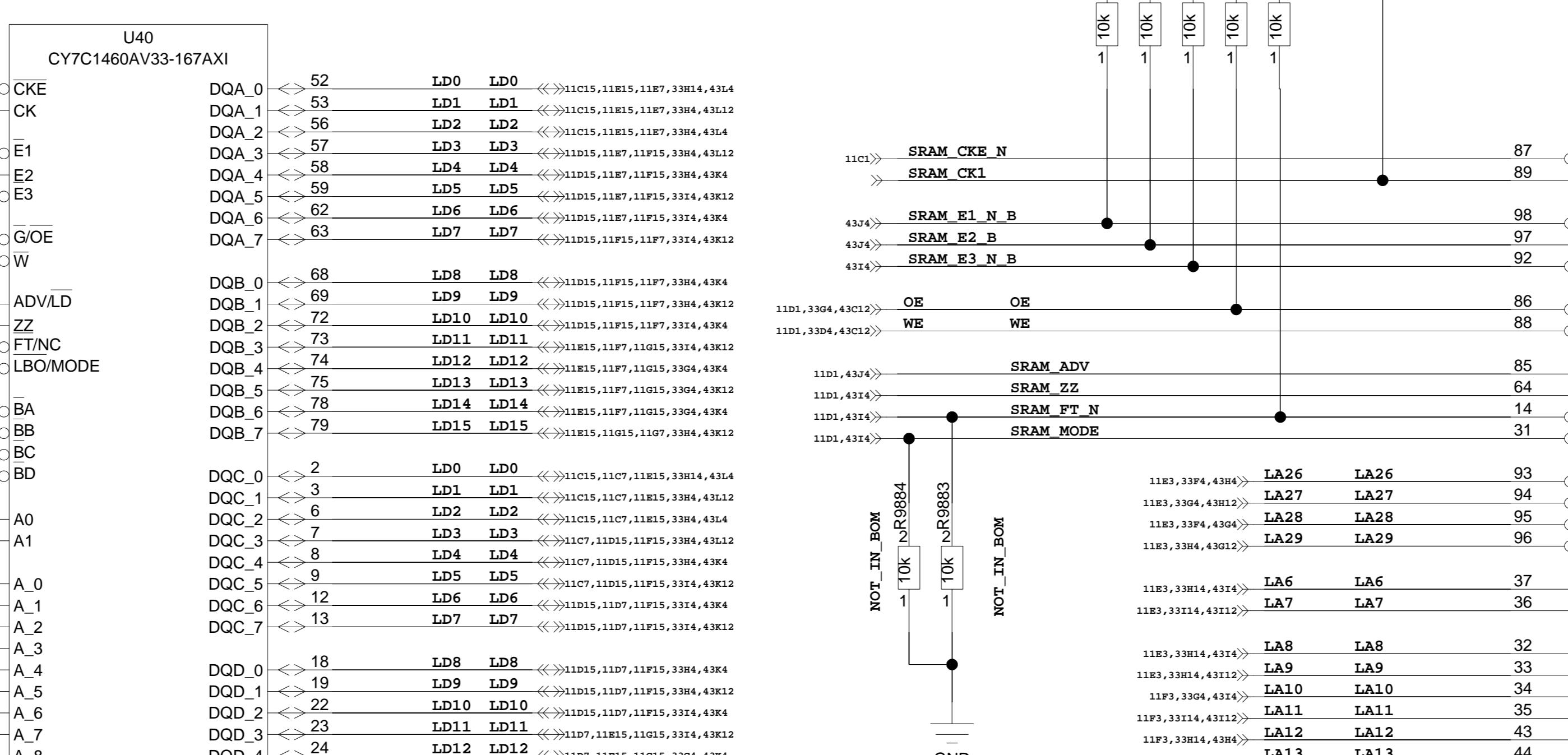
1*36Mbit SRAM

PLACE TOGETHER



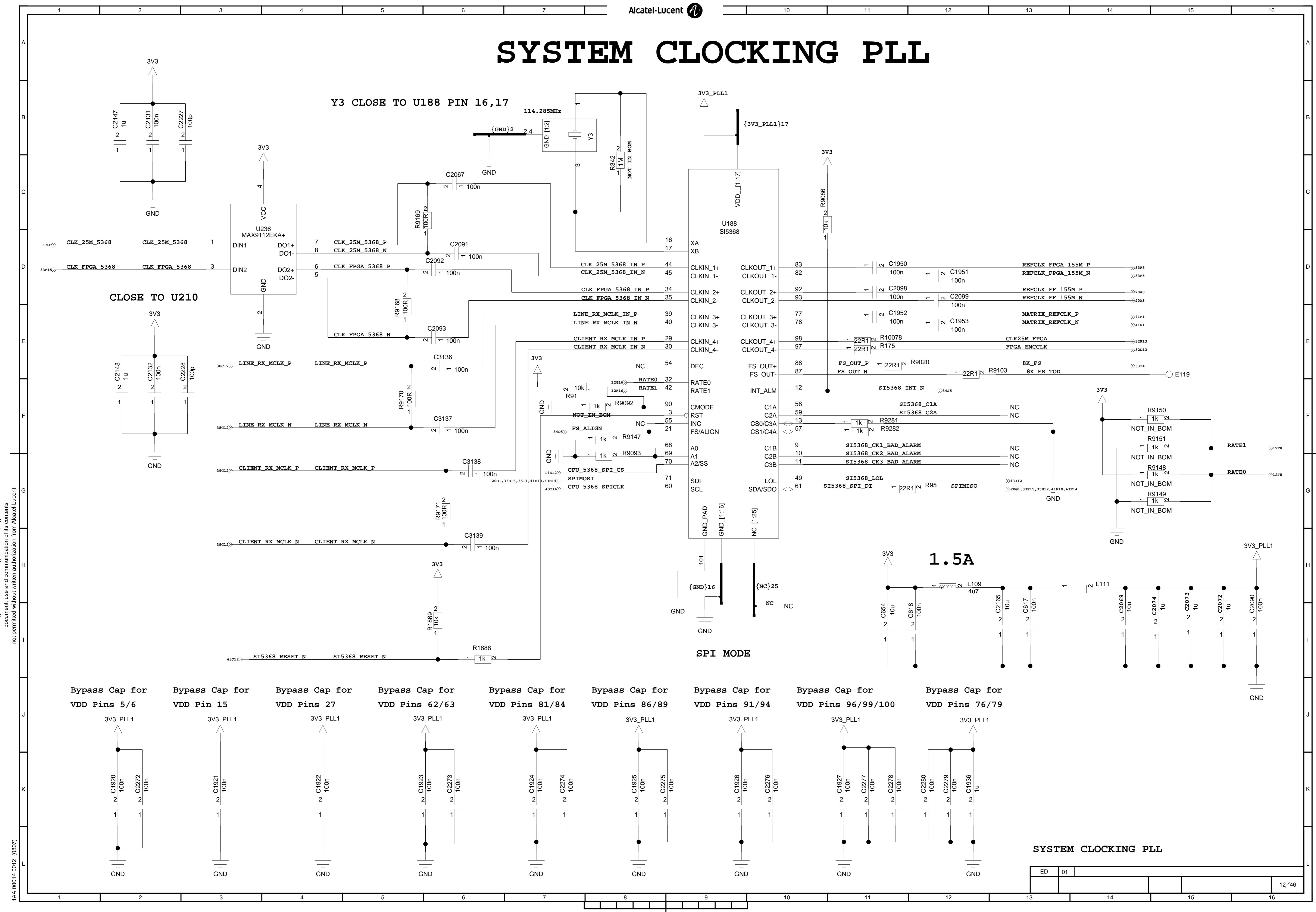
1*36Mbit SRAM

This part for backup.



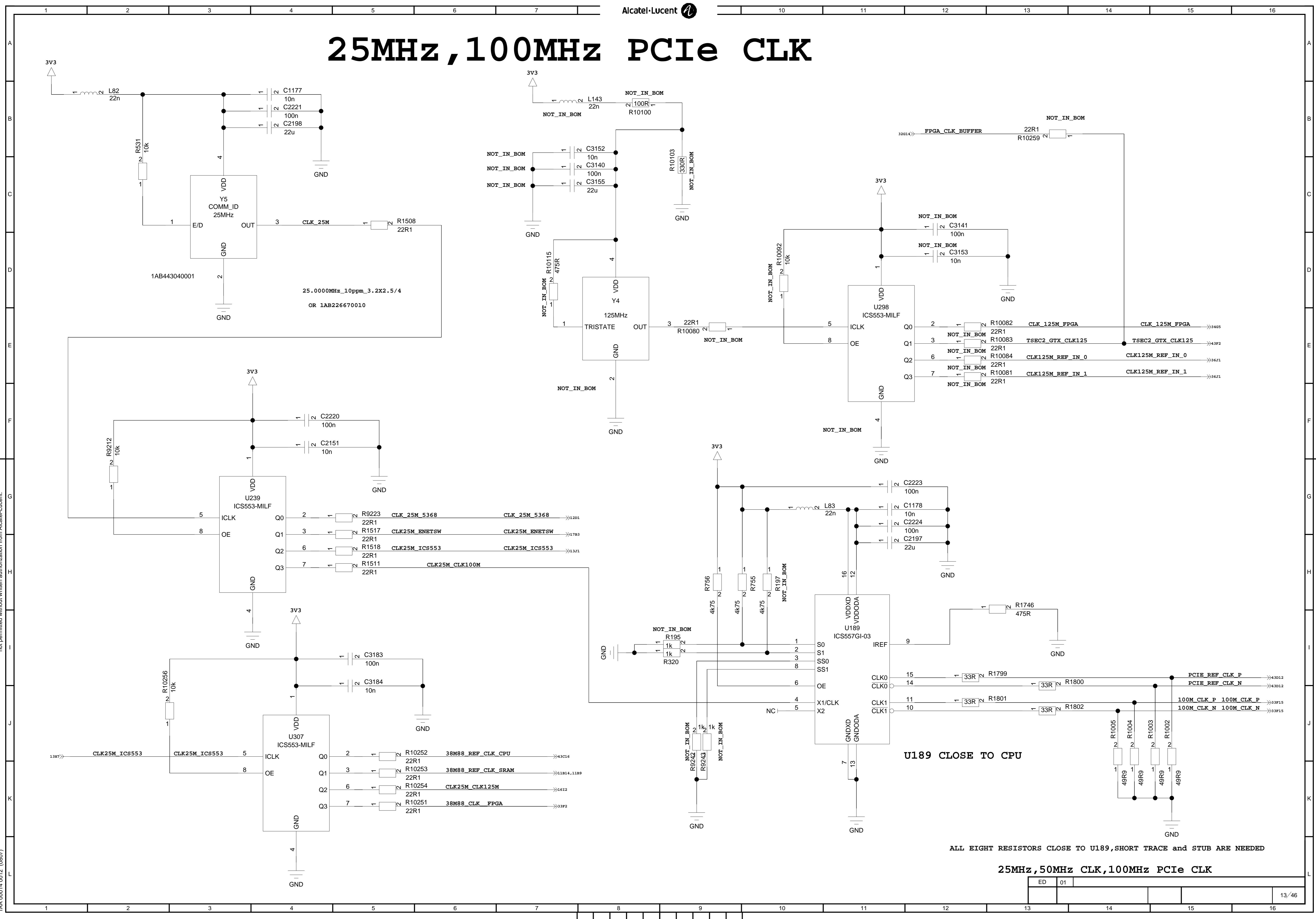
SYSTEM CLOCKING PLL

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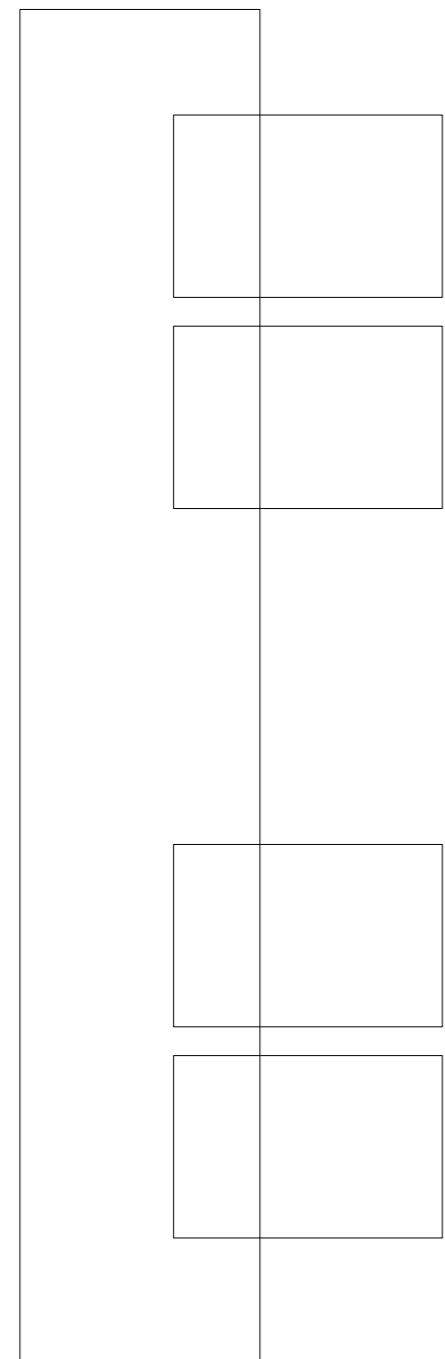


25MHz, 100MHz PCIe CLK

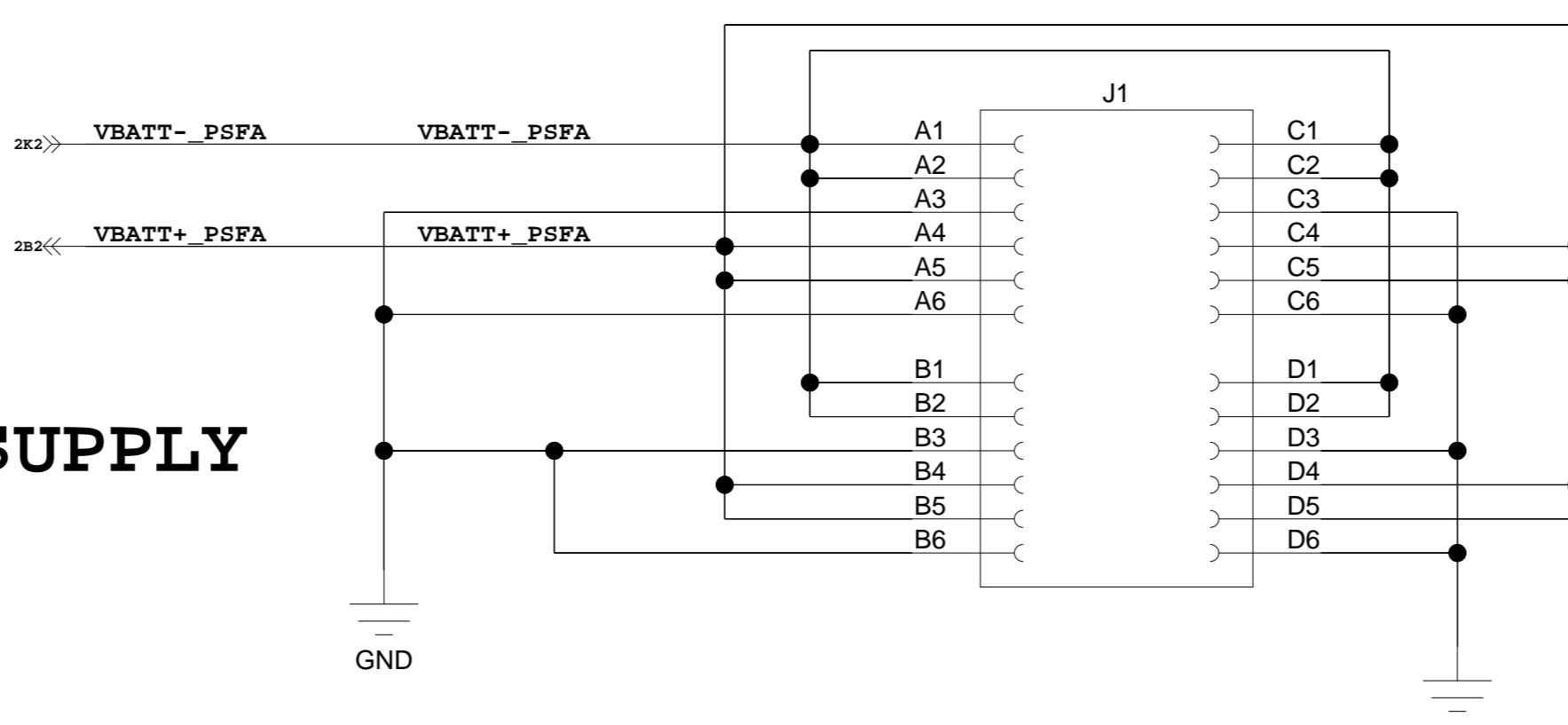
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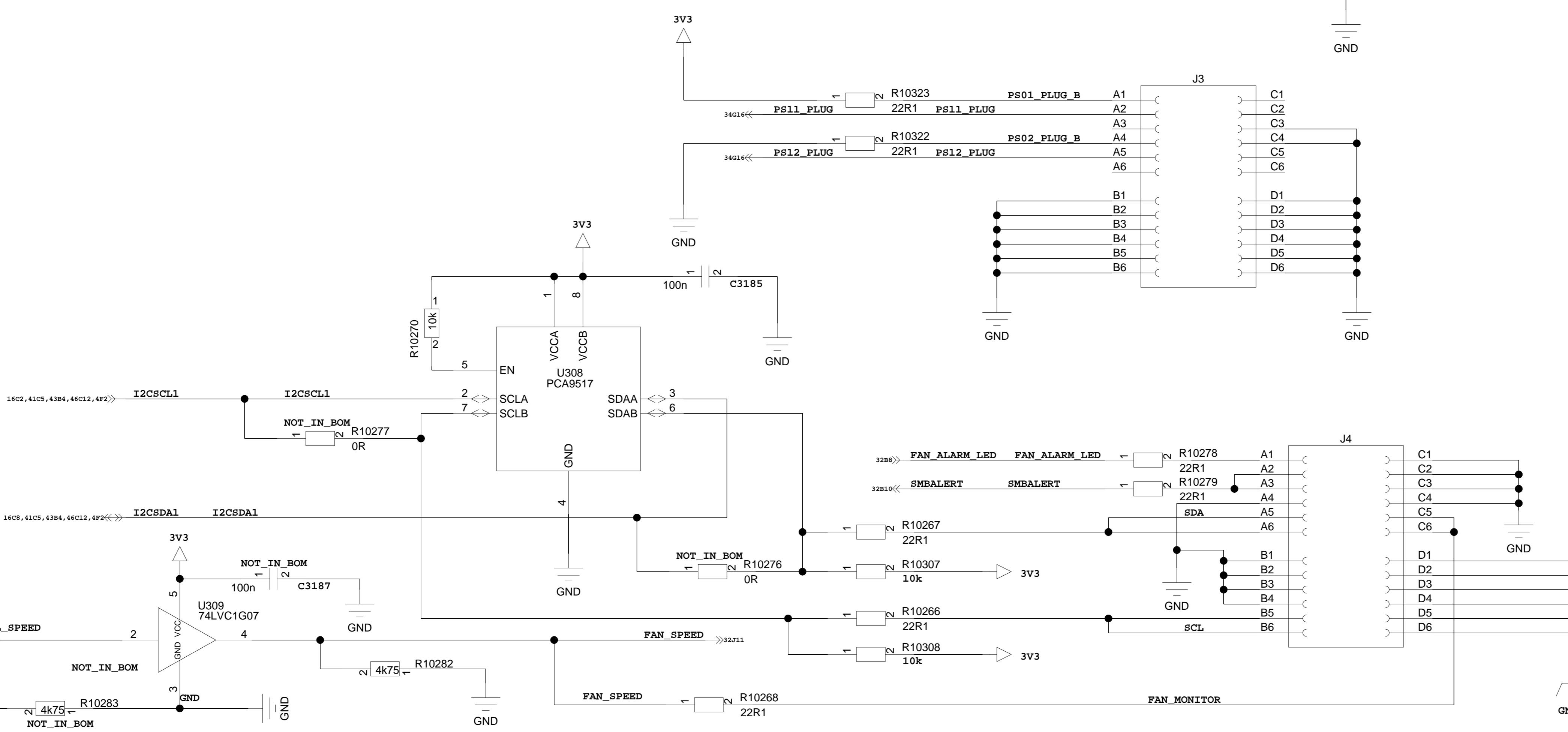
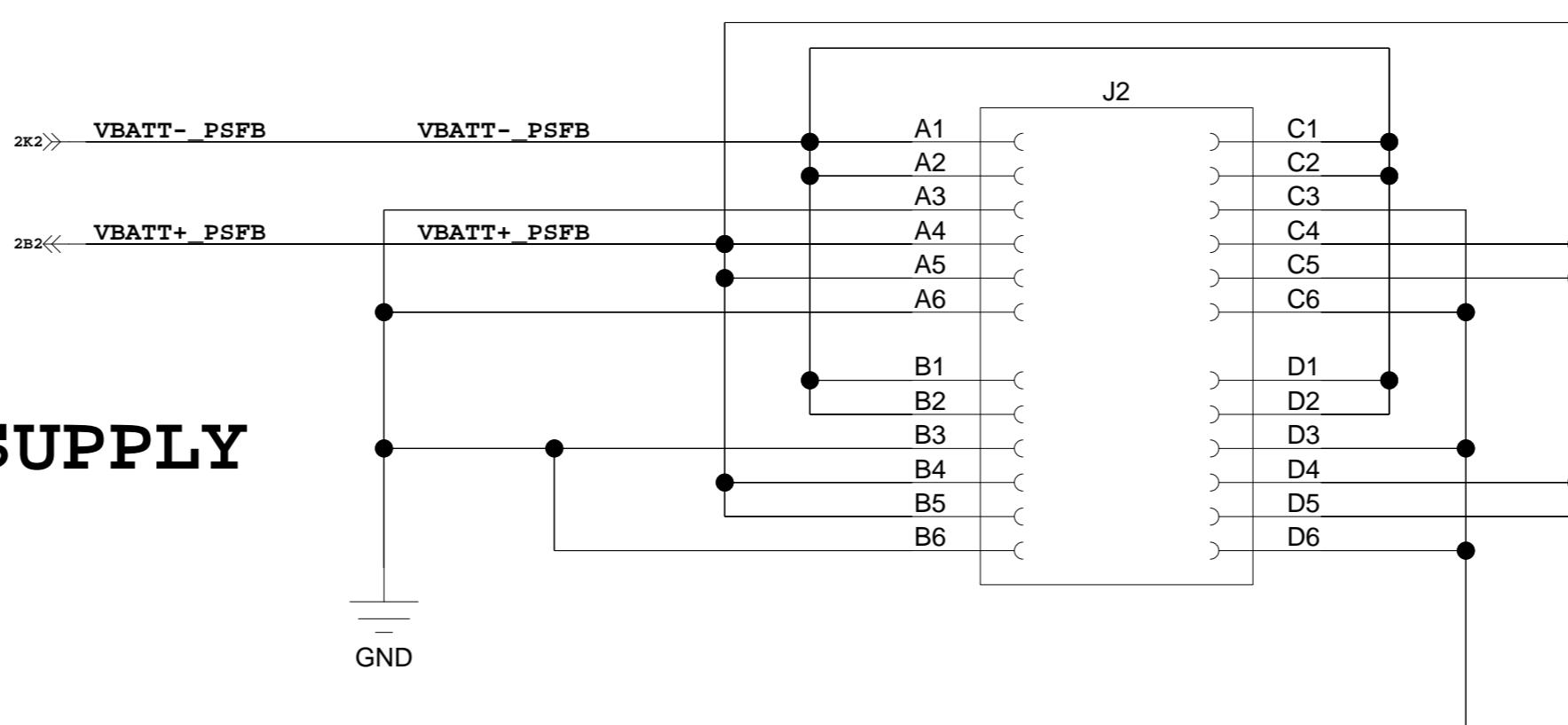
MAIN BOARD BACKPLANE CONNECTOR LOCATION

**J1****J2****J3****J4**

POWER A SUPPLY



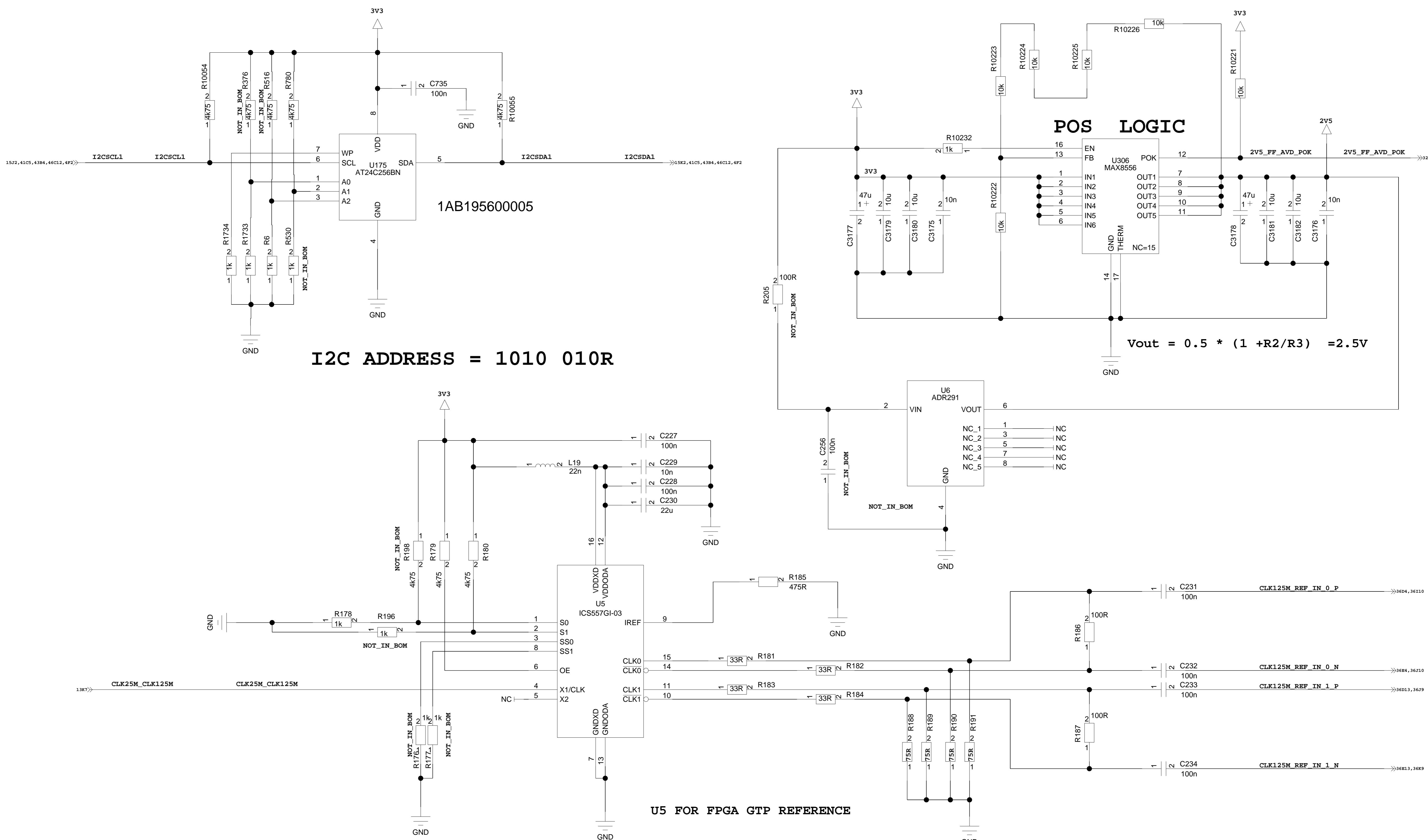
POWER B SUPPLY



BATTERY POWER CONNECTOR

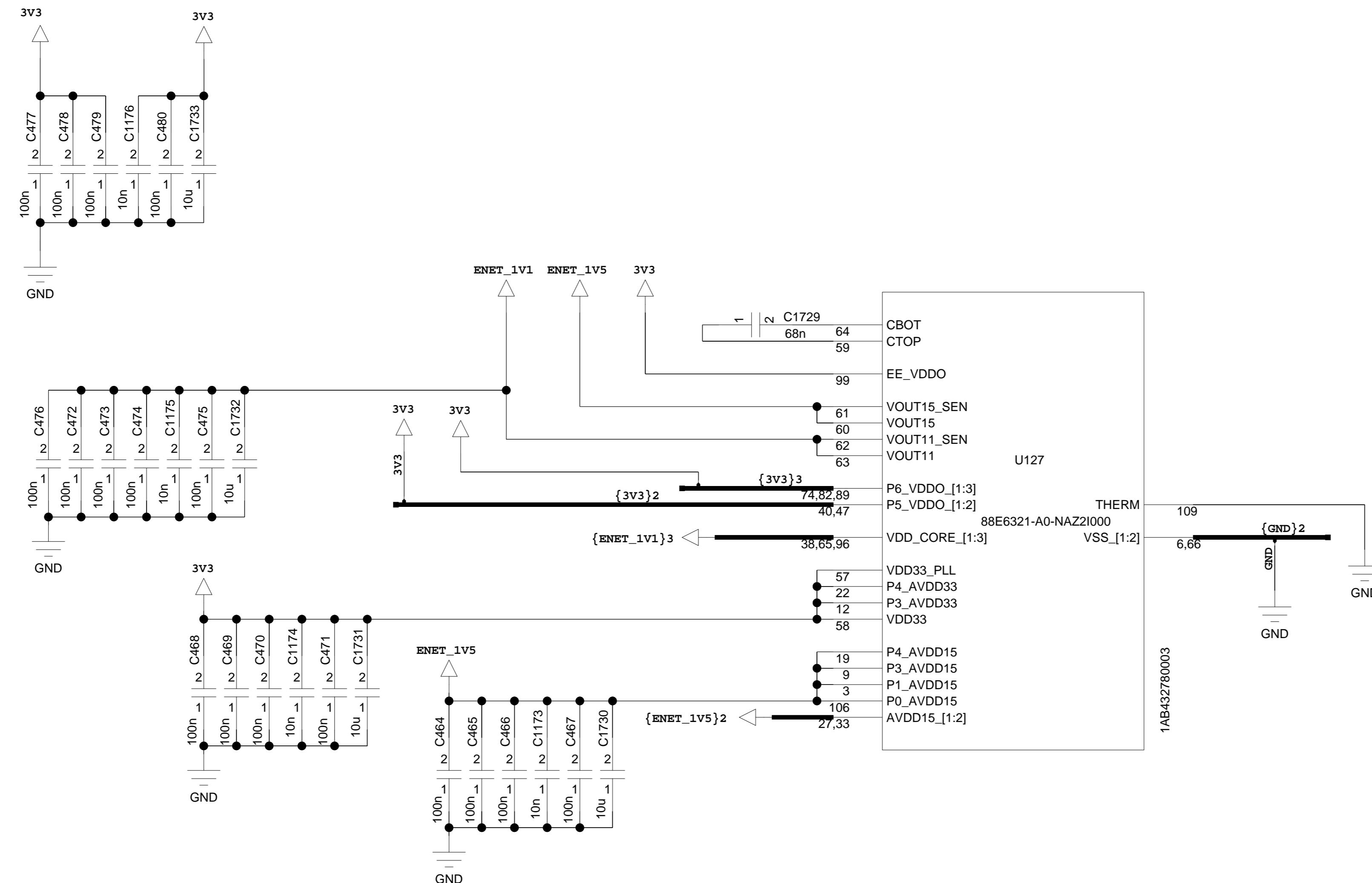
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							15/46

REMOTE INVENTORY, I2C BUS TRANSLATOR & TEST HEADER

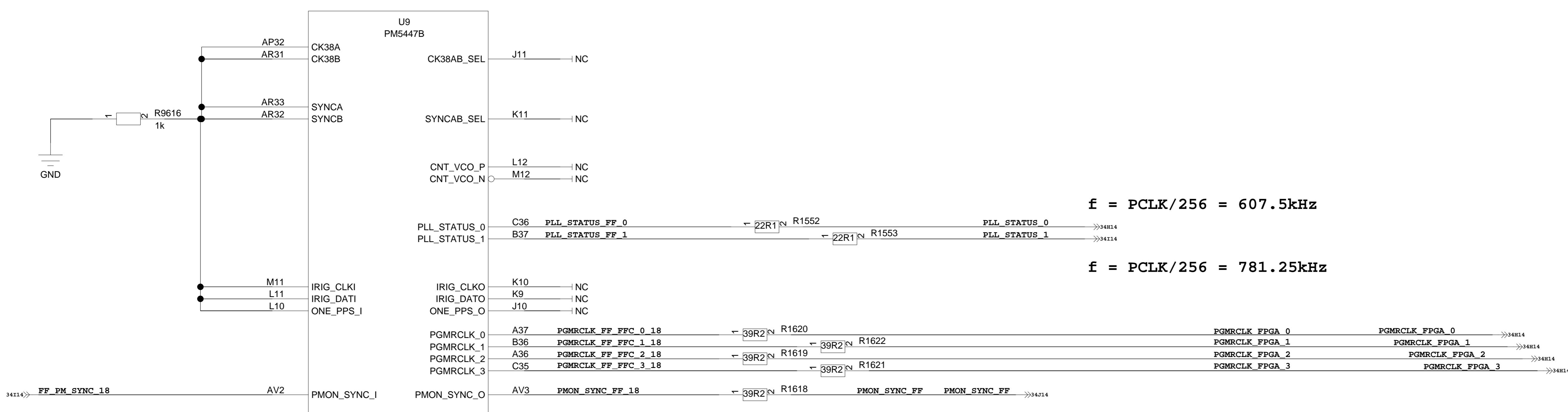


ETHERNET SWITCH POWER

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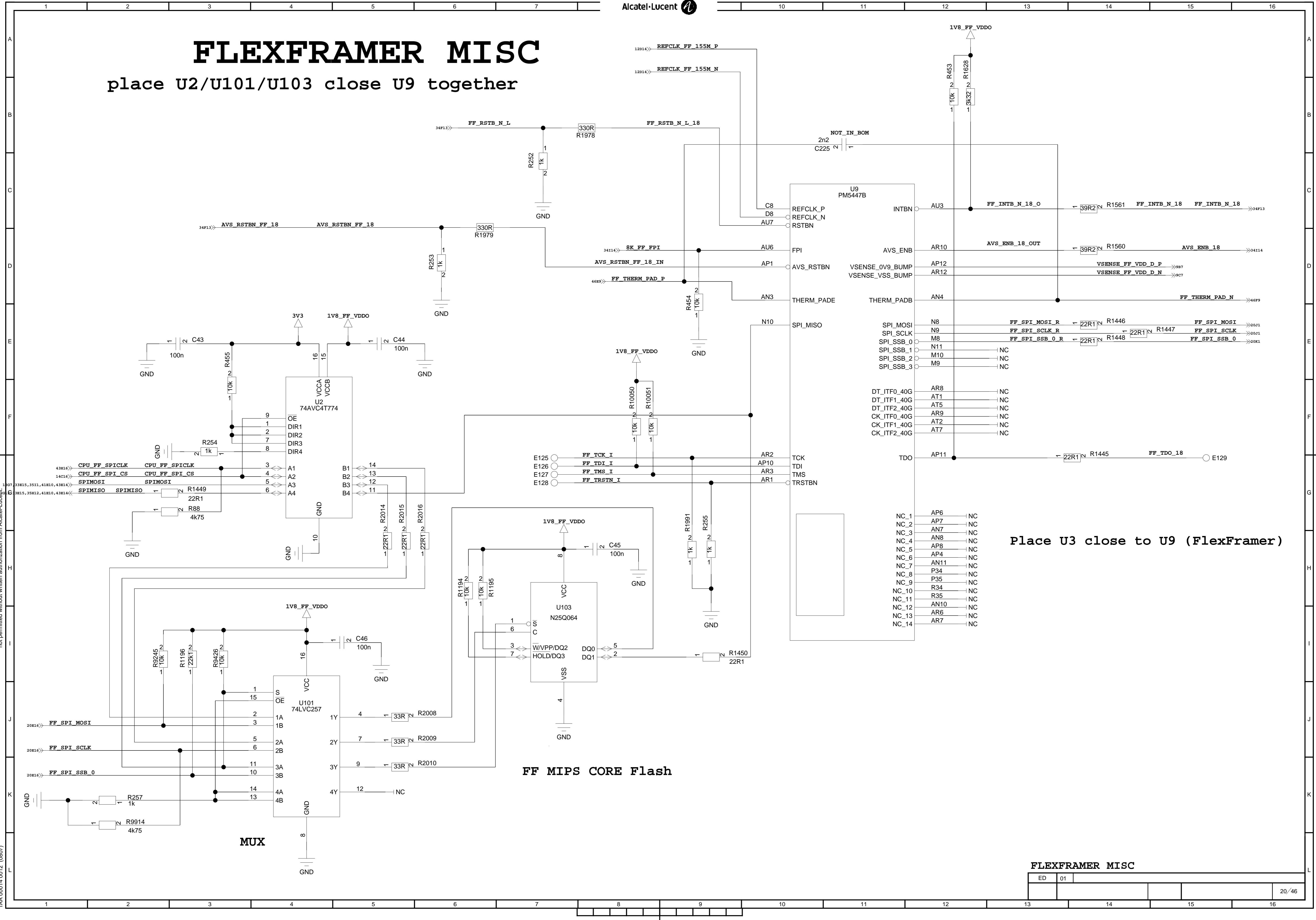
FLEXFRAMER CLK/SYNC/PTP



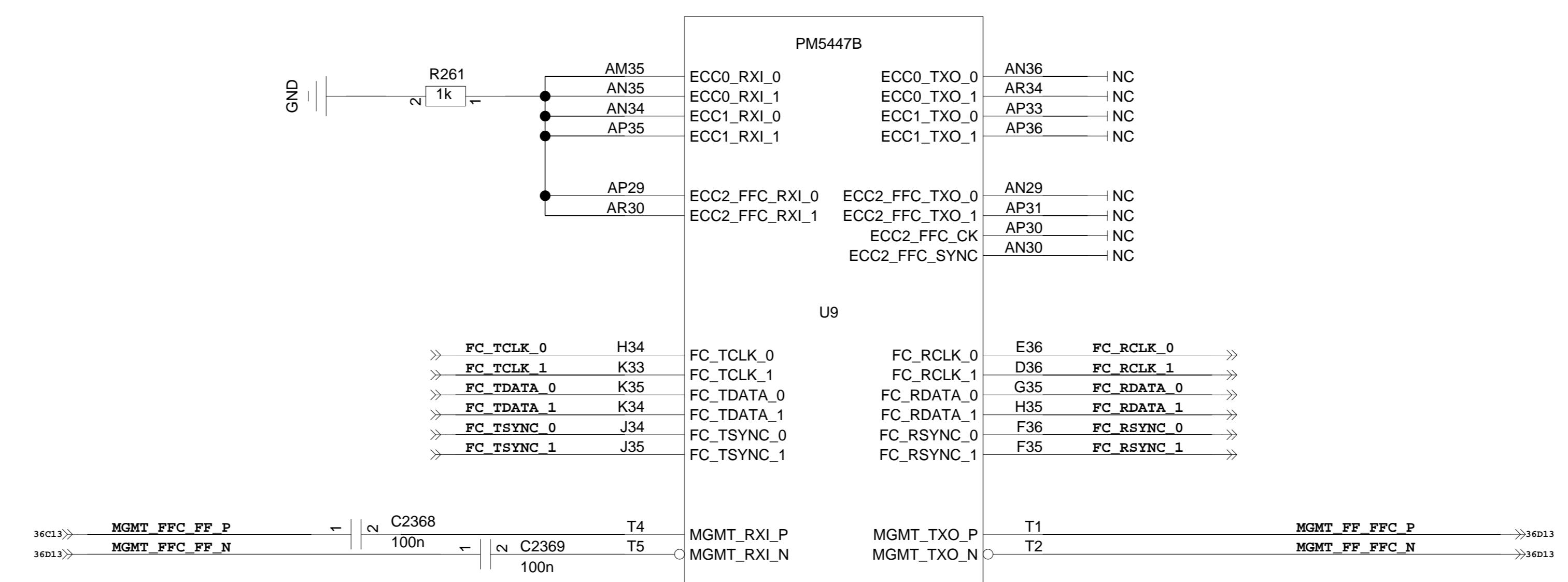
FLEXFRAMER MISC

place U2/U101/U103 close to U9 together

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FLEXFRAMER ECC/FC/MGMT



FLEXFRAMER LINE

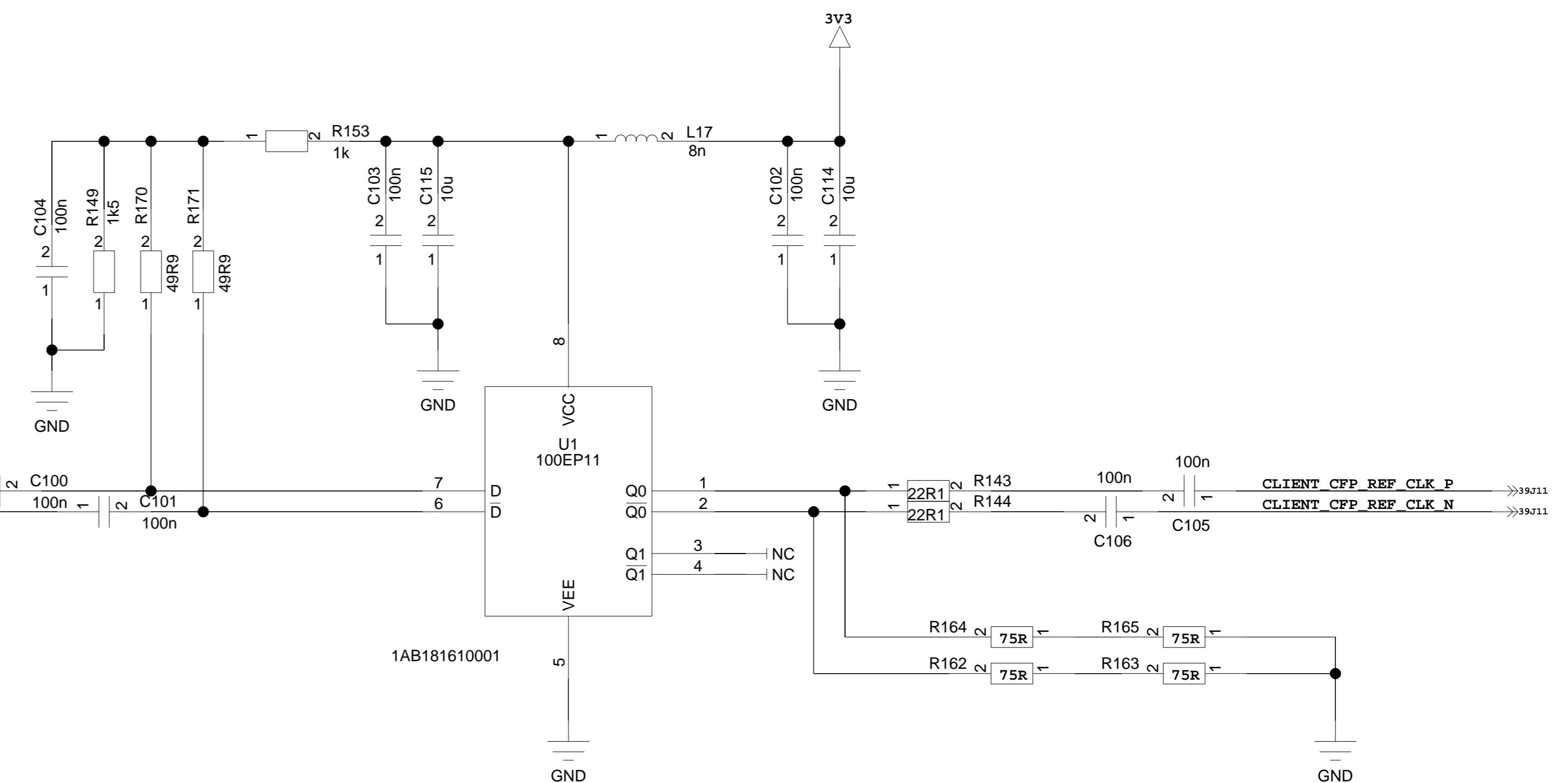
RX DC COUPLING FROM M21036 TX AC COUPLING TO M21036

	U9 PM5447B		
34D13>>	RX_LOS_SFP+_FF_0	RX_LOS_SFP+_FF_0	U10
34D13>>	RX_LOS_SFP+_FF_1	RX_LOS_SFP+_FF_1	T9
34E13>>	RX_LOS_SFP+_FF_2	RX_LOS_SFP+_FF_2	U11
34E13>>	RX_LOS_SFP+_FF_3	RX_LOS_SFP+_FF_3	T11
34E13>>	RX_LOS_SFP+_FF_4	RX_LOS_SFP+_FF_4	T10
34E13>>	RX_LOS_SFP+_FF_5	RX_LOS_SFP+_FF_5	R8
34E13>>	RX_LOS_SFP+_FF_6	RX_LOS_SFP+_FF_6	R10
34E13>>	RX_LOS_SFP+_FF_7	RX_LOS_SFP+_FF_7	R9
34E13>>	RX_LOS_SFP+_FF_8	RX_LOS_SFP+_FF_8	P8
34E13>>	RX_LOS_SFP+_FF_9	RX_LOS_SFP+_FF_9	R11
34E13>>	RX_LOS_SFP+_FF_10	RX_LOS_SFP+_FF_10	P10
34E13>>	RX_LOS_SFP+_FF_11	RX_LOS_SFP+_FF_11	P11

	U9 PM5447B	
LINE_LOS_0	LINE_REFCLK_0_P	L1
LINE_LOS_1	LINE_REFCLK_0_N	C100
LINE_LOS_2	LINE_REFCLK_1_P	100n
LINE_LOS_3	LINE_REFCLK_1_N	C101
LINE_LOS_4	LINE_REFCLK_2_P	100n
LINE_LOS_5	LINE_REFCLK_2_N	C102
LINE_LOS_6	LINE_REFCLK_3_P	100n
LINE_LOS_7	LINE_REFCLK_3_N	C103
LINE_LOS_8	LINE_REFCLK_4_P	100n
LINE_LOS_9	LINE_REFCLK_4_N	C104
LINE_LOS_10	LINE_REFCLK_5_P	100n
LINE_LOS_11	LINE_REFCLK_5_N	C105
	LINE_REFCLK_6_P	100n
	LINE_REFCLK_6_N	C106
	LINE_REFCLK_7_P	100n
	LINE_REFCLK_7_N	C107
	LINE_REFCLK_8_P	100n
	LINE_REFCLK_8_N	C108
	LINE_REFCLK_9_P	100n
	LINE_REFCLK_9_N	C109
	LINE_REFCLK_10_P	100n
	LINE_REFCLK_10_N	C110
	LINE_REFCLK_11_P	100n
	LINE_REFCLK_11_N	C111

	AM5	AM6	AM7	AK5	AK6	AJ6	AJ7	AH5	AH6	AG6	AG7	AE5	AE6	AD6	AD7	AC5	AC6	AC7	AE5	AE6	AE7	AD6	AD7	AC5	AC6	AC7	AB6	AB7	AA5	AA6	Y6	Y7																
40F15>>	LINE_RXI_0_P	LINE_RXI_0_N	LINE_RXI_1_P	LINE_RXI_1_N	LINE_RXI_2_P	LINE_RXI_2_N	LINE_RXI_3_P	LINE_RXI_3_N	LINE_RXI_4_P	LINE_RXI_4_N	LINE_RXI_5_P	LINE_RXI_5_N	LINE_RXI_6_P	LINE_RXI_6_N	LINE_RXI_7_P	LINE_RXI_7_N	LINE_RXI_8_P	LINE_RXI_8_N	LINE_RXI_9_P	LINE_RXI_9_N	LINE_RXI_10_P	LINE_RXI_10_N	LINE_RXI_11_P	LINE_RXI_11_N	LINE_RXI_0_P	LINE_RXI_0_N	LINE_RXI_1_P	LINE_RXI_1_N	LINE_RXI_2_P	LINE_RXI_2_N	LINE_RXI_3_P	LINE_RXI_3_N	LINE_RXI_4_P	LINE_RXI_4_N	LINE_RXI_5_P	LINE_RXI_5_N	LINE_RXI_6_P	LINE_RXI_6_N	LINE_RXI_7_P	LINE_RXI_7_N	LINE_RXI_8_P	LINE_RXI_8_N	LINE_RXI_9_P	LINE_RXI_9_N	LINE_RXI_10_P	LINE_RXI_10_N	LINE_RXI_11_P	LINE_RXI_11_N

	AM1	AM2	AL2	AL3	AK1	AK2	AJ2	AJ3	AH1	AH2	AG2	AG3	AE1	AE2	AD2	AD3	AC1	AC2	AC3	AE1	AE2	AD2	AD3	AC1	AC2	AC3	AB2	AB3	AA1	AA2	Y2	Y3								
	LINE_RXO_0_P	1	2	2	100n	1	2	2	100n	1	2	100n	1	2	2	100n	1	2	2	100n	1	2	2	100n																



FLEXFRAMER LINE

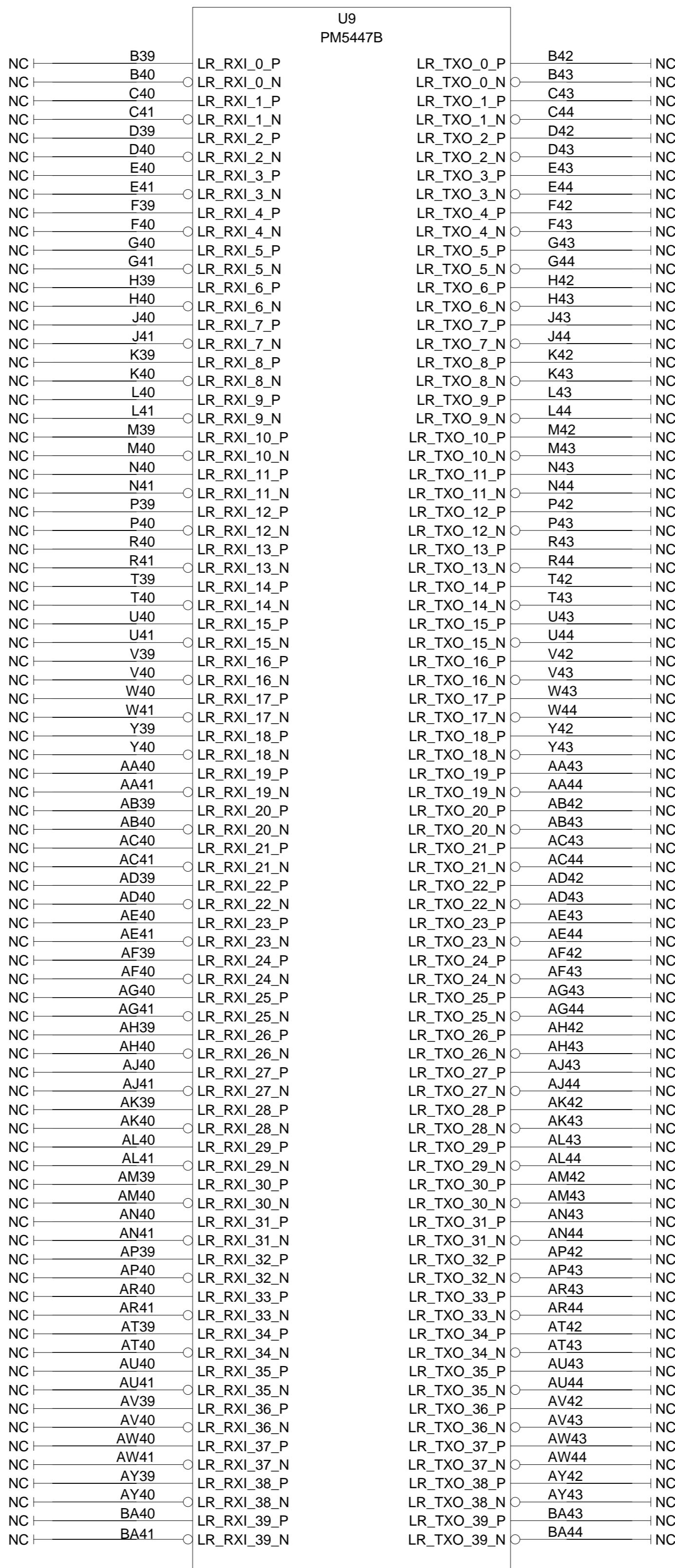
FLEXFRAMER BACKPLANE LR

LR 0

LR 0

LR 1

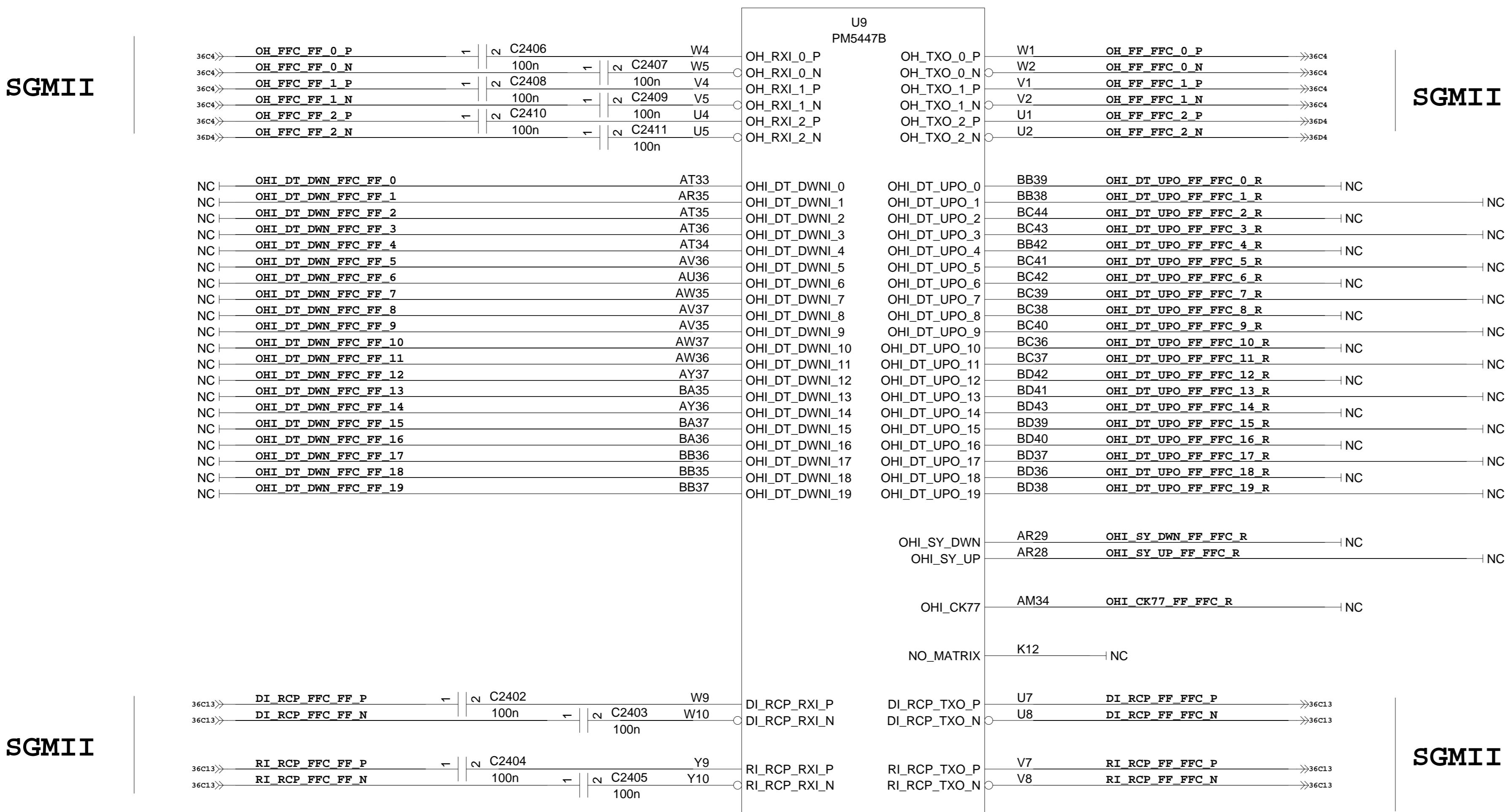
LR 1



FLEXFRAMER BACKPLANE LR

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23/46				

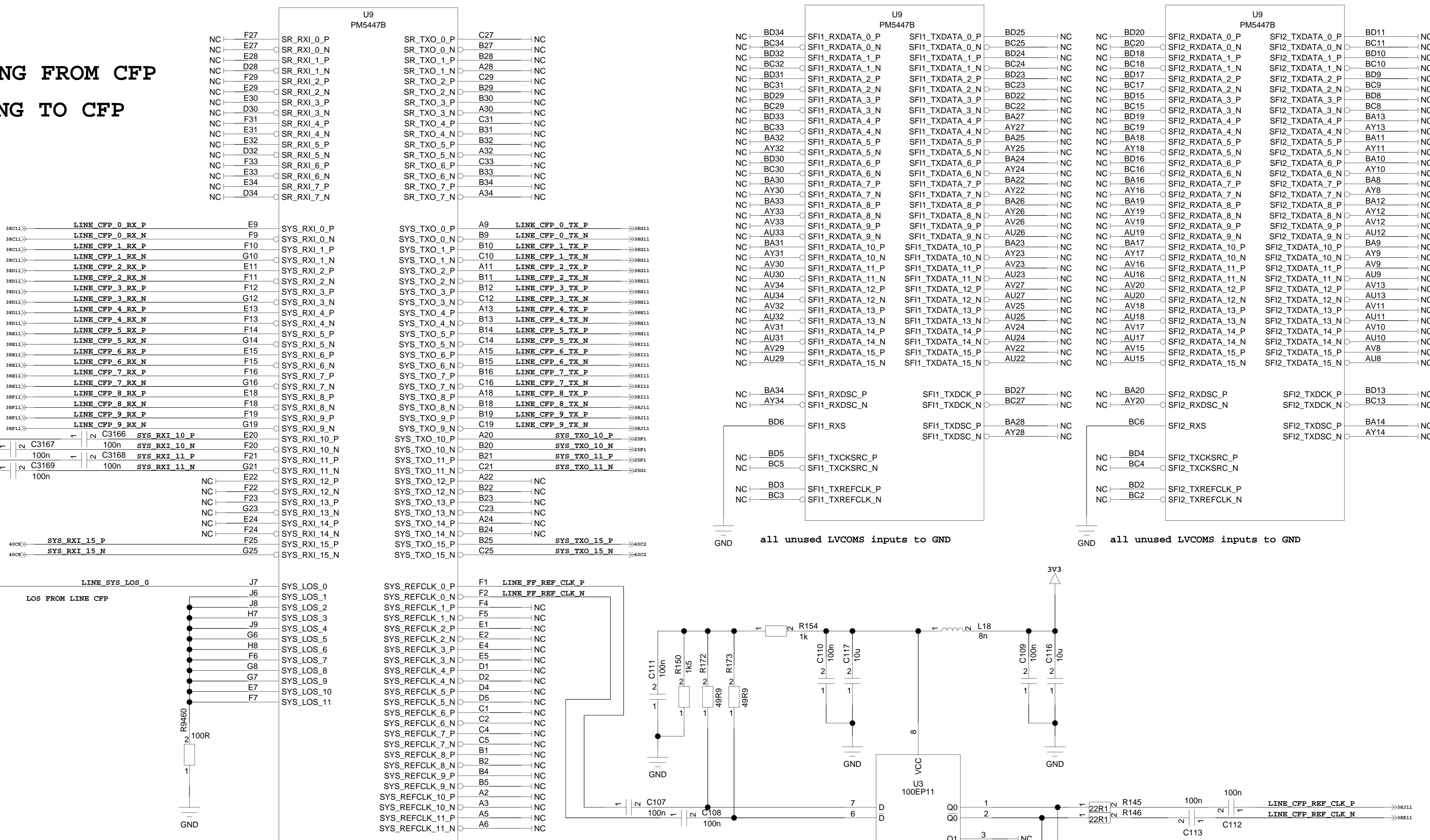
FLEXFRAMER OH/OHI



FLEXFRAMER SFI-5.1/SYS/SR

RX AC COUPLING FROM CFP

TX AC COUPLING TO CFP

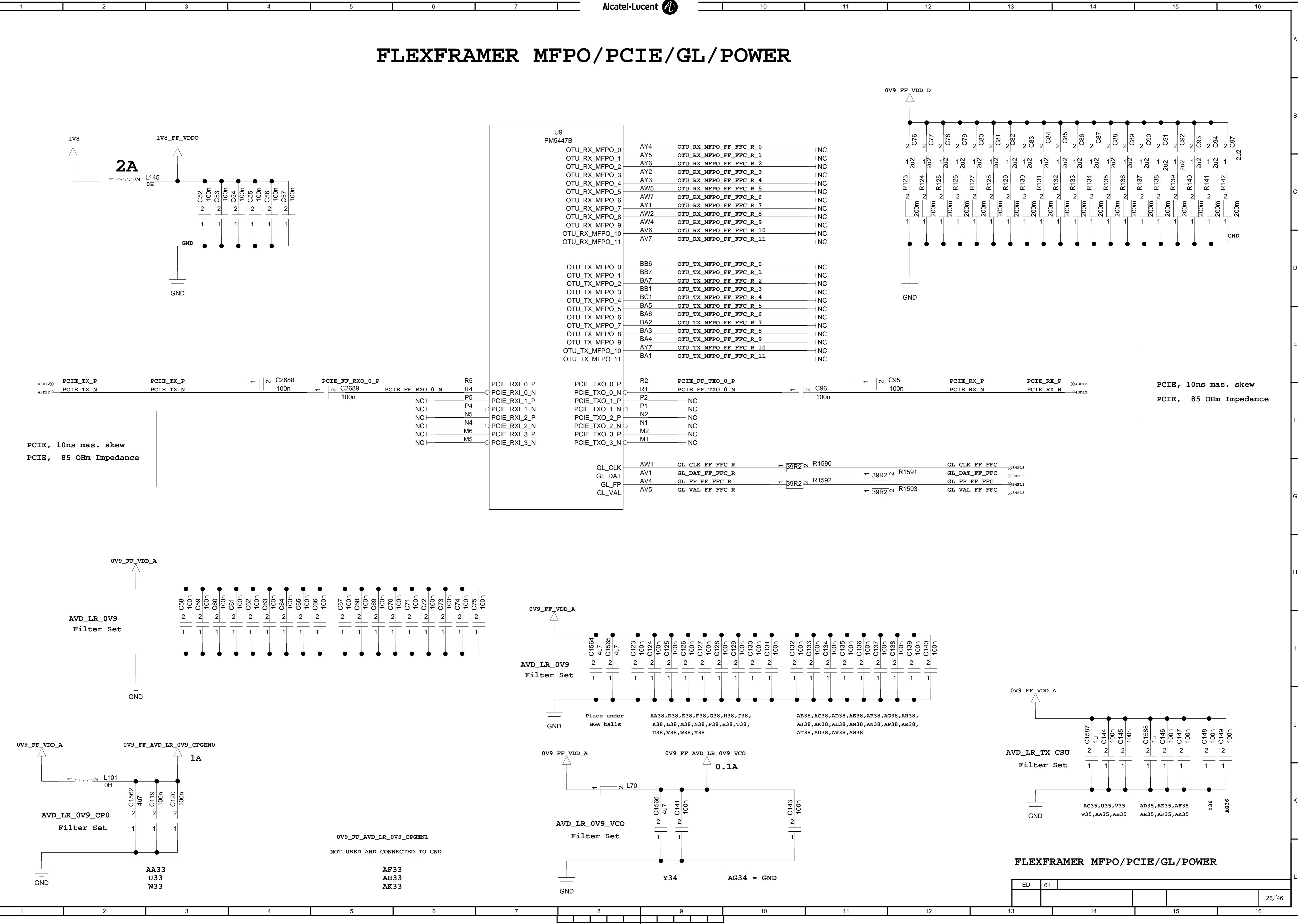


FLEXFRAMER SFI-5.1/SYS/SR

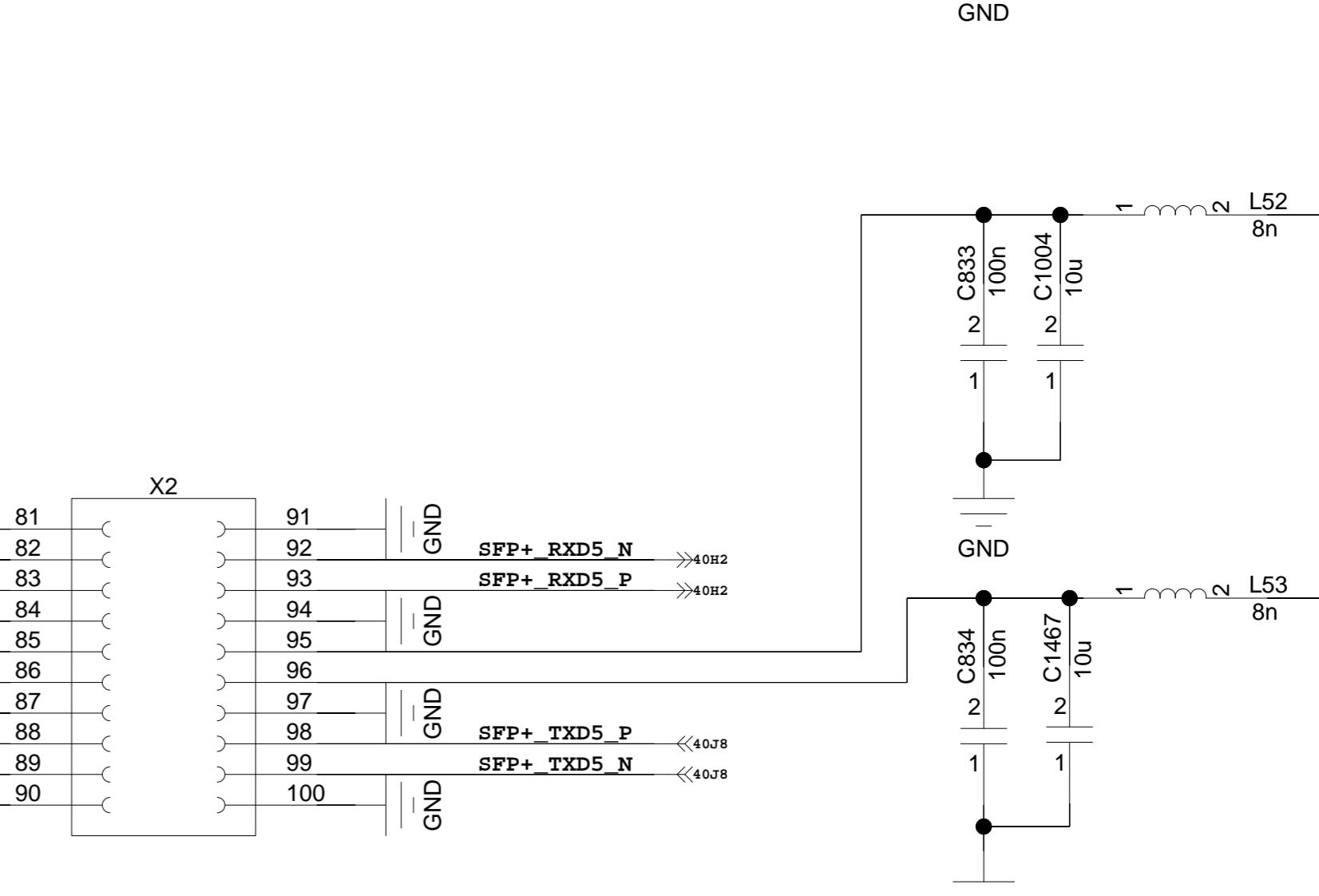
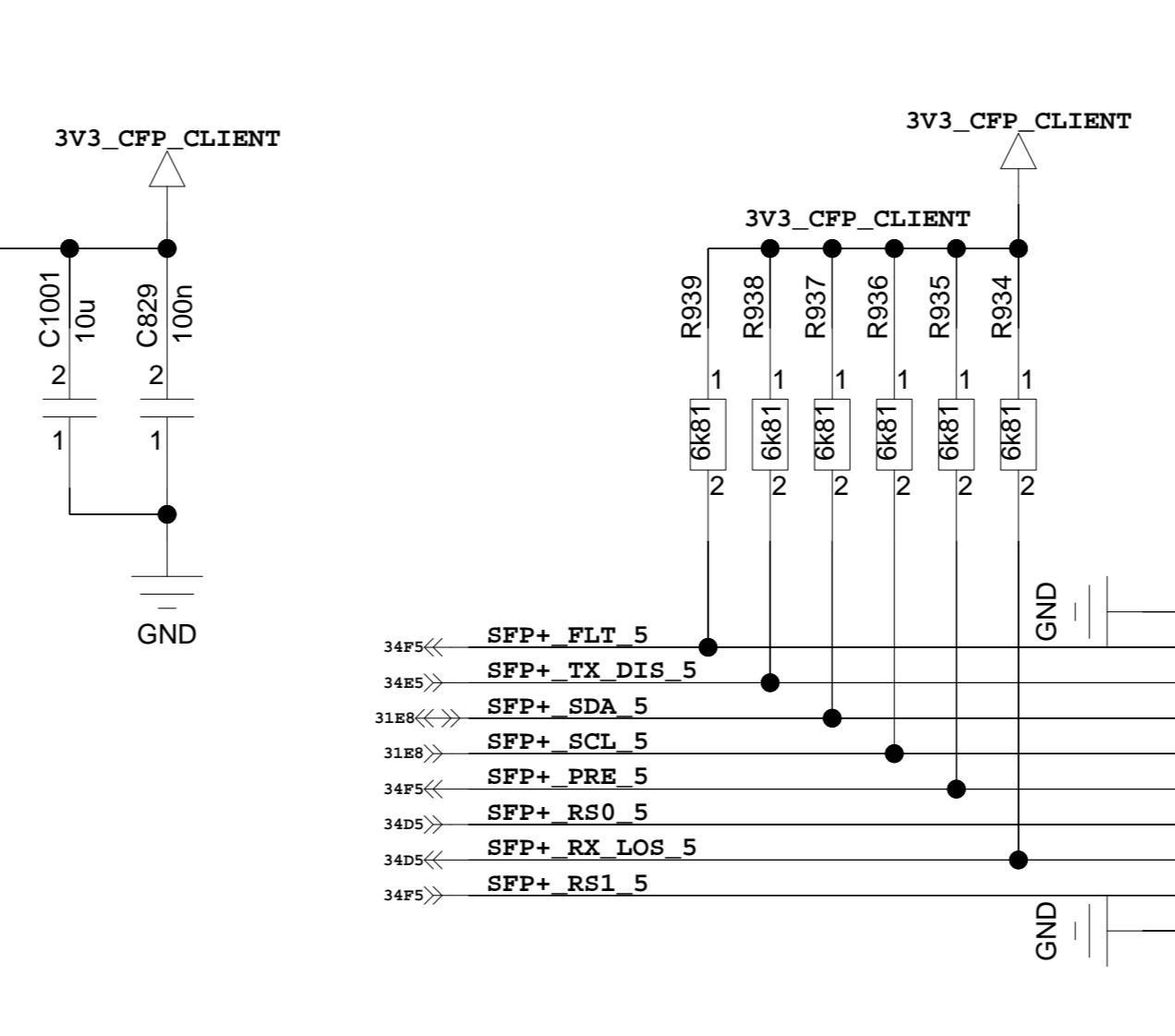
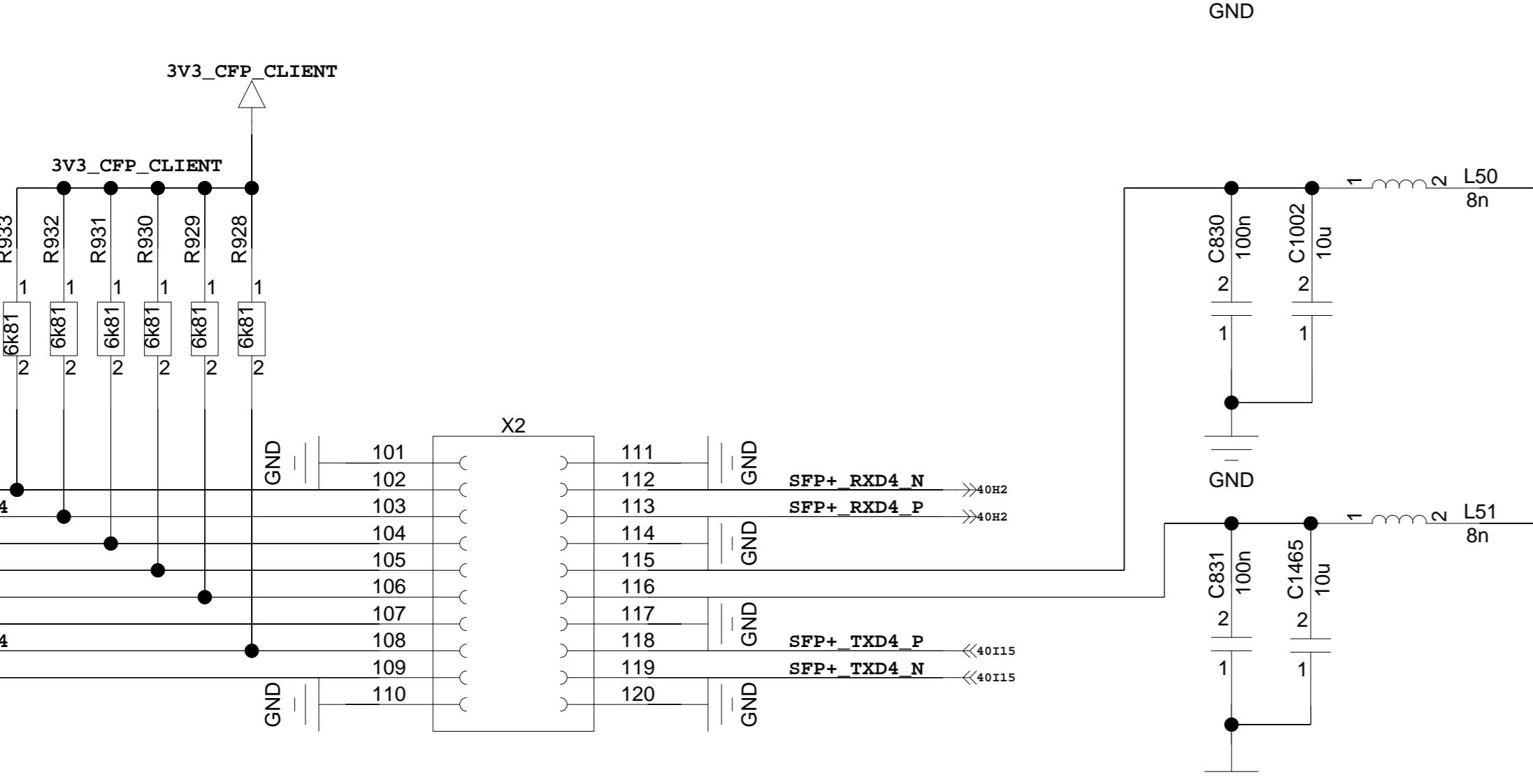
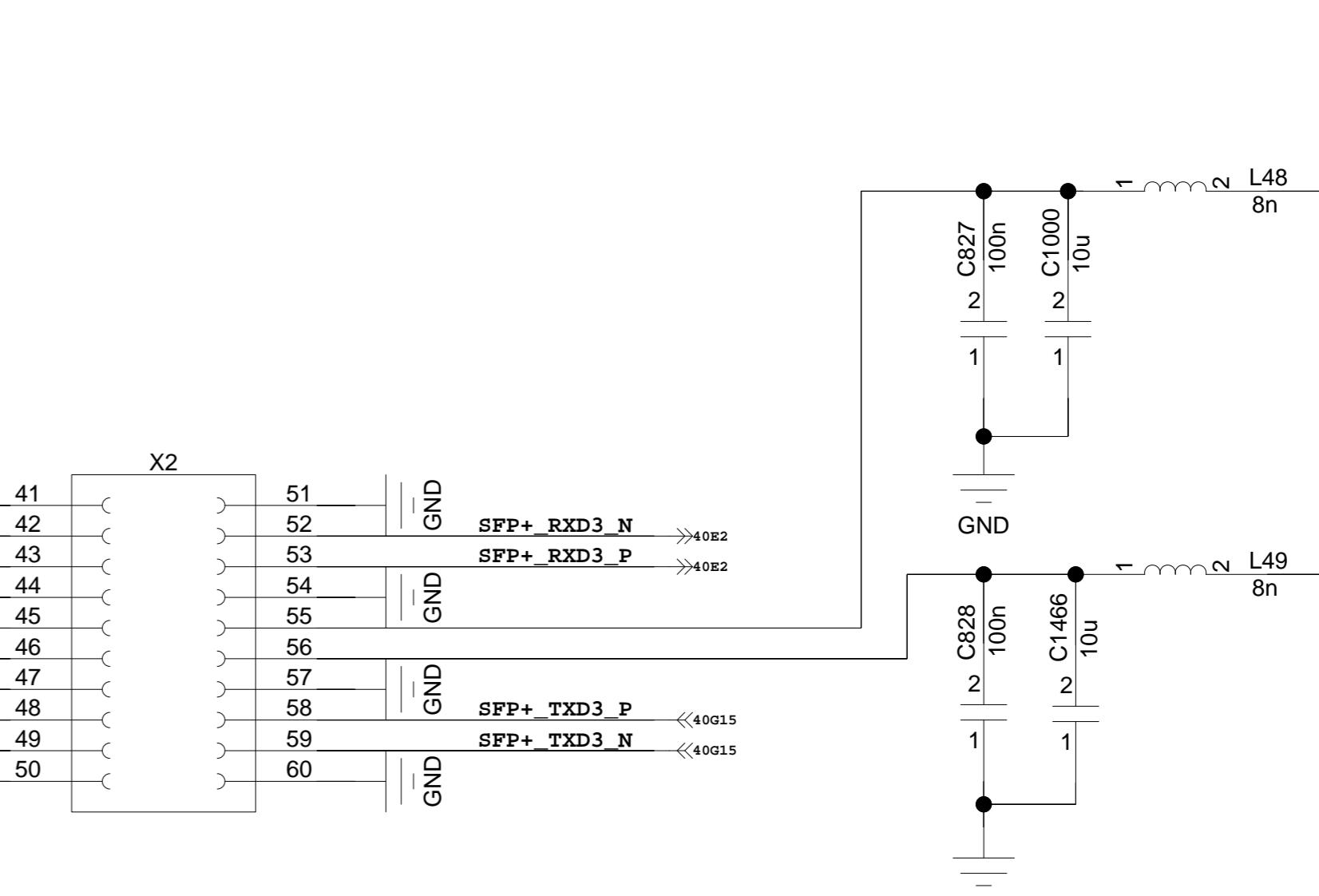
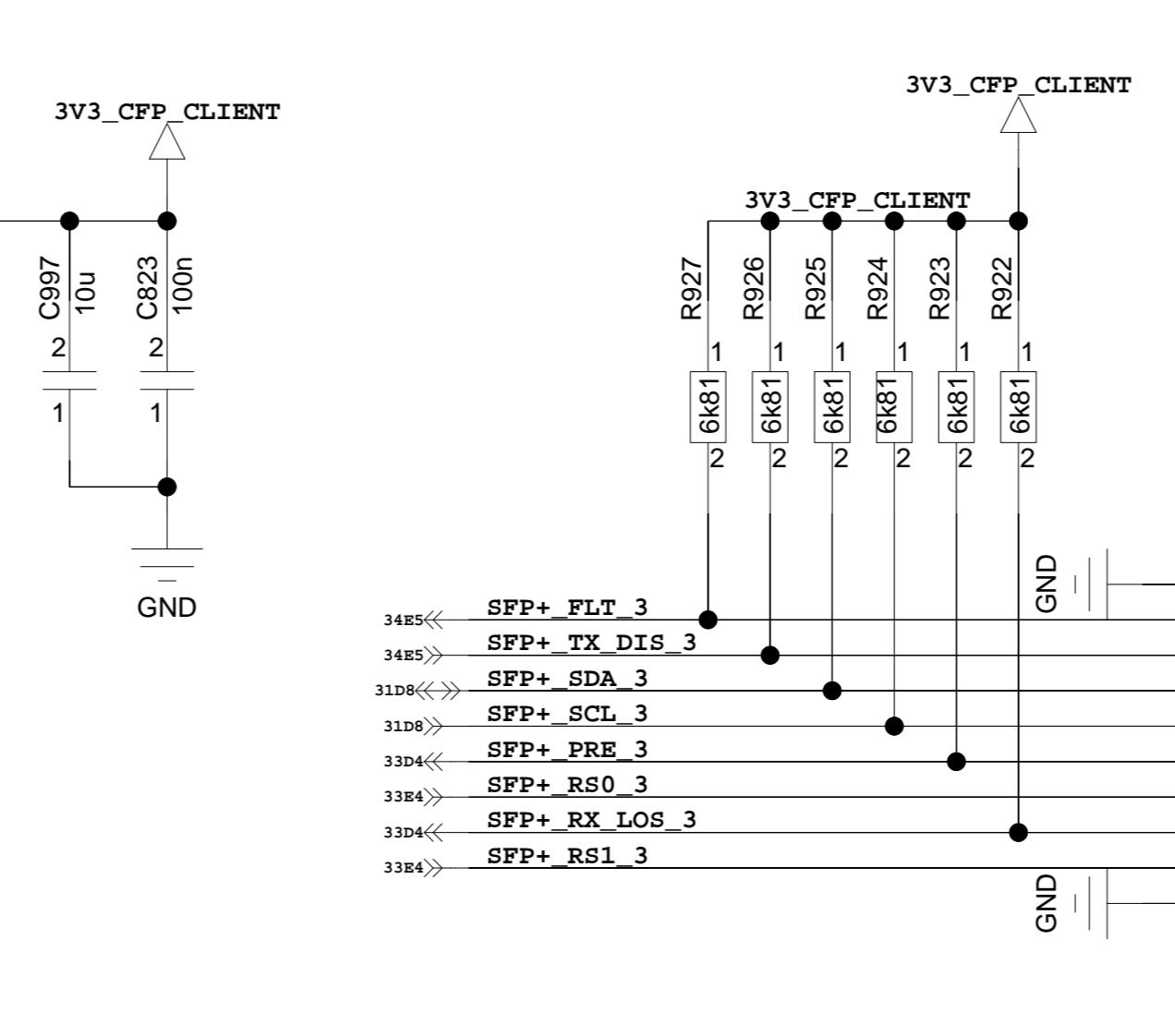
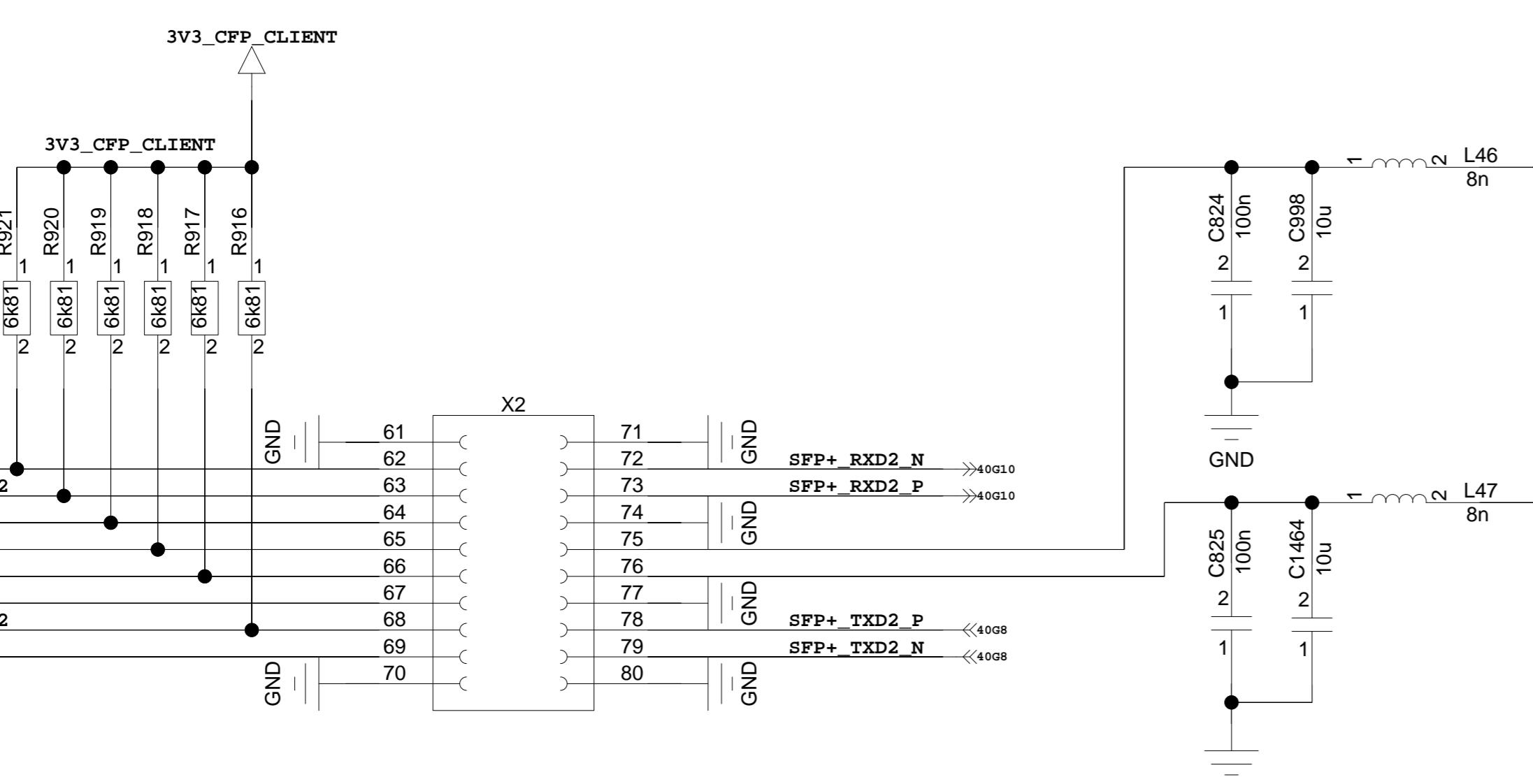
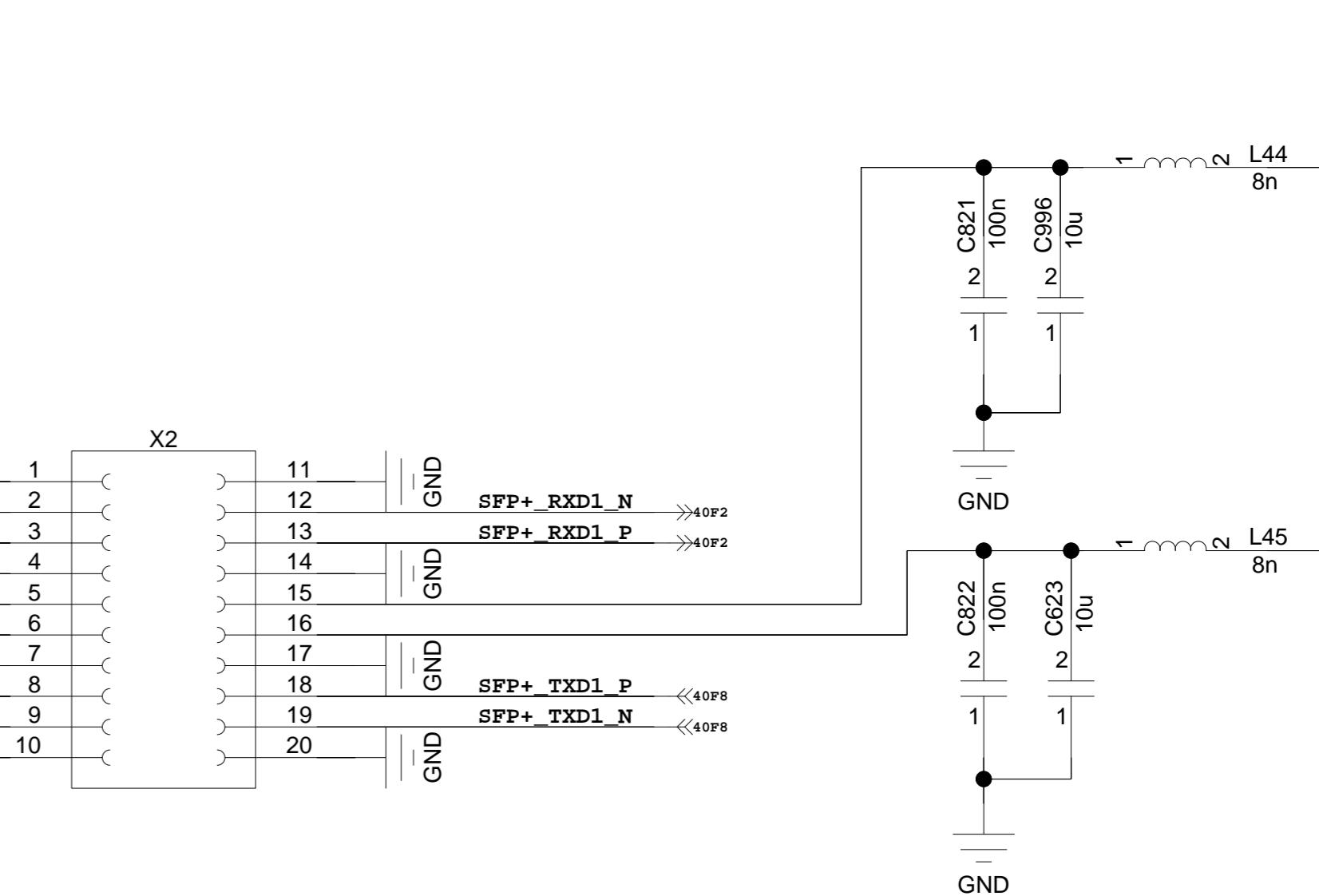
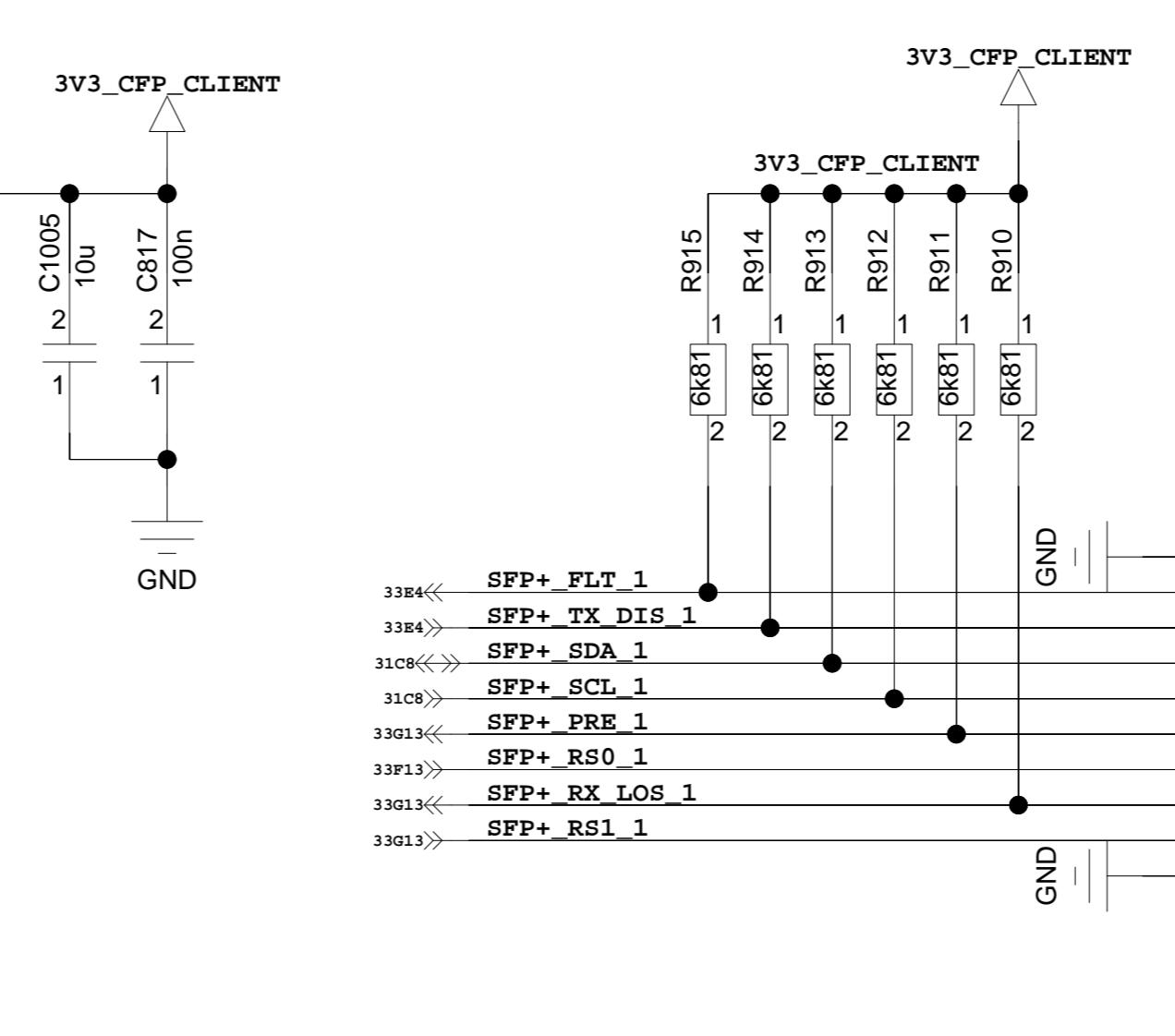
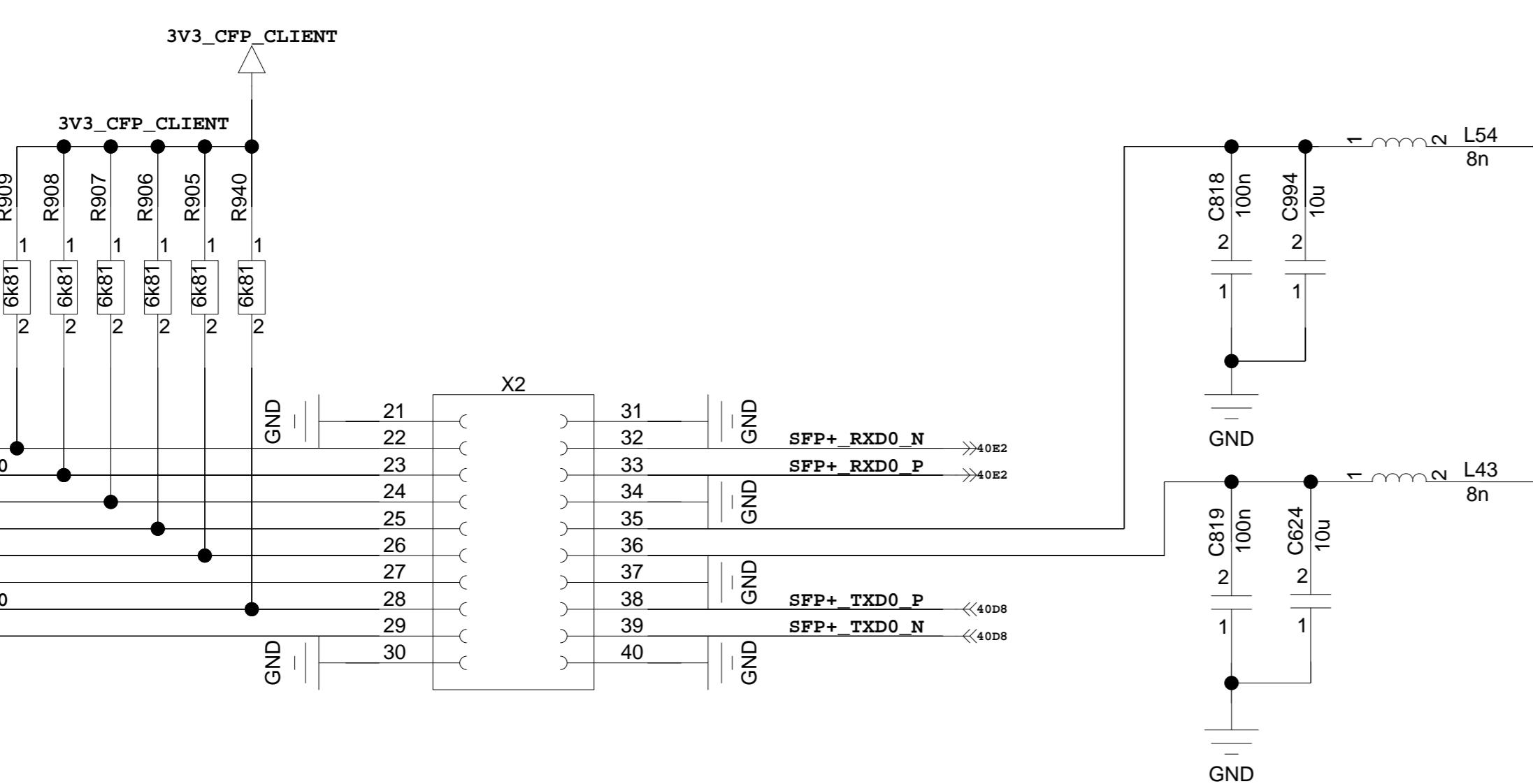
ED 01 | 25/

FLEXFRAMER MFPO/PCIE/GL/POWER

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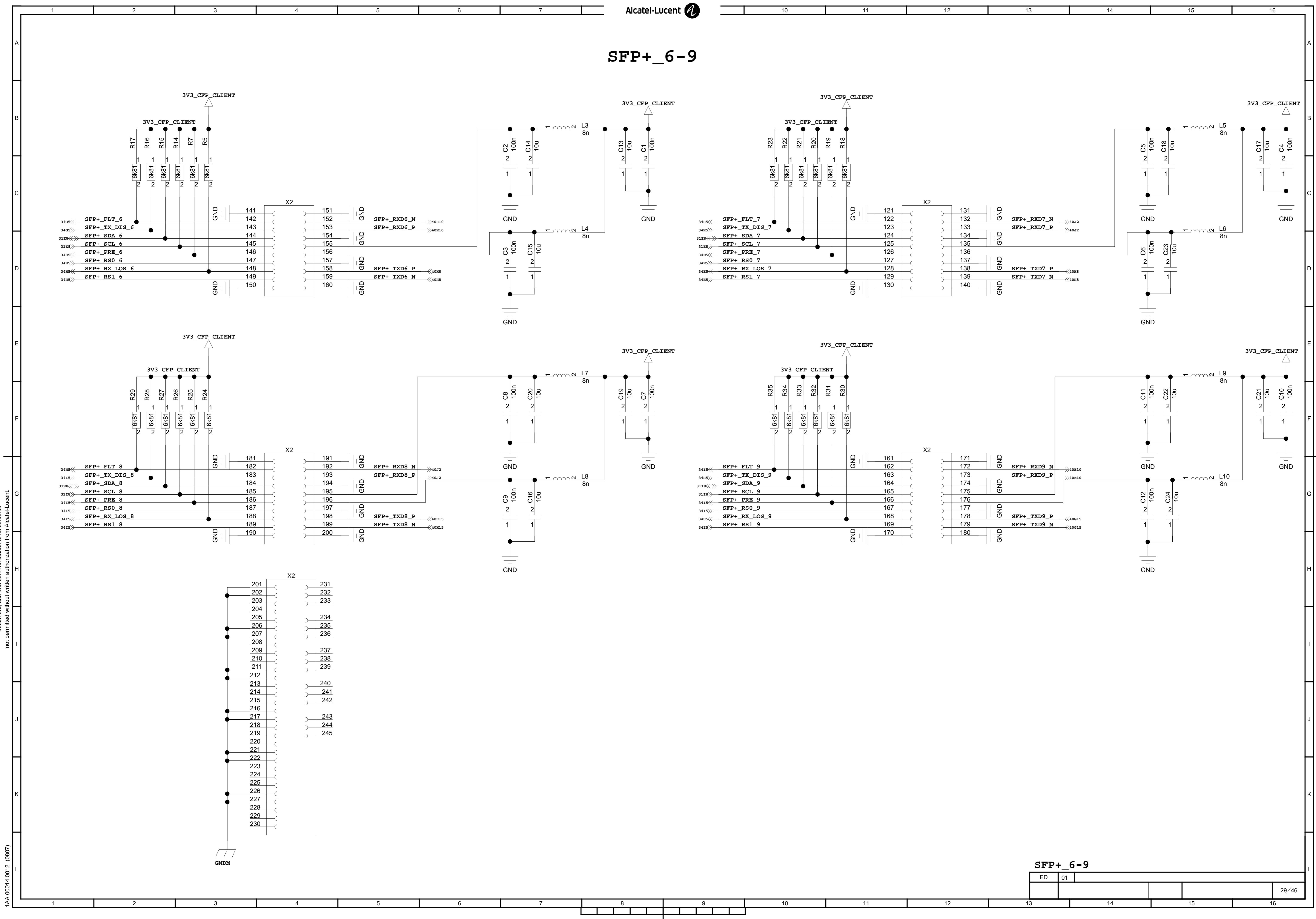


SFP+_0-5



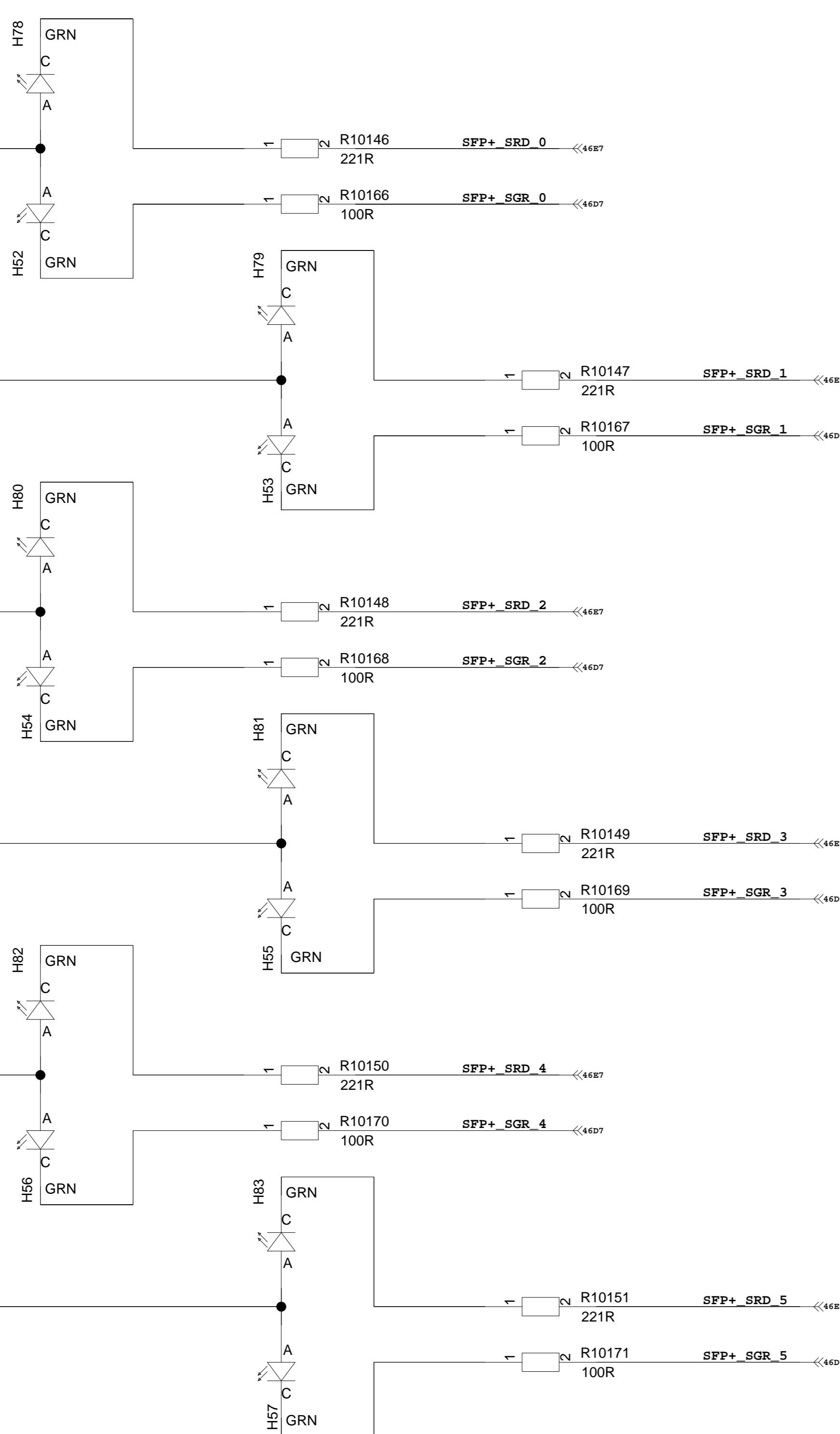
SFP+_0-5

SFP+_6-9

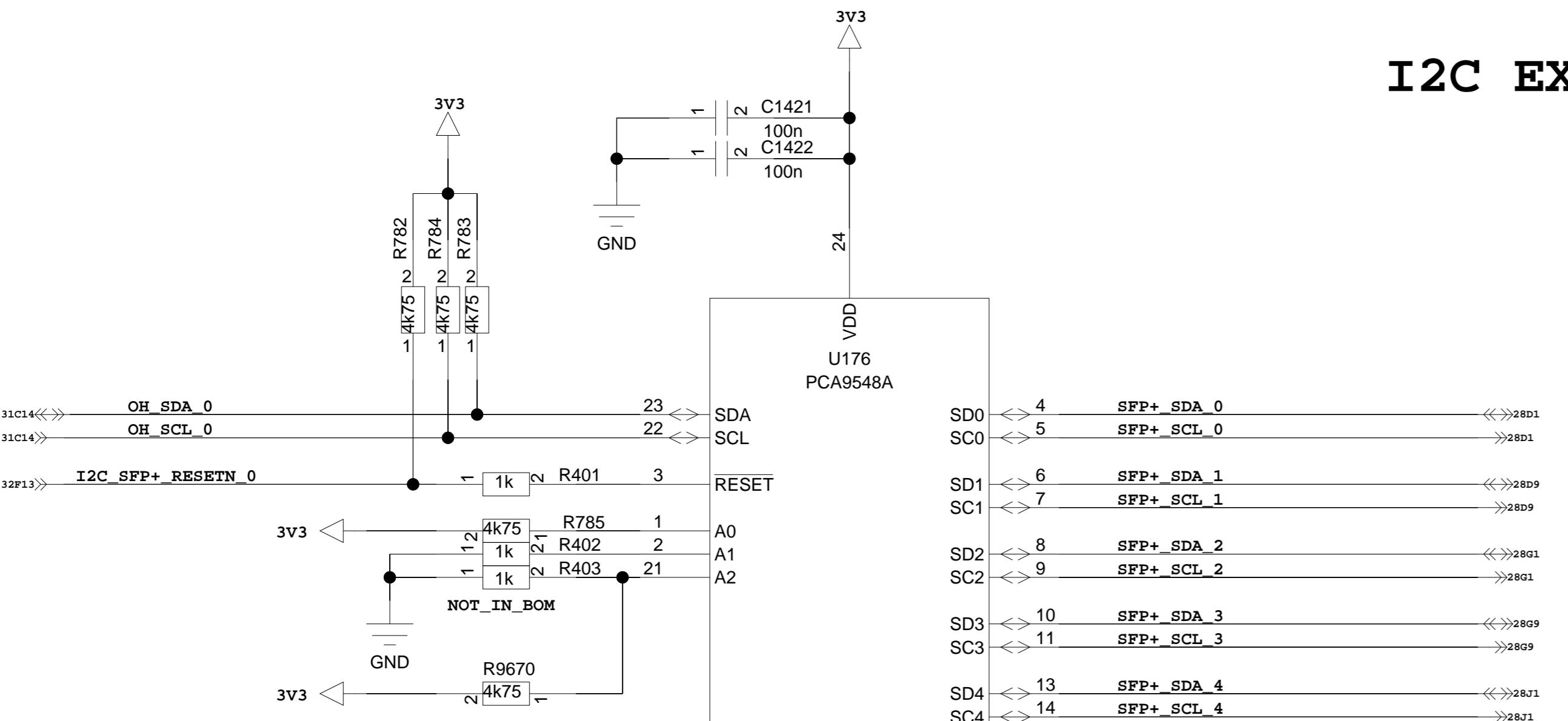


SFP+ LINK/PORT LEDS PART 1

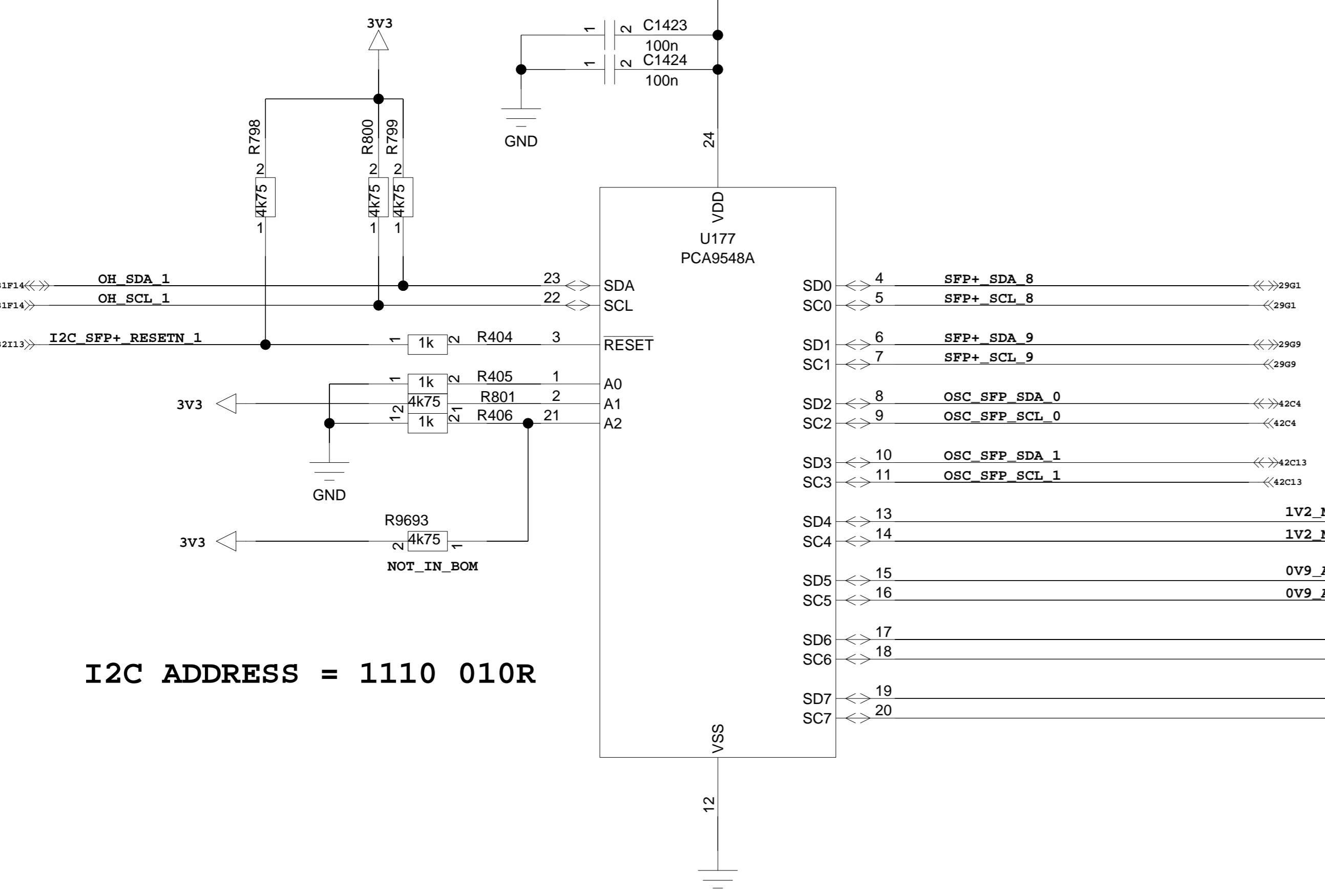
STATUS LEDS



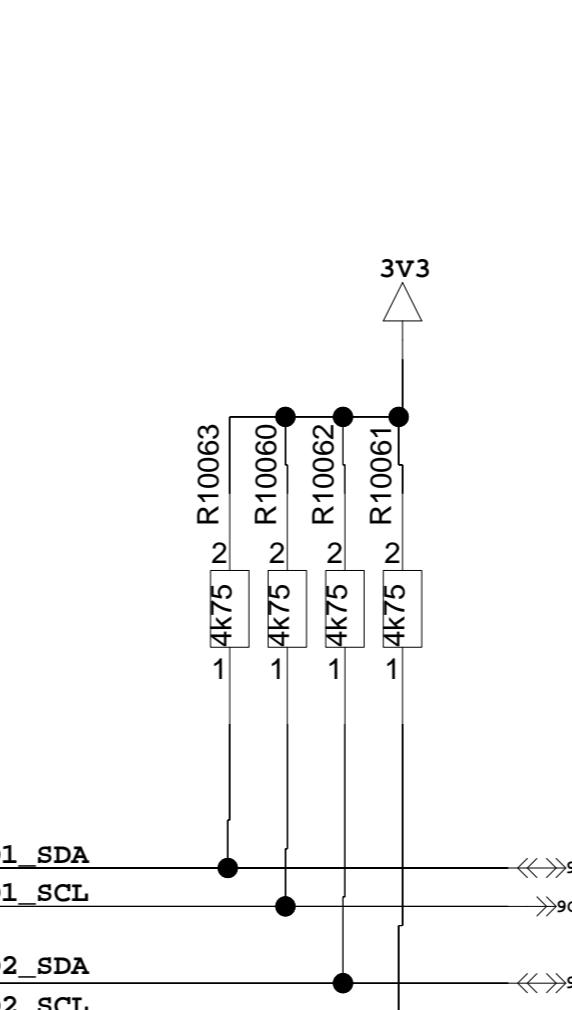
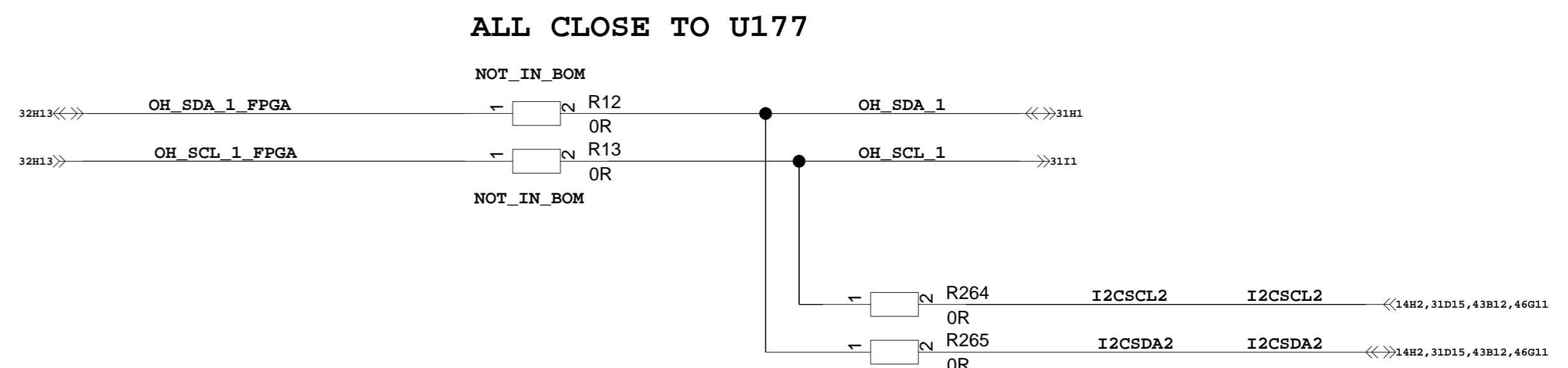
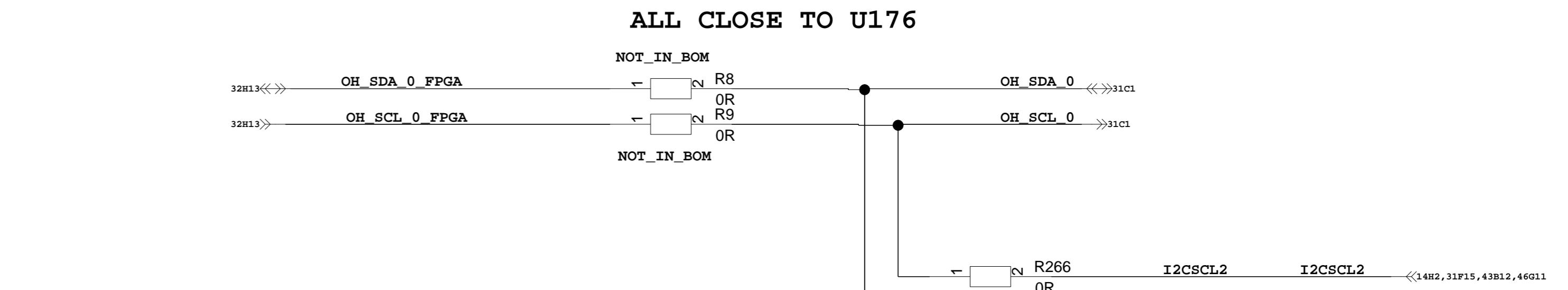
I2C EXPANDERS



I2C ADDRESS = 1110 101R



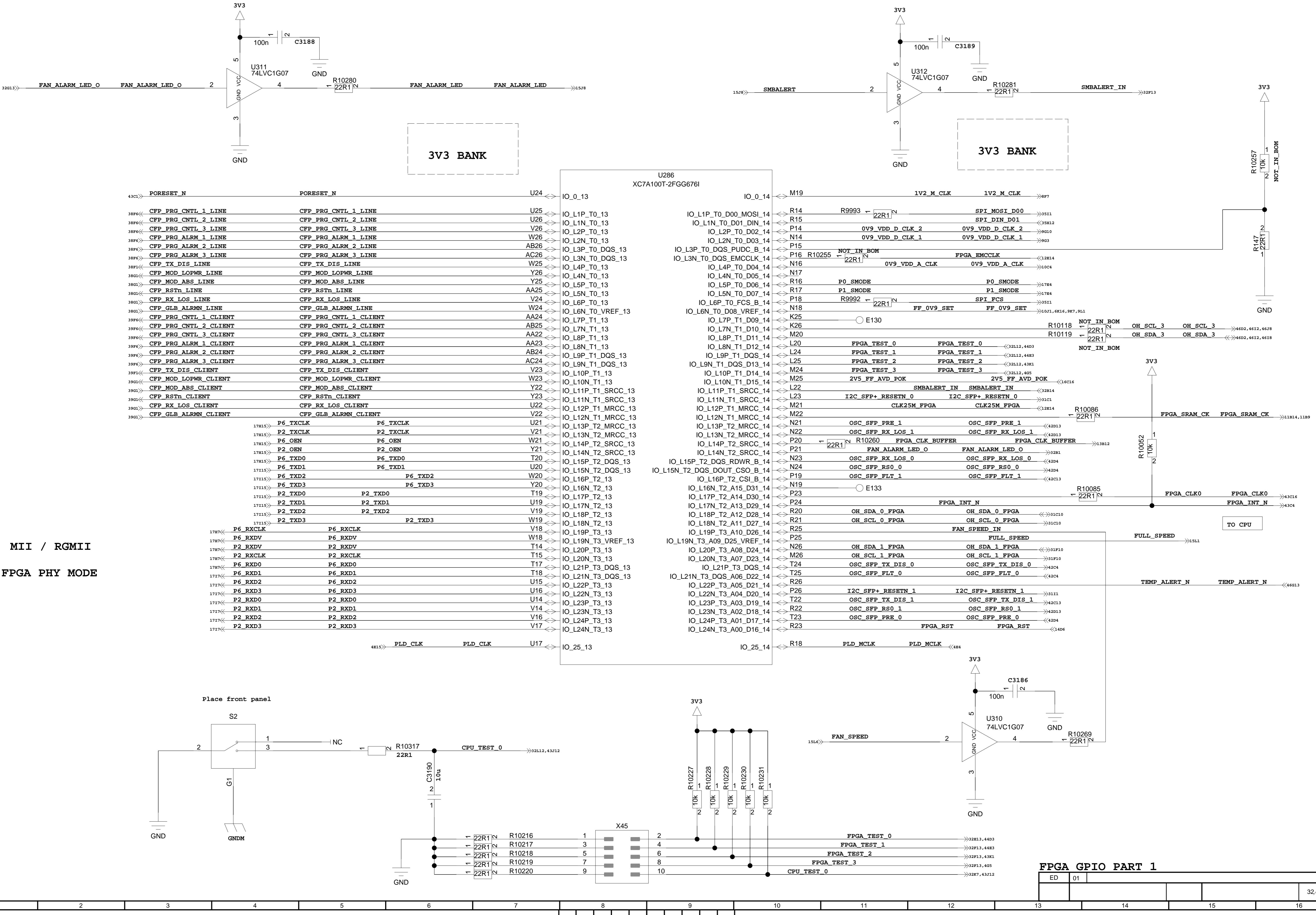
I2C ADDRESS = 1110 010R



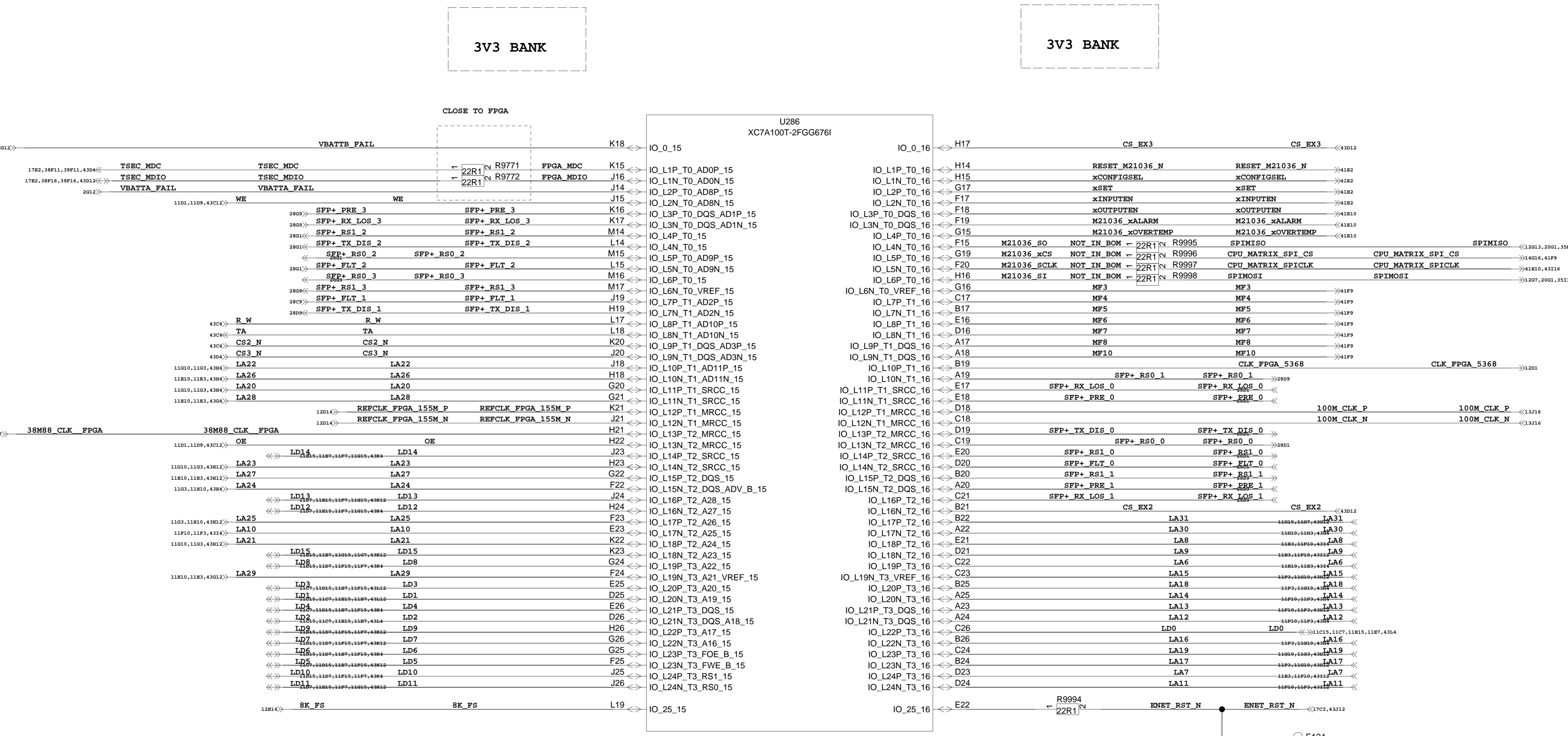
I²C EXPANDERS

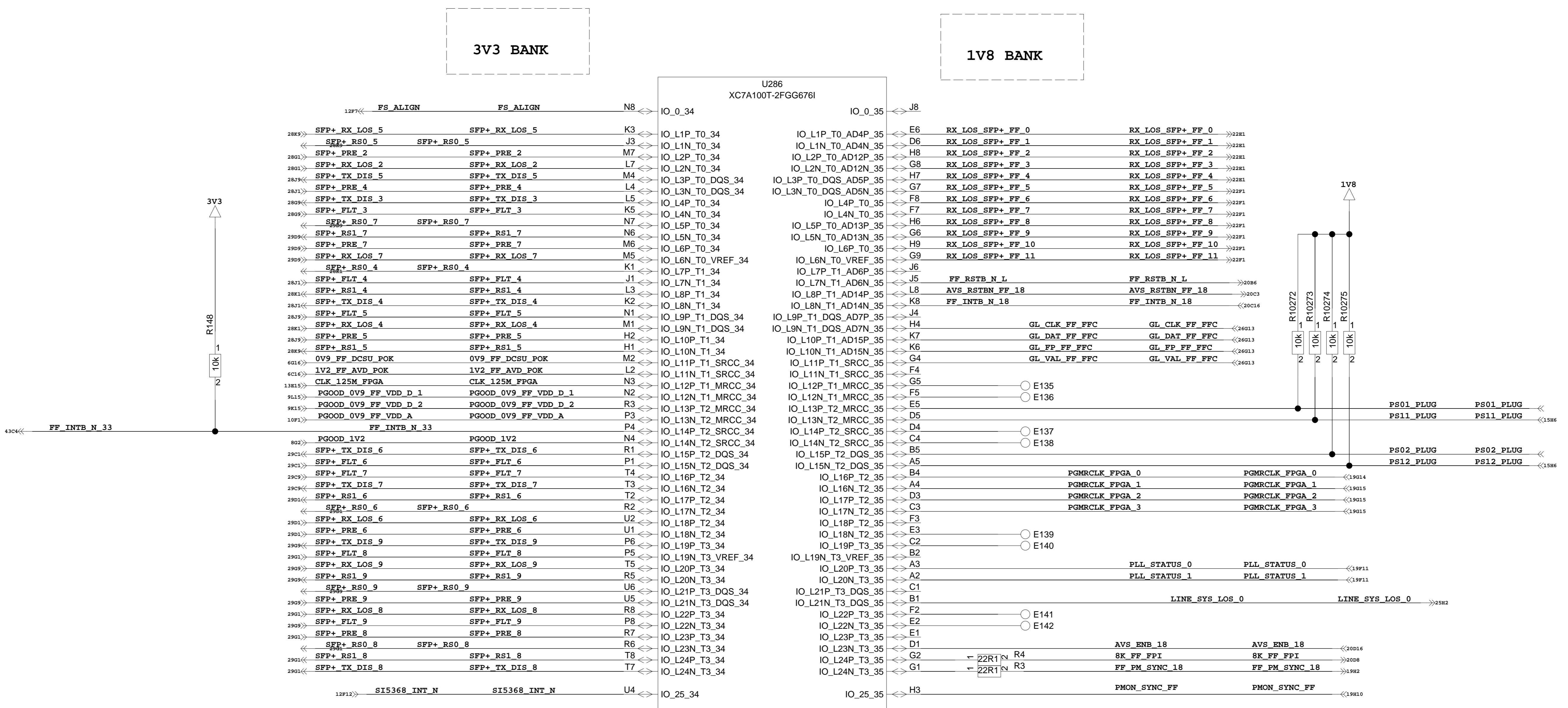
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FPGA GPIO PART 1

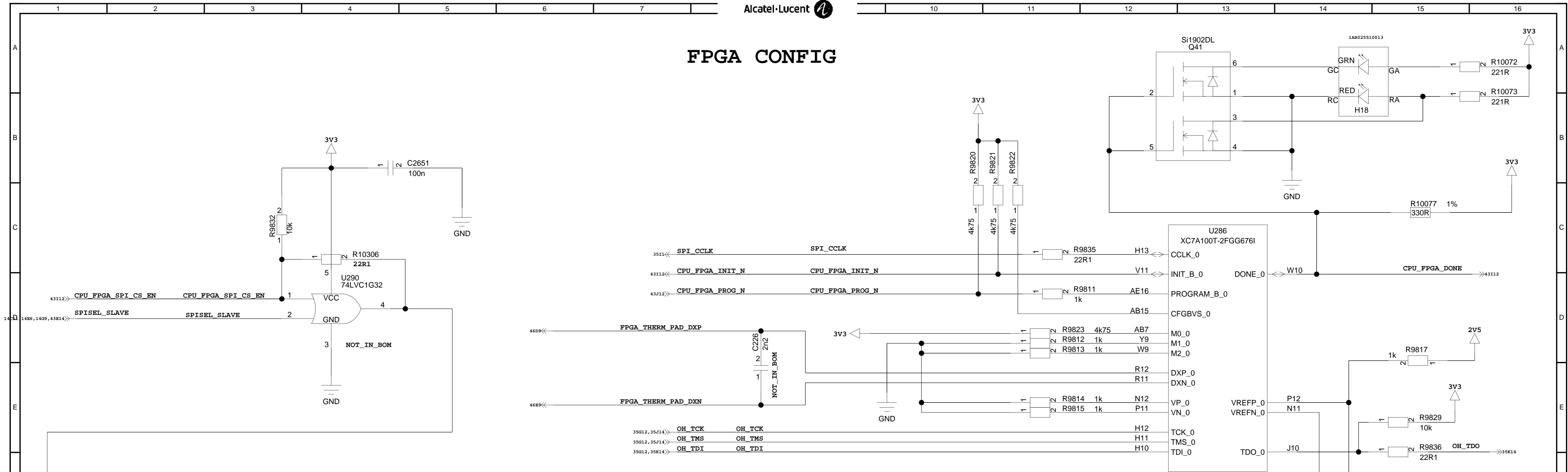


FPGA GPIO PART 2

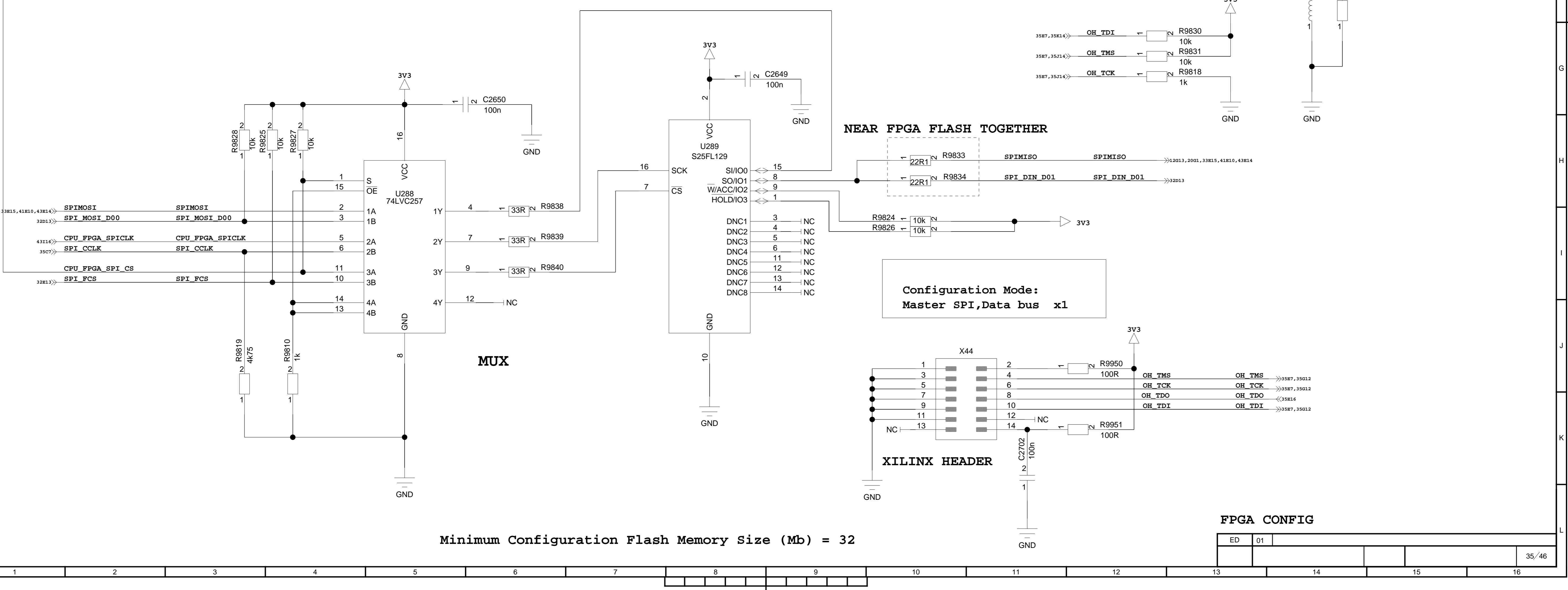




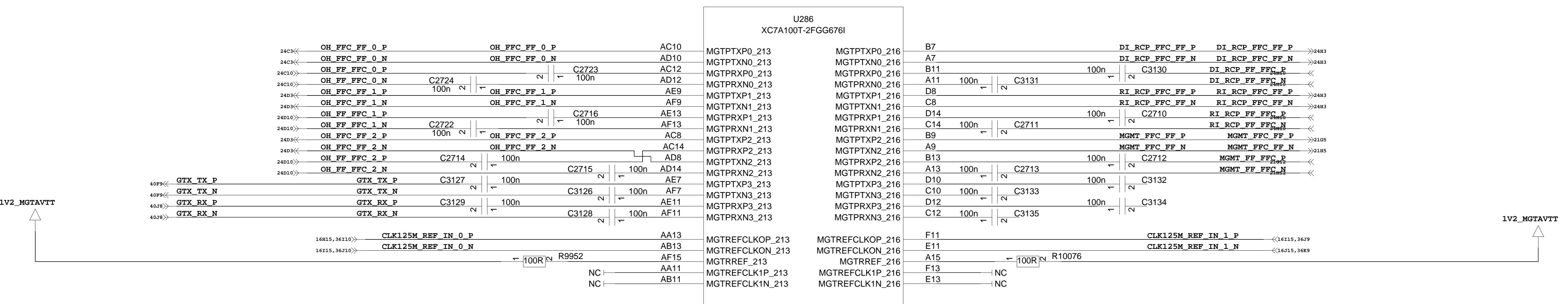
FPGA CONFIG



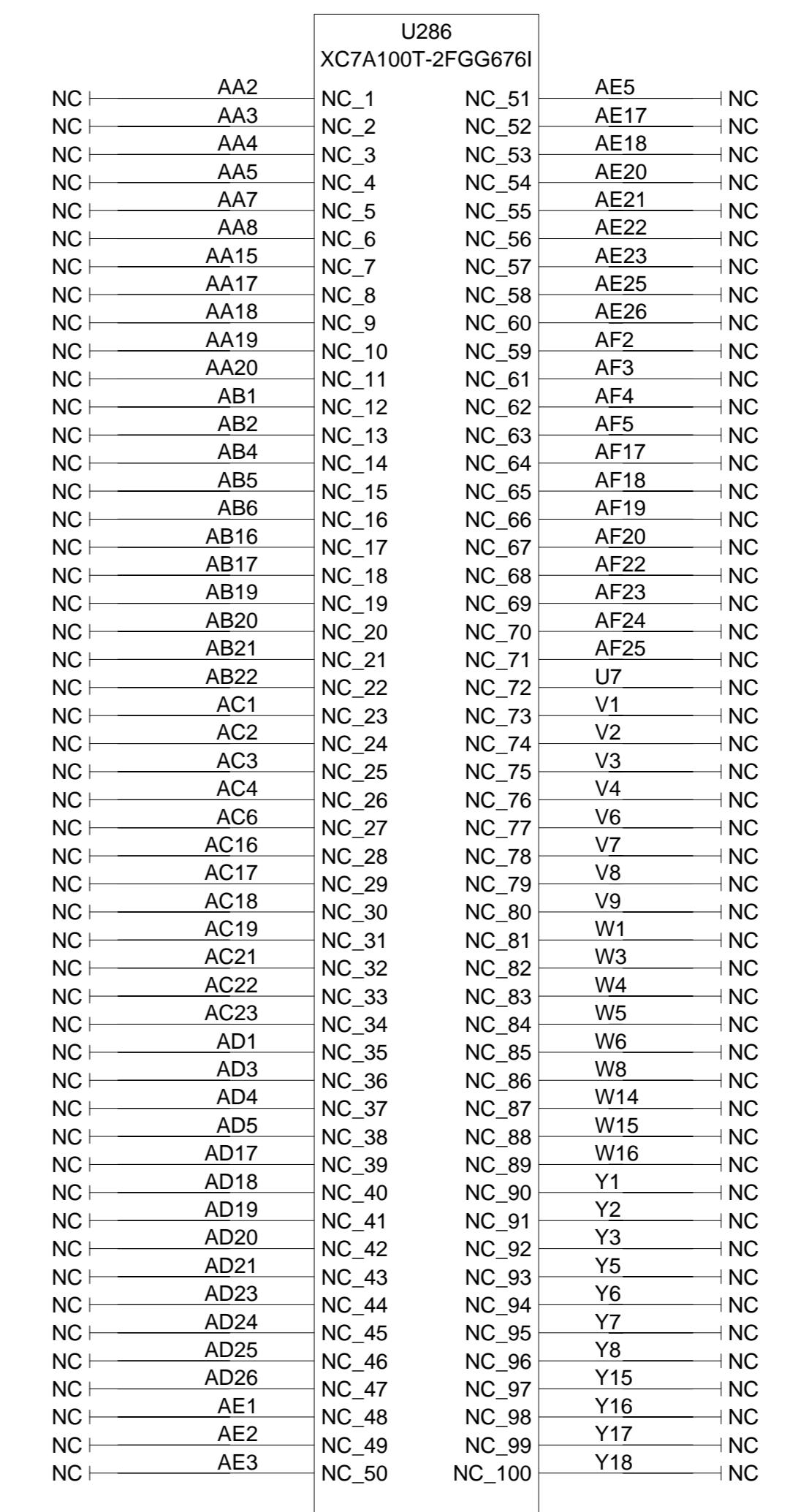
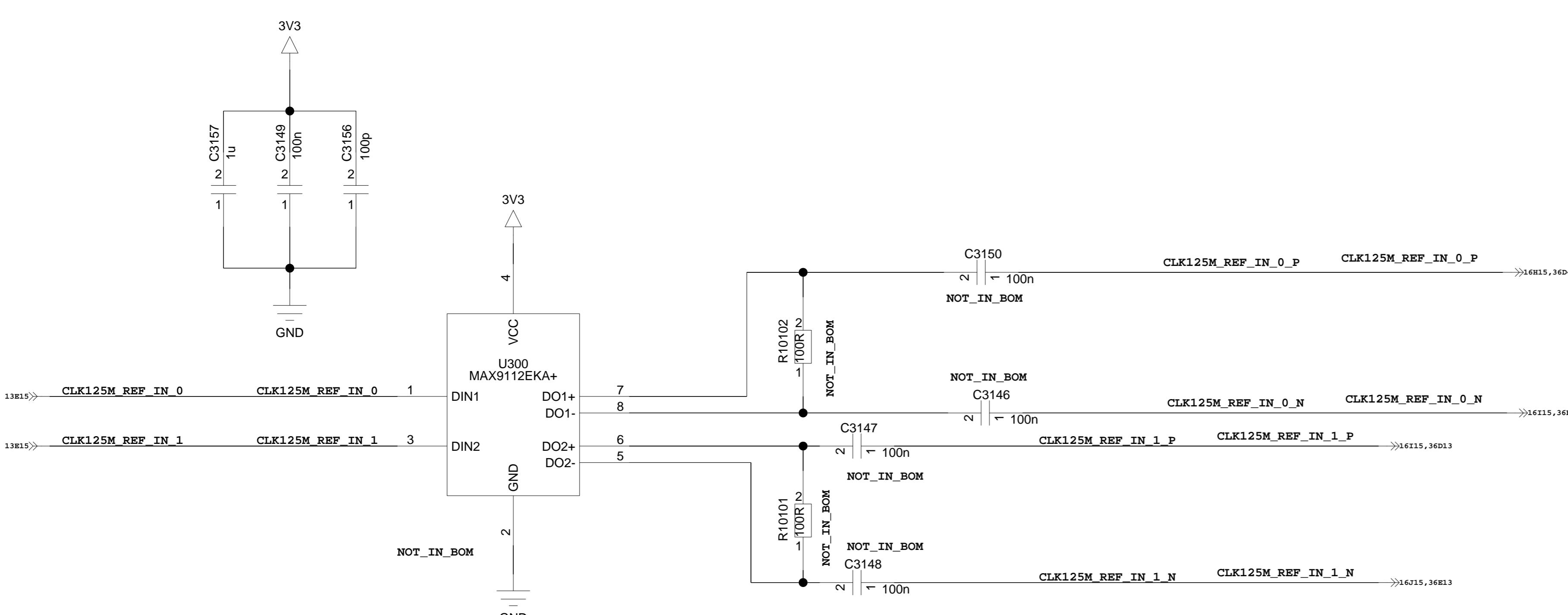
place U288, U289 and U290 close together near U286

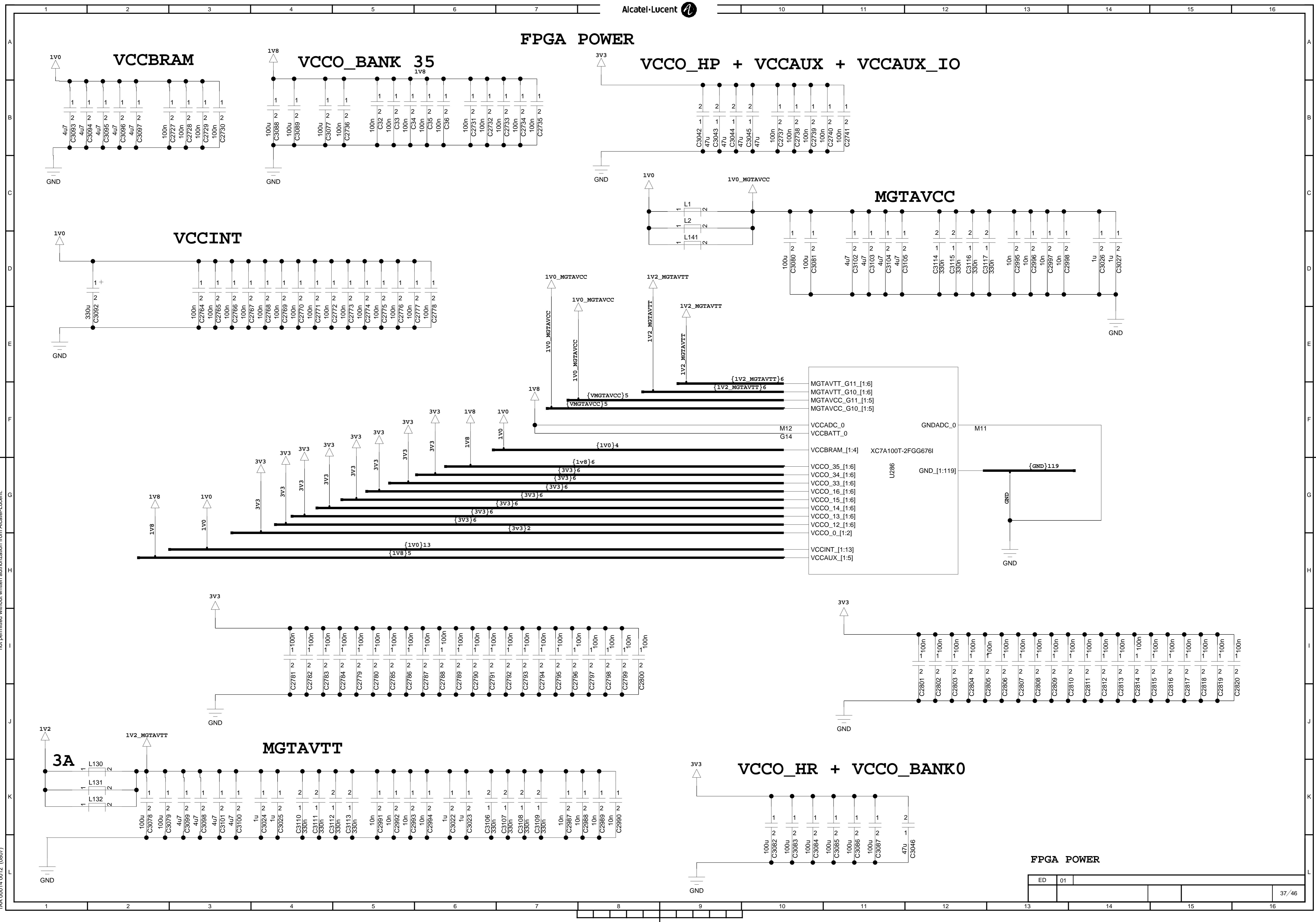


FPGA GTX PORTS

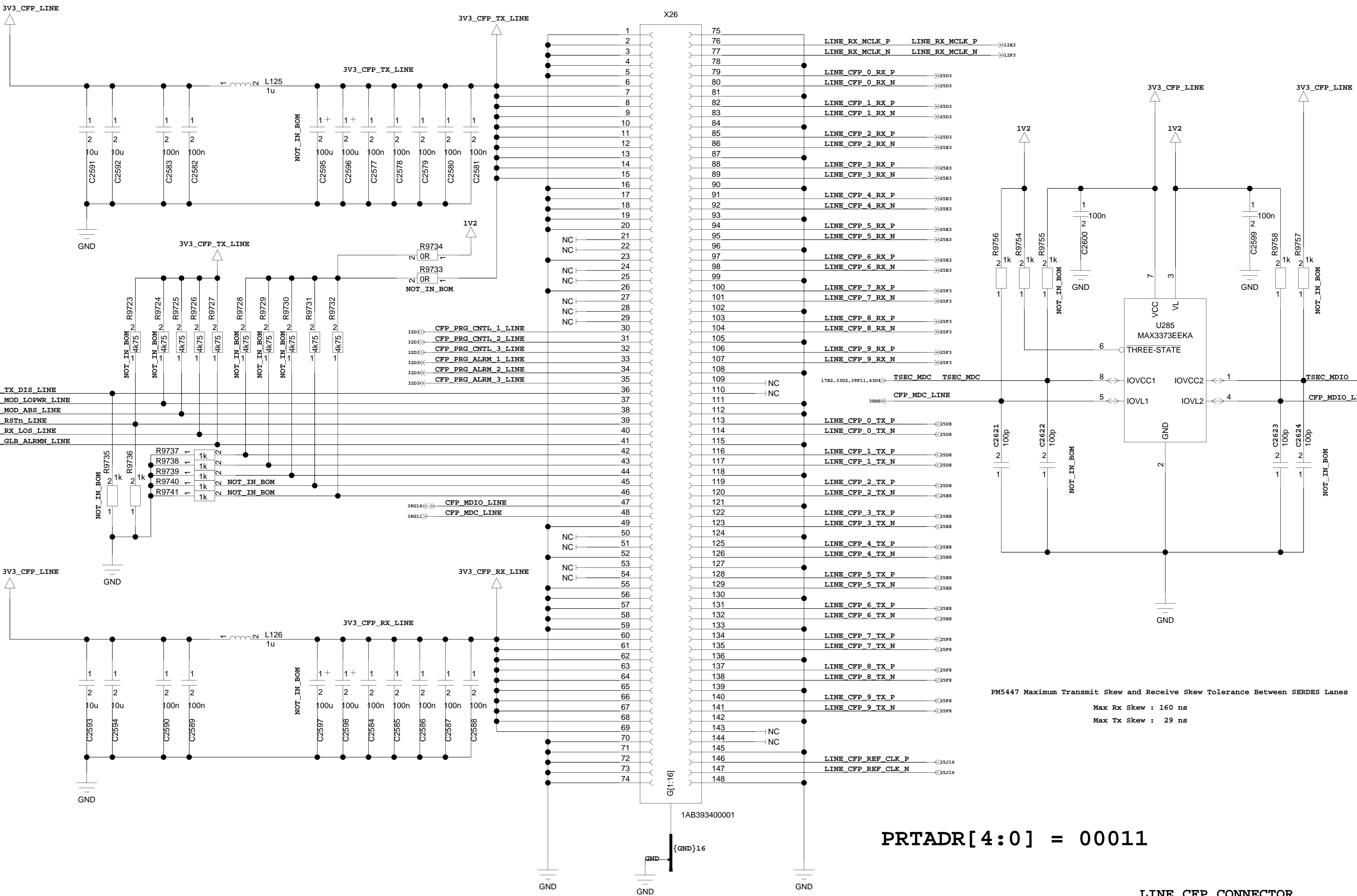


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LINE CFP CONNECTOR



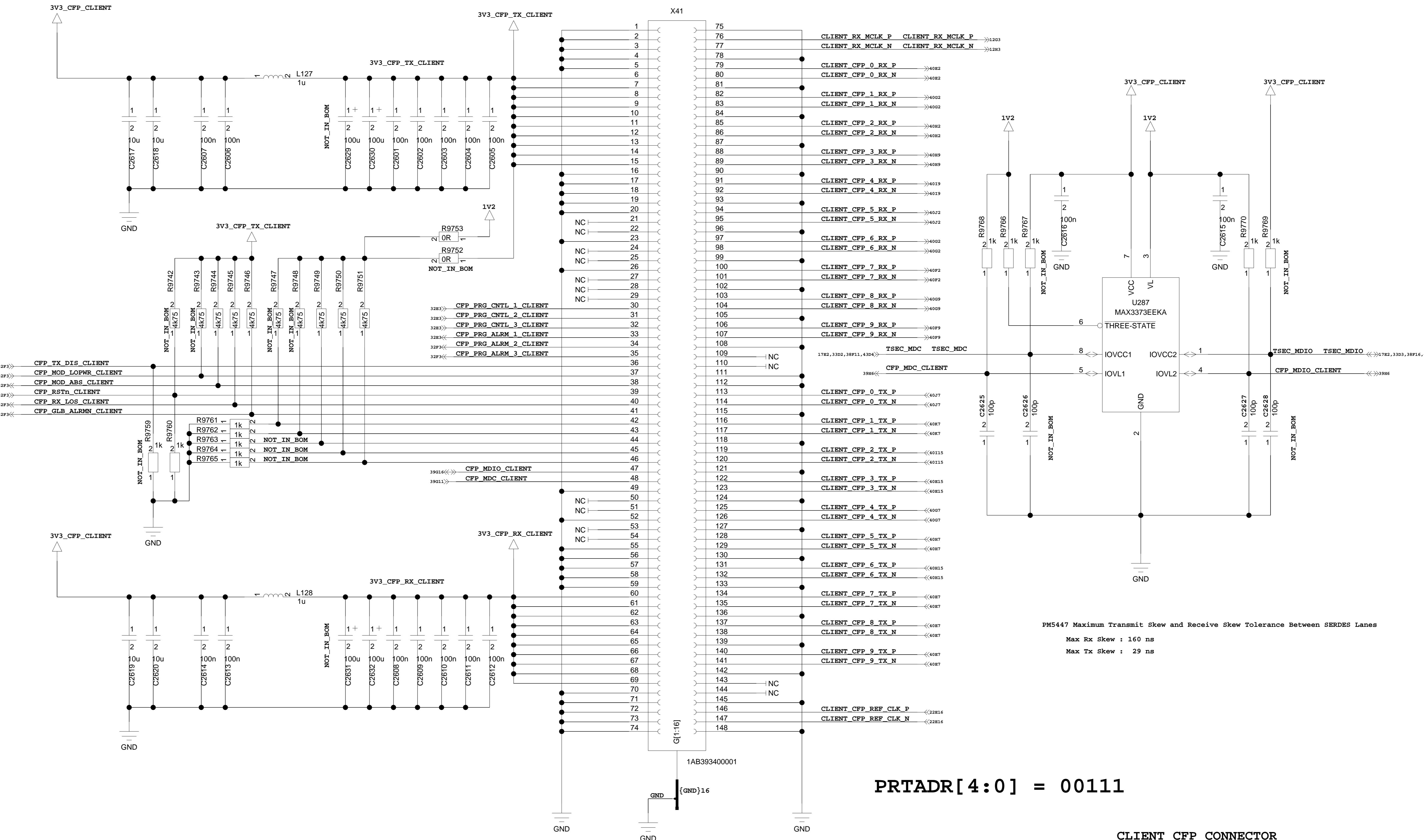
PRTADR[4:0] = 00011

LINE CFP CONNECTOR

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CLIENT CFP CONNECTOR

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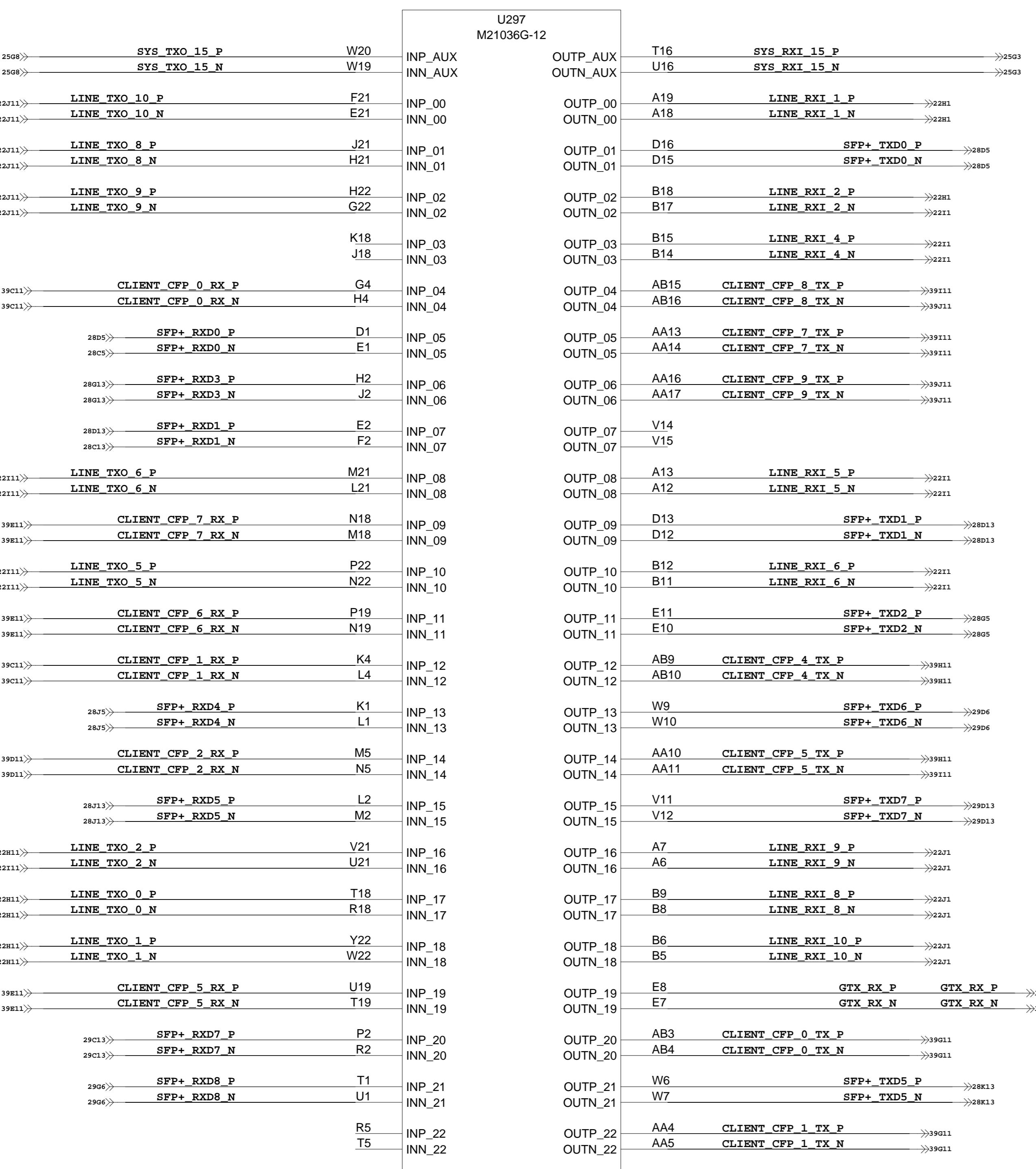


PRTADR[4:0] = 00111

ENT CFP CONNECTOR

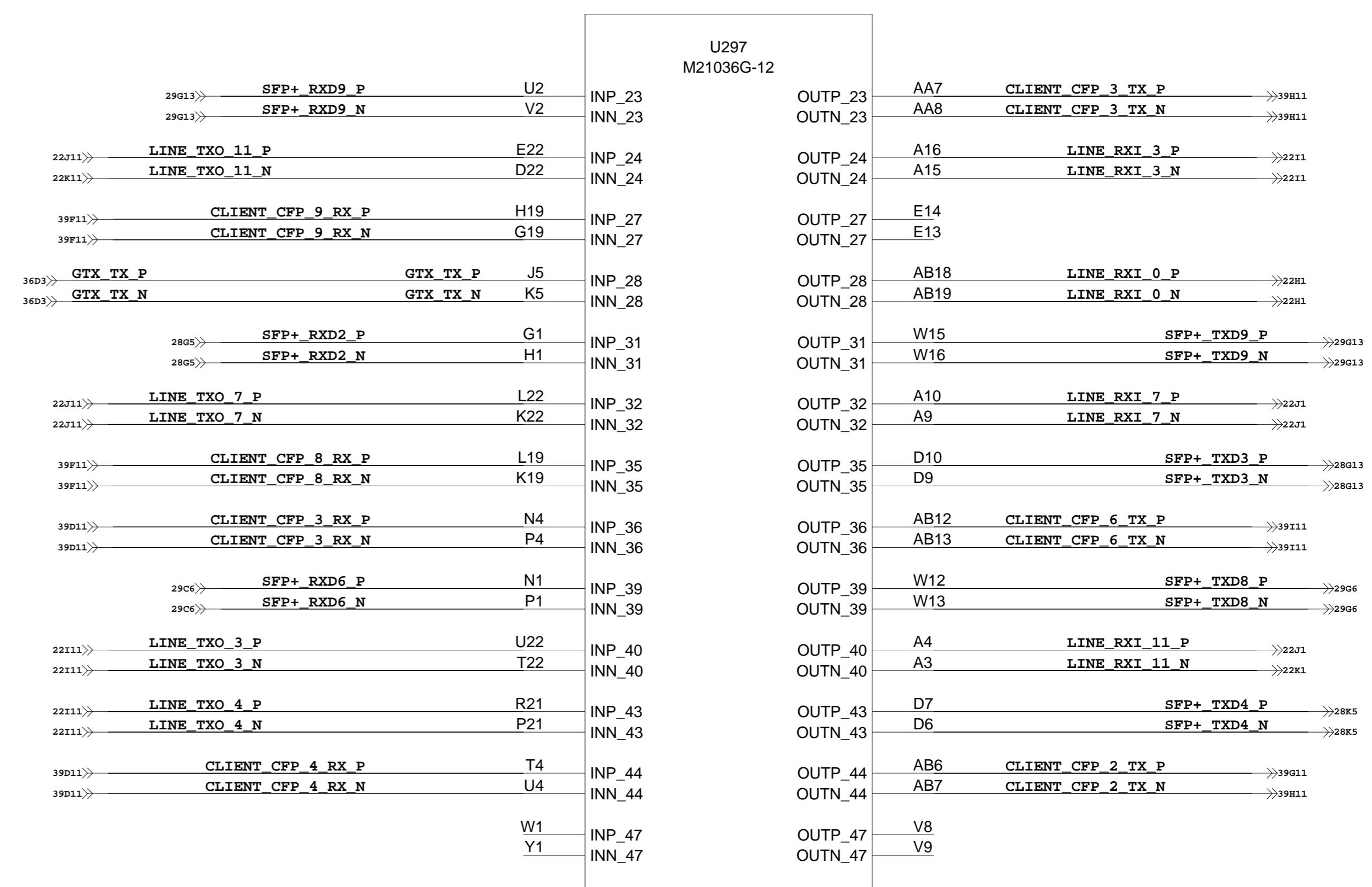
ED	01				39/46
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MATRIX XAUI/SYS



RX AC COUPLING FROM PM5447

TX DC COUPLING TO PM5447

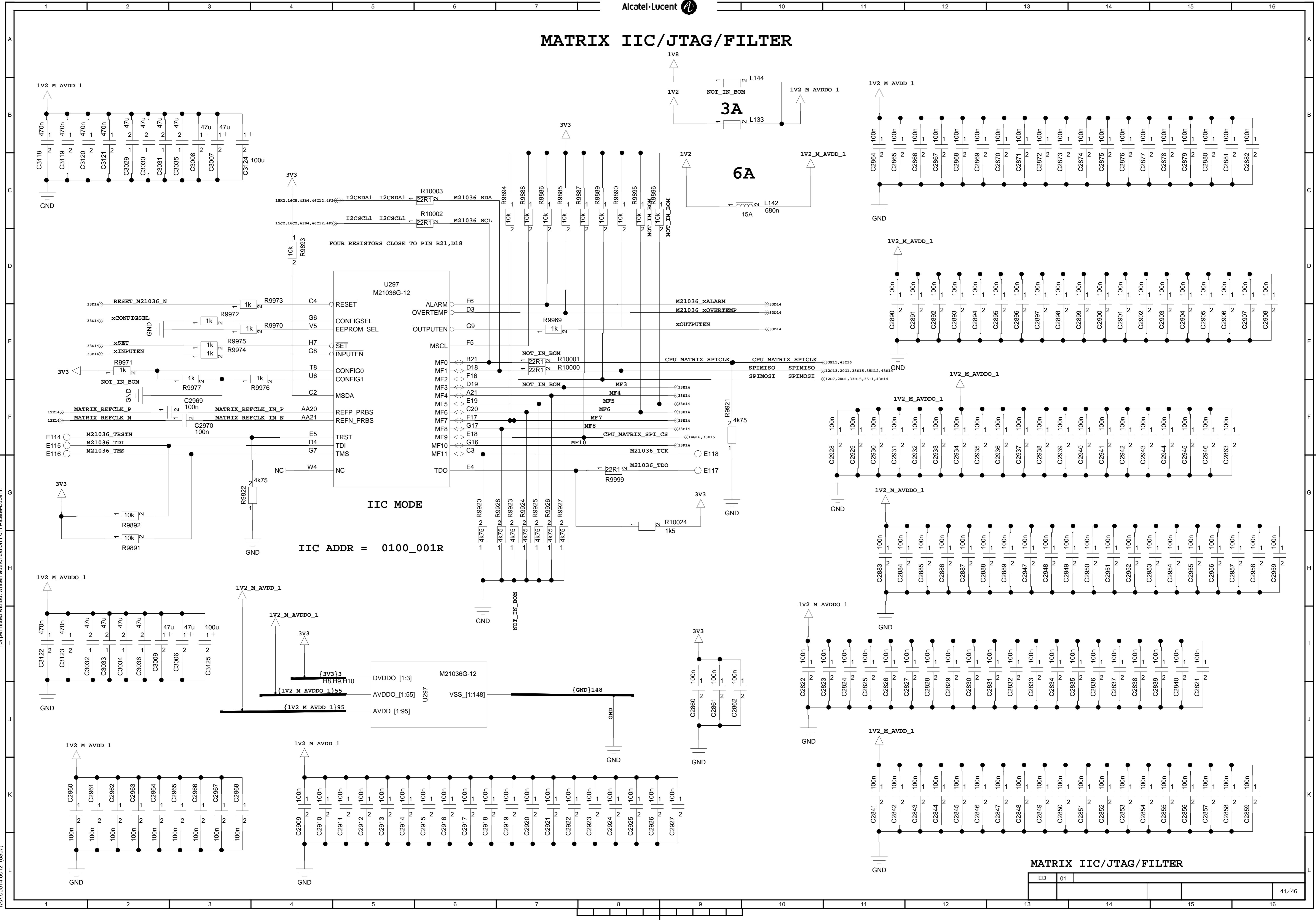


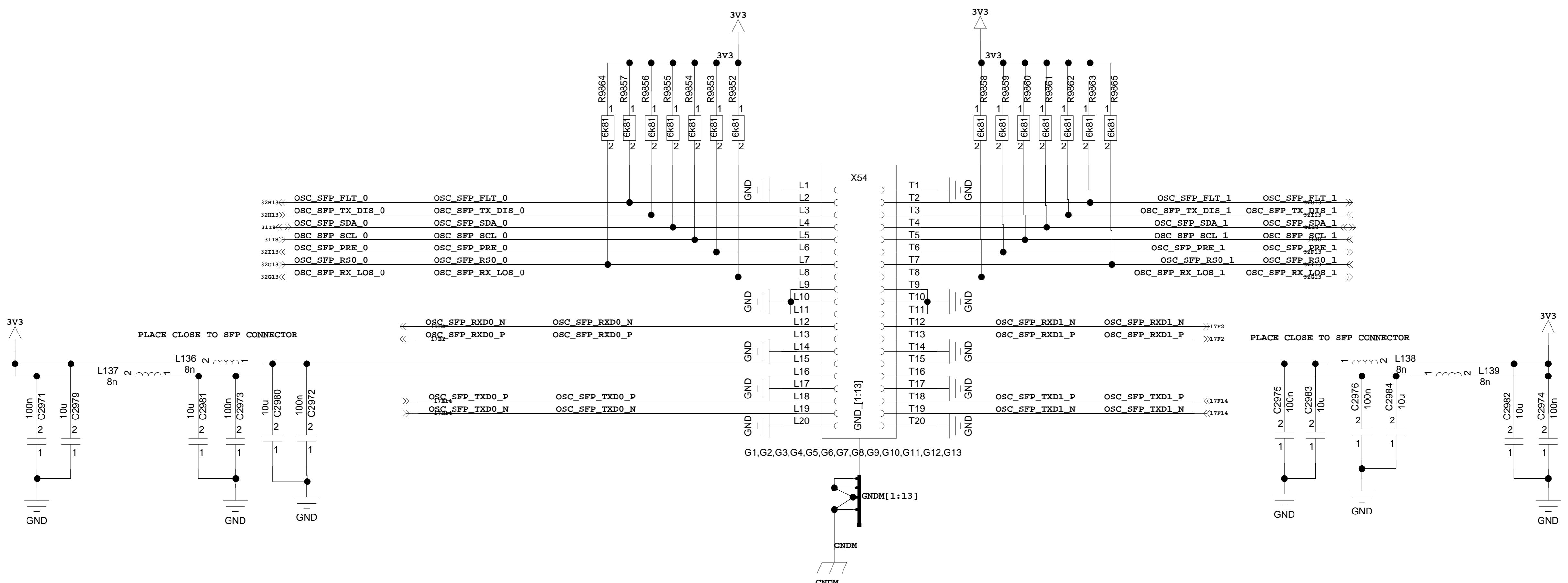
MATRIX XAUI/SYS

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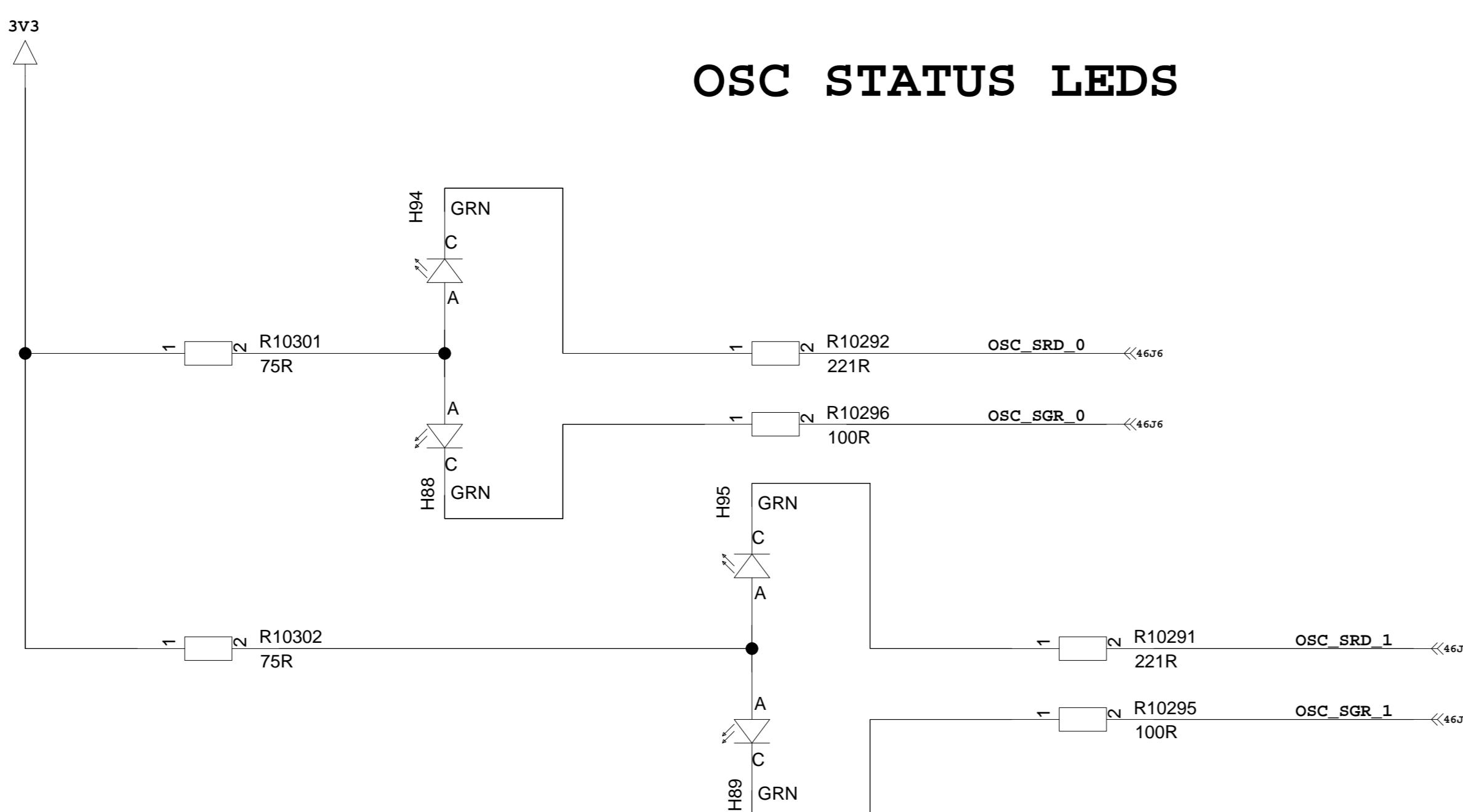
MATRIX IIC/JTAG/FILTER

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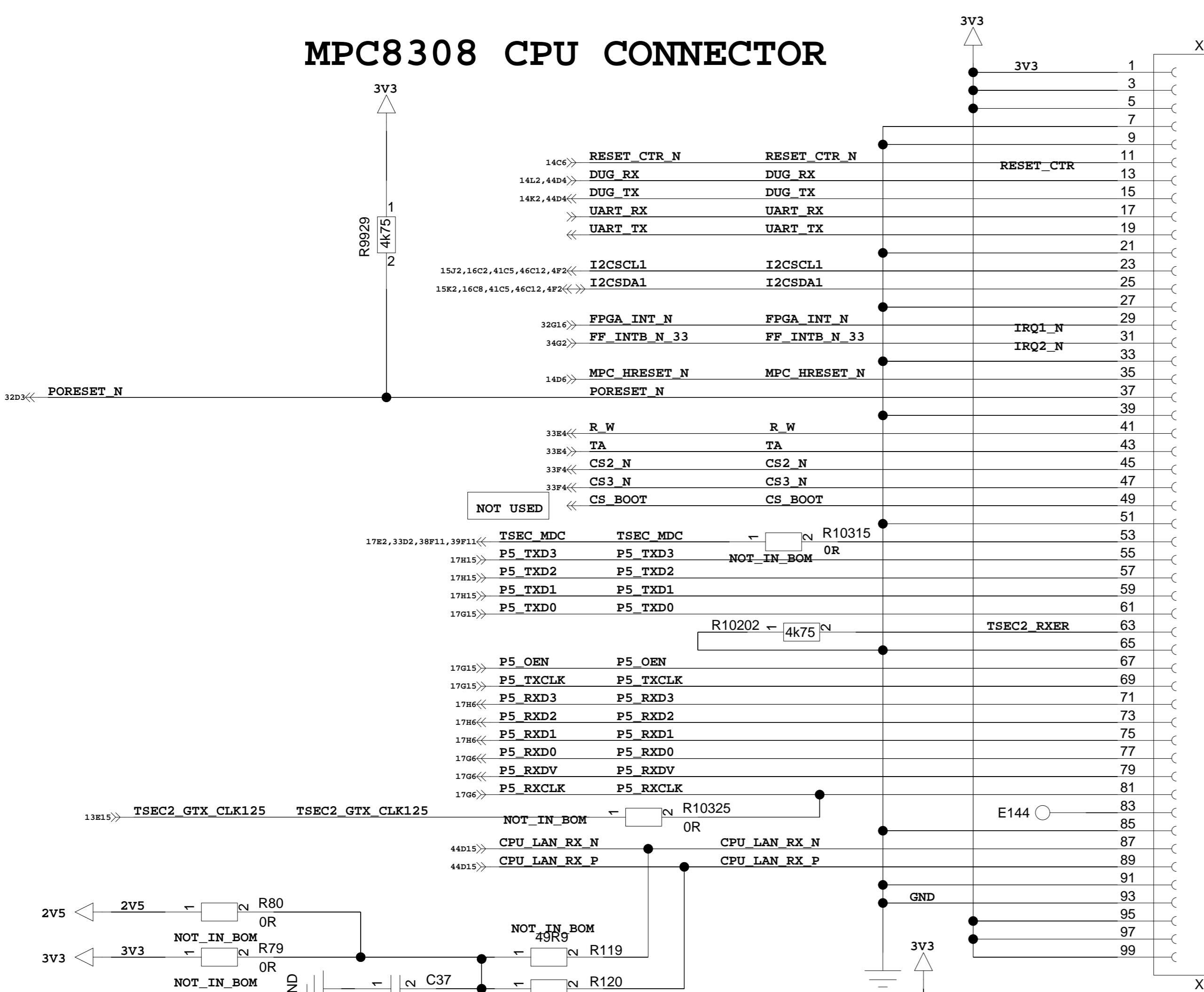
OSC STATUS LEDS



OSC : 100BASE-FX / 1000BASE-X

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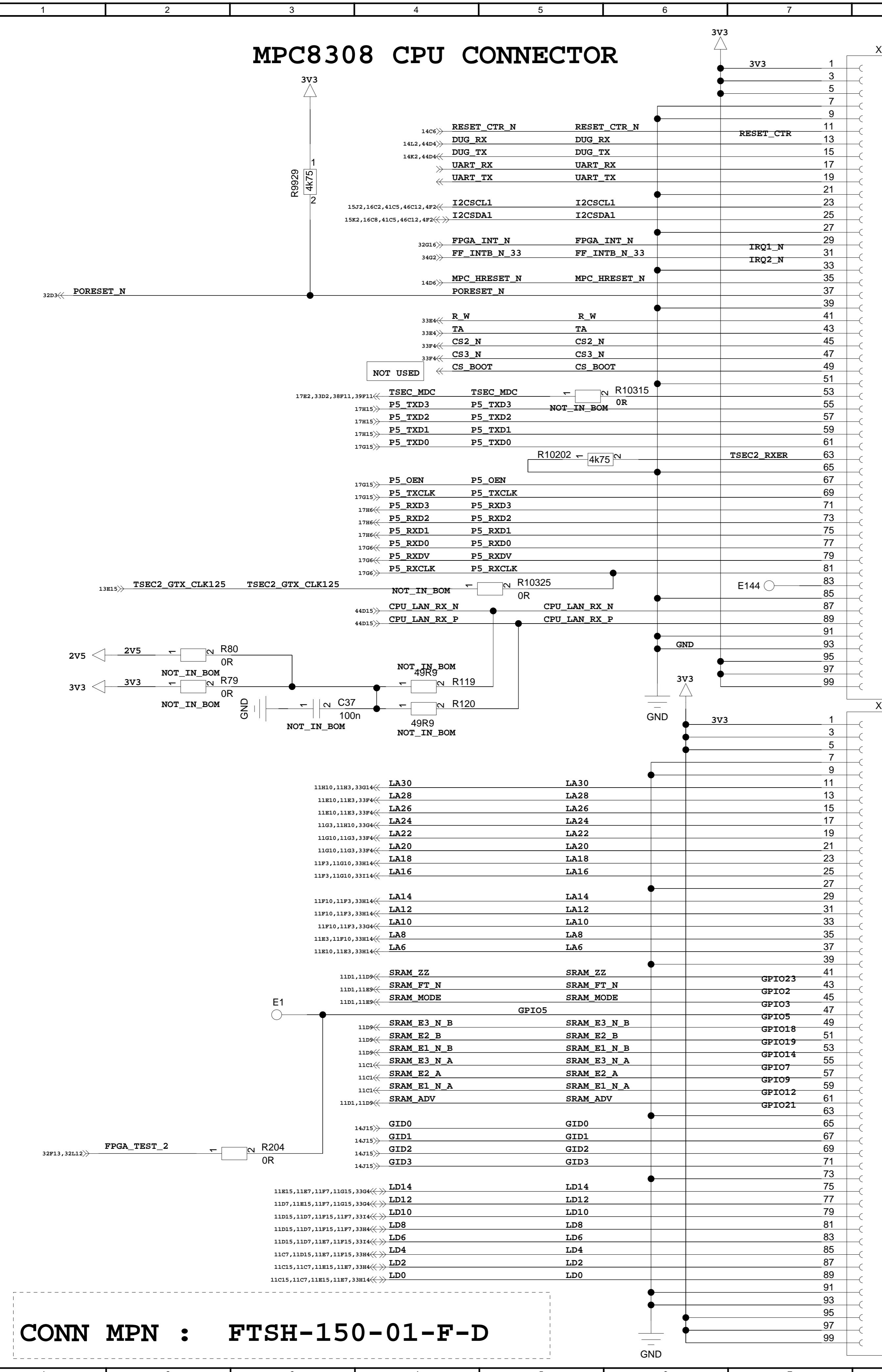
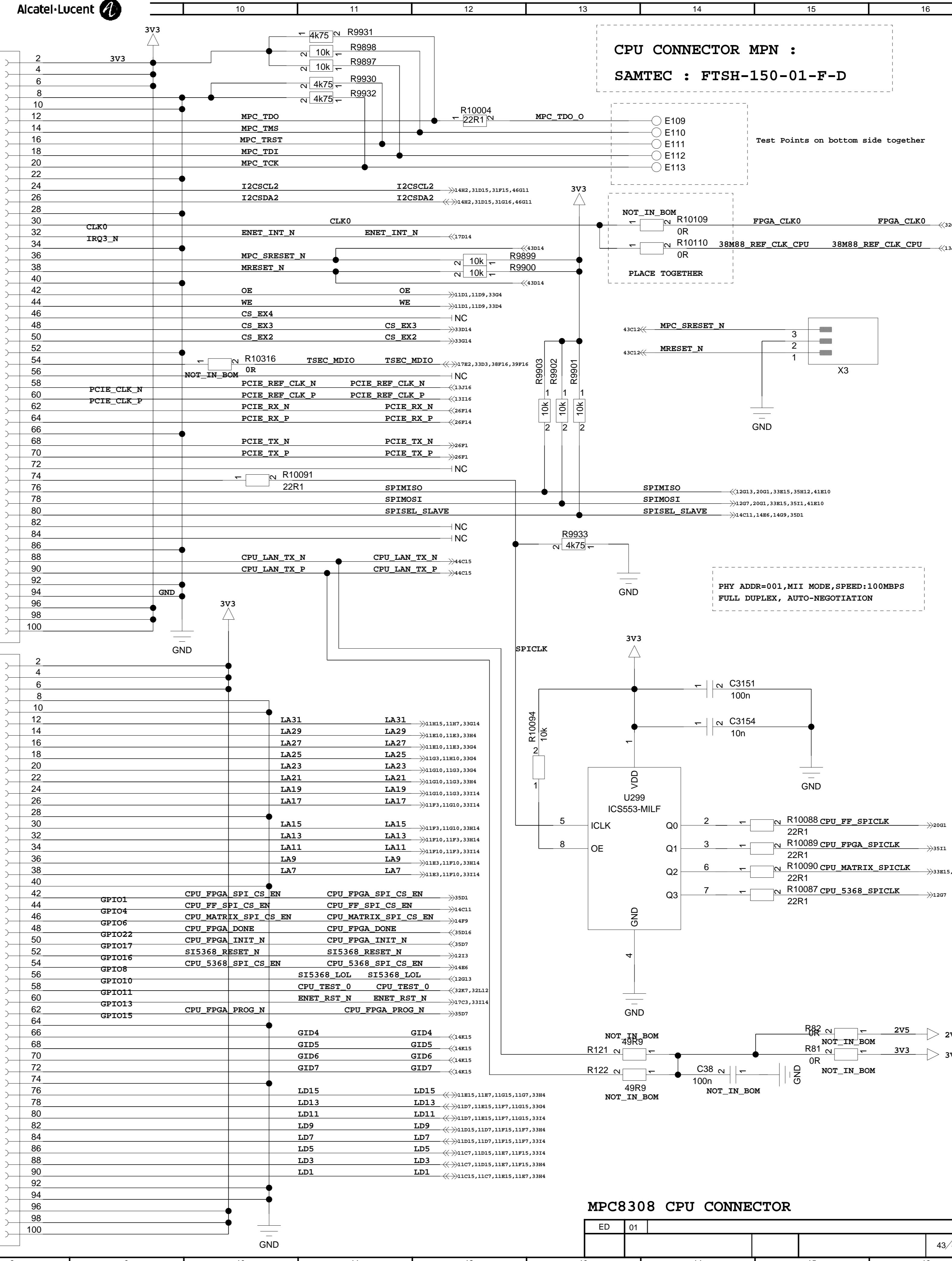
MPC8308 CPU CONNECTOR



CPU CONNECTOR MPN :

SAMTEC : FTSH-150-01-F-D

Test Points on bottom side together

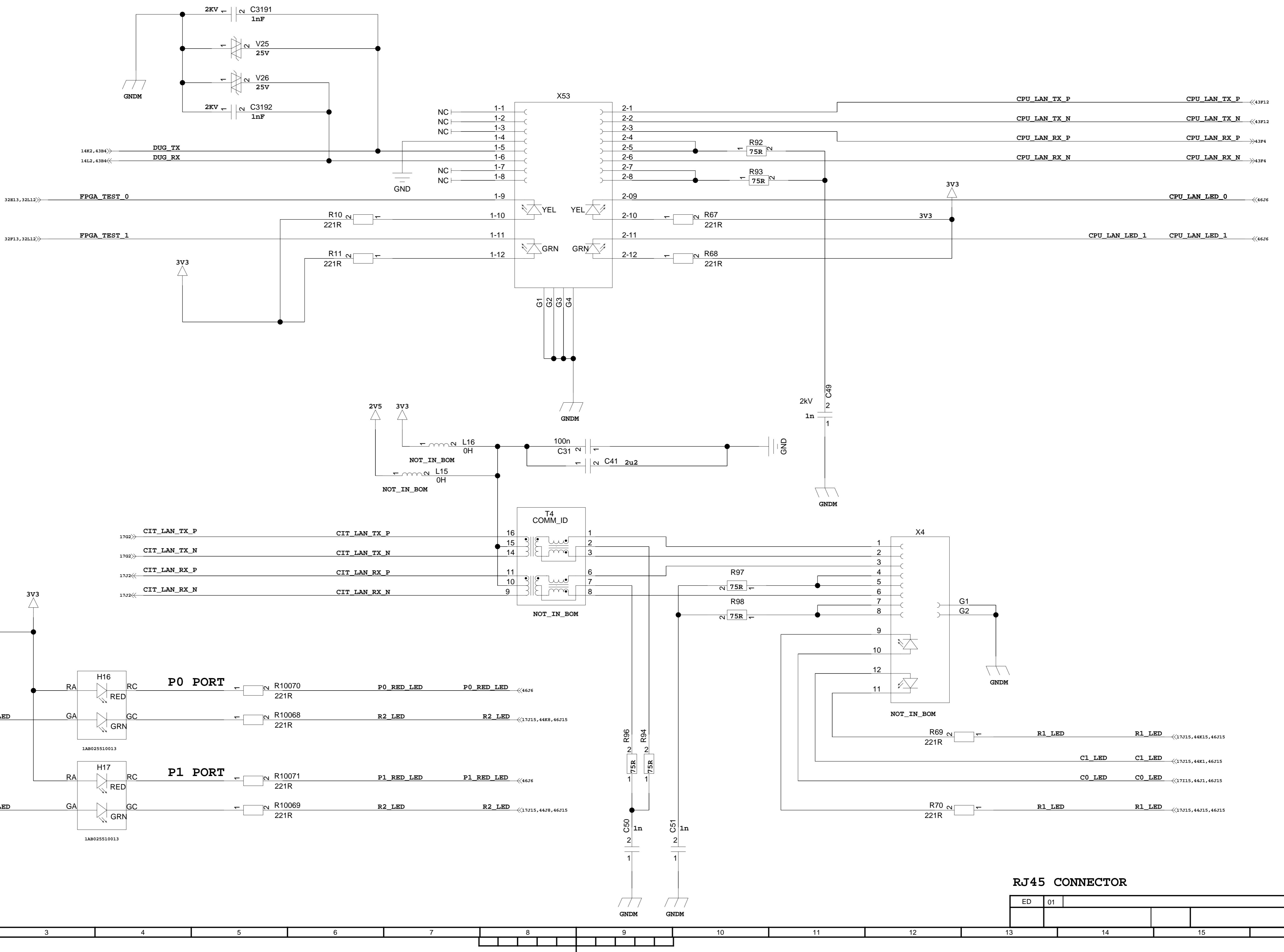


CONN MPN : FTSH-150-01-F-D

MPC8308 CPU CONNECTOR

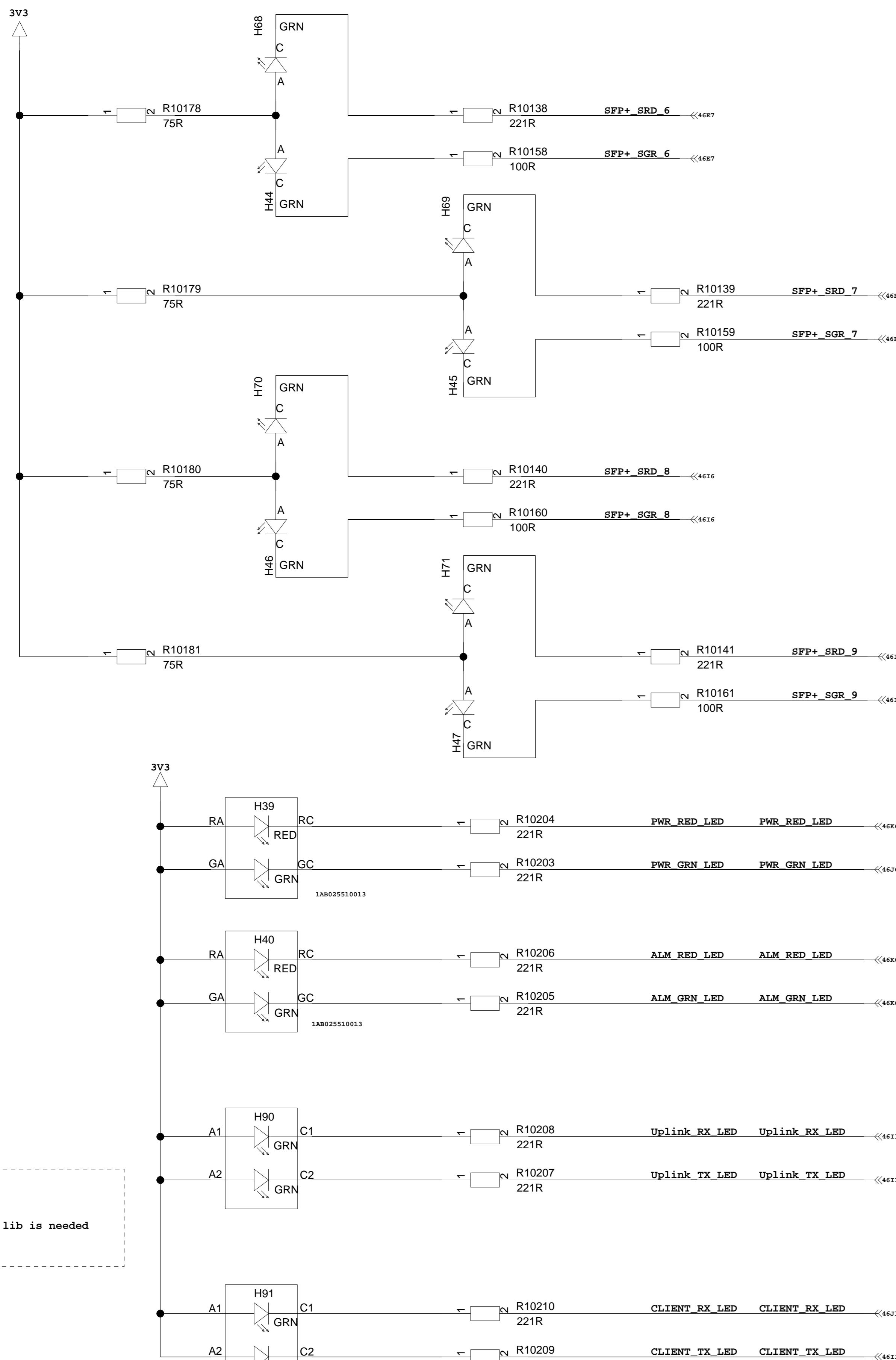
ED	01			
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RJ45 CONNECTOR

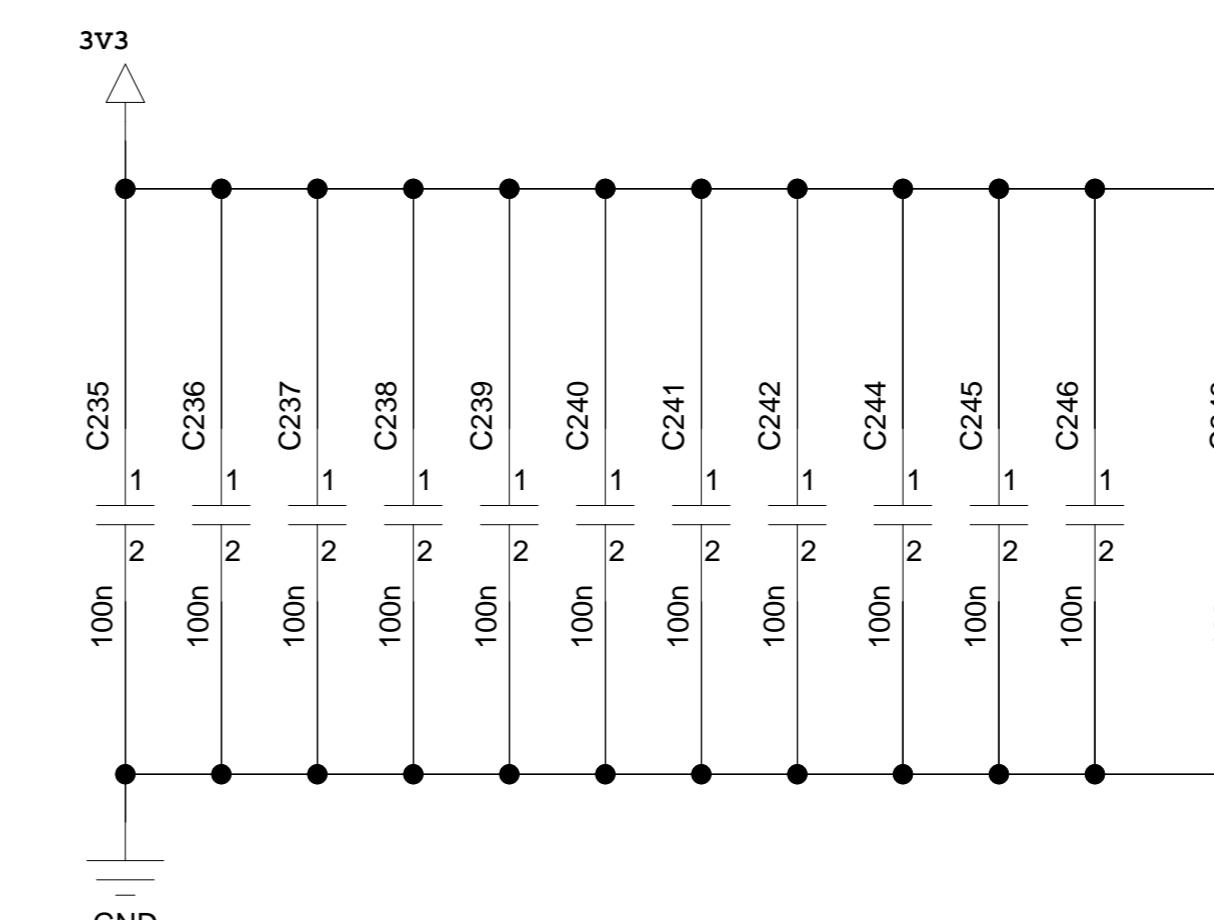
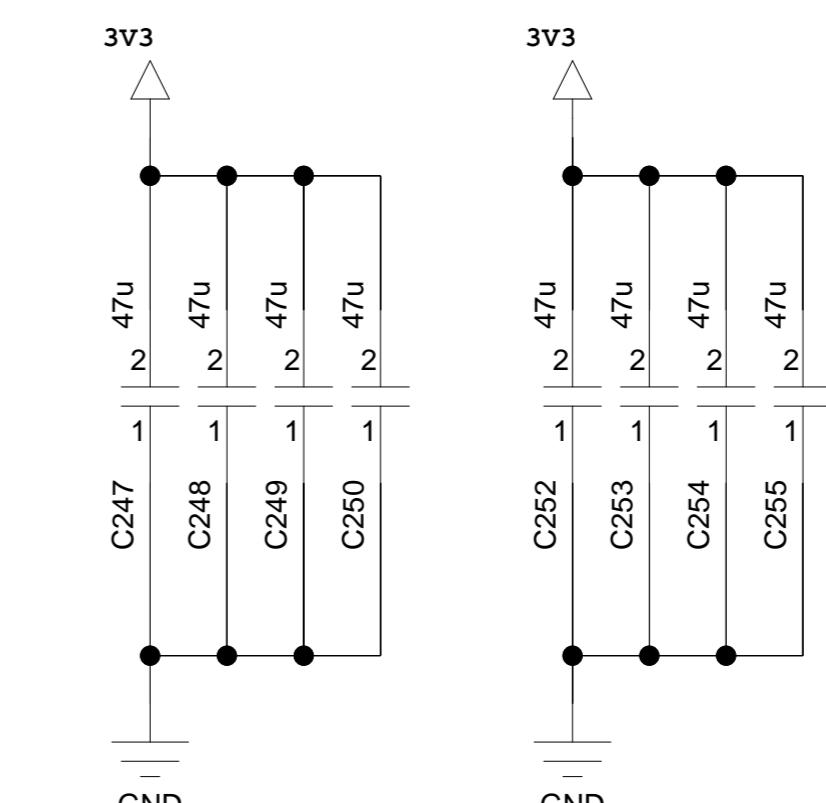


SFP+ LINK/PORT LEDS PART 2

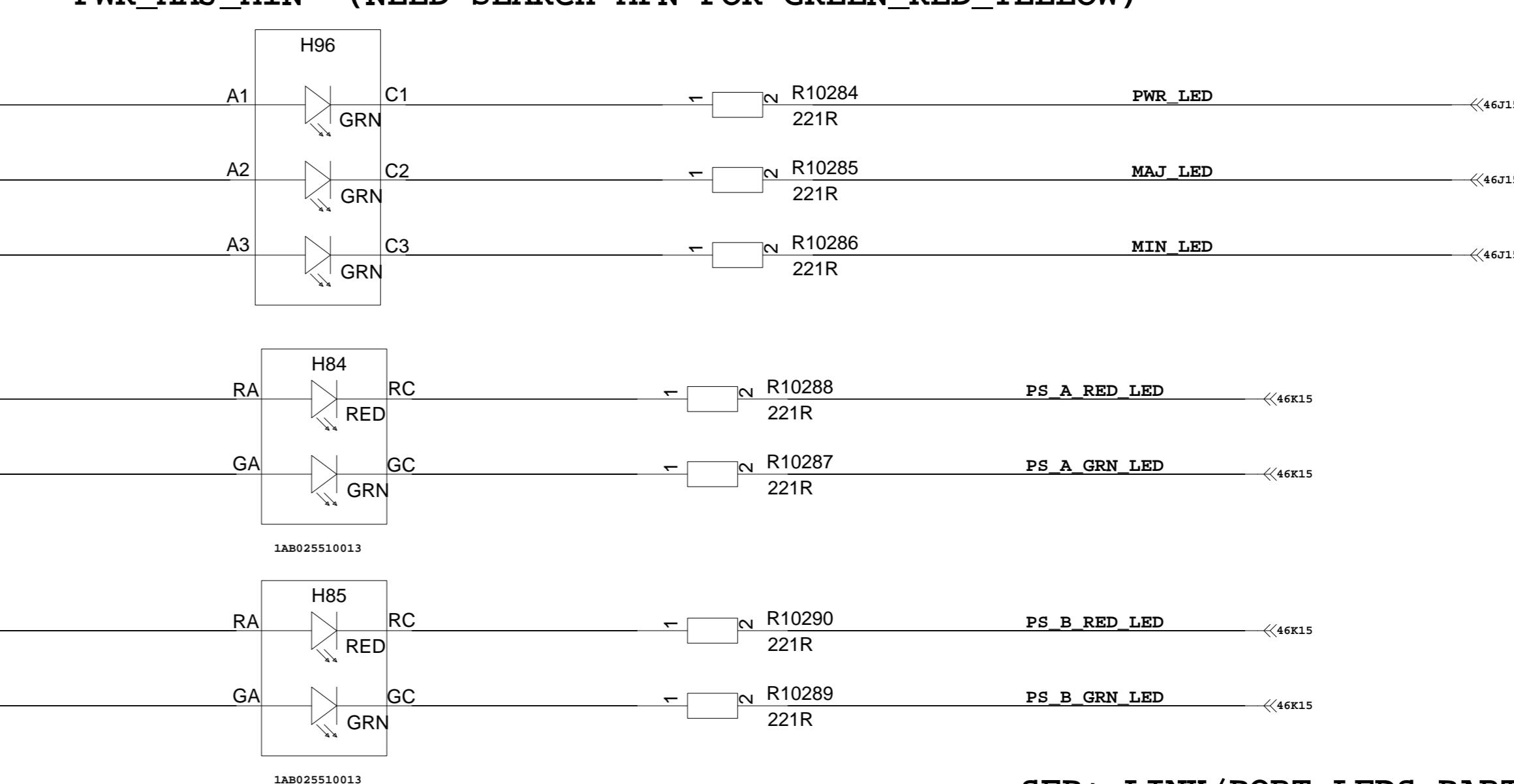
STATUS LEDS



CPU DECOUPLE CAPACITORS



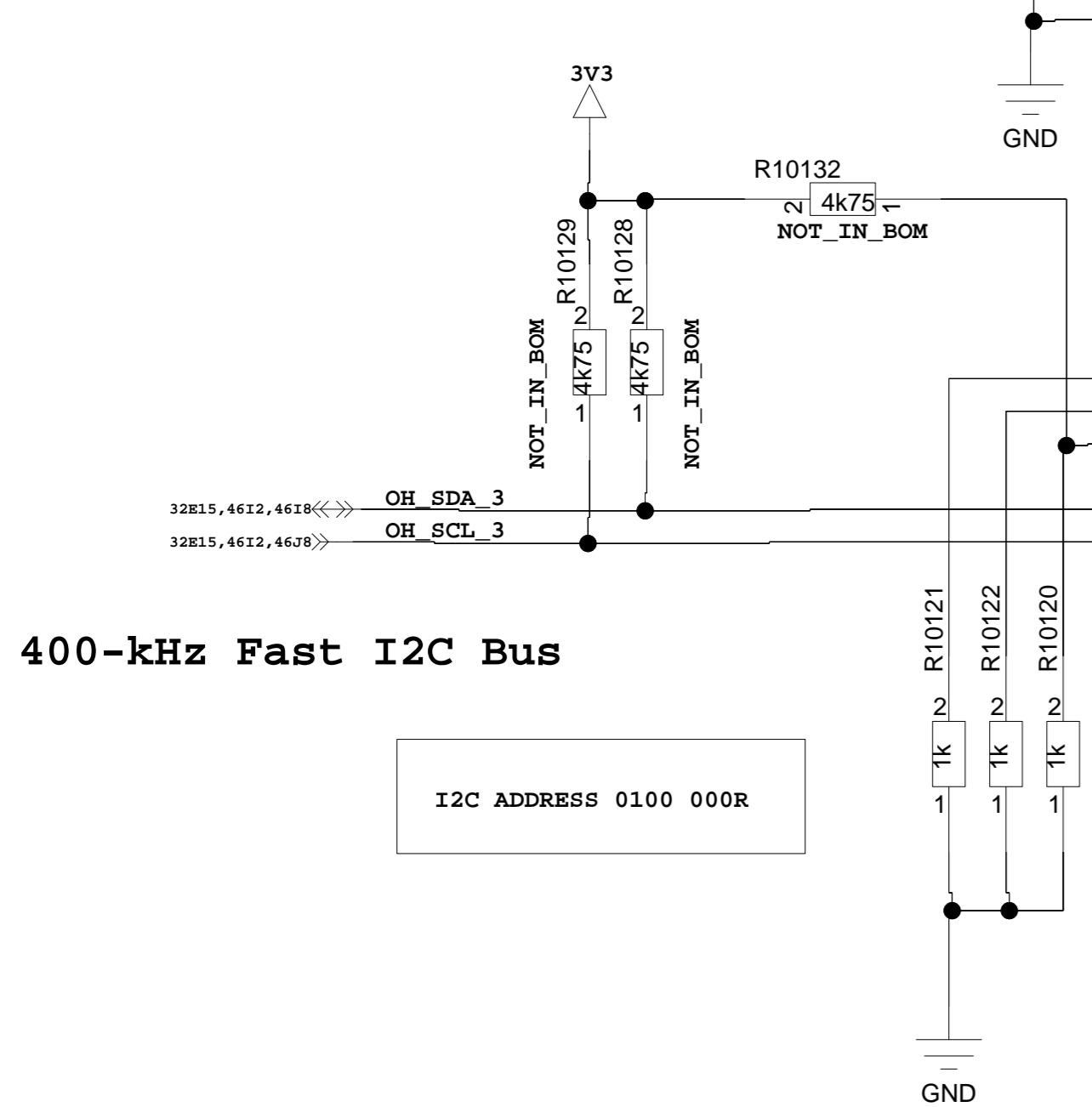
PWR_MAJ_MIN (NEED SEARCH MPN FOR GREEN_RED_YELLOW)



SFP+ LINK/PORT LEDS PART 2

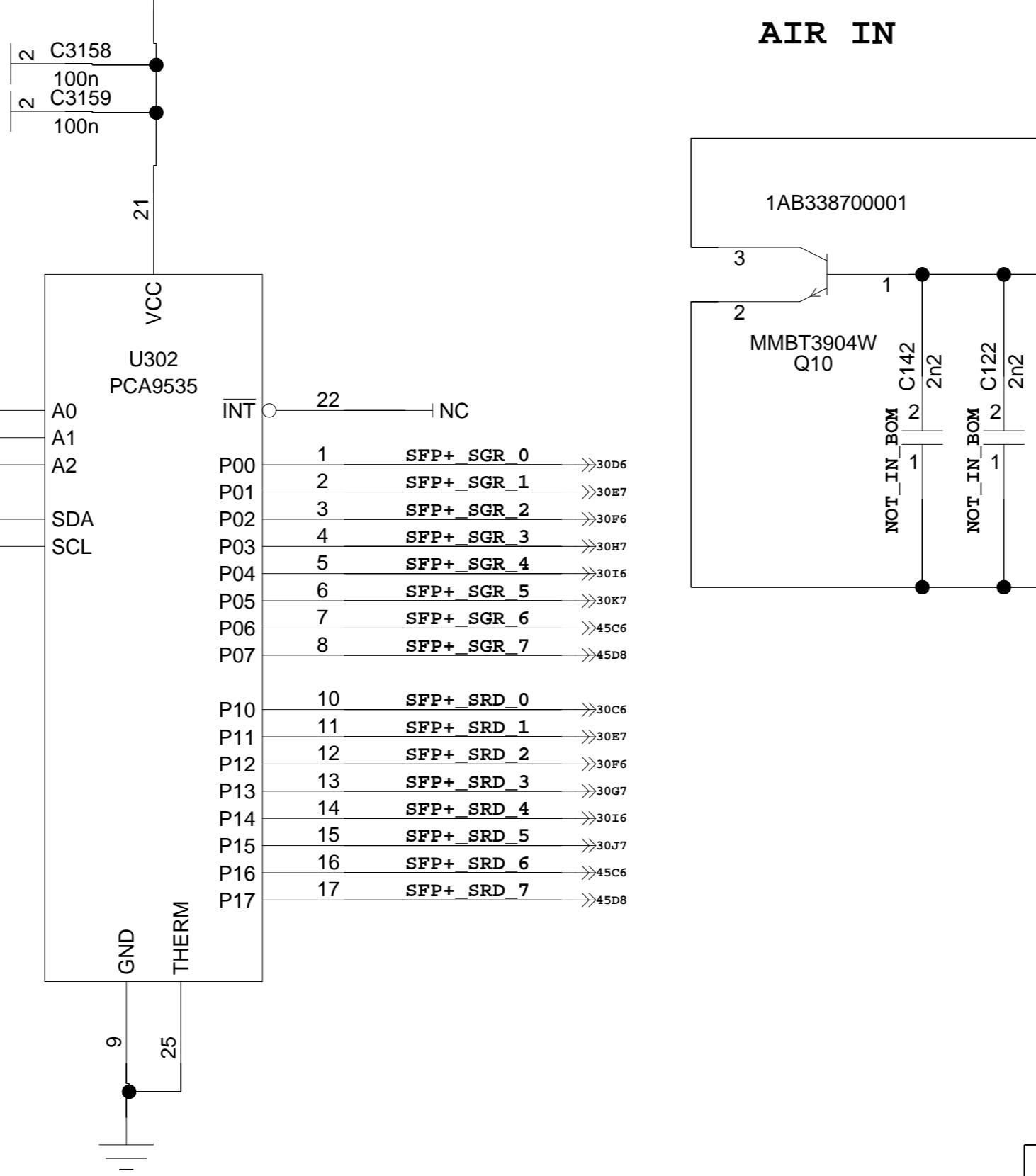
ED	01			

I2C GPIO EXPANDERS



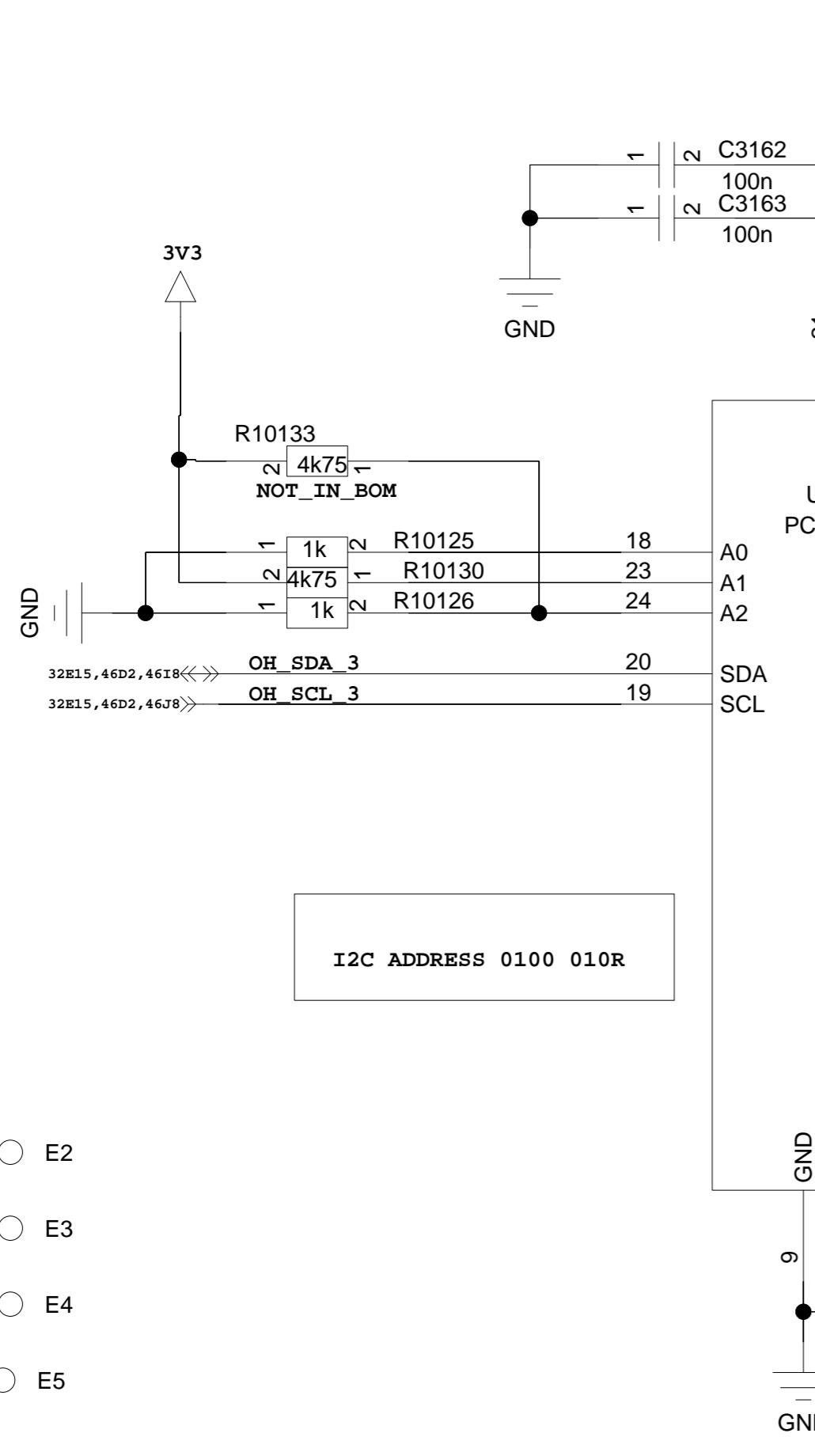
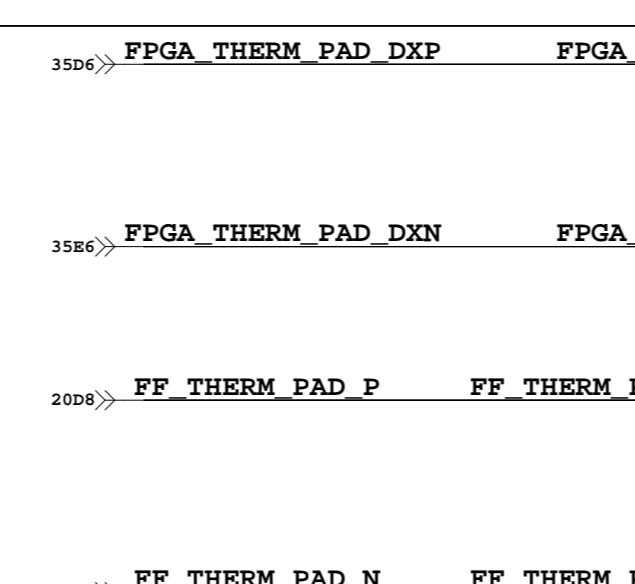
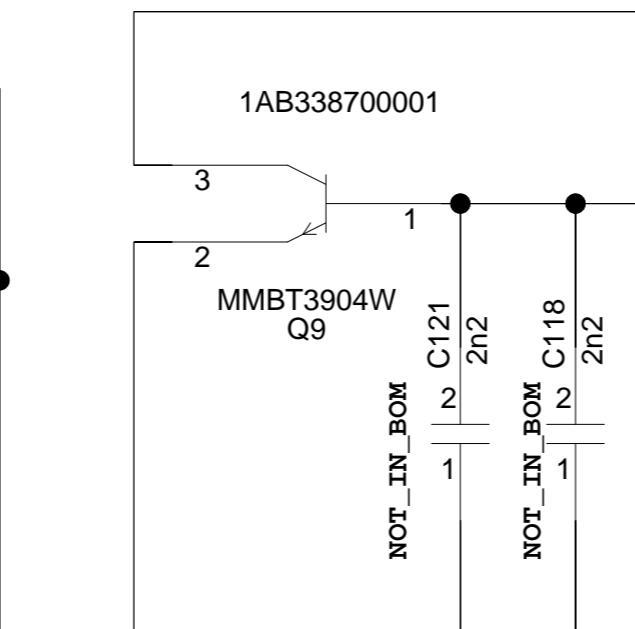
400-kHz Fast I2C Bus

I2C ADDRESS 0100 000R

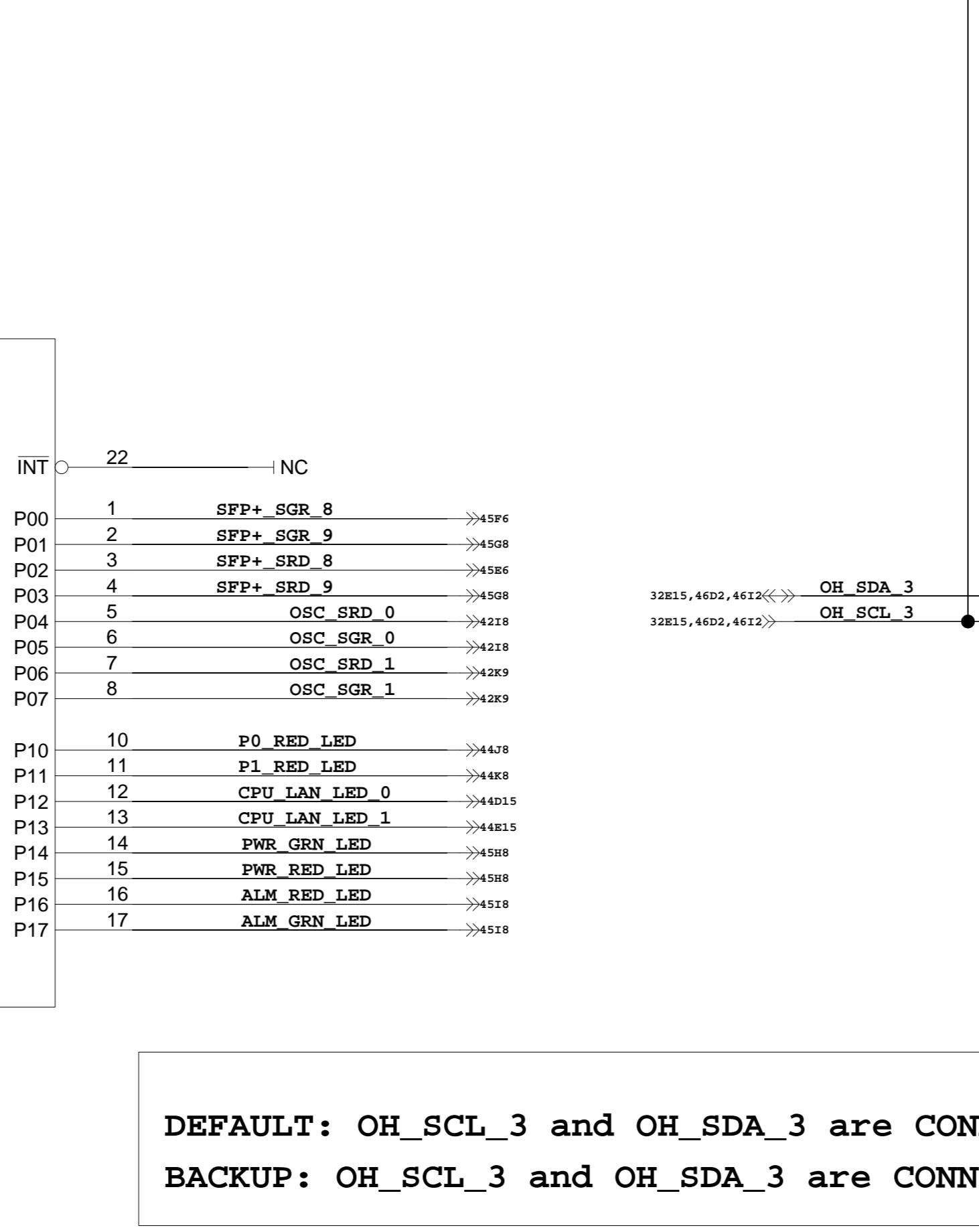


AIR IN

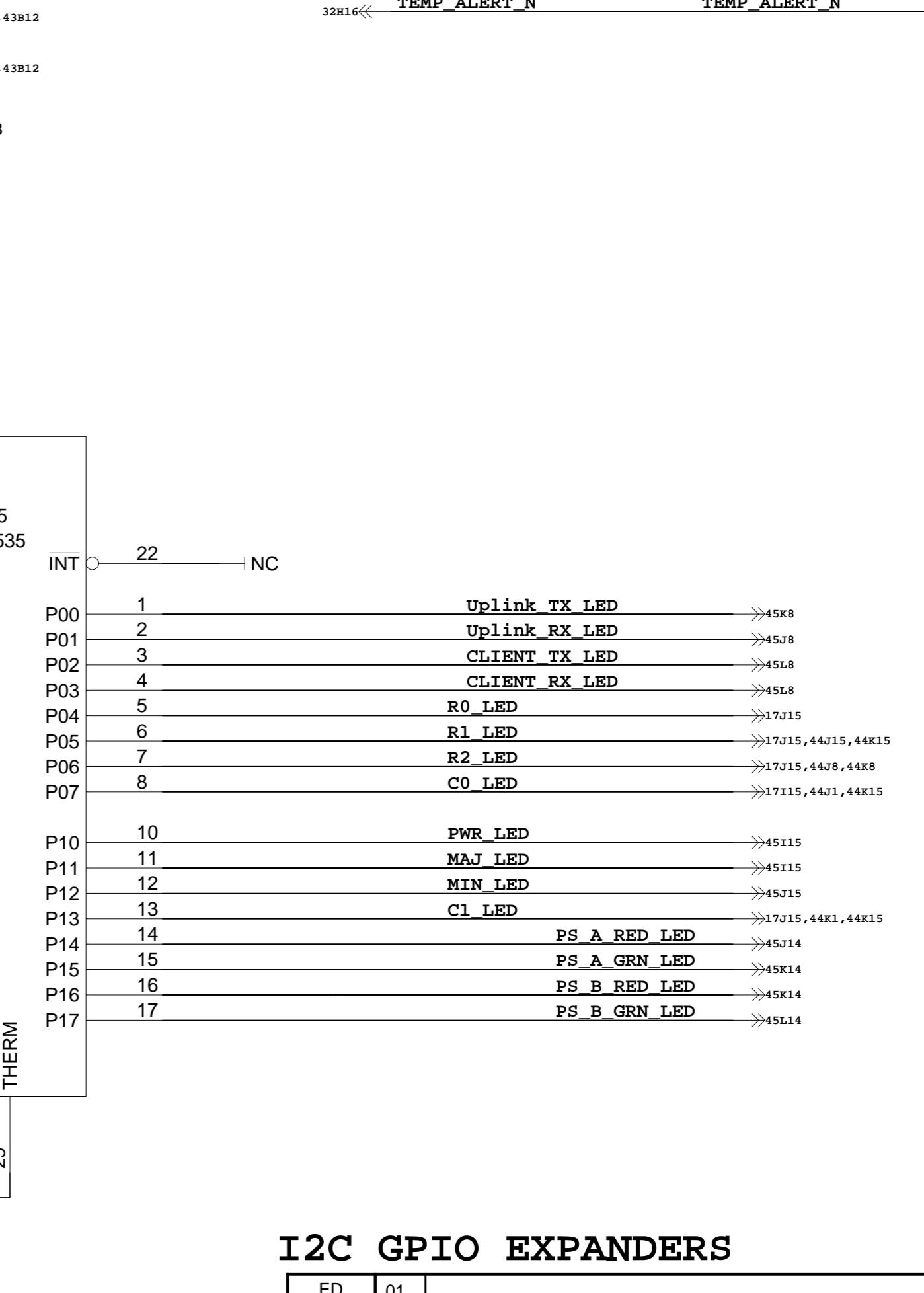
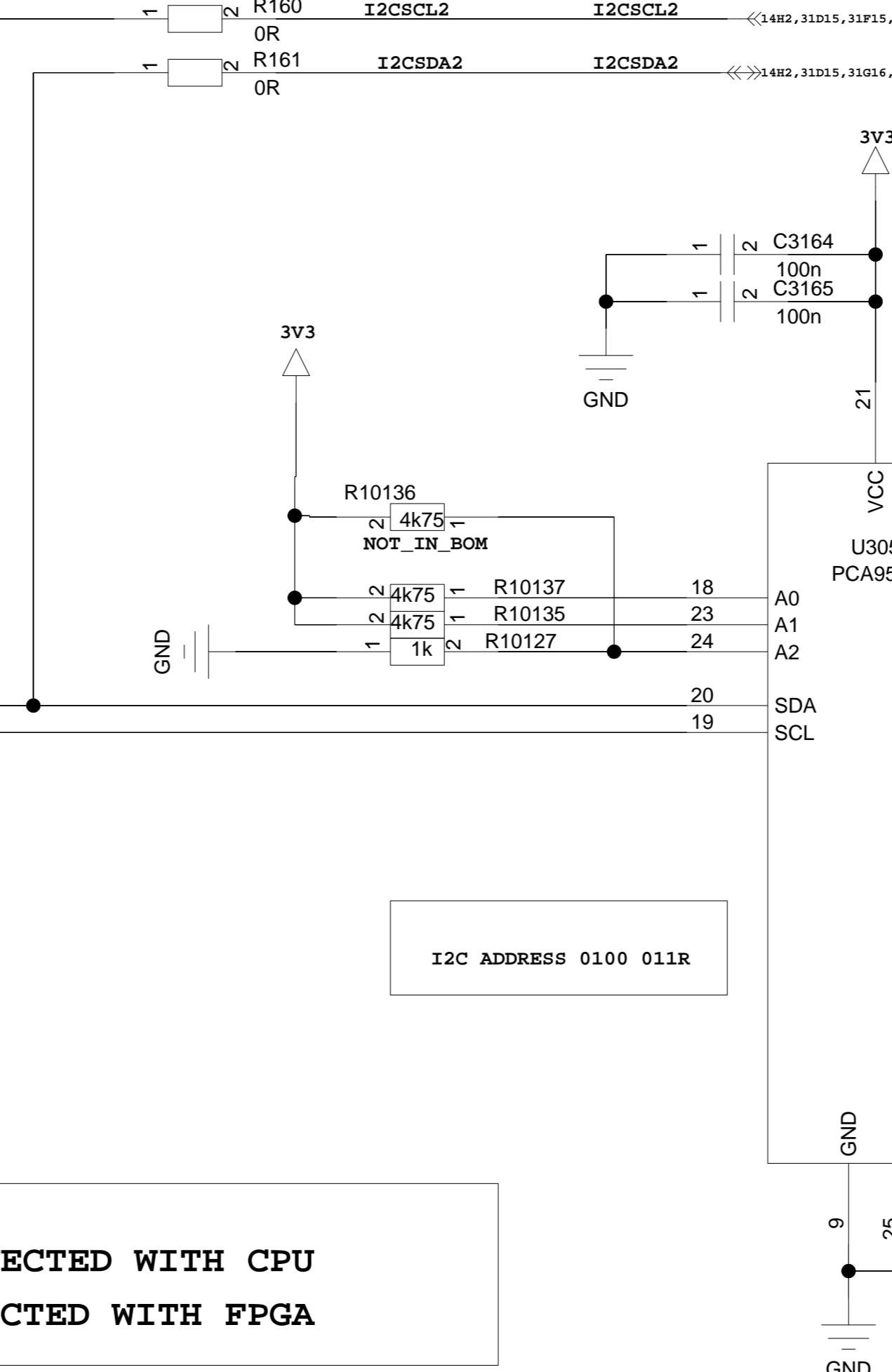
AIR OUT



I2C ADDRESS 0100 010R



DEFAULT: OH_SCL_3 and OH_SDA_3 are CONNECTED WITH CPU
BACKUP: OH_SCL_3 and OH_SDA_3 are CONNECTED WITH FPGA



I2C GPIO EXPANDERS

ED	01				
					46/46