DS

1. LATTICE ISPPAC-POWR1014A（U98） 上电时序控制电路
   1. 管脚描述

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Item No | Pin No | Name | Description | Comment |
| 1 | 43 | PLD\_MCLK | CMOS Output | 8MHz Clock I/O (Tristate) , CMOS; For future use |
| 2 | 39 | I2CSCL1 | Input | I2C Serial Clock Input |
| 3 | 38 | I2CSDA1 | Bi-directional | I2C Serial Data, Bi-directional Pin, Open Drain |
| 4 | 25 | VMON1 | Input | 3V3\_CFP\_CLIENT |
| 5 | 26 | VMON2 | Input | 0V9\_VDD\_A |
| 6 | 27 | VMON3 | Input | 0V9\_VDD\_D |
| 7 | 28 | VMON4 | Input | 0V9\_FF\_DCSU |
| 8 | 32 | VMON5 | Input | 1V0 |
| 9 | 33 | VMON6 | Input | 1V2 |
| 10 | 34 | VMON7 | Input | 1V2\_FF\_AVD |
| 11 | 35 | VMON8 | Input | 1V8 |
| 12 | 36 | VMON9 | Input | 3V3 |
| 13 | 37 | VMON10 | Input | 3V3\_CFP\_LINE |
| 14 | 42 | PLD\_CLK | CMOS Output | 250kHz PLD Clock Output (Tristate), CMOS; For future use |
| 15 | 12 | OUT4 | Open-Drain Output | EN\_0V9\_VDD\_A |
| 16 | 11 | OUT5 | Open-Drain Output | EN\_0V9\_VDD\_D |
| 17 | 10 | OUT6 | Open-Drain Output | EN\_0V9\_FF\_DCSU |
| 18 | 9 | OUT7 | Open-Drain Output | EN\_1V0 |
| 19 | 8 | OUT8 | Open-Drain Output | EN\_1V2 |
| 20 | 6 | OUT9 | Open-Drain Output | EN\_1V2\_FF\_AVD |
| 21 | 5 | OUT10 | Open-Drain Output | EN\_1V8 |
| 22 | 4 | OUT11 | Open-Drain Output | EN\_3V3\_CPU\_FPGA |
| 23 | 3 | OUT12 | Open-Drain Output | EN\_3V3\_CFP\_L |
| 24 | 2 | OUT13 | Open-Drain Output | EN\_3V3\_CFP\_C |
| 25 | 1 | OUT14 | Open-Drain Output | LOCAL\_PWR\_STATUS |

Table 1: Lattice CPLD Pin Assignment

* 1. 上电时序要求描述

单板上电从OTU4开始，按顺序升序直至OUT14,使能间隔为200ms左右；低电平使能有效。电源的输出电压有效范围见下表。

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **VMON Channel** | **Monitored Power** | **MIN** | **MAX** | **Ripple** | **Noise** | **Rising Time** | **Falling Time** |
| VMON1 | **3V3\_CFP\_CLIENT** | 2.97 | 3.63 |  |  |  |  |
| VMON2 | **0V9\_VDD\_A** | 0.7875 | 1.0175 |  |  |  |  |
| VMON3 | **0V9\_VDD\_D** | 0.7875 | 1.0175 |  |  |  |  |
| VMON4 | **0V9\_FF\_DCSU** | 0.7875 | 1.0175 |  |  |  |  |
| VMON5 | **1V0** | 0.9 | 1.1 |  |  |  |  |
| VMON6 | **1V2** | 1.08 | 1.32 |  |  |  |  |
| VMON7 | **1V2\_FF\_AVD** | 1.08 | 1.32 |  |  |  |  |
| VMON8 | **1V8** | 1.62 | 1.98 |  |  |  |  |
| VMON9 | **3V3** | 2.97 | 3.63 |  |  |  |  |
| VMON10 | **3V3\_CFP\_LINE** | 2.97 | 3.63 |  |  |  |  |

Table 1: ASC0 Voltage & Current Min/Max Values

Note: 1. 12V power supply is powered up when the main board is inserted.

* 1. IIC要求描述

IIC 传输速度**100KHZ**；

IIC Address = **1011\_110R;**

CPU上边连接器(XS1)引脚定义如下：

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 3V3 | Host Map | 模块电源输入，  3.3V |
| 2 | 3V3 |  |
| 3 | 3V3 |  |
| 4 | E\G |  | 电源地 |
| 5 | E\G |  |
| 6 | /RESET\_CTR | **RESET\_CTR\_N** | 上电复位输出控制线，模块外部输入信号 |
| 7 | DUG\_RX |  | 调试口，RS232接口，信号接收线 |
| 8 | DUG\_TX |  | 调试口，RS232接口，信号发送线 |
| 9 | UART\_RX |  | 串口收，TTL接口 |
| 10 | UART\_TX |  | 串口发，TTL接口 |
| 11 | E\G |  | 电源地 |
| 12 | I2CSCL1 |  | I2C接口1时钟 |
| 13 | I2CSDA1 |  | I2C接口1数据线 |
| 14 | E\G |  |  |
| 15 | /IRQ1 | **FPGA\_INT\_N** | 外部中断请求1 |
| 16 | /IRQ2 | **FF\_INTB\_N\_33** | 外部中断请求2 |
| 17 | E\G |  | 电源地 |
| 18 | /MPC\_HRESET | **MPC\_HRESET\_N** | CPU硬复位输入 |
| 19 | /PORESET | **PORESET\_N** | 复位输出，控制模块外的外设复位，输出受/RESET\_CTR信号控制 |
| 20 | E\G |  |  |
| 21 | /R/W | **R\_W** | 本地总线读/写控制线，输出， |
| 22 | TA | **TA** |  |
| 23 | /CS2 | **CS2\_N** | 本地总线片选2 |
| 24 | /CS3 | **CS3\_N** | 本地总线片选3 |
| 25 | /CS\_BOOT |  | 本地总线片选0，如果BOOT芯片在模块外使用 |
| 26 | E\G |  | 电源地 |
| 27 | /TSEC\_MDC | **TSEC\_MDC** | 模块外接以太网接口 |
| 28 | /TSEC2\_RXD3 | **P5\_TXD3** |
| 29 | /TSEC2\_RXD2 | **P5\_TXD2** |
| 30 | /TSEC2\_RXD1 | **P5\_TXD1** |
| 31 | /TSEC2\_RXD0 | **P5\_TXD0** |
| 32 | /TSEC2\_RXER |  | 接电阻到电源地 |
| 33 | E\G |  | 电源地 |
| 34 | /TSEC2\_RX\_DV | **P5\_OEN** | 模块外接以太网接口 |
| 35 | /TSEC2\_RX\_CLK | **P5\_TXCLK** |
| 36 | /TSEC2\_TXD3 | **P5\_RXD3** |
| 37 | /TSEC2\_TXD2 | **P5\_RXD2** |
| 38 | /TSEC2\_TXD1 | **P5\_RXD1** |
| 39 | /TSEC2\_TXD0 | **P5\_RXD0** |
| 40 | /TSEC2\_TX\_EN | **P5\_RXDV** |
| 41 | /TSEC2\_GTX\_CLK125 | **TSEC2\_GTX\_CLK125** |
| 42 | /TSEC2\_GTX\_CLK | **P5\_RXCLK** |
| 43 | E\G |  | 电源地 |
| 44 | RX- | **CPU\_LAN\_RX\_N** | 模块百兆以太网接口收- |
| 45 | RX+ | **CPU\_LAN\_RX\_P** | 模块百兆以太网接口收+ |
| 46 | E\G |  | 电源地 |
| 47 | E\G |  |
| 48 | 3V3 |  | 模块电源输入，  3.3V |
| 49 | 3V3 |  |
| 50 | 3V3 |  |

|  |  |  |  |
| --- | --- | --- | --- |
| 100 | 3V3 | Host Map | 模块电源输入，  3.3V |
| 99 | 3V3 |  |
| 98 | 3V3 |  |
| 97 | E\G |  | 电源地 |
| 96 | E\G |  |
| 95 | MPC\_TDO |  | JTAG， |
| 94 | MPC\_TMS |  |
| 93 | MPC\_TRST |  |
| 92 | MPC\_TDI |  |
| 91 | /MPC\_TCK |  |
| 90 | E\G |  | 电源地 |
| 89 | I2CSCL2 |  | I2C接口2时钟 |
| 88 | I2CSDA2 |  | I2C接口2数据线 |
| 87 | E\G |  |  |
| 86 | CLK0 |  | 时钟 |
| 85 | /IRQ3 | **ENET\_INT\_N** | 外部中断请求3 |
| 84 | E\G |  | 电源地 |
| 83 | /MPC\_SRESET | **MPC\_SRESET\_N** | CPU软复位输入 |
| 82 | /MRESET | **MRESET\_N** | 人工复位输入 |
| 81 | E\G |  |  |
| 80 | /OE |  | 输出使能控制，输出 |
| 79 | /WE |  | 写使能 |
| 78 | /CS\_EX4 |  | 扩展片选，由CS1,LA6和LA7译码产生，依次产生：读板卡地址，CS\_EX2, CS\_EX3 ,CS\_EX4 |
| 77 | /CS\_EX3 | **CS\_EX3** |
| 76 | /CS\_EX2 | **CS\_EX2** |
| 75 | E\G |  | 电源地 |
| 74 | /TSEC\_MDIO | **TSEC\_MDIO** |  |
| 73 |  |  |  |
| 72 | PCIE\_CLKN | **PCIE\_REF\_CLK\_N** | PCIE接口信号 |
| 71 | PCIE\_CLKP | **PCIE\_REF\_CLK\_P** |
| 70 | PCIE\_RXN | **PCIE\_RX\_N** |
| 69 | PCIE\_RXP | **PCIE\_RX\_P** |
| 68 | E\G |  | 电源地 |
| 67 | PCIE\_TXN | **PCIE\_TX\_N** | PCIE接口信号 |
| 66 | PCIE\_TXP | **PCIE\_TX\_P** |
| 65 |  |  |  |
| 64 | SPICLK | **SPICLK** | SPI接口时钟 |
| 63 | SPIMISO | **SPIMISO** | SPI数据输入 |
| 62 | SPIMOSI | **SPIMOSI** | SPI数据输出 |
| 61 | SPISEL\_SLAVE | **SPISEL\_SLAVE** | SPI片选 |
| 60 |  |  |  |
| 59 |  |  |  |
| 58 | E\G |  | 电源地 |
| 57 | TX- | **CPU\_LAN\_TX\_N** | 模块百兆以太网接口发- |
| 56 | TX+ | **CPU\_LAN\_TX\_P** | 模块百兆以太网接口发+ |
| 55 | E\G |  | 电源地 |
| 54 | E\G |  |
| 53 | 3V3 |  | 模块电源输入，  3.3V |
| 52 | 3V3 |  |
| 51 | 3V3 |  |

CPU下边连接器(XS2)引脚定义如下：

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 3V3 | Host Map | 模块电源输入，  3.3V |
| 2 | 3V3 |  |
| 3 | 3V3 |  |
| 4 | E\G |  | 电源地 |
| 5 | E\G |  |
| 6 | LA30 |  | 本地总线地址线 |
| 7 | LA28 |  |
| 8 | LA26 |  |
| 9 | LA24 |  |
| 10 | LA22 |  |
| 11 | LA20 |  |
| 12 | LA18 |  |
| 13 | LA16 |  |
| 14 | E\G |  | 电源地 |
| 15 | LA14 |  | 本地总线地址线 |
| 16 | LA12 |  |
| 17 | LA10 |  |
| 18 | LA8 |  |
| 19 | LA6 |  |
| 20 | E\G |  | 电源地 |
| 21 | GPIO23 | **SRAM\_ZZ** | CPU输入输出端口 |
| 22 | GPIO2 | **SRAM\_FT\_N** |
| 23 | GPIO3 | **SRAM\_MODE** |
| 24 | GPIO5 |  |
| 25 | GPIO18 | **SRAM\_E3\_N\_B** |
| 26 | GPIO19 | **SRAM\_E2\_B** |
| 27 | GPIO14 | **SRAM\_E1\_N\_B** |
| 28 | GPIO7 | **SRAM\_E3\_N\_A** |
| 29 | GPIO9 | **SRAM\_E2\_A** |
| 30 | GPIO12 | **SRAM\_E1\_N\_A** |
| 31 | GPIO21 | **SRAM\_ADV** |
| 32 | E\G |  | 电源地 |
| 33 | GID0 | GID0 | 板卡地址码，外部输入，由CS1,LA7和LA6译码产生读板卡地址片选 |
| 34 | GID1 | GID1 |
| 35 | GID2 | GID2 |
| 36 | GID3 | GID3 |
| 37 | E\G |  | 电源地 |
| 38 | LD14 |  | 本地总线数据线 |
| 39 | LD12 |  |
| 40 | LD10 |  |
| 41 | LD8 |  |
| 42 | LD6 |  |
| 43 | LD4 |  |
| 44 | LD2 |  |
| 45 | LD0 |  |
| 46 | E\G |  | 电源地 |
| 47 | E\G |  |
| 48 | 3V3 |  | 模块电源输入，  3.3V |
| 49 | 3V3 |  |
| 50 | 3V3 |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 100 | 3V3 | Host Map | | 模块电源输入，  3.3V |
| 99 | 3V3 |  | |
| 98 | 3V3 |  | |
| 97 | E\G |  | | 电源地 |
| 96 | E\G |  | |
| 95 | LA31 |  | | 本地总线地址线 |
| 94 | LA29 |  | |
| 93 | LA27 |  | |
| 92 | LA25 |  | |
| 91 | LA23 |  | |
| 90 | LA21 |  | |
| 89 | LA19 |  | |
| 88 | LA17 |  | |
| 87 | E\G |  | | 电源地 |
| 86 | LA15 |  | | 本地总线地址线 |
| 85 | LA13 |  | |
| 84 | LA11 |  | |
| 83 | LA9 |  | |
| 82 | LA7 |  | |
| 81 | E\G |  | | 电源地 |
| 80 | GPIO1 | **CPU\_FPGA\_SPI\_CS\_EN** | | CPU输入输出端口 |
| 79 | GPIO4 | **CPU\_FF\_SPI\_CS\_EN** | |
| 78 | GPIO6 | **CPU\_MATRIX\_SPI\_CS\_EN** | |
| 77 | GPIO22 | **CPU\_FPGA\_DONE** | |
| 76 | GPIO17 | **CPU\_FPGA\_INIT\_N** | |
| 75 | GPIO16 | **SI5368\_RESET\_N** | |
| 74 | GPIO8 | **PU\_5368\_SPI\_CS\_EN** | |
| 73 | GPIO10 | **SI5368\_LOL** | |
| 72 | GPIO11 | **CPU\_TEST\_0** | |
| 71 | GPIO13 | **ENET\_RST\_N** | |
| 70 | GPIO15 | **CPU\_FPGA\_PROG\_N** | |
| 69 | E\G |  | | 电源地 |
| 68 | GID4 | GID4 | | 板卡地址码，外部输入，由CS1,LA7和LA6译码产生读板卡地址片选 |
| 67 | GID5 | GID5 | |
| 66 | GID6 | GID6 | |
| 65 | GID7 | GID7 | |
| 64 | E\G |  | | 电源地 |
| 63 | LD15 |  | | 本地总线数据线 |
| 62 | LD13 |  | |
| 61 | LD11 |  | |
| 60 | LD9 |  | |
| 59 | LD7 |  | |
| 58 | LD5 |  | |
| 57 | LD3 |  | |
| 56 | LD1 |  | |
| 55 | E\G | |  | 电源地 |
| 54 | E\G | |  |
| 53 | 3V3 | |  | 模块电源输入，  3.3V |
| 52 | 3V3 | |  |
| 51 | 3V3 | |  |

1. XILINX XC7A100T-2FGG676I（U286）pin assignment
2. IIC 1: IIC Address Assignment

|  |  |  |  |
| --- | --- | --- | --- |
| # | Ref | Primary IIC Address | Backup IIC Address |
| 1 | U175 | **1010 010R** | **1010 XXXR** |
| 2 | U308 | **XXXX XXXR** | **XXXX XXXR** |
| 3 | U98 | **1011 110R** | **1011 010R** |
| 4 | U297 | **0100 001R** | **0000 001R** |
| 5 | U4 | **0011 000R** | **0011 011R** |



1. IIC 2: GPIO EXPANDERS(PCA9535) Address Assignment

|  |  |  |  |
| --- | --- | --- | --- |
| # | Ref | Primary IIC Address | Backup IIC Address |
| 1 | U302 | **0100 000R** | **0100 100R** |
| 2 | U304 | **0100 010R** | **0100 110R** |
| 3 | U305 | **0100 011R** | **0100 111R** |

1. IIC 2: IIC EXPANDERS(PCA9548A) Address Assignment

|  |  |  |  |
| --- | --- | --- | --- |
| # | Ref | Primary IIC Address | Backup IIC Address |
| 1 | U176 | **1110 101R** | **1110 001R** |
| 2 | U177 | **1110 010R** | **1110 110R** |



1. MDIO: Address Assignment

|  |  |  |  |
| --- | --- | --- | --- |
| # | Ref | Primary Address | Note |
| 1 | U127 | **00010** | Ethernet Switch |
| 2 | X26 | **00011** | **CFP Line** |
| 3 | X41 | **00111** | **CFP Client** |

IIC Expander ports assignment:

1. U176 = **1110 101R**

|  |  |  |
| --- | --- | --- |
| Port No | IIC Port Map | Note |
| 0 | SFP+ 0 | SFP + module Access |
| 1 | SFP+ 1 | SFP + module Access |
| 2 | SFP+ 2 | SFP + module Access |
| 3 | SFP+ 3 | SFP + module Access |
| 4 | SFP+ 4 | SFP + module Access |
| 5 | SFP+ 5 | SFP + module Access |
| 6 | SFP+ 6 | SFP + module Access |
| 7 | SFP+ 7 | SFP + module Access |

1. U176 = **1110 010R**

|  |  |  |
| --- | --- | --- |
| Port No | IIC Port Map | Note |
| 0 | SFP+ 8 | SFP + module Access |
| 1 | SFP+ 9 | SFP + module Access |
| 2 | OSC SFP 0 | OSC SFP module Access |
| 3 | OSC SFP 1 | OSC SFP module Access |
| 4 | 1V2 power module | 1V2 power module Access |
| 5 | 0V9\_A power module | 0V9\_A power module Access |
| 6 | 0V9\_D\_1 power module | 0V9\_D\_1 power module Access |
| 7 | 0V9\_D\_2 power module | 0V9\_D\_2 power module Access |

# Main Clock Configuration Data：

# Name: Si5368

#INPUT

# Name: CKIN

# Channel: 1

# Frequency (MHz): 25.000000

# N3: 625

# Maximum (MHz): 28.483072

# Minimum (MHz): 24.363827

#END\_INPUT

#PLL

# Name: PLL

# Frequency (MHz): 4976.640000

# f3 (MHz): 0.040000

# N1\_HS: 4

# N2\_HS: 8

# N2\_LS: 15552

# Phase Offset Resolution (ns): 0.80376

# BWSEL\_REG Option: Frequency (Hz)

# 5: 93

# 4: 186

# 3: 376

# 2: 769

# 1: 1612

#END\_PLL

#OUTPUT

# Name: CKOUT

# Channel: 1

# Frequency (MHz): 155.520000

# NC1\_LS: 8

# CKOUT1 to CKIN1 Ratio: 3888 / 625

# Maximum (MHz): 177.187494

# Minimum (MHz): 151.562495

#END\_OUTPUT

#OUTPUT

# Name: CKOUT

# Channel: 2

# Frequency (MHz): 155.520000

# NC\_LS: 8

# CKOUT2 to CKOUT1 Ratio: 1 / 1

# Maximum (MHz): 177.187494

# Minimum (MHz): 151.562495

#END\_OUTPUT

#OUTPUT

# Name: CKOUT

# Channel: 3

# Frequency (MHz): 155.520000

# NC\_LS: 8

# CKOUT3 to CKOUT1 Ratio: 1 / 1

# Maximum (MHz): 177.187494

# Minimum (MHz): 151.562495

#END\_OUTPUT

#OUTPUT

# Name: CKOUT

# Channel: 4

# Frequency (MHz): 622.080000

# NC\_LS: 2

# CKOUT4 to CKOUT1 Ratio: 4 / 1

# Maximum (MHz): 708.749977

# Minimum (MHz): 606.249980

#END\_OUTPUT

#OUTPUT

# Name: CKOUT

# Channel: 5

# Frequency (MHz): 38.880000

# NC\_LS: 32

# CKOUT5 to CKOUT1 Ratio: 1 / 4

# Maximum (MHz): 44.296873

# Minimum (MHz): 37.890623

#END\_OUTPUT

#CONTROL\_FIELD

# Register-based Controls

# FREE\_RUN\_EN: 0x0

# CKOUT\_ALWAYS\_ON: 0x1

# CK\_CONFIG\_REG: 0x0

# BYPASS\_REG: 0x0

# CK\_PRIOR4: 0x3

# CK\_PRIOR3: 0x2

# CK\_PRIOR2: 0x1

# CK\_PRIOR1: 0x0

# CKSEL\_REG: 0x0

# DHOLD: 0x0

# SQ\_ICAL: 0x1

# BWSEL\_REG: 0x5

# AUTOSEL\_REG: 0x2

# HIST\_DEL: 0x1B

# ICMOS: 0x1

# SFOUT1\_REG: 0x3

# SFOUT2\_REG: 0x3

# SFOUT3\_REG: 0x3

# SFOUT4\_REG: 0x2

# SFOUT\_FSYNC\_REG: 0x2

# FOSREFSEL: 0x2

# HLOG\_4: 0x0

# HLOG\_3: 0x0

# HLOG\_2: 0x0

# HLOG\_1: 0x0

# HIST\_AVG: 0x18

# HLOG\_FSYNC: 0x0

# DSBLFSYNC\_REG: 0x0

# DSBL4\_REG: 0x0

# DSBL3\_REG: 0x0

# DSBL2\_REG: 0x0

# DSBL1\_REG: 0x0

# ALIGN\_THR: 0x2

# PD\_CK4: 0x1

# PD\_CK3: 0x1

# PD\_CK2: 0x1

# PD\_CK1: 0x0

# FSYNC\_SKEW: 0x0

# FSYNC\_PW: 0x1

# FPW\_VALID: 0x1

# FSYNC\_ALIGN\_REG: 0x0

# FSYNC\_SWTCH\_REG: 0x0

# FSKEW\_VALID: 0x1

# CLAT: 0x0

# FLAT: 0x0

# FLAT\_VALID: 0x1

# FOS\_EN: 0x0

# FOS\_THR: 0x1

# VALTIME: 0x1

# LOCKT: 0x4

# ALRMOUT\_PIN: 0x1

# CK3\_BAD\_PIN: 0x1

# CK2\_BAD\_PIN: 0x1

# CK1\_BAD\_PIN: 0x1

# LOL\_PIN: 0x1

# INT\_PIN: 0x0

# INCDEC\_PIN: 0x1

# FSYNC\_ALIGN\_PIN: 0x1

# CK4\_ACTV\_PIN: 0x1

# CK3\_ACTV\_PIN: 0x1

# CK2\_ACTV\_PIN: 0x1

# CK1\_ACTV\_PIN: 0x1

# CKSEL\_PIN: 0x1

# FSYNC\_ALIGN\_POL: 0x1

# FSYNC\_POL: 0x1

# FSYNCOUT\_POL: 0x1

# CK\_ACTV\_POL: 0x1

# CK\_BAD\_POL: 0x1

# LOL\_POL: 0x1

# INT\_POL: 0x1

# LOS4\_MSK: 0x1

# LOS3\_MSK: 0x1

# LOS2\_MSK: 0x1

# LOS1\_MSK: 0x1

# LOSX\_MSK: 0x1

# ALIGN\_MSK: 0x1

# FOS4\_MSK: 0x1

# FOS3\_MSK: 0x1

# FOS2\_MSK: 0x1

# FOS1\_MSK: 0x1

# LOL\_MSK: 0x1

# N1\_HS: 0x0

# NC1\_LS: 0x7

# NC2\_LS: 0x7

# NC3\_LS: 0x7

# NC4\_LS: 0x1

# NC5\_LS: 0x1F

# N2\_LS: 0x3CBF

# N2\_HS: 0x4

# N31: 0x270

# N32: 0x270

# N33: 0x270

# N34: 0x270

# CLKIN4RATE: 0x0

# CLKIN3RATE: 0x0

# CLKIN2RATE: 0x0

# CLKIN1RATE: 0x0

# LOS1\_EN: 0x3

# LOS2\_EN: 0x3

# LOS3\_EN: 0x3

# LOS4\_EN: 0x3

# FOS1\_EN: 0x1

# FOS2\_EN: 0x1

# FOS3\_EN: 0x1

# FOS4\_EN: 0x1

# INDEPENDENTSKEW1: 0x0

# INDEPENDENTSKEW2: 0x0

# INDEPENDENTSKEW3: 0x0

# INDEPENDENTSKEW4: 0x0

# INDEPENDENTSKEW5: 0x0

#END\_CONTROL\_FIELD

#REGISTER\_MAP

0, 34h

1, E4h

2, 52h

3, 15h

4, 9Bh

5, 5Bh

6, 13h

7, 12h

8, 00h

9, C0h

10, 00h

11, 4Eh

12, 88h

13, 01h

14, 00h

15, 00h

16, 00h

17, 80h

18, 00h

19, 2Ch

20, 3Eh

21, FFh

22, DFh

23, 1Fh

24, 3Fh

25, 00h

26, 00h

27, 07h

28, 00h

29, 00h

30, 07h

31, 00h

32, 00h

33, 07h

34, 00h

35, 00h

36, 01h

37, 00h

38, 00h

39, 1Fh

40, 80h

41, 3Ch

42, BFh

43, 00h

44, 02h

45, 70h

46, 00h

47, 02h

48, 70h

49, 00h

50, 02h

51, 70h

52, 00h

53, 02h

54, 70h

55, 00h

56, 00h

131, 1Fh

132, 02h

138, 0Fh

139, FFh

140, 00h

141, 00h

142, 00h

143, 00h

144, 00h

136, 40h

#END\_REGISTER\_MAP

#END\_PROFILE

Debug Connectors：

1. Lattice debug header



IIC EXPANDERS ports assignment:

1. U 176

|  |  |
| --- | --- |
| Port No. | Port assignment |
| 0 | **SFP+ 0** |
| 1 | **SFP+ 1** |
| 2 | **SFP+ 2** |
| 3 | **SFP+ 3** |
| 4 | **SFP+ 4** |
| 5 | **SFP+ 5** |
| 6 | **SFP+ 6** |
| 7 | **SFP+ 7** |

1. U 177

|  |  |
| --- | --- |
| Port No. | Port assignment |
| 0 | **SFP+ 8** |
| 1 | **SFP+ 9** |
| 2 | **OSC\_SFP 0** |
| 3 | **OSC\_SFP 1** |
| 4 | **1V2\_M power module for test** |
| 5 | **0V9\_A power module for test** |
| 6 | **0V9\_D1 power module for test** |
| 7 | **0V9\_D2 power module for test** |

M21036 Port Assignment:

|  |  |
| --- | --- |
| Port No. | Port assignment |
| IN\_AUX | **SYS\_TXO\_15** |
| IN\_00 | **LINE\_TXO\_10** |
| IN\_01 | **LINE\_TXO\_8** |
| IN\_02 | **LINE\_TXO\_9** |
| IN\_03 |  |
| IN\_04 | **CLIENT\_CFP\_0\_RX** |
| IN\_05 | **SFP+\_RXD0** |
| IN\_06 | **SFP+\_RXD3** |
| IN\_07 | **SFP+\_RXD1** |
| IN\_08 | **LINE\_TXO\_6** |
| IN\_09 | **CLIENT\_CFP\_7\_RX** |
| IN\_10 | **LINE\_TXO\_5** |
| IN\_11 | **CLIENT\_CFP\_6\_RX** |
| IN\_12 | **CLIENT\_CFP\_1\_RX** |
| IN\_13 | **SFP+\_RXD4** |
| IN\_14 | **CLIENT\_CFP\_2\_RX** |
| IN\_15 | **SFP+\_RXD5** |
| IN\_16 | **LINE\_TXO\_2** |
| IN\_17 | **LINE\_TXO\_0** |
| IN\_18 | **LINE\_TXO\_1** |
| IN\_19 | **CLIENT\_CFP\_5\_RX** |
| IN\_20 | **SFP+\_RXD7** |
| IN\_21 | **SFP+\_RXD8** |
| IN\_22 |  |
| IN\_23 | **SFP+\_RXD9** |
| IN\_24 | **LINE\_TXO\_11** |
| IN\_27 | **CLIENT\_CFP\_9\_RX** |
| IN\_28 | **GTX\_TX** |
| IN\_31 | **SFP+\_RXD2** |
| IN\_32 | **LINE\_TXO\_7** |
| IN\_35 | **CLIENT\_CFP\_8\_RX** |
| IN\_36 | **CLIENT\_CFP\_3\_RX** |
| IN\_39 | **SFP+\_RXD6** |
| IN\_40 | **LINE\_TXO\_3** |
| IN\_43 | **LINE\_TXO\_4** |
| IN\_44 | **CLIENT\_CFP\_4\_RX** |
| IN\_47 |  |

|  |  |
| --- | --- |
| Port No. | Port assignment |
| OUT\_AUX | **SYS\_RXI\_15** |
| OUT \_00 | **LINE\_RXI\_1** |
| OUT \_01 | **SFP+\_TXD0** |
| OUT \_02 | **LINE\_RXI\_2** |
| OUT \_03 | **LINE\_RXI\_4** |
| OUT \_04 | **CLIENT\_CFP\_8\_TX** |
| OUT \_05 | **CLIENT\_CFP\_7\_TX** |
| OUT \_06 | **CLIENT\_CFP\_9\_TX** |
| OUT \_07 |  |
| OUT \_08 | **LINE\_RXI\_5** |
| OUT \_09 | **SFP+\_TXD1** |
| OUT \_10 | **LINE\_RXI\_6** |
| OUT \_11 | **SFP+\_TXD2** |
| OUT \_12 | **CLIENT\_CFP\_4\_TX** |
| OUT \_13 | **SFP+\_TXD6** |
| OUT \_14 | **CLIENT\_CFP\_5\_TX** |
| OUT \_15 | **SFP+\_TXD7** |
| OUT \_16 | **LINE\_RXI\_9** |
| OUT \_17 | **LINE\_RXI\_8** |
| OUT \_18 | **LINE\_RXI\_10** |
| OUT \_19 | **GTX\_RX** |
| OUT \_20 | **CLIENT\_CFP\_0\_TX** |
| OUT \_21 | **SFP+\_TXD5** |
| OUT \_22 | **CLIENT\_CFP\_1\_TX** |
| OUT \_23 | **CLIENT\_CFP\_3\_TX** |
| OUT \_24 | **LINE\_RXI\_3** |
| OUT \_27 |  |
| OUT \_28 | **LINE\_RXI\_0** |
| OUT \_31 | **SFP+\_TXD9** |
| OUT \_32 | **LINE\_RXI\_7** |
| OUT \_35 | **SFP+\_TXD3** |
| OUT \_36 | **CLIENT\_CFP\_6\_TX** |
| OUT \_39 | **SFP+\_TXD8** |
| OUT \_40 | **LINE\_RXI\_11** |
| OUT \_43 | **SFP+\_TXD4** |
| OUT \_44 | **CLIENT\_CFP\_2\_TX** |
| OUT \_47 |  |

GPIO EXPANDERS(PCA9535) Port Assignment

1. U302

|  |  |
| --- | --- |
| Port No. | Port assignment |
| P00 | **SFP+\_SGR\_0** |
| P01 | **SFP+\_SGR\_1** |
| P02 | **SFP+\_SGR\_2** |
| P03 | **SFP+\_SGR\_3** |
| P04 | **SFP+\_SGR\_4** |
| P05 | **SFP+\_SGR\_5** |
| P06 | **SFP+\_SGR\_6** |
| P07 | **SFP+\_SGR\_7** |
| P10 | **SFP+\_SRD\_0** |
| P11 | **SFP+\_SRD\_1** |
| P12 | **SFP+\_SRD\_2** |
| P13 | **SFP+\_SRD\_3** |
| P14 | **SFP+\_SRD\_4** |
| P15 | **SFP+\_SRD\_5** |
| P16 | **SFP+\_SRD\_6** |
| P17 | **SFP+\_SRD\_7** |

2.304

|  |  |
| --- | --- |
| Port No. | Port assignment |
| P00 | **SFP+\_SGR\_8** |
| P01 | **SFP+\_SGR\_9** |
| P02 | **SFP+\_SRD\_8** |
| P03 | **SFP+\_SRD\_9** |
| P04 | **OSC\_SRD\_0** |
| P05 | **OSC\_SGR\_0** |
| P06 | **OSC\_SRD\_1** |
| P07 | **OSC\_SGR\_1** |
| P10 | **P0\_RED\_LED** |
| P11 | **P1\_RED\_LED** |
| P12 | **CPU\_LAN\_LED\_0** |
| P13 | **CPU\_LAN\_LED\_1** |
| P14 | **PWR\_GRN\_LED** |
| P15 | **PWR\_RED\_LED** |
| P16 | **ALM\_RED\_LED** |
| P17 | **ALM\_GRN\_LED** |

1. U305

|  |  |
| --- | --- |
| Port No. | Port assignment |
| P00 | **Uplink\_TX\_LED** |
| P01 | **Uplink\_RX\_LED** |
| P02 | **CLIENT\_TX\_LED** |
| P03 | **CLIENT\_RX\_LED** |
| P04 | **R0\_LED** |
| P05 | **R1\_LED** |
| P06 | **R2\_LED** |
| P07 | **C0\_LED** |
| P10 | **PWR\_LED** |
| P11 | **MAJ\_LED** |
| P12 | **MIN\_LED** |
| P13 | **C1\_LED** |
| P14 | **PS\_A\_RED\_LED** |
| P15 | **PS\_A\_GRN\_LED** |
| P16 | **PS\_B\_RED\_LED** |
| P17 | **PS\_B\_GRN\_LED** |

Temperature Monitoring:

|  |  |
| --- | --- |
| Port No. | Port assignment |
| 1 | Air output |
| 2 | Air input |
| 3 | FPGA |
| 4 | Flexframer |