1. Consider the following code.

a. Assume that we have a hazard detection unit in a 5-stage pipelined architecture as learned in the class. We do not have a forwarding unit. The hazard detection unit stalls

```
instructions to resolve hazards. How many cycles would take to execute the code?

4 total Stalls, Since 2 WB instructions which are dependent sources.
                                        : N+K-1+2× * of dependent sources = 6+5-1+2×2 = 14 cycles
      N=6 total instructions
      k = 5 Stage processor
```

b. Repeat a. but assume that we also have a forwarding unit that forwards data from

```
N+k-1=6+5-1=10 eyeles since no stalls because for forwarding we have 0 stalls for any instruction other than Lw.
```

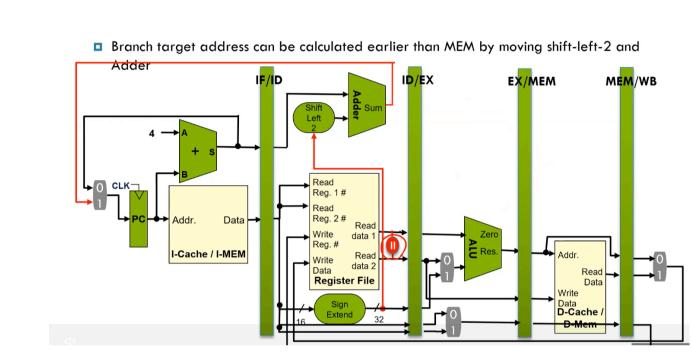
2. Consider the following code.

						Notation:
I1:	LOOP:	lw	\$a0,	0 (\$sı	(۱	· IF = F
I2:		slti	\$t0,	\$a0,	1	$\bullet$ ID = D
I3:		beq	\$t0,	\$zer	o, L1	• EXE = E
I4:		addi	\$v0,	\$zer	o <b>,</b> 1	• WB = W
I5:		addi	\$sp,	\$sp,	8	
I6:	L1:	lw	\$ra,	4 (\$s)	OV	· Data hazard
I7:		addi	\$t4,	\$ra,	8	o F → Flush
I8:		sw	\$t4,	0(\$t:	1)	$o  T \longrightarrow Take$
I9:		b	LOOP			
I10:		add	\$t4,	\$t4,	\$t3	o   → Forward

Assume that we have data forwarding paths from EX/MEM to EXE stage and from MEM/WB to EXE stage. We do early branch determination (branch outcome is generated in ID stage and the PC value is updated in ID stage). Branches are predicted untaken but the actual outcomes are as shown in the table. Show the first 18-cycles of execution of the code in a timing diagram shown below. When an instruction is stalled in a pipeline stage, fill the pipeline stage's name for the instruction until the end of stall (as shown on the page 44 of the lecture slide, "CSE140\_Lecture-4\_Processor-4"). Draw additional rows if needed. Show instruction id to the first column.

ID	Branch instructions	Branch outcome					
		(NT: not taken, T: taken)					
13	beq \$t0, \$zero, L1	T at the first					
		iteration					
		NT from the second					
		iteration					
19	b LOOP	Always T					

	CC1	CC2	ССЗ	CC4	CC5	CC6	CC7	CC8	CC9	CC10	CC11	CC12	CC13	CC14	CC15	CC16	CC17	CC18
11	F	D	E	M	W													
IZ		۴	D	D	لعلى	M	3											
L3			щ	F	D	םע	E	*	W									
I4					щ	4	F	F	F	F								
I6							F	D	E	M	W							
17								F	٥	D	لاا	M	W					
18									F	F	Δ	E	25	8				
I9											щ	D	E	M	3			
T10												F	F	F	Щ	F		
ΙI													F	D	E	M	)W	
<b>I</b> 2														F	D	D	E	M
13															F	F	D	D
邛																	F	F





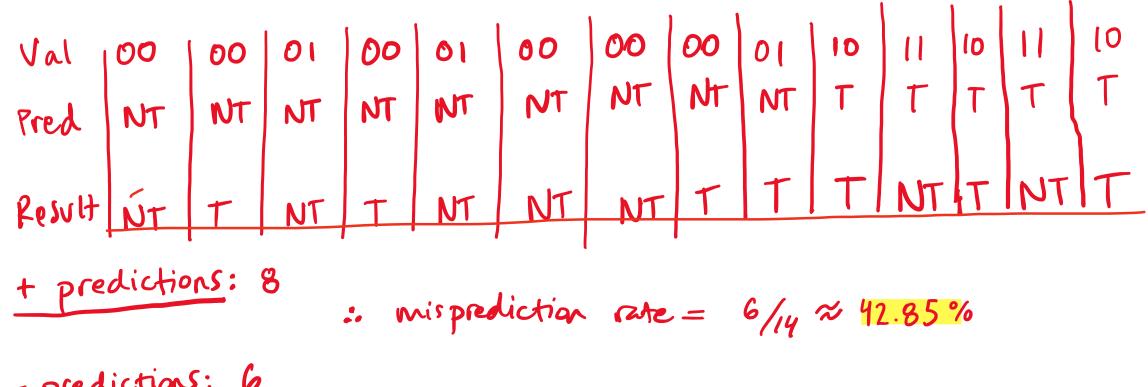
3. Consider a branch instruction that has following outcomes:

What is the misprediction rate of always-taken and always-not-taken predictors for this sequence of branch outcomes?

What is the misprediction rate of one-bit branch predictor for this sequence of branch outcomes? The initial predictor state is 0.

Outcon	rateomes. The initial predictor state is o.															
Val	10	۵	1	0	1	0	0	01	1	12	1	0	110	+ predictions:	5	
Pred	NT	NT	T	NT		NT	NT	NT	十	T	T	M	T NT NT T	المحارب المحارب	9	(9/14 \$ 64.28% m/sprediction) rate
Result	NT	\ T	NT	T	NT	NT	NT	T	T	T	NT	T	NTT	- predictions.	•	

What is the misprediction rate of two-bit branch predictor for this sequence of branch outcomes? The initial predictor state is 00.



- predictions: 6