Sunday, February 21, 2021 2:17 PM

Single and Pipelined Datapaths (10pts)

2. Assume that the execution time of individual steps of an instruction execution are like below:

IF	ID	EX	MEM	WB
100ps	120ps	220ps	300ps	120ps

a. If you design a single-cycle processor with the above latency information, what is the clock latency?

Clock Latency is the sum of all the steps.

100 + 120 + 220 + 300 + 120 = 860 ps

b. If you design a five-stage pipelined processor with the above latency information, what is the clock latency?

The clock latency would be the maximum sized time step.

This would be the memory step

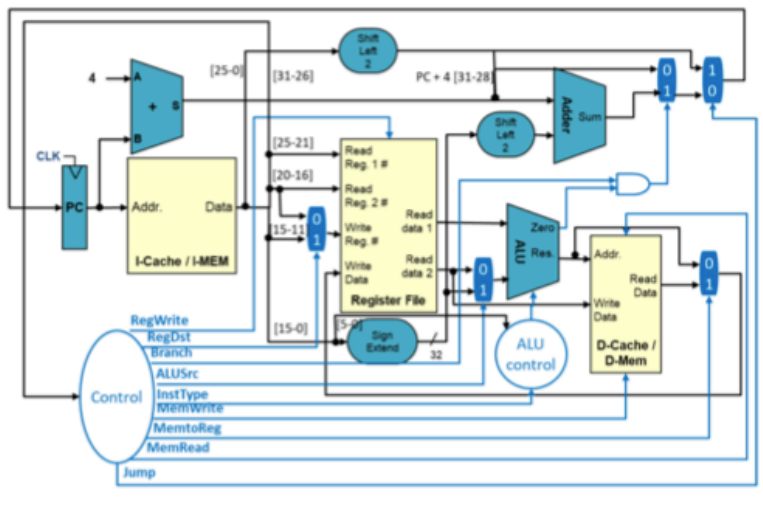
So the clock latency is 300 ps.

Single-cycle MIPS Architecture (10pts)

1. Assume that core components of single-cycle processor (shown below) have the following latencies:

I-Mem	Adder	Mux	ALU	Regs Rd/Wr	D-Mem	Sign-Extend	Shift-Left-2
40ps	50ps	20ps	100ps	80ps/60ps	200ps	20ps	20ps

Single-cycle processor data path:



Suppose that this data path executes only two types of instruction:

```
sub $rd, $rs, $rt
lw  $rt, offset($rs)
```

What would be the clock period to correctly execute the two instructions on the above single-cycle processor? Assume that PC register doesn't take any latency (i.e. Propagating a new PC value to I-Cache/I-Mem doesn't take any cycle).

40 ps $rd 80 ps

mux + AW = 20 + 100 = 120 ps

mux + wr = 20 + 60 = 80 ps

Total = 40 + 80 + 120 + 80 = 320 ps

Imem = 40 ps

For the input at $rs = 80 ps

Lastly for Dmem = 200 ps

mux + AW = 20 + 100 = 120

mux + wr = 20 + 60 = 80

Total = 200 + 80 + 40 + 80 + 120 = 520

520 > 320 ∴ Clock Period = 520 ps