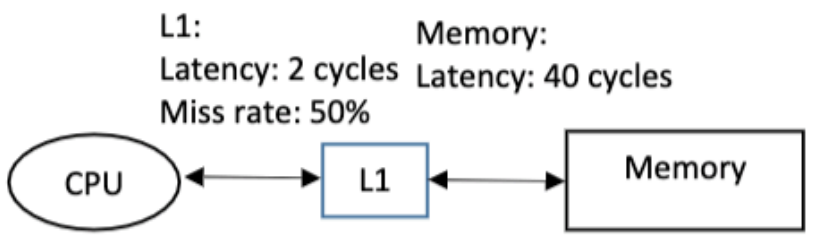
Friday, April 23, 2021 8:15 PM

CSE 140 Lab/HW#6 – 4/26 11:59PM

Caches (15pts + 15pts)

1. Suppose the following cache hierarchies.



a. What is the average memory access time?

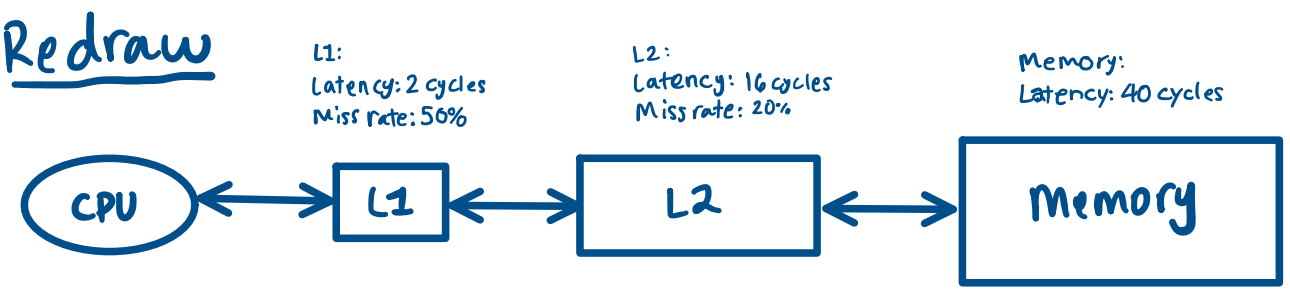
Miss penalty: time to access memory
Hit time: time to access cache.

AMAT = Hit time + miss rate × miss penalty
AMAT = 2 cycles + 0.5 × 40 cycles = 22 cycles

AMAT = 22 cycles

b. You want to improve the average memory access time so you added a L2 cache between L1 an Memory. L2 takes 16 cycles and miss rate is 20%. What is the average memory access time? And what is the speedup over the initial design (the above hierarchy)?

Redraw



$AMAT = Hit\ time_{L1} + Miss\ rate_{L1} \times [miss\ penalty_{L1}]$

$AMAT = Hit\ time_{L1} + Miss\ rate_{L1} \times [Hit\ time_{L2} + Miss\ rate_{L2} \times miss\ penalty_{L2}]$

$AMAT = 2\ cycles + 0.5 \times [16\ cycles + 0.2 \times 40\ cycles]$

AMAT = 14 cycles

Speed up $\Rightarrow \frac{22}{14} = 1.57$ times faster

Virtual memory (30pts)

2. Consider the following assumptions:
   - Size of virtual address: 32 bits
   - Size of physical memory: 2 GB
   - Page size: 16 KB → $2^{10} = 1\ kB \therefore 2^{14} = 16\ kB \therefore$ 14 bits needed for page offset number.
   - Size of an entry in page tables: 32 bits (or 4 B)

   What would be the size of the page table for this system?

32 − 14 = 18 bit virtual page numbers.

↳ Total entries in page table: 2^{18} entries

↳ Size of an entry: 2^2 bytes = 4 bytes

Size of page table = Total entries in page table * Size of an entry = $2^{18} \cdot 2^2$

$= 2^{18} \cdot 2^2$

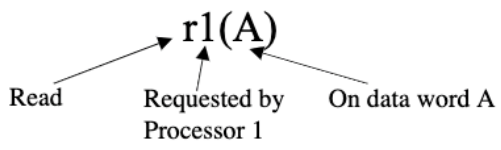
$= 2^{20}$

Cache Coherence (40 pts)

3. Consider the following reference stream:

   r1(A), r2(A), w3(B), r2(A), r3(A), r1(B), r2(B), w3(B), w3(A), r1(A)

   All of the references in the stream are to the same cache block but for different data words, A and B within the same cache block. r and w indicate read and write, respectively, and the digit refers to the processor issuing the reference.



   We run MESI protocol. Assume that all caches are initially empty and the accessed cache block is not evicted while executing the reference stream. Use the following cost model:
   - Read / write cache hit with no bus access: 1 cycle
   - Invalidation broadcasting without requesting the cache block (BusUpgr): 10 cycles
   - Request remote processor to send updated a cache block (BusRd / BusRdX): 50 cycles
   - Request the memory (or next level cache) to send a cache block (BusRd): 150 cycles

Fill the following table with the coherence state of the three processors, coherence message, and cache hit/miss for each memory references. Each column should show the status of the corresponding data word (either A or B). Show the total number of cycles used for running the reference stream.

	r1(A)	r2(A)	w3(B)	r2(A)	r3(A)	r1(B)	r2(B)	w3(B)	w3(A)	r1(A)
hit/miss	M	M	M	M	H	M	H	H	H	M
bus	BusRd	BusRd	BusRdX	BusRd	--	BusRd	--	BusUpgr	--	BusRd
State1	E	S	I	I	I	S	S	I	I	S
State2	I	S	I	S	S	S	S	I	I	I
State3	I	I	M	S	S	S	S	M	M	S
cycles	150	150	50	50	1	150	1	10	1	50

Total cycles: 613