Lab 3 Project Planning

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Feature Lists:

2 Weeks:

green: IFU
yellow: Single Cycle CPU
red: Math Libraries

4 Weeks:

green: Multi Cycle CPU, Basic Math Libraries
yellow: More Extensive Math Libraries
red: Pipelined CPU

8 Weeks:

green: Multi Cycle CPU, Extensive Math Library
yellow: More Math, Optimization
red: Pipelined CPU

6 Months:

green: Pipelined CPU, Optimization, Full Math Library
yellow:
red:

Unanswered Questions:

1. How do you implement an instruction fetch unit?
2. How do you implement memory?
3. How do you synchronize everything?
4. How do you implement math libraries?
5. How do you connect different parts together?
6. How do you debug?
7. How do you deal with hazards?
8. How do you organize everything?
9. How do you interface between MIPS and Verilog?
10. How do you implement memory?

Research Schedule:

Week 1: 1, 10
Week 2: 5
Week 3: 2, 4, 6
Week 4: 8
Week 5: 3
Week 6:

Week 7:
Week 8:

Month 3: 7, 9
Month 4:
Month 5:
Month 6:

Division of Labor:
Week 1: get IFU working (Berit, Joe); start integrating rest of CPU (Orion)
Week 2: debug IFU (Berit, Joe); finish integrating CPU (Orion)
Week 3: Start implementing math libraries (Berit); Optimize and final testing on CPU (Joe, Orion)
Week 4: Debug and integrate math libraries (Berit, Orion, Joe)
Week 5: Start implementing multi-cycle (Joe, Orion); Further work on math library (Berit)
Week 6: Finish implementing multi-cycle (Joe, Orion); More work on math library (Berit)
Week 7: Math libraries! (Joe, Orion, Berit)
Week 8: Math libraries! (Joe, Orion, Berit)

Month 3: Get pipelining working (Joe, Orion, Berit)
Month 4: Work out any bugs and hazards in the CPU (Joe, Orion, Berit)
Month 5: Optimization (Joe, Orion, Berit)
Month 6: Optimization (Joe, Orion, Berit)