

# RFVLSI Latex Template

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**Abstract**—This paper is intended to use as to speed up the learning curve of writing Latex IEEE journal papers in RFVLSI-Lab, NCTU.

**Index Terms**—energy harvesting, rectifying circuits

## I. INTRODUCTION

THIS document serves as a starting template for writing IEEE-trans. paper in NCTU, RFVLIS-Lab.

### A. First Time Usa of Latex

- 1) Download Miktex, and open package manager. Remember to synchronize package list.
- 2) Use package MANAGER TO install the following packages: **please note the different fonts in this paragraph.**
  - All IEEE transactions/bibtex packages. (the **ieeetran**, and **biblatex-ieee** package)
  - **Textcomp**: support some symbols. (the **was** package)
  - **amsmath**: support some maths.
  - **subfiles**: support independent compilable subfiles .tex structure as used in this template.
  - **dblfloatfix**: fixes double column figures ordering problems. (**dblfloatfix** package.)

### B. Useful Commands

- 1) Use: `\textbackslash`: to show \
- 2) Use: `\label{aaaa}` inside figure, table, equations, or floats: and use it later with `\ref{aaaa}`
- 3) Use: `\cite{paperXXX}` to cite the paper in the \*.bib file. For the item content of \*.bib file, please go to IEEEExplore and click download citation with BibTex format.

### C. Equation Templates

In all of the following approaches, a gate DC bias  $V_{g,bias}$  is introduced as in Eq. XXXX.

$$V_{out} = N(V_{RF,Peak} - V_{th} + V_{gs,bias}). \quad (1)$$

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TABLE I  
DEFINITION OF SENSITIVITY AND POWER CONVERSION EFFICIENCY.

Terminology	Definition
<i>Power Sensitivity</i>	The minimum input power required to achieve a specified DC output current, or voltage, or both.
<i>Voltage Sensitivity</i>	The minimum input voltage required to achieve a specified DC output current, or voltage, or both.
<i>Power Conversion Efficiency (PCE)</i>	$PCE \equiv \frac{\text{Output DC power}}{\text{Input RF power}}$

### D. Table Templates

- use `{v/t/v/t/}` to control columns and column separating rule(line). Note that the separating rule are also treated as a column.
- use `\IEEEeqnarrayrulerow`, `\IEEEeqnarrayrulerow[rule_thickness]`, `\IEEEeqnarraydblrulerow`, `\IEEEeqnarraydblrulerow[rule_thickness][spacing]`, `\IEEEeqnarraydblrulerowcut`, `\IEEEeqnarraydblrulerowcut[rule_thickness][spacing]` to control horizontal separating rules. Use `\IEEEeqnarraystrutsizetadd{4pt}{4pt}` in the last hidden column in each row to add spaces above/below each row: `\IEEEeqnarraystrutsizetadd{4pt}{4pt}`
- Use `\parbox{18ex}{}` to control width.
- Use `\raggedright`, `\raggedleft`, and to adjust left/right alignment inside each cell.

### E. Inductive Peaking Approach

### F. Other Approaches

## II. CONCLUSION

The use of IPVM can produce a larger  $v_{gs}$  than  $v_{ds}$  in a passive manner at resonant frequencies for rectifying transistors. When IPVM is used to form the IGR, the rectifier will achieve a lower forward resistance, lower reverse leakage current, and lower effective threshold. Each of these properties will improve both the sensitivity and PCE of the rectifier. This is experimentally proved in a 53GHz mmWave rectifier IC which achieves 20% at 7dBm. IGR is an effective approach to improve sensitivity and PCE in high-frequency RF-to-DC rectifier. The IGR can be implemented in a CMOS process without additional photo-mask, this allows integration of IGR into a complete wireless-powered system with high sensitive and PCE in the future.

TABLE II  
SUMMARY OF THE UHF RF-TO-DC RECTIFIER PERFORMANCE.

Specification	This work	A	B	C
Frequency(MHz)	900	950	915	915
Technology	0.28 $\mu$ m thick-gate oxide CMOS in 65nm process	0.35 $\mu$ m	90nm	0.2 $\mu$ m
PCE@Output power	27.97%@19.3mW	15.1%@0.6 $\mu$ W	11%@13.1 $\mu$ W	71.5%@0.285mW
Number of stage / type of the rectifier	5/half-wave	1 (six stacks) / full-wave	17/half-wave	1/full-wave
Chip area	0.442mm <sup>2</sup>	0.104mm <sup>2</sup>	0.19mm <sup>2</sup>	0.133mm <sup>2</sup>

TABLE III  
SUMMARY OF THE MMWAVE RF-TO-DC RECTIFIER PERFORMANCE.

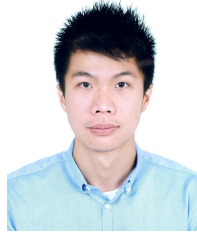
	This Work	[1]	[2]
Technology	65nm	90nm	65nm
Number of Stages	7	10	3
Operating Frequency	46-56GHz	45GHz	70-72GHz
Peak Efficiency	20.65%	0.5%	8%
Input Sensitivity	-6dBm @2 $\mu$ A, 1.2V	2dBm	5dBm

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#### REFERENCES

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- [2] H. Gao, M. Matters-Kammerer, P. Harpe, D. Milosevic, U. Johannsen, A. van Roermund, and P. Baltus, "A 71 Ghz rf energy harvesting tag with 8% efficiency for wireless temperature sensors in 65nm cmos," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE*, 2013, pp. 403–406.



**Yu-Jiu Wang (S'04 - M'09)** received the B.S. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2001, and the M.S. and Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, in 2006 and 2009, respectively. Since 2009, he joined the Department of Electronics Engineering, National Chiao Tung University, Hsin-Chu, Taiwan, where he is now an assistant professor. His current researches include high-efficiency RF rectifier and power amplifier ICs, phased-array transceivers, circuit theories and design automation. He was a research assistant with the MMIC group in National Taiwan University, where he studied Q-band and V-band compound semiconductor MMICs from 1999 to 2001. He served as a naval officer for the obligatory military service from 2001 to 2003. He was an assistant instructor for the Electronics Laboratory at NTU from 2003 to 2004. He studied wireless phased-array transceivers, broadband circuits and noise theories during his Ph.D. in Caltech from 2004-2009. Dr.Wang was the First Prize winner of the National Physics Competition and the Silver Medal winner of the 27th and 28th International Physics Olympiad, in Oslo, Norway, in 1996 and Ontario, Canada, in 1997, respectively. He also led a team to win the championship in the National Entrepreneurship Competition