RFVLSI Latex Template

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***Abstract*—This paper is intended to use as to speed up the learning curve of writing Latex IEEE journal papers in RFVLSI-Lab, NCTU.**

***Index Terms*—energy harvesting, rectifying circuits**

I. Introduction

THIS document serves as a starting template for writing IEEE-trans. paper in NCTU, RFVLIS-Lab.

A. First Time Usa of Latex

1) Download Miktex.
2) *Use package* MANAGER TO install the following packages:
   - All IEEE transactions/bibtex packages
   - **Textcomp**: support some symbols.
   - **amsmath**: support some maths.
   - **Subfiles**: support independent compilable subfiles .tex structure as used in this template.
   - **Dblfloatfix**: fixes double column figures ordering problems.

B. Specialized Semiconductor Process

1 Some forwords about why needs a rectifier?.
2 Focus on introduction of several representative topologies.
3 Bring up the the later sections.

C. Equation Templates

In all of the following approaches, a gate DC bias $V_{g,bias}$ is introduced as in Eq. XXXX.

$$V_{out} = N(V_{RF,Peak} - V_{th} + V_{gs,bias}). \quad (1)$$

D. Table Templates

E. Inductive Peaking Approach

F. Other Approaches

II. Conclusion

The use of IPVM can produce a larger v_{gs} than v_{ds} in a passive manner at resonant frequencies for rectifying transistors. When IPVM is used to form the IGR, the rectifier will achieve a lower forward resistance, lower reverse leakage current, and lower effective threshold. Each of these properties will improve both the sensitivity and PCE of the rectifier. This is experimentally proved in a 53GHz mmWave rectifier IC which achieves 20% at 7dBm. IGR is an effective approach to improve sensitivity and PCE in high-frequency RF-to-DC rectifier. The IGR can be implemented in a CMOS process without additional photo-mask, this allows integration of IGR into a complete wireless-powered system with high sensitive and PCE in the future.

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Yu-Jiu Wang (S'04 - M'09) received the B.S. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2001, and the M.S. and Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, in 2006 and 2009, respectively. Since 2009, he joined the Department of Electronics Engineering, National Chiao Tung University, Hsin-Chu, Taiwan, where he is now an assistant professor. His current researches include high-efficiency RF rectifier and power amplifier ICs, phased-array transceivers, circuit theories and design automation, He was a research assistant with the MMIC group in National Taiwan University, where he studied Q-band and V-band compound semiconductor MMICs from 1999 to 2001. He served as a naval officer for the obligatory military service from 2001 to 2003. He was an assistant instructor for the Electronics Laboratory at NTU from 2003 to 2004. He studied wireless phased-array transceivers, broadband circuits and noise theories during his Ph.D. in Caltech from 2004-2009. Dr.Wang was the First Prize winner of the National Physics Competition and the Silver Medal winner of the 27th and 28th International Physics Olympiad, in Oslo, Norway, in 1996 and Ontario, Canada, in 1997, respectively. He also led a team to win the championship in the National Entrepreneurship Competition

TABLE I
SUMMARY OF THE UHF RF-TO-DC RECTIFIER PERFORMANCE.

Specification	**This work**	**A**	**B**	**C**
Frequency(MHz)	900	950	915	915
Technology	0.28μm thick-gate oxide CMOS in 65nm process	0.35μm	90nm	0.2μm
PCE@Output power	27.97%@19.3mW	15.1%@0.6μW	11%@13.1μW	71.5%@0.285mW
Number of stage / type of the rectifier	5/half-wave	1 (six stacks) / full-wave	17/half-wave	1/full-wave
Chip area	0.442mm^2	0.104mm^2	0.19mm^2	0.133mm^2