# RFVLSI Homework Template

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***Abstract*—All RF-VLSI Design homework must be written in IEEE journal laTex format, and submitted in PDF format. This file serves as a template for you to quickly pickup important features in writing laTex based IEEE journal papers.**

***Index Terms*—energy harvesting, rectifying circuits**

## I. Introduction

THIS document serves as a starting template for writing IEEE-trans. paper in NCTU, RFVLSI-Lab.

### A. First Time Use of Latex

1) Download Miktex, and open package manager. Remember to synchronize package list.
2) *Use package* MANAGER TO install the following packages: **(Please note the different fonts in this paragraph on purpose. Please read source files for commands)**
   - All IEEE transactions/bibtex packages. (the **ieeetran**, and **biblatex-ieee** package)
   - **Textcomp**: support some symbols. (the **was** package)
   - **amsmath**: support some maths.
   - **subfiles**: support independent compilable subfiles .tex structure as used in this template.
   - **dblfloatfix**: fixes double column figures ordering problems. (**dblfloatfix** package.)

### B. Useful Commands

1) Use: **textbackslash**: to show \
2) Use: **label**{**aaaa**} inside figure, table, equations, or floats: and use it later with **ref**{**aaaa**}
3) Use: **cite**{**paperXXX**} to cite the paper in the *.bib file. For the item content of *.bib file, please go to IEEExplore and click download citation with BibTex format.

Please look for useful formats in this document, and read their source files directly.

### C. Equation Templates

In all of the following approaches, a gate DC bias $V_{g,bias}$ is introduced as in Eq. XXXX.

$$V_{out} = N(V_{RF,Peak} - V_{th} + V_{gs,bias}). \tag{1}$$

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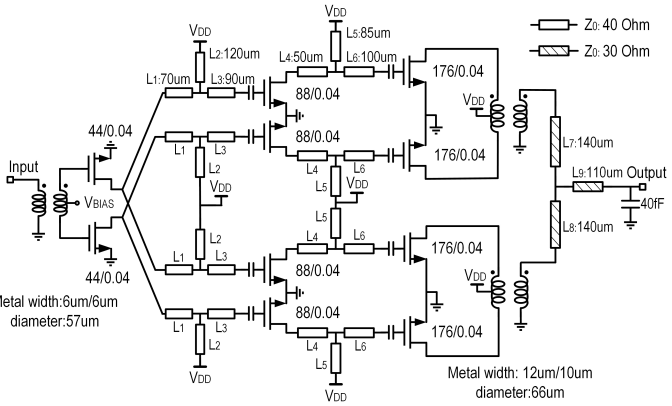


Fig. 1. The simplified schematic of the 60 GHz power amplifier.

Below is a **IEEEeqnarray** example. Note, it is a 2 by 2 array for alignment.

$$\begin{aligned} V_G &= A_v \cdot V_{in} - (V_{th} - V_{ITC,bias}) \\ &= A_v \cdot \left( V_{in} - \frac{V_{th} - V_{ITC,bias}}{A_v} \right). \end{aligned} \tag{2}$$

### D. Table Templates

- use {v/t/v/t/} to control columns and column separating rule(line). Note that the separating rule are also treated as a column.
- use **IEEEeqnarrayrulerow,** **IEEEeqnarrayrulerow[rule_thickness]**, **IEEEeqnarraydblrulerow** , **IEEEeqnarraydblrulerow[rule_thickness][spacing]**, **IEEEeqnarraydblrulerowcut,** **IEEEeqnarraydblrulerowcut[rule_thickness][spacing]** to control horizontal separating rules. Use \IEEEeqnarraystrutsizeadd{4pt}{4pt} in the last hidden column in each row to add spaces above/below each row: **IEEEeqnarraystrutsizeadd**{**4pt**}{**4pt**}
- Use **parbox**{**18ex**}{} to control width.
- Use **raggedright**, **raggedleft**, and to adjust left/right alignment inside each cell.

### E. Put your own subsections.

*1) Put your own subsubsections1.:*
*2) Put your own subsubsections2.:*

### F. Online Resources.

There are many on-line resources for IEEE journal laTex format. Please read: **"How to Use the IEEEtran LATEX Class"** by Michael Shell. Please read: **"How to Use the IEEEtran BibTex"** also by Michael Shell.

TABLE I
DEFINITION OF SENSITIVITY AND POWER CONVERSION EFFICIENCY.

| Terminology | Definition |
|---|---|
| *Power Sensitivity* | The minimum input power required to achieve a specified DC output current, or voltage, or both. |
| *Voltage Sensitivity* | The minimum input voltage required to achieve a specified DC output current, or voltage, or both. |
| *Power Conversion Efficiency (PCE)* | $PCE \equiv \frac{\text{Output DC power}}{\text{Input RF power}}$ |

## II. CONCLUSION

## APPENDIX A
## PROOF OF EQ.XXX

If there is a mismatch between the two reference MOSTFETs, the $\Delta G_m$ would be derived in this section. Based on the error models shown in Section **??**. As shown in Fig.**??**, the operating points will be locked by the feedback loop, while the difference of output currents is **XXXX** and the difference of input voltages is **xxxx**.

The current equations of different operating points are **don't assume square-law!!!**

$$I_2 = k^x/2(W/L)(V_2^x - V_t)^2 \tag{A.1}$$

As a result,

$$XXXXXXXXXXXXXXXXXXXXXXXXX \tag{A.2}$$

Define the transconductance which is referred to $M_2$ as

$$XXXXXXXXXXX \tag{A.3}$$

Eq.XXX can be expressed as Assuming XXXXX, we have

$$yyyy. \tag{A.4}$$

Since

(A.5)

$G_{m2}^x$ is obtained as

$$zzzzzzz. \tag{A.6}$$

## APPENDIX B
## RELATIONSHIPS BETWEEN SMALL-SIGNAL $g_m$ AND $1/R$

Taylor's expansion of $I_{out}$ at $V_0$ is:

$$I_{out}(V_0 + v) = I_0 + \sum_{i=1}^{\infty} a_i \cdot v^i \tag{B.1}$$

, with $a_i$ being the $i$-th coefficient of the expansion. Subtracting $I_{out}(V_0)$ from $I_{out}(V_0 + \Delta V)$, and dividing it by $\Delta V$ will result in:

$$\frac{\Delta I}{\Delta V} = \sum_{i=1}^{\infty} a_i \cdot \Delta V^{i-1} \equiv \frac{1}{R} \tag{B.2}$$

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## REFERENCES

[1] S. Pellerano, J. Alvarado, and Y. Palaskas, "A mm-wave power-harvesting rfid tag in 90 nm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 8, pp. 1627–1637, 2010.

[2] H. Gao, M. Matters-Kammerer, P. Harpe, D. Milosevic, U. Johannsen, A. van Roermund, and P. Baltus, "A 71 Ghz rf energy harvesting tag with 8% efficiency for wireless temperature sensors in 65nm cmos," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE*, 2013, pp. 403–406.

**Yu-Jiu Wang (S'04 - M'09)** received the B.S. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2001, and the M.S. and Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, in 2006 and 2009, respectively. Since 2009, he joined the Department of Electronics Engineering, National Chiao Tung University, Hsin-Chu, Taiwan, where he is now an assistant professor. His current researches include high-efficiency RF rectifier and power amplifier ICs, phased-array transceivers, circuit theories and design automation, He was a research assistant with the MMIC group in National Taiwan University, where he studied Q-band and V-band compound semiconductor MMICs from 1999 to 2001. He served as a naval officer for the obligatory military service from 2001 to 2003. He was an assistant instructor for the Electronics Laboratory at NTU from 2003 to 2004. He studied wireless phased-array transceivers, broadband circuits and noise theories during his Ph.D. in Caltech from 2004-2009. Dr.Wang was the First Prize winner of the National Physics Competition and the Silver Medal winner of the 27th and 28th International Physics Olympiad, in Oslo, Norway, in 1996 and Ontario, Canada, in 1997, respectively. He also led a team to win the championship in the National Entrepreneurship Competition

TABLE II
SUMMARY OF THE UHF RF-TO-DC RECTIFIER PERFORMANCE.

| **Specification** | **This work** | **A** | **B** | **C** |
|---|---|---|---|---|
| Frequency(MHz) | 900 | 950 | 915 | 915 |
| Technology | 0.28$\mu$m thick-gate oxide CMOS in 65nm process | 0.35$\mu$m | 90nm | 0.2$\mu$m |
| PCE@Output power | 27.97%@19.3mW | 15.1%@0.6$\mu$W | 11%@13.1$\mu$W | 71.5%@0.285mW |
| Number of stage / type of the rectifier | 5/half-wave | 1 (six stacks) / full-wave | 17/half-wave | 1/full-wave |
| Chip area | 0.442mm$^2$ | 0.104mm$^2$ | 0.19mm$^2$ | 0.133mm$^2$ |

TABLE III
SUMMARY OF THE MMWAVE RF-TO-DC RECTIFIER PERFORMANCE.

| | **This Work** | [1] | [2] |
|---|---|---|---|
| Technology | 65nm | 90nm | 65nm |
| Number of Stages | 7 | 10 | 3 |
| Operating Frequency | 46-56GHz | 45GHz | 70-72GHz |
| Peak Efficiency | 20.65% | 0.5% | 8% |
| Input Sensitivity | -6dBm @2$\mu$A, 1.2V | 2dBm | 5dBm |