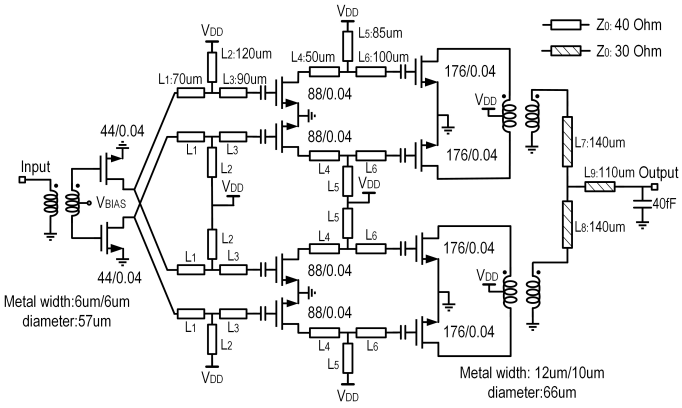

Fig. 1. The simplified schematic of the 60 GHz power amplifier.

I. Introduction

THIS document serves as a starting template for writing IEEE-trans. paper in NCTU, RFVLSI-Lab.

A. First Time Use of Latex

1) Download Miktex, and open package manager. Remember to synchronize package list.
2) *Use package* MANAGER TO install the following packages: **(Please note the different fonts in this paragraph on purpose. Please read source files for commands)**
   - All IEEE transactions/bibtex packages. (the **ieeetran**, and **biblatex-ieee** package)
   - **Textcomp**: support some symbols. (the **was** package)
   - **amsmath**: support some maths.
   - **subfiles**: support independent compilable subfiles .tex structure as used in this template.
   - **dblfloatfix**: fixes double column figures ordering problems. (**dblfloatfix** package.)

B. Useful Commands

1) Use: **textbackslash**: to show \
2) Use: **label**{**aaaa**} inside figure, table, equations, or floats: and use it later with **ref**{**aaaa**}
3) Use: **cite**{**paperXXX**} to cite the paper in the *.bib file. For the item content of *.bib file, please go to IEEEexplore and click download citation with BibTex format.

Please look for useful formats in this document, and read their source files directly.

C. Equation Templates

In all of the following approaches, a gate DC bias $V_{g,bias}$ is introduced as in Eq. XXXX.

$$V_{out} = N(V_{RF,Peak} - V_{th} + V_{gs,bias}). \tag{1}$$

TABLE I
Definition of Sensitivity and Power Conversion Efficiency.

Terminology	Definition
Power Sensitivity	The minimum input power required to achieve a specified DC output current, or voltage, or both.
Voltage Sensitivity	The minimum input voltage required to achieve a specified DC output current, or voltage, or both.
Power Conversion Efficiency (PCE)	$PCE \equiv \frac{\text{Output DC power}}{\text{Input RF power}}$

Below is a **IEEEeqnarray** example. Note, it is a 2 by 2 array for alignment.

$$\begin{aligned} V_G &= A_v \cdot V_{in} - (V_{th} - V_{ITC,bias}) \\ &= A_v \cdot \left(V_{in} - \frac{V_{th} - V_{ITC,bias}}{A_v} \right). \end{aligned} \tag{2}$$

D. Table Templates

- use {v/t/v/t/} to control columns and column separating rule(line). Note that the separating rule are also treated as a column.
- use
  IEEEeqnarrayrulerow,
  IEEEeqnarrayrulerow[rule_thickness],
  IEEEeqnarraydblrulerow,
  IEEEeqnarraydblrulerow[rule_thickness][spacing],
  IEEEeqnarraydblrulerowcut,
  IEEEeqnarraydblrulerowcut[rule_thickness][spacing]
  to control horizontal separating rules. Use \IEEEeqnarraystrutsizeadd{4pt}{4pt} in the last hidden column in each row to add spaces above/below each row: **IEEEeqnarraystrutsizeadd**{**4pt**}{**4pt**}
- Use **parbox**{**18ex**}{} to control width.
- Use **raggedright**, **raggedleft**, and to adjust left/right alignment inside each cell.

E. Put your own subsections.

1) Put your own subsubsections1.:
2) Put your own subsubsections2.:

F. Online Resources.

There are many on-line resources for IEEE journal laTex format. Please read: **"How to Use the IEEEtran LATEX Class"** by Michael Shell. Please read: **"How to Use the IEEEtran BibTex"** also by Michael Shell. Please also look for laTex wikiBook for useful tutorials.

TABLE II
SUMMARY OF THE UHF RF-TO-DC RECTIFIER PERFORMANCE.

Specification	**This work**	**A**	**B**	**C**
Frequency(MHz)	900	950	915	915
Technology	0.28μm thick-gate oxide CMOS in 65nm process	0.35μm	90nm	0.2μm
PCE@Output power	27.97%@19.3mW	15.1%@0.6μW	11%@13.1μW	71.5%@0.285mW
Number of stage / type of the rectifier	5/half-wave	1 (six stacks) / full-wave	17/half-wave	1/full-wave
Chip area	0.442mm^2	0.104mm^2	0.19mm^2	0.133mm^2

TABLE III
SUMMARY OF THE MMWAVE RF-TO-DC RECTIFIER PERFORMANCE.

	This Work	[**?**]	[**?**]
Technology	65nm	90nm	65nm
Number of Stages	7	10	3
Operating Frequency	46-56GHz	45GHz	70-72GHz
Peak Efficiency	20.65%	0.5%	8%
Input Sensitivity	-6dBm @2μA, 1.2V	2dBm	5dBm