# I. INTRODUCTION

THIS document serves as a starting template for writing IEEE-trans. paper in NCTU, RFVLIS-Lab.

### A. First Time Usa of Latex

- 1) Download Miktex, and open package manager. Remember to synchronize package list.
- 2) Use package MANAGER TO install the following packages: please note the different fonts in this paragraph.)
  - All IEEE transactions/bibtex packages. (the ieee-tran, and biblatex-ieee package)
  - Textcomp: support some symbols. (the was package)
  - amsmath: support some maths.
  - **subfiles**: support independent compilable subfiles .tex structure as used in this template.
  - dblfloatfix: fixes double column figures ordering problems. (dblfloatfix package.)

#### B. Useful Commands

- 1) Use: \textbackslash: to show \
- 2) Use: \label{aaaa} inside figure, table, equations, or floats: and use it later with \ref{aaaa}
- 3) Use: \cite{paperXXX} to cite the paper in the \*.bib file. For the item content of \*.bib file, please go to IEEEexplore and click download citation with BibTex format.

# C. Equation Templates

In all of the following approaches, a gate DC bias  $V_{g,bias}$  is introduced as in Eq. XXXX.

$$V_{out} = N(V_{RF,Peak} - V_{th} + V_{gs,bias}). \tag{1}$$

Below is a **IEEEeqnarray** example. Note, it is a 2 by 2 array for alignment.

$$V_G = A_v \cdot V_{in} - (V_{th} - V_{ITC,bias})$$

$$= A_v \cdot \left(V_{in} - \frac{V_{th} - V_{ITC,bias}}{A_v}\right). \tag{2}$$

#### D. Table Templates

- use {v/t/v/t/} to control columns and column separating rule(line). Note that the separating rule are also treated as a column.
- use

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to control horizontal separating rules. Use \IEEEeqnarraystrutsizeadd{4pt}{4pt} in the last

TABLE I
DEFINITION OF SENSITIVITY AND POWER CONVERSION EFFICIENCY.

1

Terminology	Definition		
Power Sensitivity	The minimum input power required to achieve a specified DC output current, or voltage, or both.		
Voltage Sensitivity	The minimum input voltage required to achieve a specified DC output current, or voltage, or both.		
Power Conversion Efficiency (PCE)	$PCE \equiv rac{ ext{Output DC power}}{ ext{Input RF power}}$		

hidden column in each row to add spaces above/below each row: \IEEEeqnarraystrutsizeadd{4pt}{4pt}

- Use \parbox{18ex}{}} to control width.
- Use \raggedright, \raggedleft, and to adjust left/right alignment inside each cell.

# E. Put your own subsections.

- 1) Put your own subsubsections1.:
- 2) Put your own subsubsections2.:

 $\label{table ii} \textbf{Summary of the UHF RF-to-DC rectifier performance}.$ 

Specification	This work	A	В	C
Frequency(MHz)	900	950	915	915
Technology	0.28µm thick-gate oxide CMOS in 65nm process	$0.35 \mu \mathrm{m}$	90nm	$0.2 \mu \mathrm{m}$
PCE@Output power	27.97%@19.3mW	15.1%@0.6μW	11%@13.1μW	71.5%@0.285mW
Number of stage / type of the rectifier	5/half-wave	1 (six stacks) / full-wave	17/half-wave	1/full-wave
Chip area	$0.442 \text{mm}^2$	$0.104 \text{mm}^2$	$0.19 {\rm mm}^2$	$0.133 \text{mm}^2$

 $\label{table III} \mbox{Summary of the mmWave RF-to-DC rectifier performance}.$ 

	This Work	[?]	[?]
Technology	65nm	90nm	65nm
Number of Stages	7	10	3
Operating Frequency	46-56GHz	45GHz	70-72GHz
Peak Efficiency	20.65%	0.5%	8%
Input Sensitivity	-6dBm @2μA, 1.2V	2dBm	5dBm