I. Introduction

THIS document serves as a starting template for writing IEEE-trans. paper in NCTU, RFVLIS-Lab.

A. First Time Usa of Latex

1) Download Miktex.
2) *Use package* MANAGER TO install the following packages:
   - All IEEE transactions/bibtex packages
   - **Textcomp**: support some symbols.
   - **amsmath**: support some maths.
   - **Subfiles**: support independent compilable subfiles .tex structure as used in this template.
   - **Dblfloatfix**: fixes double column figures ordering problems.

B. Specialized Semiconductor Process

1 Some forwords about why needs a rectifier?.
2 Focus on introduction of several representative topologies.
3 Bring up the the later sections.

C. Equation Templates

In all of the following approaches, a gate DC bias $V_{g,bias}$ is introduced as in Eq. XXXX.

$$V_{out} = N(V_{RF,Peak} - V_{th} + V_{gs,bias}). \tag{1}$$

D. Table Templates

- use {v/t/v/t/} to control columns and column separating rule(line). Note that the separating rule are also treated as a column.
- use **\IEEEeqnarrayrulerow,** **\IEEEeqnarrayrulerow[rule_thickness]**, **\IEEEeqnarraydblrulerow** , **\IEEEeqnarraydblrulerow[rule_thickness][spacing]**, **\IEEEeqnarraydblrulerowcut,** **\IEEEeqnarraydblrulerowcut[rule_thickness][spacing]** to control horizontal separating rules. Use \IEEEeqnarraystrutsizeadd{4pt}{4pt} in the last hidden column in each row to add spaces above/below each row: **\IEEEeqnarraystrutsizeadd{4pt}{4pt}**
- Use **\parbox{18ex}{}** to control width.
- Use **\raggedright**, and **\raggedleft** to adjust left/right alignment inside each cell.

TABLE I
DEFINITION OF SENSITIVITY AND POWER CONVERSION EFFICIENCY.

Terminology	Definition
Power Sensitivity	The minimum input power required to achieve a specified DC output current, or voltage, or both.
Voltage Sensitivity	The minimum input voltage required to achieve a specified DC output current, or voltage, or both.
Power Conversion Efficiency (PCE)	$PCE \equiv \frac{\text{Output DC power}}{\text{Input RF power}}$

E. Inductive Peaking Approach

F. Other Approaches

TABLE II
SUMMARY OF THE UHF RF-TO-DC RECTIFIER PERFORMANCE.

Specification	**This work**	**A**	**B**	**C**
Frequency(MHz)	900	950	915	915
Technology	0.28μm thick-gate oxide CMOS in 65nm process	0.35μm	90nm	0.2μm
PCE@Output power	27.97%@19.3mW	15.1%@0.6μW	11%@13.1μW	71.5%@0.285mW
Number of stage / type of the rectifier	5/half-wave	1 (six stacks) / full-wave	17/half-wave	1/full-wave
Chip area	0.442mm^2	0.104mm^2	0.19mm^2	0.133mm^2