TSMC 65nm PDK

Application Note

Statistical Simulation

TSMC North America

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NOTICE

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Introduction

In order to understand the circuit performance variation on TSMC's 65nm process, designer can take advantage of statistical models and statistical utilities in TSMC 65nm PDK to perform a series of statistical simulations and to understand the statistical distribution of interested performance parameters. This is introductory document familiarizes the circuit designer with the TSMC 65nm PDK environment for running statistical simulations.
If you run a statistical simulation on top of TSMC's 65nm statistical SPICE models, you can find out how the performance distribution in circuit relates to chip specification and ultimately, how it relates to chip design and manufacturing costs:

- What the percentage of devices meet the specification?
- How much of the over-design and timing/power/noise margins should be maintained to ensure a satisfactory percentage of qualified final products?

Monte Carlo analysis is a traditional method for simulating the effects of variations in device characteristics on circuit performance. The variations in device characteristics are represented as distributions in the TSMC SPICE model parameters. For each run of Monte Carlo analysis, random values are assigned to these TSMC SPICE model parameters and a complete simulation is executed. A series of Monte Carlo simulations produce measurement results in a distribution, which can be characterized as statistical terms such as mean value and standard deviation. With increasing number of Monte Carlo simulation runs, the shape of the distribution gets smoother and better defined as the statistical parameters (e.g. mean, variance) converge to their final values.

Mismatch Macro Model

TSMC implements 65nm mismatch function with four seed random variables: parn1, parn2, parp1 and parp2. (see Figure.1) Each random seed represents a normalized Gaussian distribution and is embedded into SPICE model parameters when "mismatchflag" is set to "1" in the model. If "mismatchflag" is set to "0", the SPICE model won't have variation. By default, all of the SPICE models with "mismatchflag" parameter are turned off don't have variation except for the macro models "nch_*mac" and "pch_*mac" (* is a wild card), in which mismatch flag is turn ON.
To run statistical simulation on standard Vt core transistors, designer simply changes normal MOSFET transistors from (nch, pch) to (nch_mac, pch_mac) in the SPICE

netlist and then includes necessary corner library models in the simulation deck file. For the HSPICE/Eldo Circuit Simulator, the corner library models are the same as the regular ones such as FF, TT, and SS.

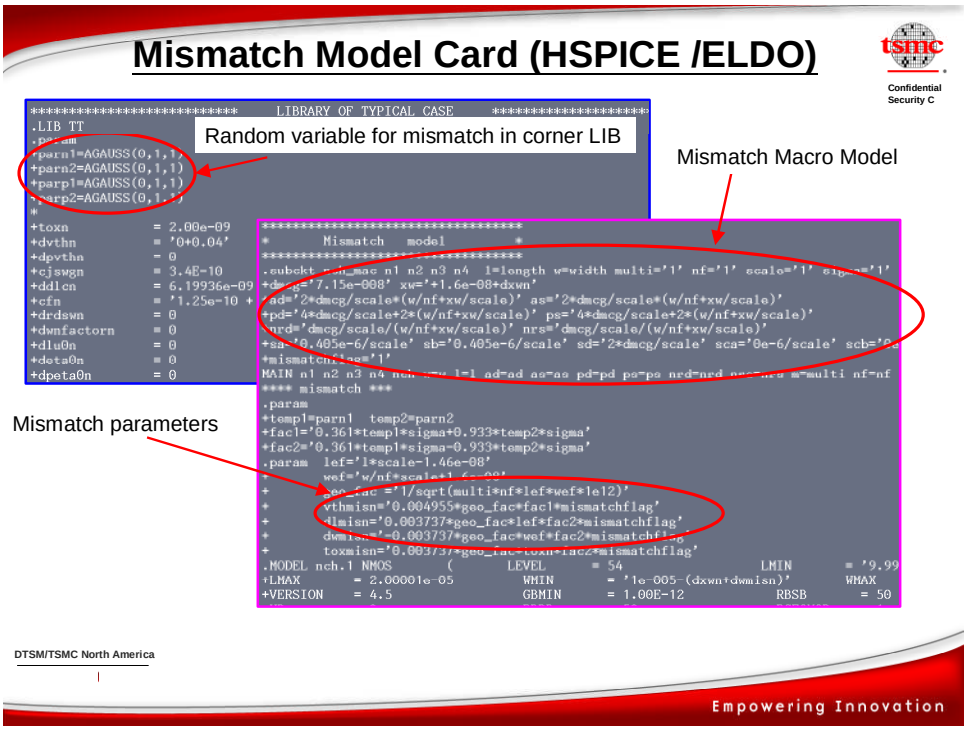
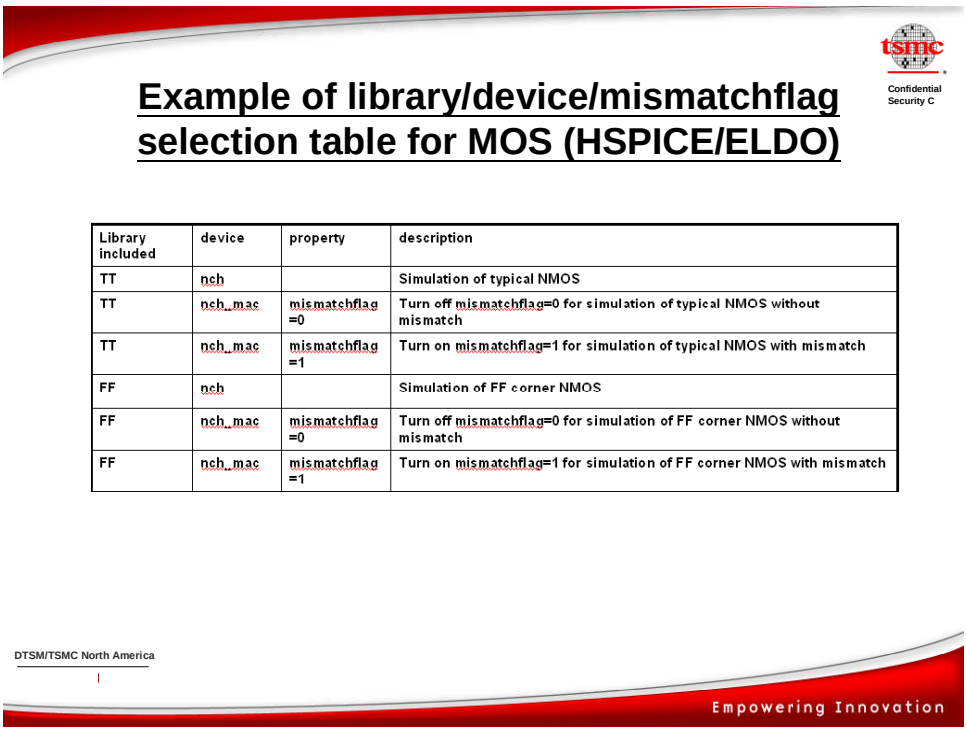


Figure.1 TSMC 65nm "nch_mac" HSPICE/ELDO mismatch model



Library included	device	property	description
TT	nch		Simulation of typical NMOS
TT	nch_mac	mismatchflag =0	Turn off mismatchflag=0 for simulation of typical NMOS without mismatch
TT	nch_mac	mismatchflag =1	Turn on mismatchflag=1 for simulation of typical NMOS with mismatch
FF	nch		Simulation of FF corner NMOS
FF	nch_mac	mismatchflag =0	Turn off mismatchflag=0 for simulation of FF corner NMOS without mismatch
FF	nch_mac	mismatchflag =1	Turn on mismatchflag=1 for simulation of FF corner NMOS with mismatch

Table.1 TSMC HSPICE/Eldo Mismatch MOS device name and model library

For Spectre Simulator, designer must include one additional library “stat_mis” in simulation deck file to introduce mismatch variation.

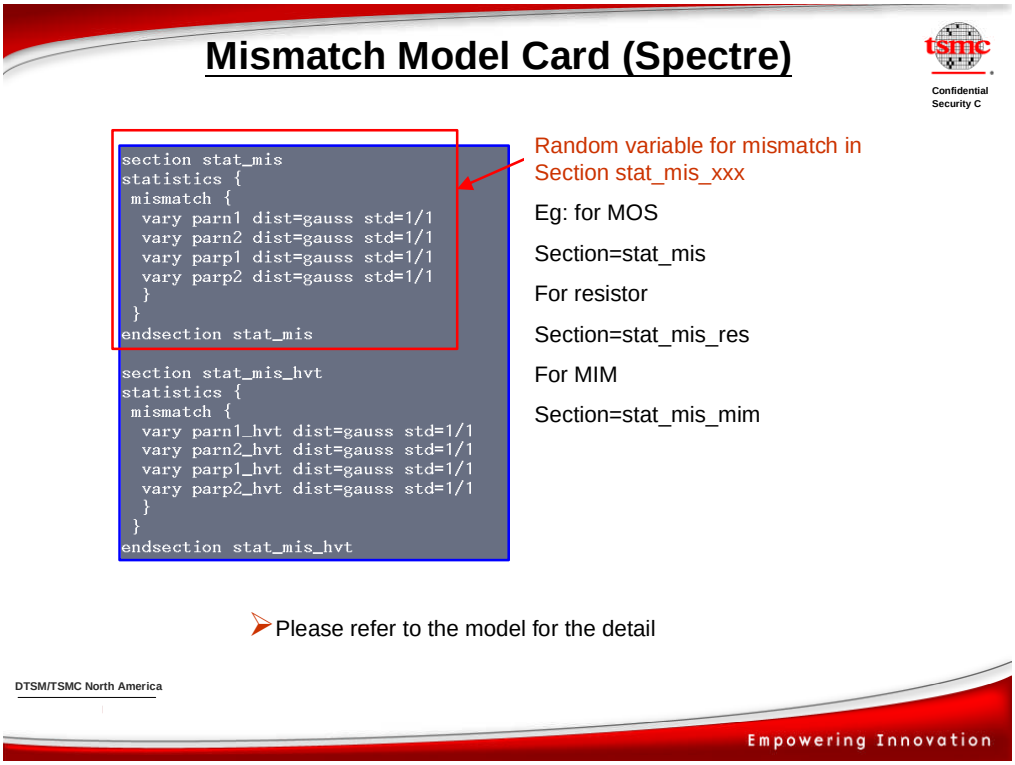
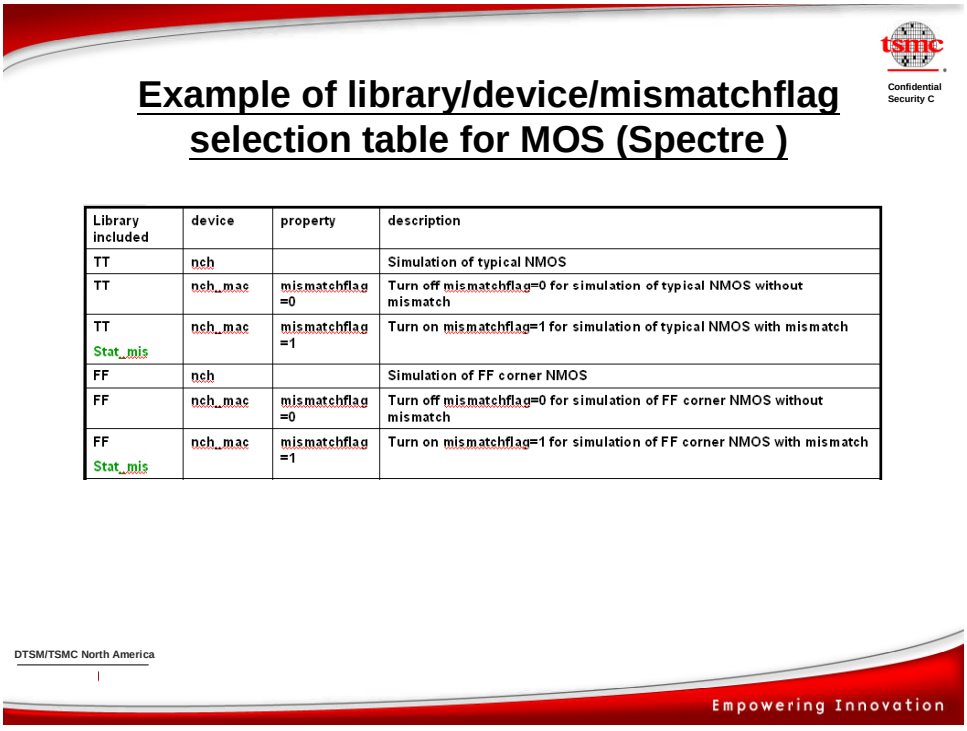


Figure.2 TSMC 65nm “nch_mac” Spectre mismatch model



Library included	device	property	description
TT	nch		Simulation of typical NMOS
TT	nch_mac	mismatchflag =0	Turn off mismatchflag=0 for simulation of typical NMOS without mismatch
TT Stat_mis	nch_mac	mismatchflag =1	Turn on mismatchflag=1 for simulation of typical NMOS with mismatch
FF	nch		Simulation of FF corner NMOS
FF	nch_mac	mismatchflag =0	Turn off mismatchflag=0 for simulation of FF corner NMOS without mismatch
FF Stat_mis	nch_mac	mismatchflag =1	Turn on mismatchflag=1 for simulation of FF corner NMOS with mismatch

Table.2 TSMC HSPICE/Eldo Mismatch MOS device name and model library

RF Mismatch Model

All of the 65nm RF SPICE models have “mismatchflag” parameter. The TSMC 65nm RF models are listed in Table.3.

Device name	Model Library Corners				
1.2V standard Vt MOS	TT_RFMOS	FF_RFMOS	SS_RFMOS	SF_RFMOS	FS_RFMOS
1.2V high Vt MOS	TT_RFMOS_hvt	FF_RFMOS_hvt	SS_RFMOS_hvt	SF_RFMOS_hvt	FS_RFMOS_hvt
1.2V low Vt MOS	TT_RFMOS_lvt	FF_RFMOS_lvt	SS_RFMOS_lvt	SF_RFMOS_lvt	FS_RFMOS_lvt
2.5V MOS	TT_RFMOS_25	FF_RFMOS_25	SS_RFMOS_25	SF_RFMOS_25	FS_RFMOS_25
1.8V MOS (2.5V under-drive)	TT_RFMOS_18	FF_RFMOS_18	SS_RFMOS_18	SF_RFMOS_18	FS_RFMOS_18
3.3V MOS (2.5V over-drive)	TT_RFMOS_33	FF_RFMOS_33	SS_RFMOS_33	SF_RFMOS_33	FS_RFMOS_33
MIM capacitor	TT_RFMIM	FF_RFMIM	SS_RFMIM	N/A	N/A
Inductor	TT_RFIND	FF_RFIND	SS_RFIND	N/A	N/A
1.2V standard Vt MOS Varactor	TT_RFMVAR	FF_RFMVAR	SS_RFMVAR	N/A	N/A
1.2V high Vt MOS Varactor	TT_RFMVAR_HVT	FF_RFMVAR_HVT	SS_RFMVAR_HVT	N/A	N/A
2.5V MOS Varactor	TT_RFMVAR_25	FF_RFMVAR_25	SS_RFMVAR_25	N/A	N/A
P+/NW Junction Varactor	TT_RFJVAR	FF_RFJVAR	SS_RFJVAR	N/A	N/A
Salicide POLY resistor	TT_RFRES_SA	FF_RFRES_SA	SS_RFRES_SA	N/A	N/A
non-Salicide POLY resistor	TT_RFRES_RPO	FF_RFRES_RPO	SS_RFRES_RPO	N/A	N/A
MOM capacitor	TT_RFRTMOM	FF_RFRTMOM	SS_RFRTMOM	N/A	N/A

Table 3: All 65nm RF device models have “mismatchflag” parameter

In addition to RF models, some baseband models have mismatch flags, too. They are listed below:
Resistors: rnod*, rpod*, rnpoly*, rppoly*
Varactors: moscap*
MiM Capacitors: mincap*
MoM Capacitor: crtmon

Statistical Simulation Example #1: Pre-Layout Mismatch (local variation) Sim

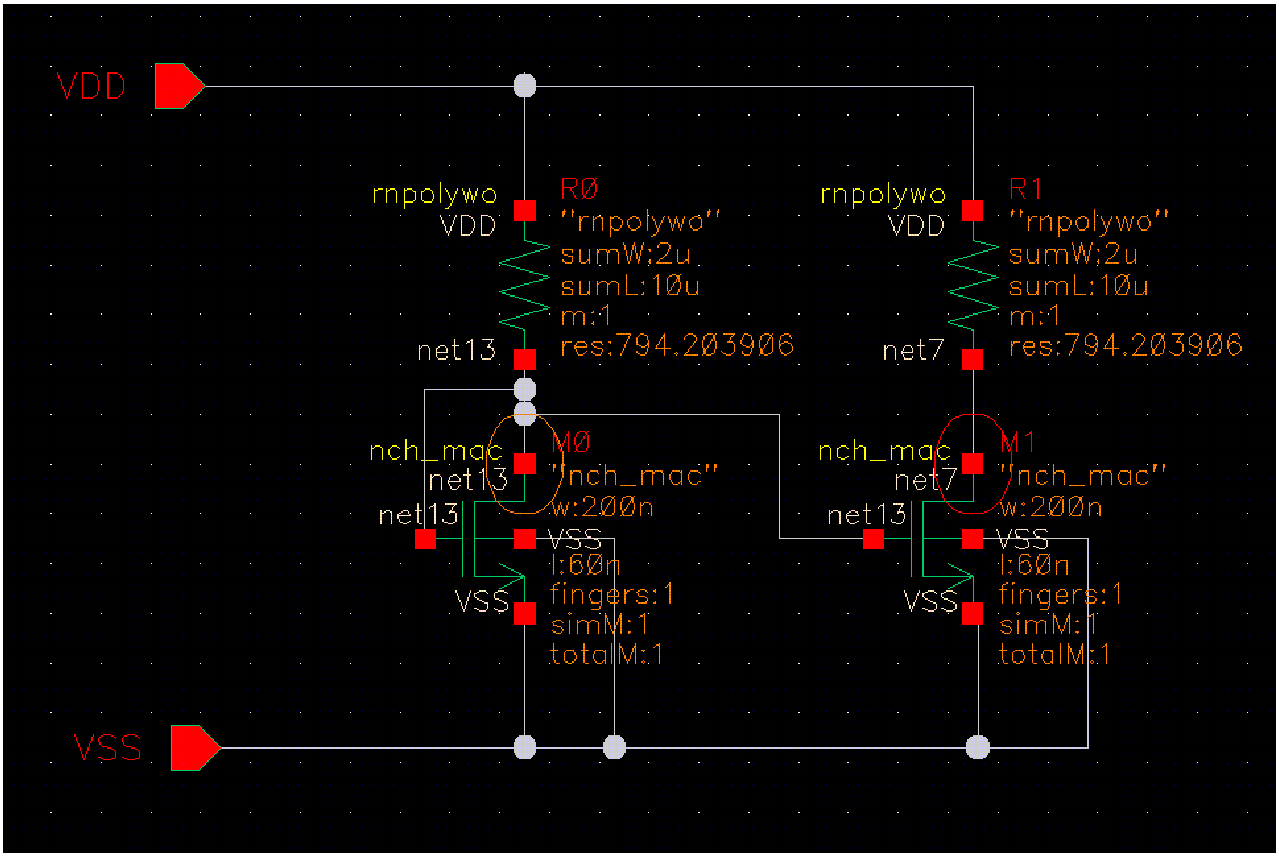


Figure. 3 A 65nm sample current mirror circuit with mismatch macro model "nch_mac"

This is a Spectre example to demonstrate the Monte Carlo runs for current mismatch between two branches of current mirror. In this simulation setup of typical PVT (TT, 1.2V, 25C) corner, the currents flowing through M0 drain node and M1 drain node are probed in each Monte Carlo run and then plotted in a histogram. The difference of two currents is also plotted in a separate histogram.

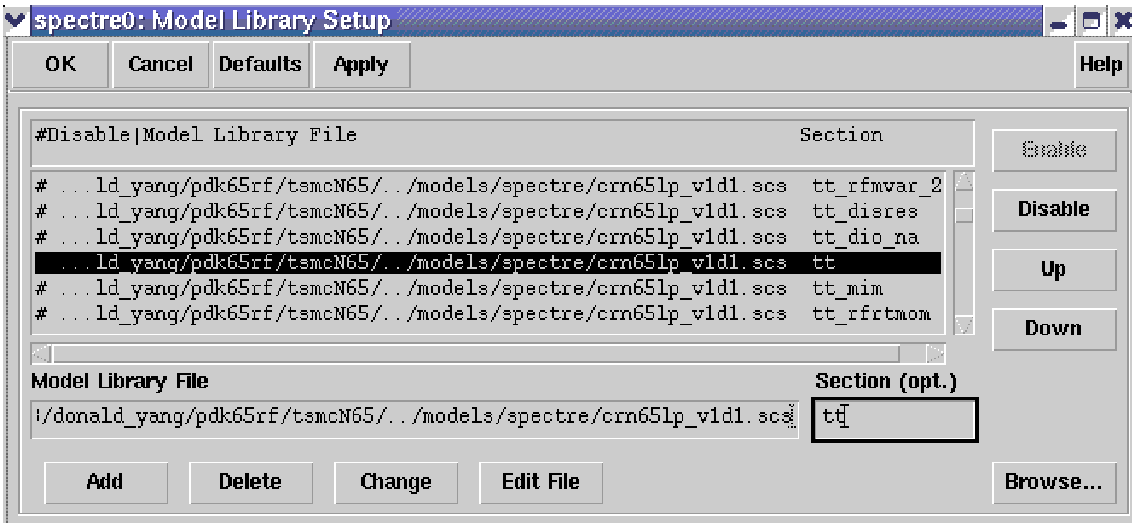


Figure. 4 Enable "TT" in Virtuoso ADE's Spectre "Model Library Setup" Window

To setup the "Typical Corner" simulation condition, enable "TT" section in "Model Library Setup" window. Setup the temperature to be 25C and VDD to be 1.2 volt. To add statistical seeds in simulation, add "stat_mis" section in "Model Library Setup".

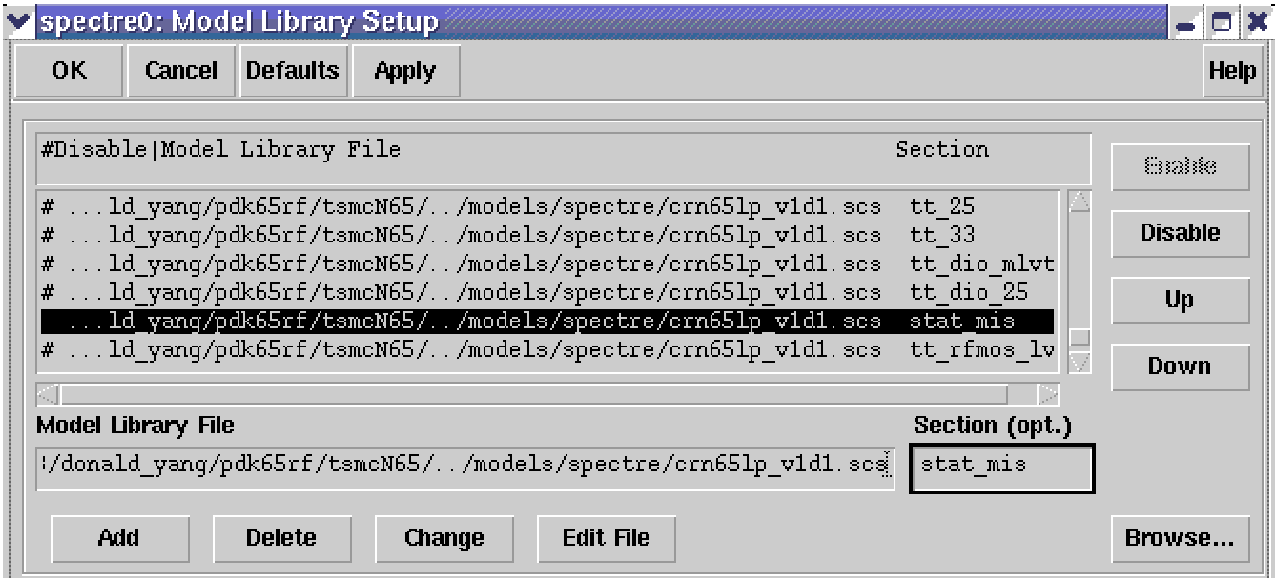


Figure. 5 Add "stat_mis" section in "Model Library Setup"

To add statistical seeds in simulation, add "stat_mis" section in "Model Library Setup". Pop up "Monte Carlo" window in "Tools" menu item as shown in Figure.6. If you only want to run intra-die local mismatch simulation **(this is nothing to do with inter-die chip-to-chip global manufacturing variation)** on typical manufacturing corner, select "Mismatch Only" in the Monte Carlo window as shown in Firgure.7.

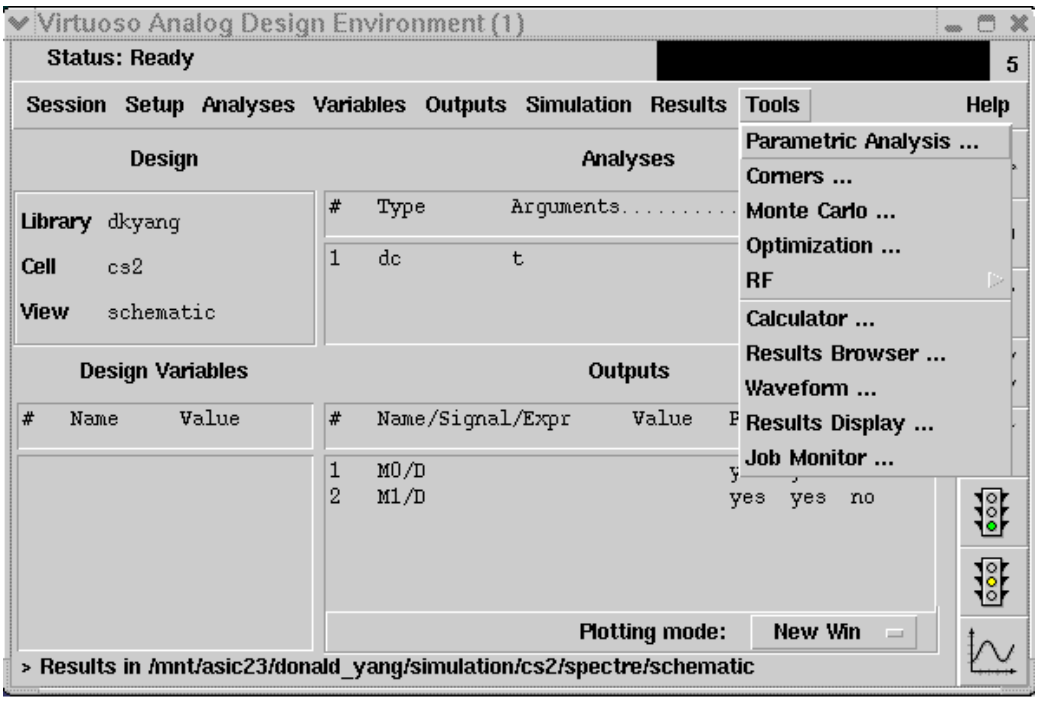


Figure. 6 In Virtuoso ADE environments, choose "Tools" and select "Monte Carlo"

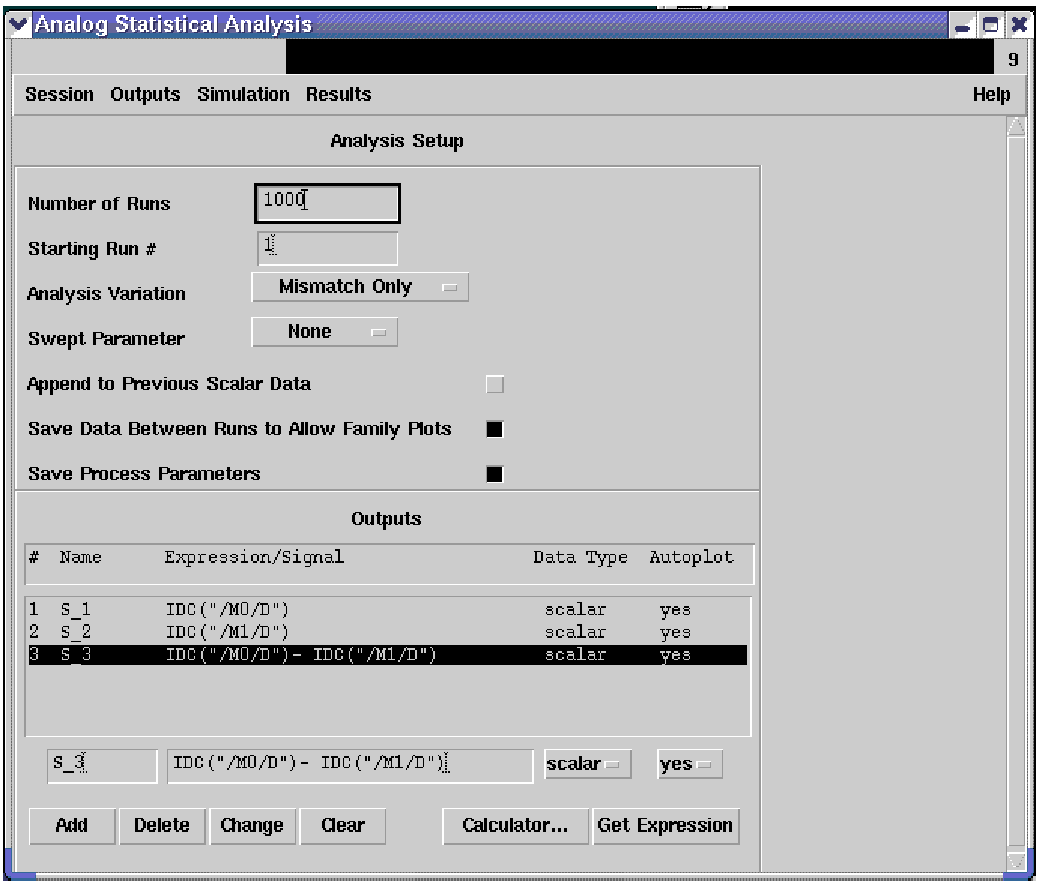


Figure. 7 Setup "Mismatch Only" in Analysis Variation and specify current outputs

After everything is setup ready, start the 1000-sample mismatch simulation running and you should be able to see the result window popping up after the job completion. The result shows that the left branch of the current mirror has 90.59uA Mean DC current with 5.213 uA standard deviation. The right branch of the current mirror has 89.41uA Mean DC current with 6.361uA standard deviation. The rightmost graph shows the difference between the two branches: most of the differences are less than +/-20uA.

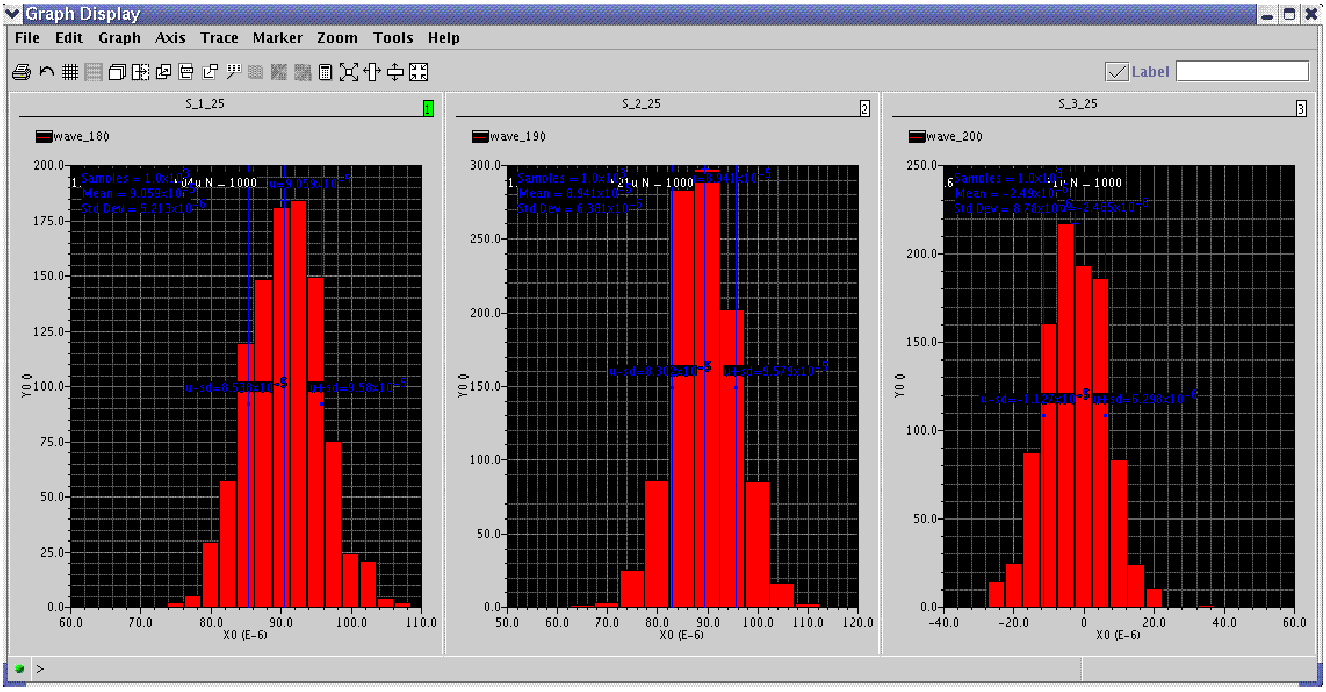


Figure. 8 Mismatch current mirror Monte Carlo Simulation Result

Statistical Simulation Example #2: Process (Global) Variation

To setup this inter-die process variation simulation, you can use regular transistor models instead of macro mismatch models. Figure.9 shows the sample current mirror schematics.

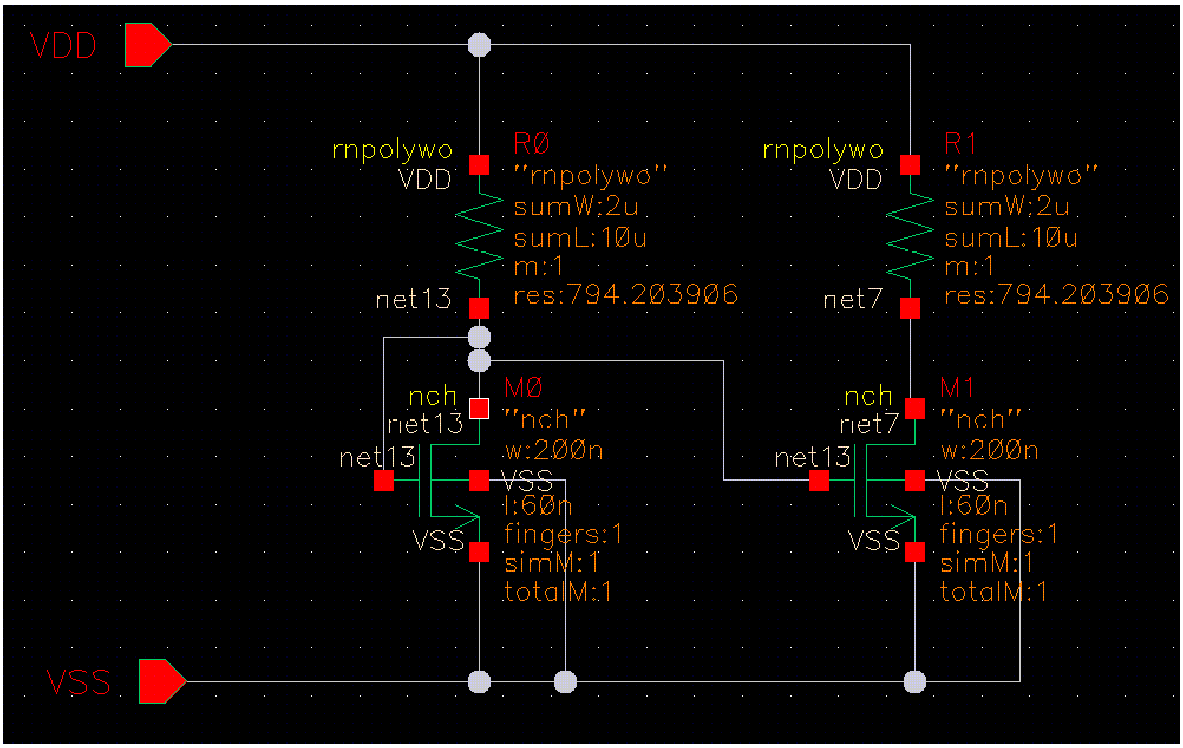


Figure. 9 A 65nm sample current mirror circuit for process variation

Include “mc” and “stat” corner libraries in the SPICE model card as shown in Figure.10. Don’t include “TT’ or any other process corner. In the Spectre “Monte Carlo” window, setup the Process Variation to be “Process Only” as shown in Figure.11. In this example, 1000 Monte Carlo runs are performed to get a mirror current distribution based on process variation. The result is shown in Figure.12. In this global variation result, both current mirror branches show exactly the same distribution because mismatch effect is not included in this simulation, and because the two circuits are exactly matched with the same size of transistors.

The Mean of 1000 samples is 91.88uA and the standard deviation is 7.8uA, which is larger than the 5.21uA standard deviation from the Example #1 local variation simulation.

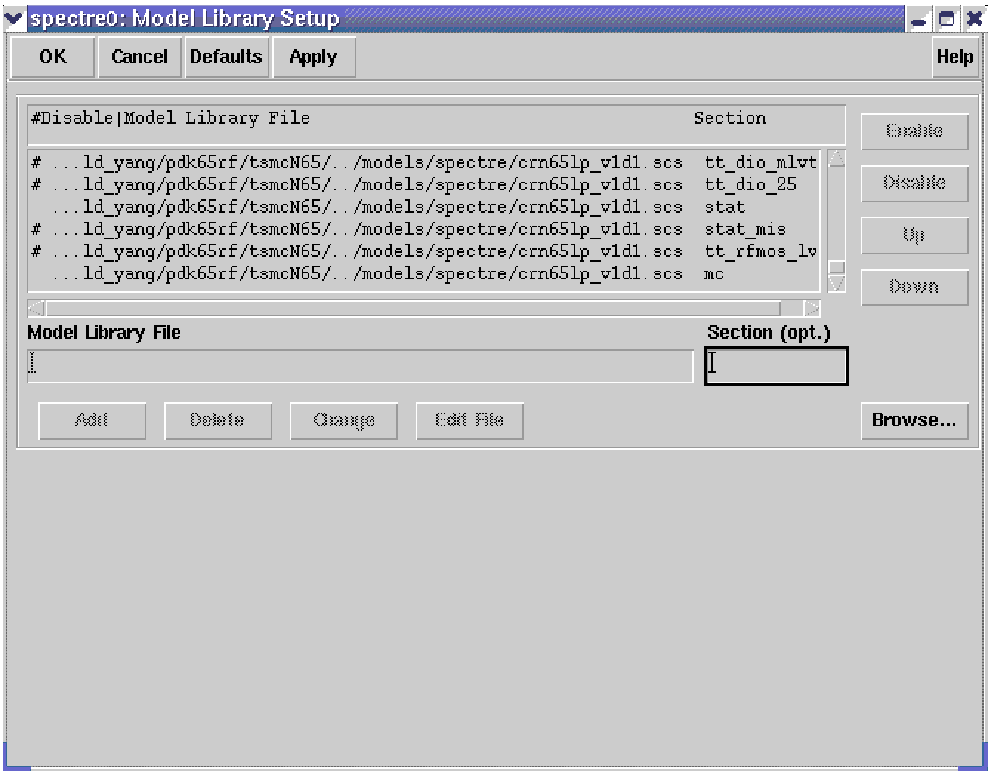


Figure. 10 Enable “mc” and “stat” section in the “Model Library Setup” window

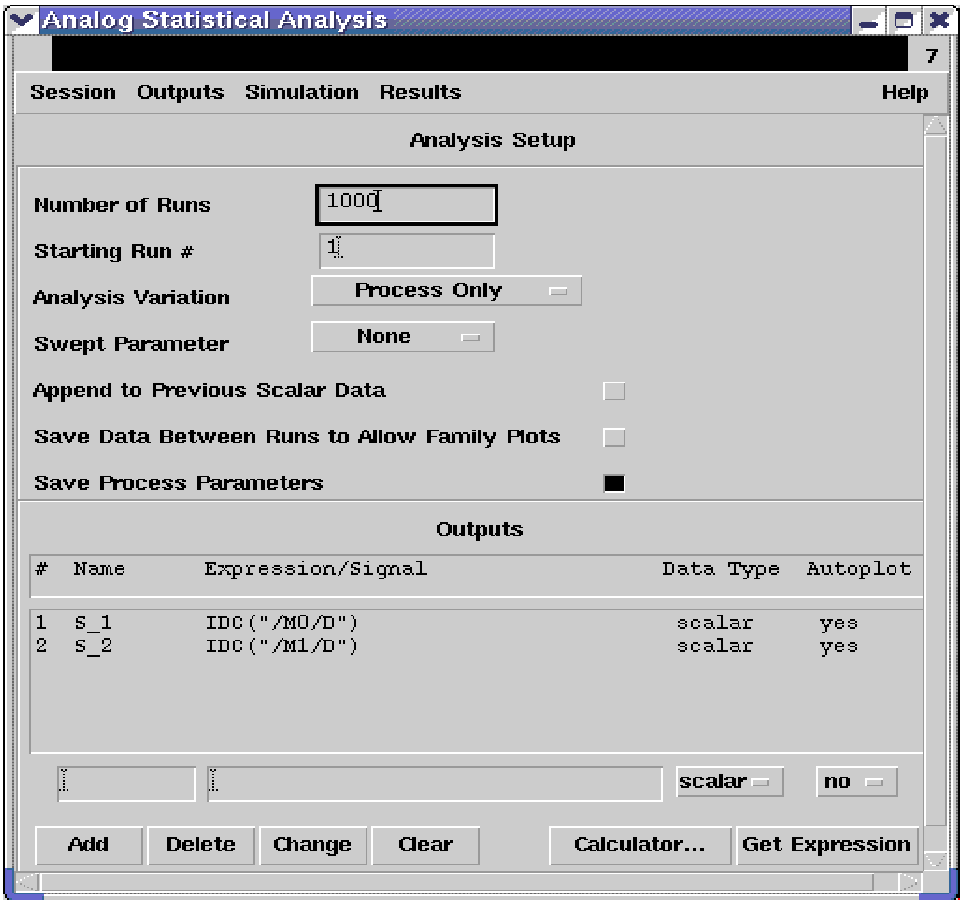


Figure. 11 Setup “Analysis Variation” to be “Process Only”

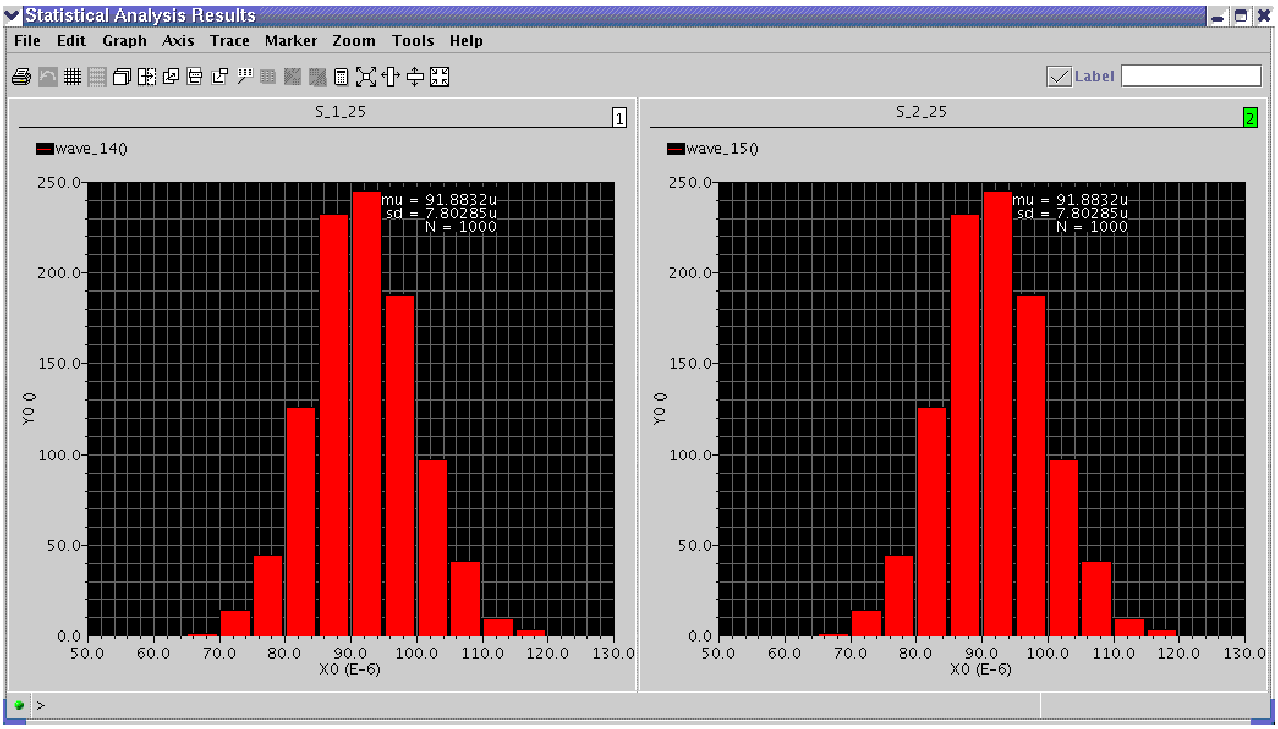


Figure. 12 Simulation result for both right and left branches of current mirror

Post-layout Mismatch Statistical Simulation

Starting from CRN65LP PDK v1.1, TSMC defines a (208:1) CAD layer for extracting mismatch devices. This LVS dummy layer (called “LVSDMY” in Layout Editor) is used to distinguish a mismatch MOS from regular MOS. If a transistor is covered by this (208:1) layer, the RC extraction tool will extract this transistor as a mismatch transistor (i.e. nch_mac or pch_mac) instead of a regular transistor. (i.e. nch or pch)

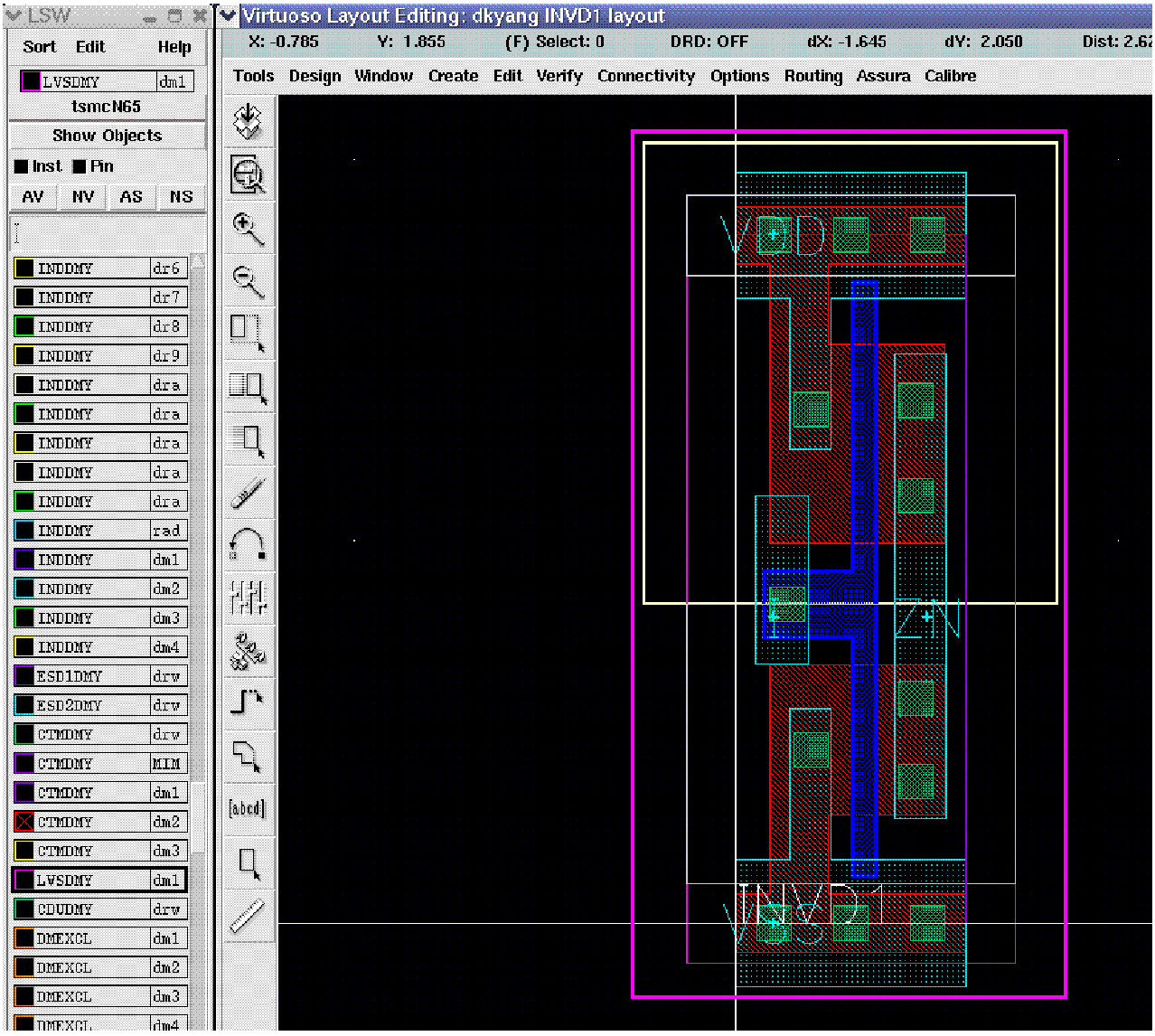


Figure. 13 Sample inverter layout with “LVSDMY” covering the cell

Figure.13 shows an example inverter standard cell covered with a LVSDMY layer. TSMC LVS/RC Extraction rule deck file can recognize this layer and extract all the devices in this layer as mismatched transistors for post-layout Monte Carlo

mismatch simulation.

```
**************************************************************
* CIRCUIT NETLIST
**************************************************************
.subckt INVD1 I ZN

XM0 ZN I VSS VSS nch_mac L=6e-08 W=3.9e-07 AD=7.02e-14 AS=1.1085e-13
+ PD=1.14e-06 PS=1.57e-06 NRD=0.461538 NRS=0.728797 SA=2.15e-07 SB=1.8e-07
+ SCC=0.00111744 SCA=19.9854 SCB=0.0179656 $X=0.305 $Y=0.285
XM1 ZN I VDD VDD pch_mac L=6e-08 W=5.2e-07 AD=9.36e-14 AS=1.388e-13 PD=1.4e-06
+ PS=1.83e-06 NRD=0.346154 NRS=0.513314 SA=2.15e-07 SB=1.8e-07 SCC=0.000852393
+ SCA=17.9818 SCB=0.0156662 $X=0.305 $Y=0.995

c_6 ZN VSS 0.163659f
c_9 I VSS 0.126418f
cc_1 ZN VSS 0.0338861f
cc_2 I VSS 0.0465218f
cc_3 I ZN 0.11698f

.ends
```

Figure. 14 The post-layout extraction tool extracts “nch_mac” and “pch_mac” in INVD1 cell

Figure.14 shows the post-layout extracted netlist with mismatch transistors. Designer can use this LPE netlist for running post-layout mismatch simulation and getting a better sense of circuit performance distribution after the real layout is done. The post-layout mismatch simulation flow and setup is the same as pre-layout mismatch simulation.

Appendix A: Reference Documents

T-N65-CM-SP-012-K1: TSMC 65 NM CMOS MIXED SIGNAL RF LOW POWER 1P9M SALICIDE CU_LOWK 1.2&3.3V PDK (CRN65LP)
T-N65-CM-SP-006-K1: TSMC 65 NM CMOS MIXED-SIGNAL GENERAL PURPOSE PLUS 1P9M AL_RDL SALICIDE CU_LOWK 1.0&2.5V PDK (CMN65G+)
T-N65-CL-SP-031-K1: TSMC 65 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M+AL_RDL SALICIDE CU_LOWK 1.0&1.8V PDK (CLN65G+)
T-N65-CM-SP-007: TSMC 65NM CMOS MIXED SIGNAL RF LOW POWER 1P9M SALICIDE CU_LOWK 1.2&2.5V SPICE MODEL
T-N65-CM-DR-001: TSMC 65 NM CMOS MIXED SIGNAL RF GENERAL PURPOSE 1P9M SALICIDE CU_LOWK DESIGN RULE
T-N65-CL-SP-009: TSMC 65 NM CMOS LOGIC LOW POWER 1P9M+AL_RDL SALICIDE CU_LOWK 1.2&2.5V HD BEOL SPICE MODEL (CLN65LP)