An Ultra-Broadband Power Amplifier Design

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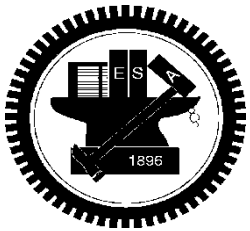
Advisor：Prof. Yu-Jiu Wang



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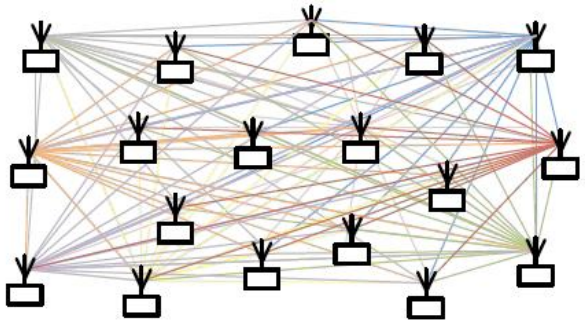
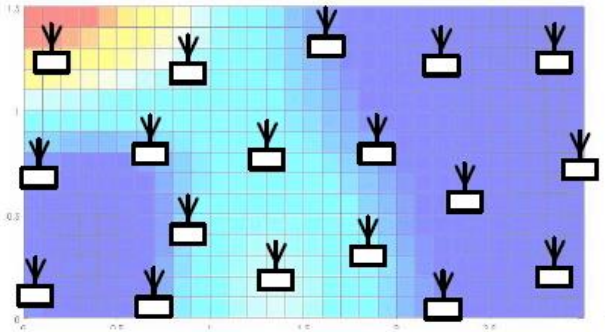
Outline

- Motivation and Architecture
- Amplifier Design and Transistor's Modeling
- Passive Circuit Design and Analysis
- Simulation and Measurement Results
- Debugging Discussion

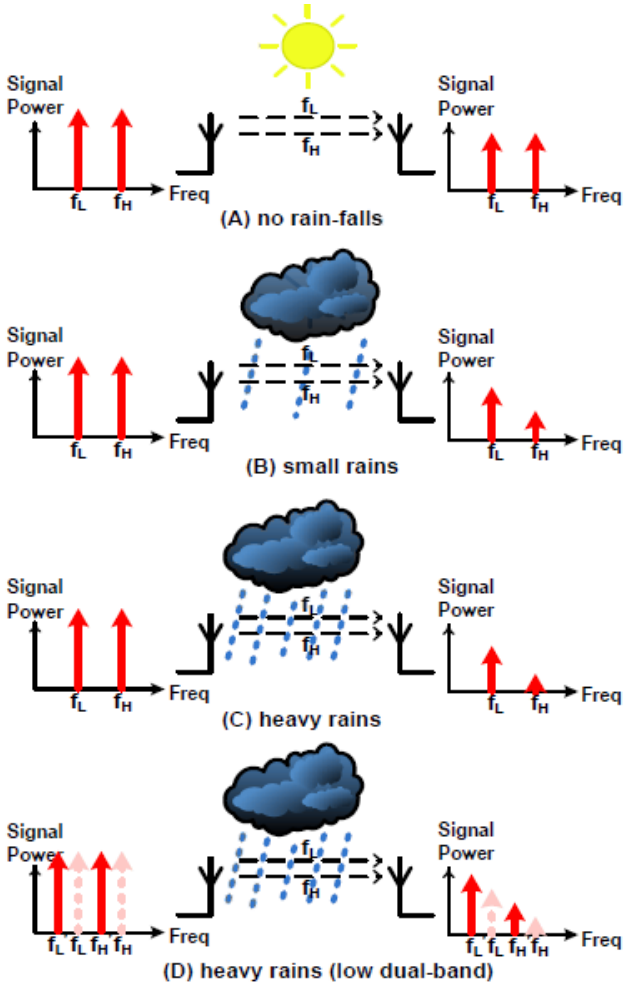
Motivation- Concurrent Dual-band, Dual-mode TRX Rainfall Detection



TRX network



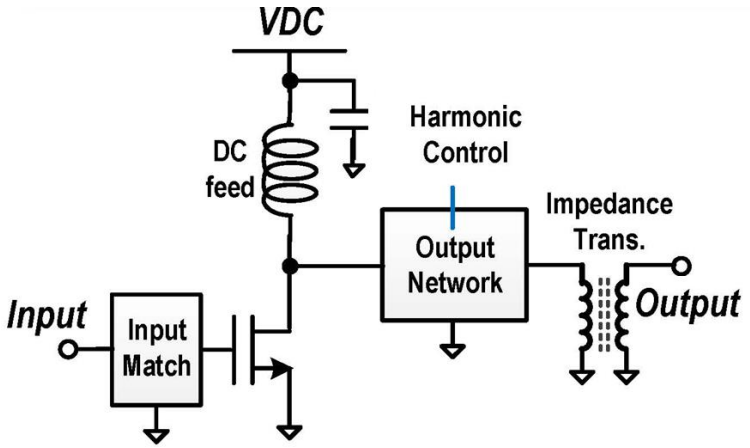
Rainfall Distribution (CT)



RF signal attenuation

Block Diagram of Power Amplifier

- Output Network
  - Impedance Transformation
  - Power Combining
  - Harmonic Control

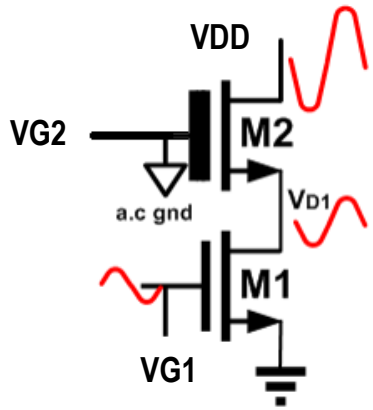


(1) Filtering: Only 1st harmonic tone passed to the 50Ω load.

(2) To shape **transistor's output** I/V waveform provides necessarily impedance at different harmonics for e.g. class F, class J.

Cascode Topology

- Thick Gate Oxide Device
  - higher breakdown voltage
  - lower process speed



- Common Gate Amplifier
  - improve twice PA's max. output voltage swing
  - Vgs is limited by M1

CG PA Size Choosing, Bias Conditions

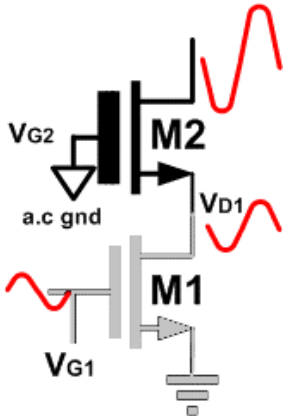
- PA Design Flow:

1. M1's breakdown $V_{DS} = 1.2V, V_{GS,GD} = 1.5V$

   $V_{G2} = V_{D1}(\max) + V_{th2} = 1.5 + 0.6 = 2.1V$

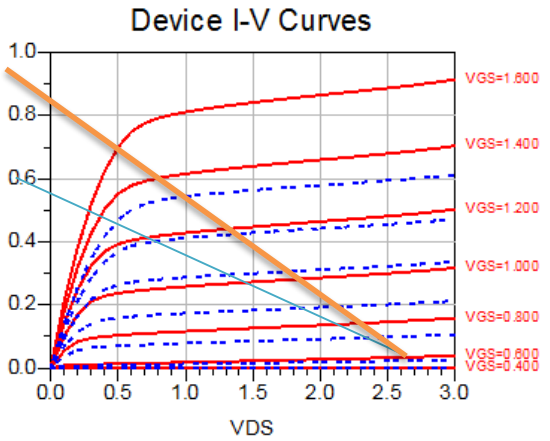
   M2's breakdown $V_{DS} = 2.7V, V_{GS,GD} = 4.5V$

   $V_{DD}=V_{D1}(DC)+V_{knee_2}+V_{DS2}(swing)=1+0.5+1=2.5V$



$\frac{W}{L} = \frac{3100}{0.28}$

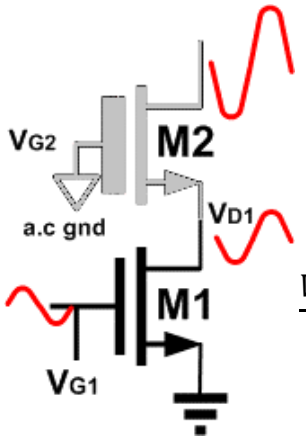
2. With limited V_{D1} headroom and $V_{DS2}(\max)$, M2's size corresponds to target output power.
   - M2 Size $\propto$ current magnitude $\propto$ output power $\propto \frac{1}{R_{load}}$
   - the same Vknee with different sizes



- Drain efficiency depends on input waveform

CS Driver Size Choosing, Bias Conditions

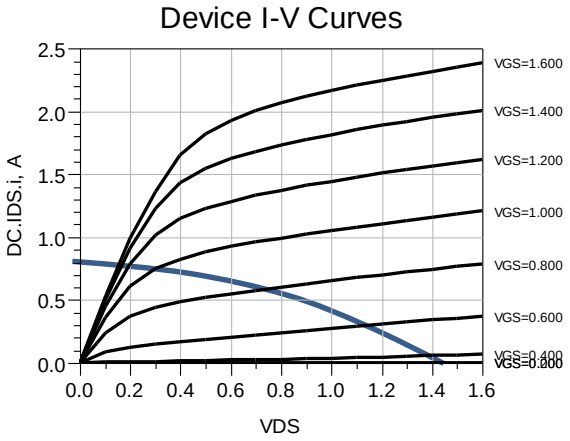
- Z_{load} = 1/G_{m2} paralleled with parasitic caps on inter-node
- $V_{D1_{max}}$ =1.5V based on breakdown criteria
- $I_{1max}=I_{2max}\times\frac{\sqrt{\left(G_{m2}^2+(\omega_o C_p)^2\right)}}{G_{m2}}$, C_p is parasitic cap. at D1 node



$\frac{W}{L}=\frac{1440}{0.06}$

- $V_{G1_{min}}$ = $V_{D1_{max}}$ -V_{DG}(breakdown)
- $V_{G1_{max}}$ =V_{GS1}(breakdown)
- V_{G1}(bias)=($V_{G1_{max}}$ + $V_{G1_{min}}$)/2= 0.8V

- M1 size: when gate voltage swing “touch” the triode region

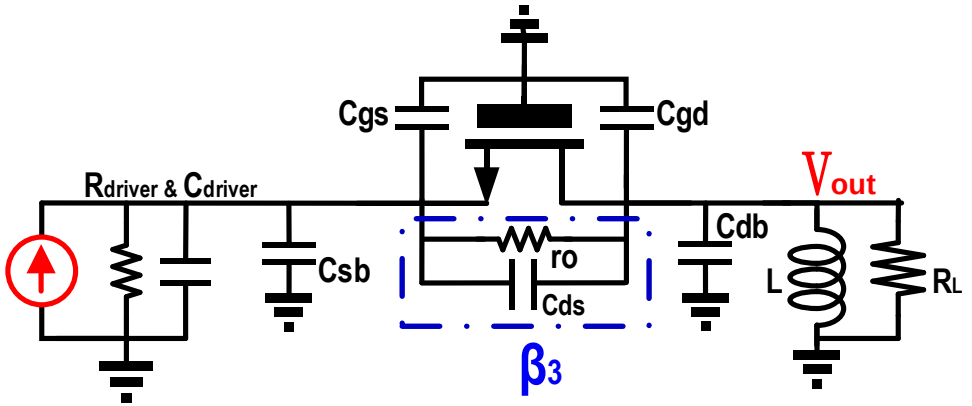


Oscillation Conditions

- Barkhausen Criterion: loop gain $|\beta H(\omega)| \geq 1$ and $\angle \beta H(\omega) = 180^{o}$

- $$\beta H(\omega) = \frac{(sC_{ds} + \frac{1}{r_o})(sL + R_L)(1 - s\frac{C_{ds}}{G_M})}{(1 + \frac{s}{\omega_{P1}})(1 + \frac{s}{\omega_{P2}})(1 + \frac{s}{\omega_{P3}})}$$

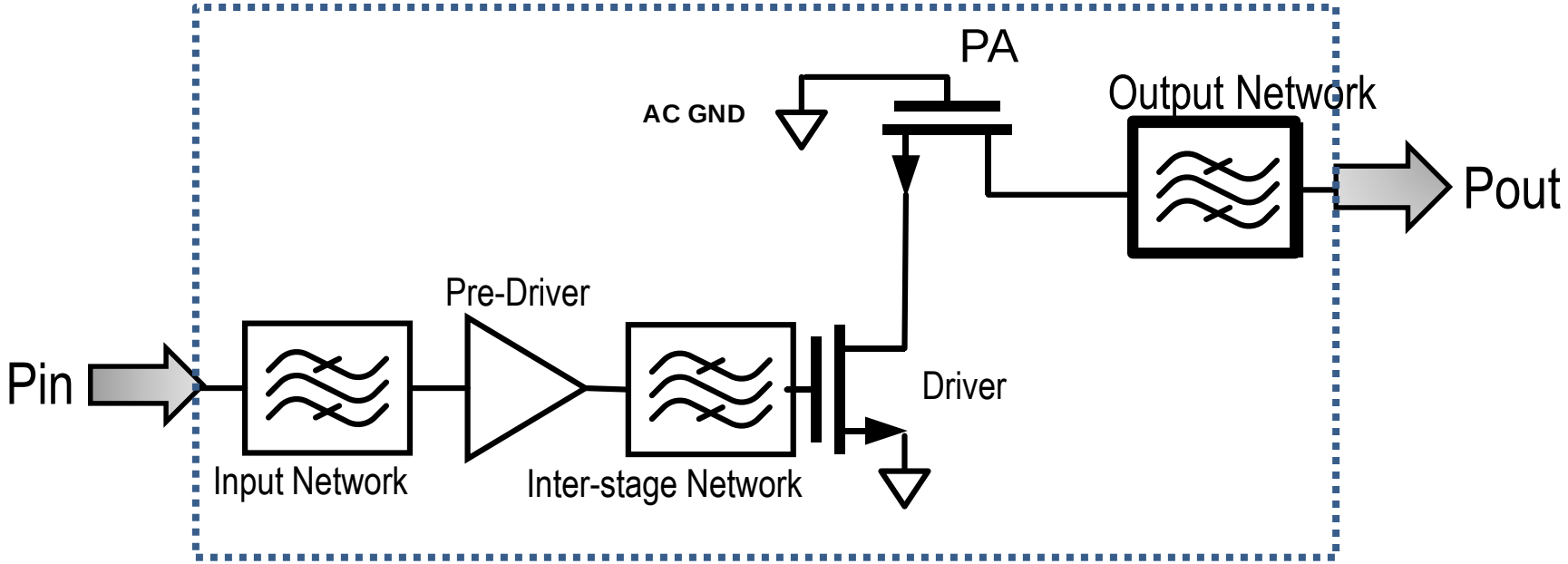
$\omega_{P1}, \omega_{P2}, \omega_{P3}$ equals to $\frac{1}{R_L C_{out}}, \frac{1}{R_{in} C_{in}}, \frac{R_L}{L}$



- Oscillation Conditions:

  If $\omega_{P1} >> \omega_{Z2}$ and $|\beta H(\omega)| > 1$ b.t. ω_{z2} to ω_{p1}

Simplified Chip Block Diagram



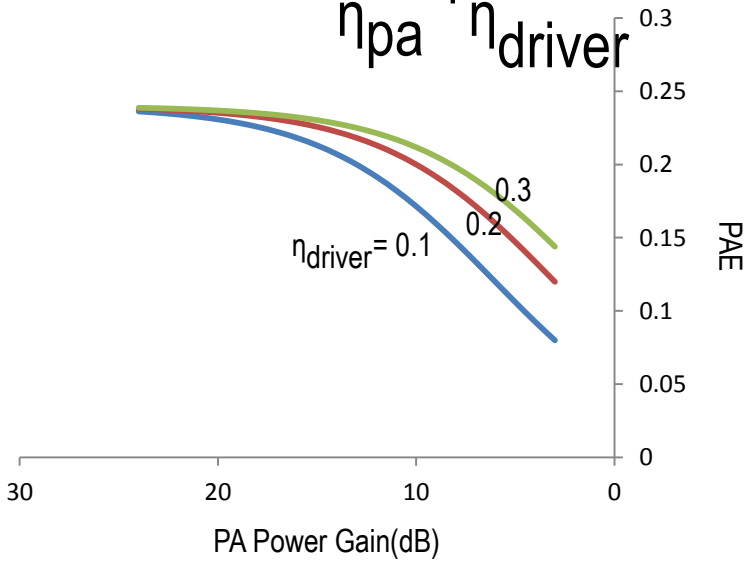
PA Specifications

- P_{SAT} : MAX power whole PA could deliver = PA's maximum drain power * efficiency of output network

- $$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{Eff_{output} G_{PA} G_{driver} P_{in} - P_{in}}{P_{DC_{PA}} + P_{DC_{driver}}} \cong \frac{Eff_{output} * G_{PA}}{\frac{G_{PA}}{\eta_{pa}} + \frac{1}{\eta_{driver}}}$$

where η=transistor's drain efficency= $\frac{P_{RF_{OUT}}}{P_{DC}}$

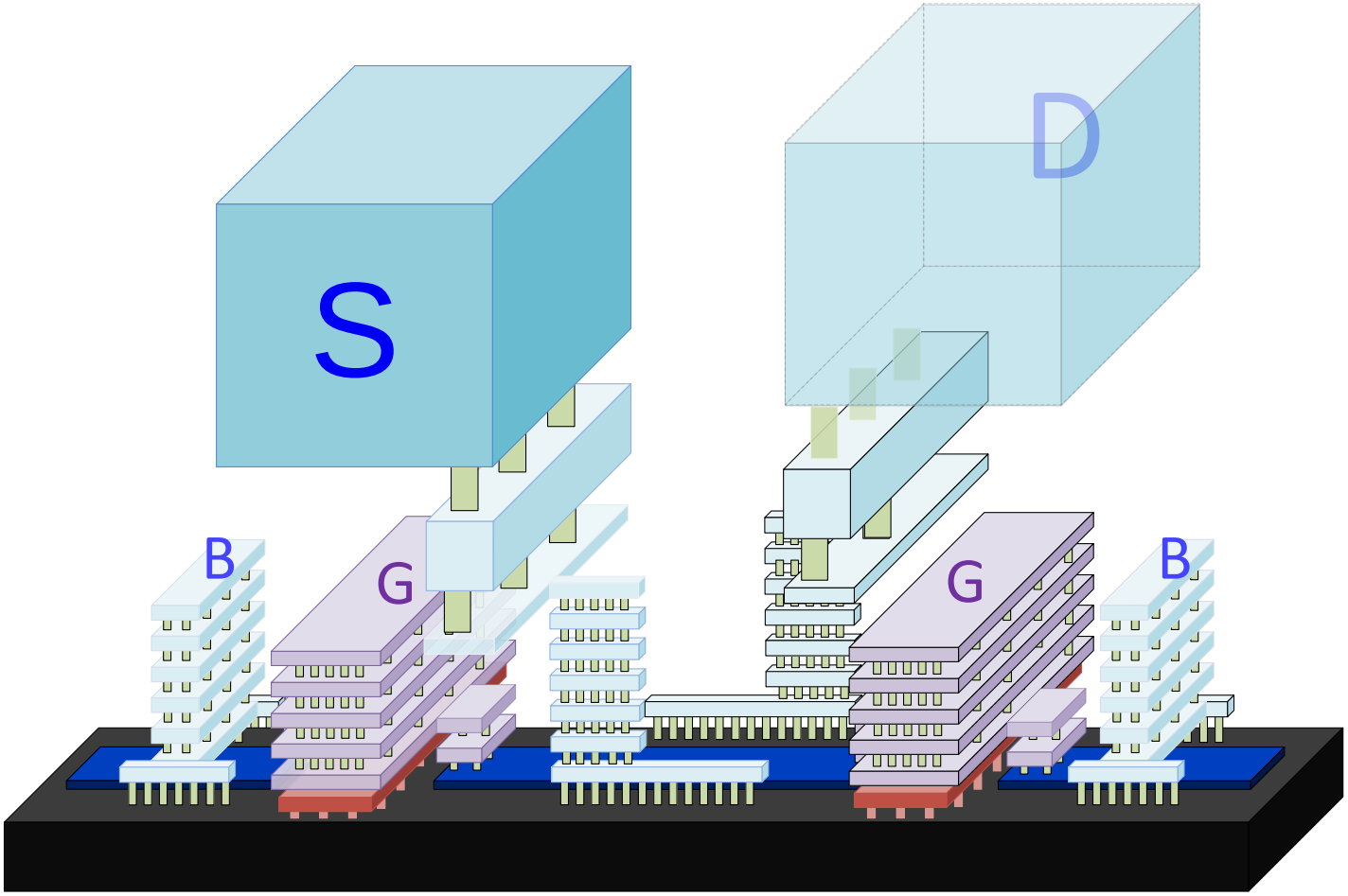
and assume $Eff_{output} G_{PA} G_{driver} \gg 1$



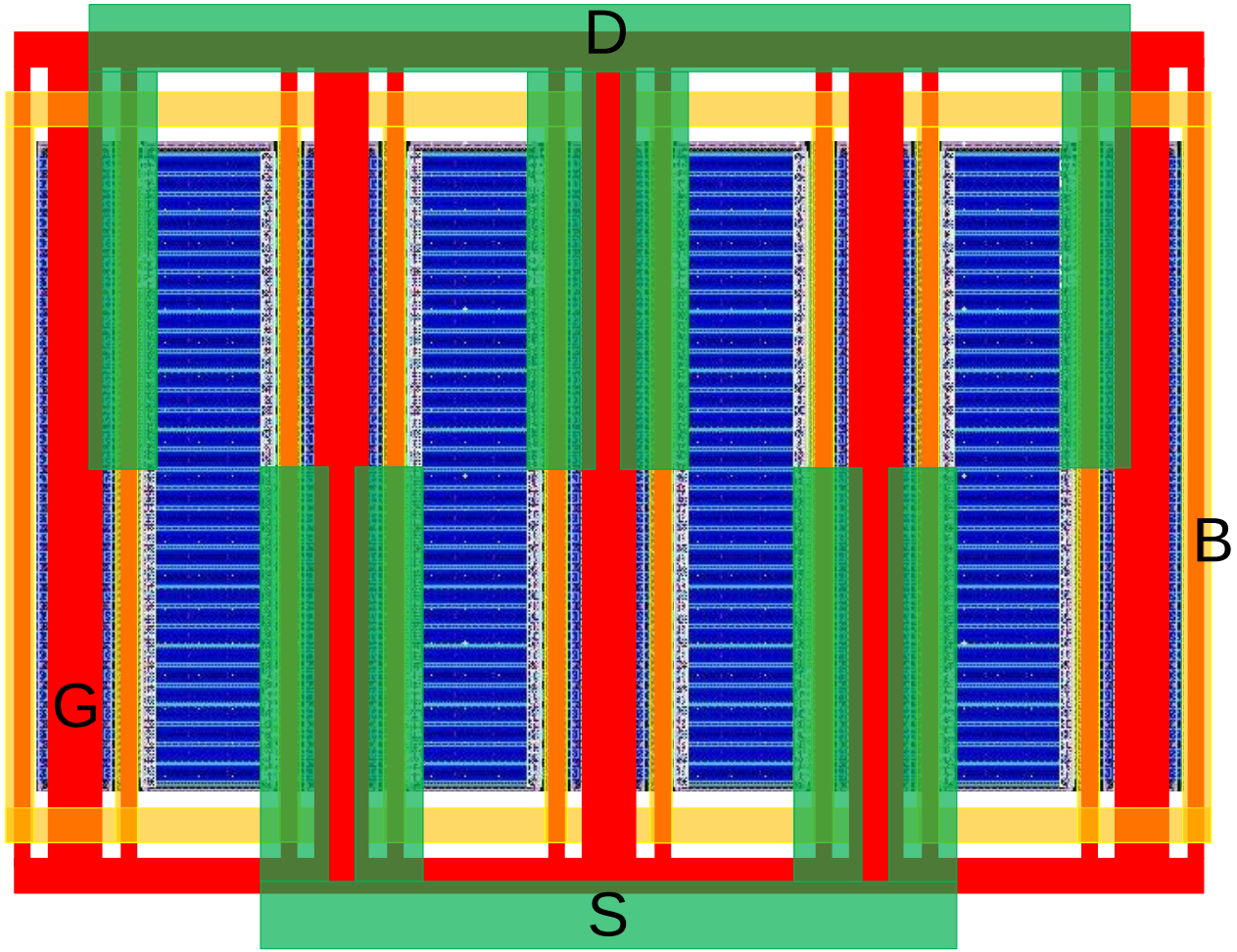
Power Transistor Design

- Determine how to connect multi-finger transistors in parallel
  - layout placement and metal's reliability to DC/AC current
  - reduce parasitic R,C related to output power/bandwidth performances
- Modeling, optimization

Single Transistor Layout Structure Design for Common Gate



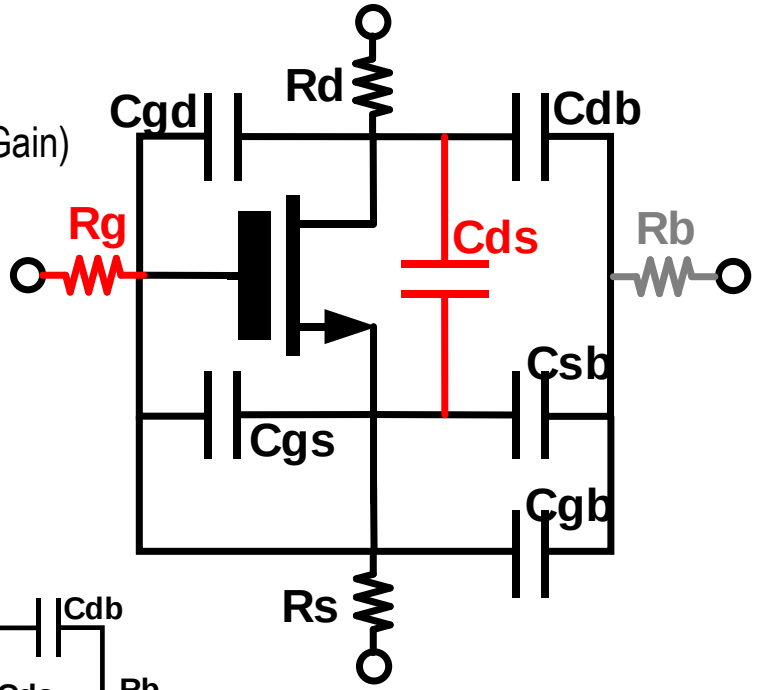
Parallel Combining of multi-finger Transistors



PA - Common Gate Amplifier

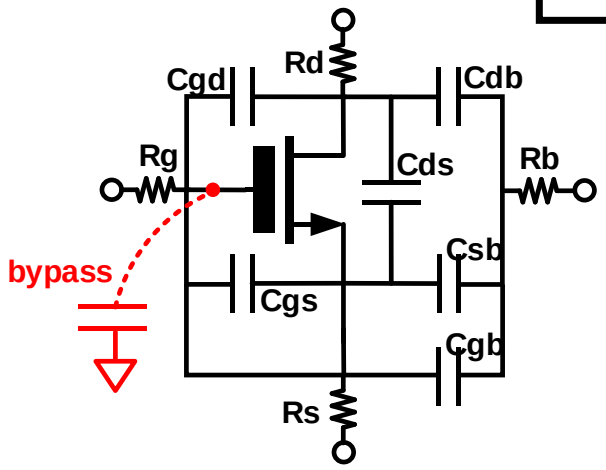
- $\beta = \frac{1}{Z_{C_{DS}}} = j\omega \mathbf{C_{DS}}$, $H_{close} = \frac{H_{open}}{1+H_{open}\beta}$ (Transimpedance Gain)
- Rg: decrease the equivalent Gm when freq. increase

$$V_{GS} = \frac{Z_{Cgs}}{R_g + Z_{Cgs}} V_S = \frac{1}{j\omega \mathbf{R_g} C_{gs} + 1} V_S$$



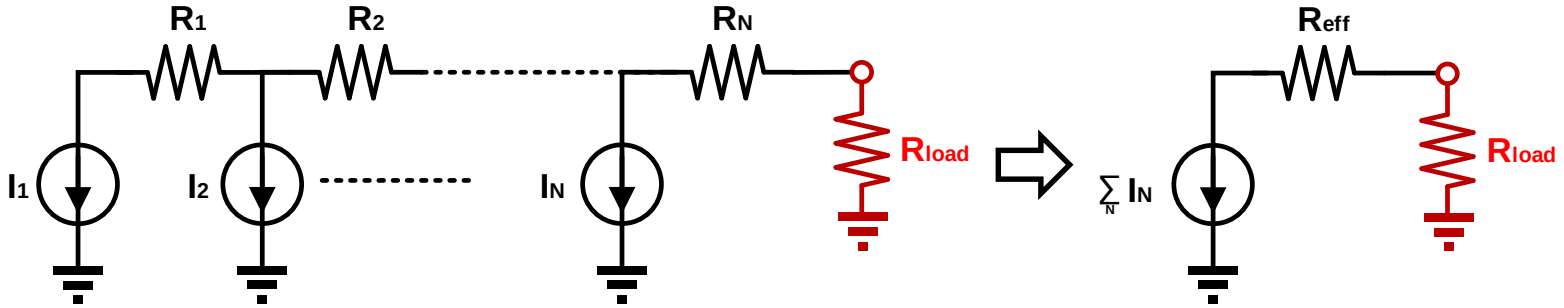
Rg: Insert Gate to Body bypass using MOS Cap. between two multi-finger transitors (the same finger # with transistors beside)

$Rg_{new} = Rg // Z_{bypass}$



Modeling of Layout Parasitic

- effective resistance

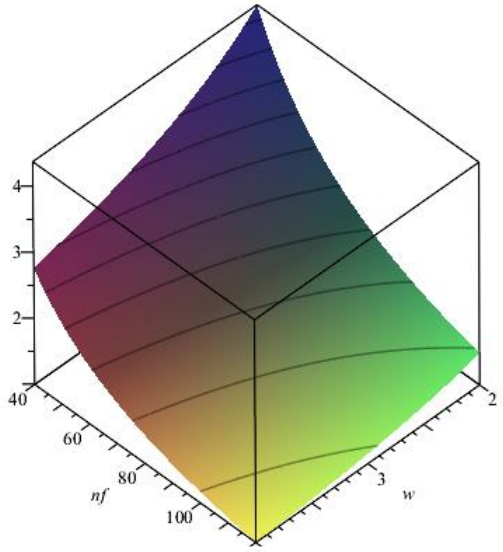


(e.g.) If $I_1 = I_2 = \ldots = I_n = I$, and $R_1 = R_2 = \ldots = R_N = R$

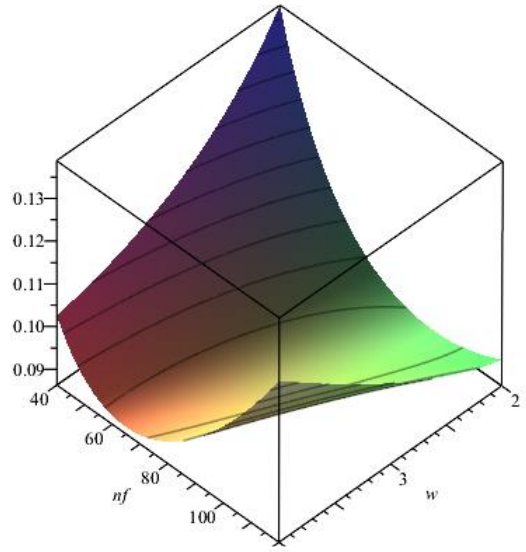
$$I^2 \times R + (2I)^2 \times R + \ldots + (NI)^2 \times R = (NI)^2 \times R_{eff},\ R_{eff} = \frac{(N+1) \times (2N+1)}{6N} R \cong \frac{1}{3} NR \quad \text{(if N is large)}$$

- to model parasitic Caps. by interpolation of PEX results

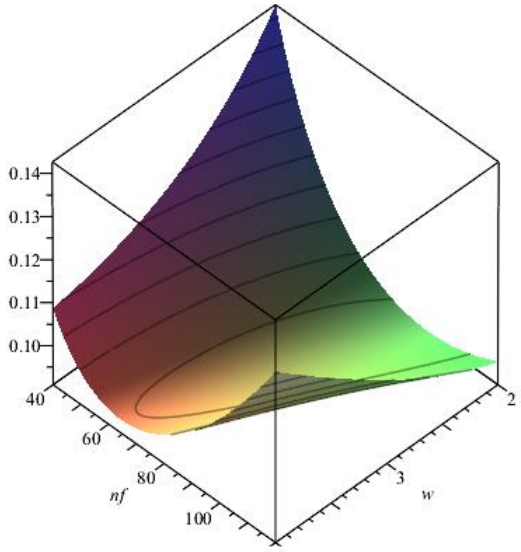
Common Gate Power Transistor Optimization



(a) Rg (total)

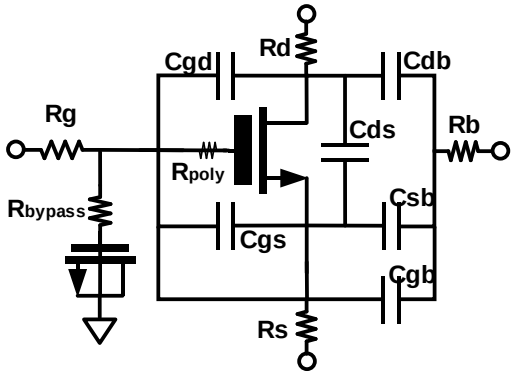


(b) Rs



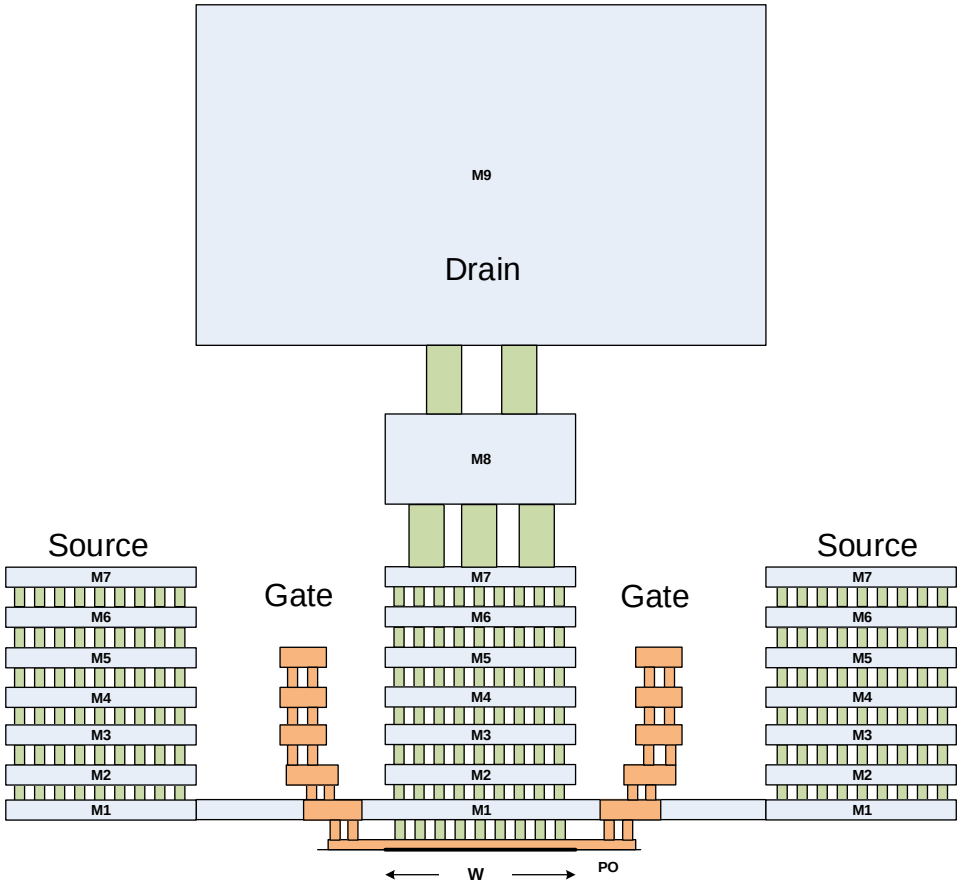
(c) Rd

(1) fix total W, minimize R_X(w,nr)
(2) metal reliability criteria with min. Cds, nr ≤ α*(160/w)

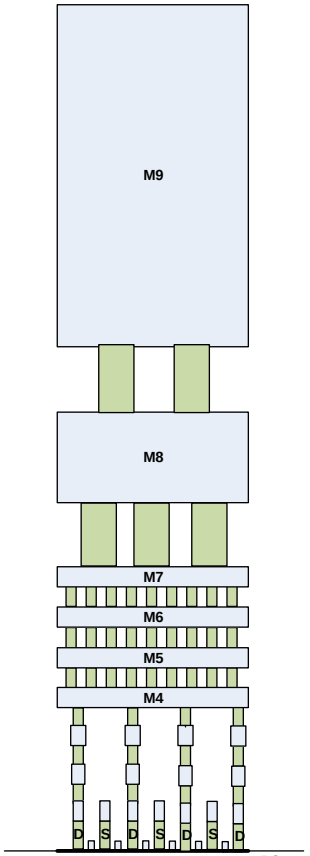


(e.g.) Total Width=3000
w=3.3μm, nr=90, M=10

Single Transistor Layout Structure Design for Common Source



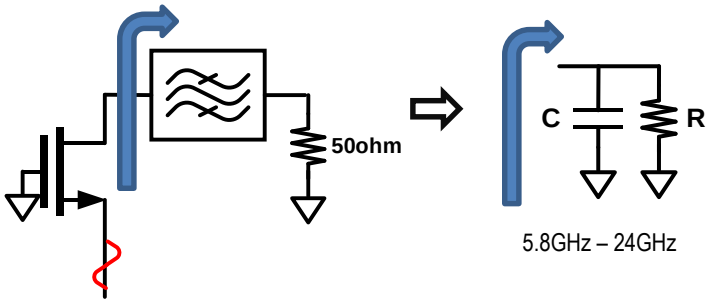
SIDE #1



SIDE #2

Broadband Optimum Load & Passive Output Network

- $\frac{Q_{load}}{\omega_o} = \frac{1}{R_{load} C_{out}} \propto$ 3dB Bandwidth



$$R \cong \frac{\max V_{swing}}{I_{swing}}$$

$$C \cong -(C_{DG} + C_{DB} + C_{DS})$$

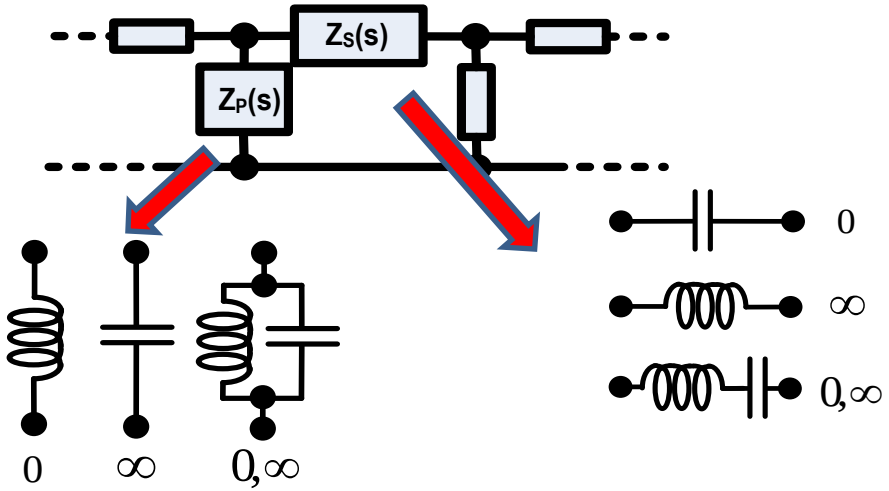
(1) $\tau_{network} = R_L C_L \geq R_{opt} C_{out} = 2 \frac{V_{swing}}{V_{in}} \times \frac{C_{out}}{G_m}$

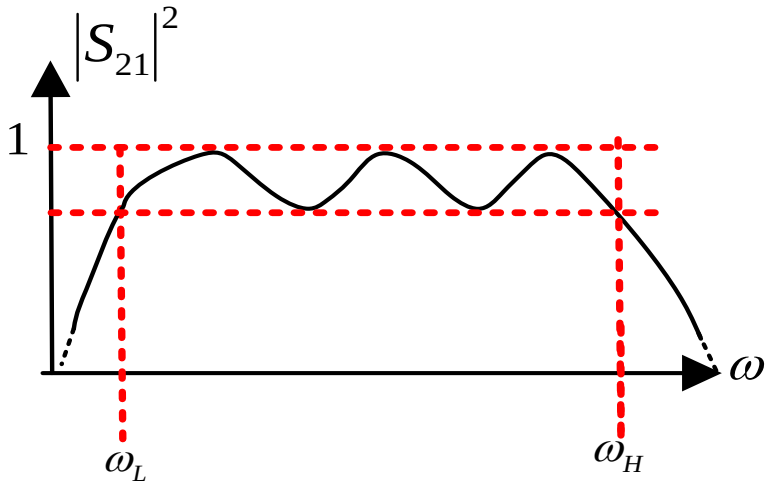
$$V_{swing} \leq \frac{1}{2} \tau_{network} \times \frac{G_m}{C_{out}} \times V_{in}$$

(2) impedance transformation ratio

(3) network's passive efficiency

To Define Two-Port Band-pass LC-Ladder Network





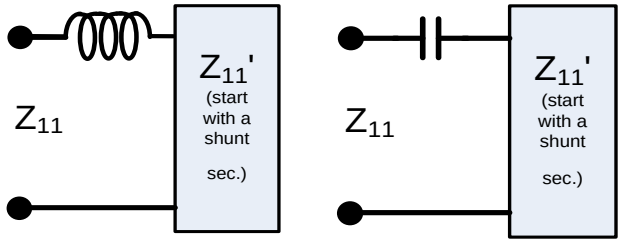
- Bode-Fano limit: $\int_0^\infty \ln\frac{1}{|\Gamma(j\omega)|}d\omega \le \pi\left(\frac{1}{R_{opt}C_{out}}\right)$
- Passive Ladder: $|S_{21}(s)|^2 = H(\omega^2) = \frac{1-C}{1+C\cdot\frac{A_N s^{2N}+A_{N-1}s^{2(N-1)}+\cdots+A_1 s^2+A_0}{s^{2M}}} = \frac{1-C}{1+C\cdot F}$
- Chebyshev Filter : find $F \in [-1,1]$ with $\omega \in [\omega_L, \omega_H]$
- Relations among ripple, N to BW, impedance transformation ratio

Darlington's Insertion-loss Method

- **General Procedures:**
  1. Find out $|S_{21}(s)|^2$ as a function of ω^2.
  2. Determine $|S_{11}(s)|^2 = 1 - |S_{21}(s)|^2$.
  3. Determine all possible S_{11} from $|S_{11}|^2$.
  4. Determine $Z_{11} = \frac{1+S_{11}}{1-S_{11}}$ from each S_{11}.
  5. Determine all possible realizations of Z_{11} and choose the best one.

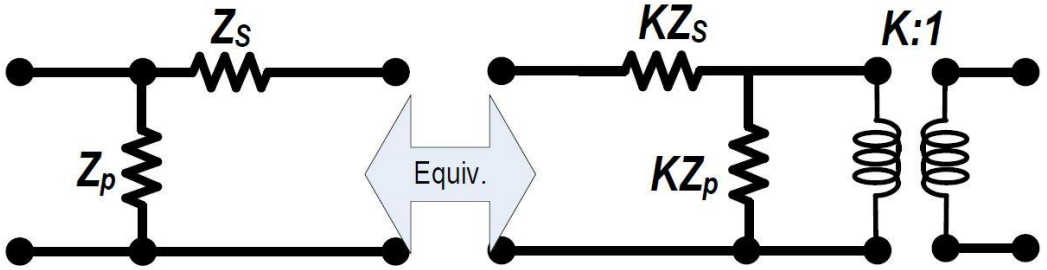
(e.g.) $Z_{11} = sL + Z'_{11}$? Z'_{11} is reduced-order, and has no pole at $\omega = \infty$.

$Z_{11} = \frac{1}{sC} + Z'_{11}$? Z'_{11} is reduced-order, and has no pole at $\omega = 0$.



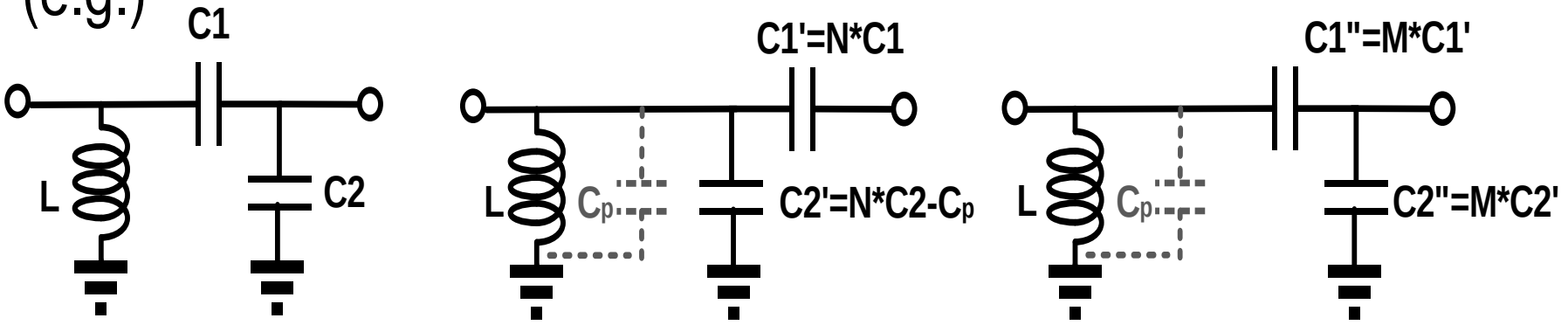
Node Parasitic Cap. Compensation

- Norton's Transformation



$$K = \frac{Z_p}{Z_p + Z_s}$$

- (e.g.)

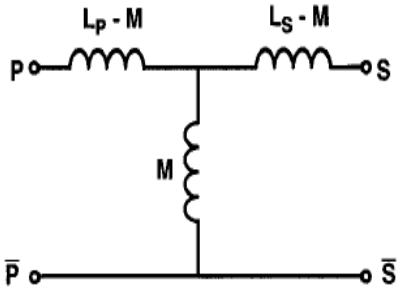


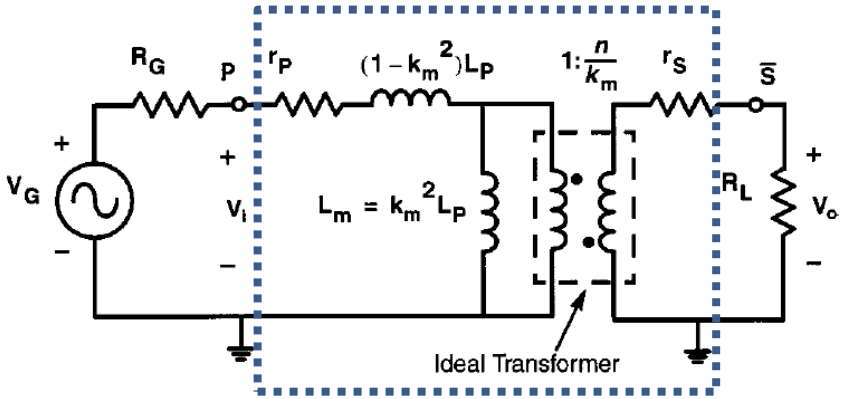
Limitation of Broadband Load Tracking

- $|S11|^2 + |S21|^2 +$ power loss(ratio) =1, when loss is large, load tracking failed.
  - How to define wideband flat Z_{out} Synthesis ?
  - How to formulate passive efficiency, impedance transform ratio and bandwidth?

Output Network

- Impedance transformation ratio $\eta_{diff} = 4\eta_{com}$
- Insert transformer to network



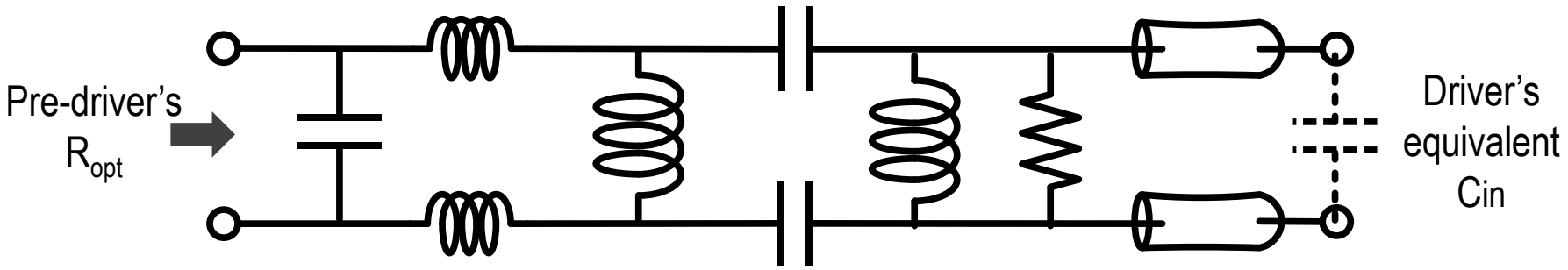


- $\frac{k_m^2 L_p}{(1-k_m^2)L_p}$ is positively correlated with network's bandwidth
  $\rightarrow$ network BW↑ required transformer's k_m↑
- Transformer's passive efficiency

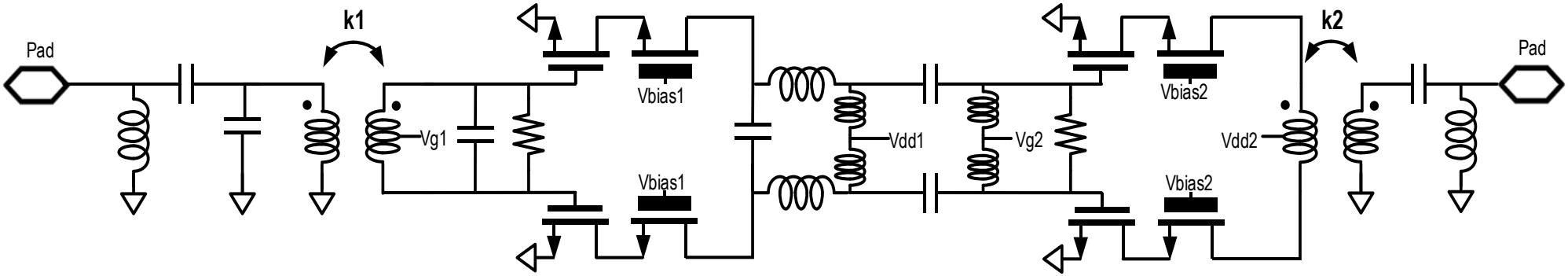
Pre-Driver & Inter-Stage Network

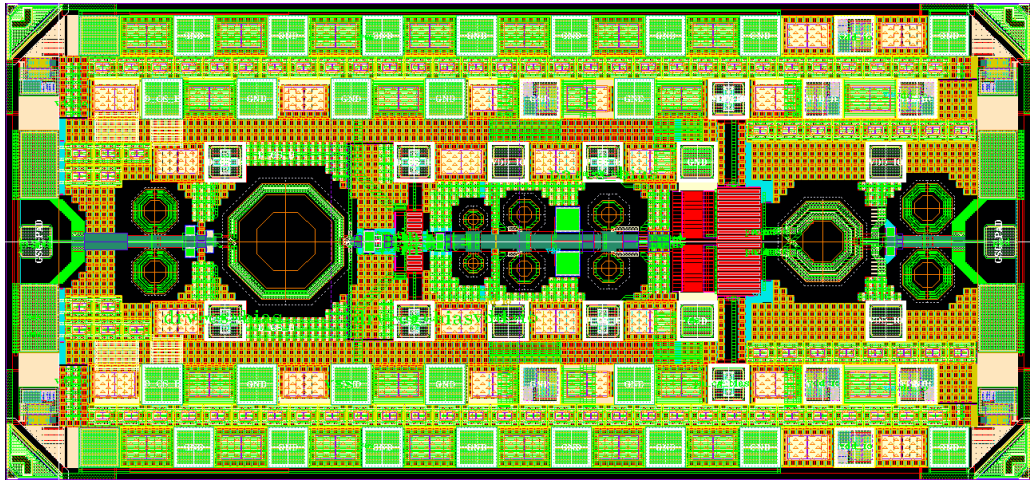
- Pre-driver stage operates in Class-A mode to improve gain and linearity.
  - cascode amplifier with $\left(\frac{W}{L}\right)_{nch} = \frac{250\ \mu m}{0.06 \mu m}$ and $\left(\frac{W}{L}\right)_{nch25} = \frac{530\ \mu m}{0.28 \mu m}$
  - Ratio of driver's max. input voltage and pre-driver's max output voltage

  ➔ impedance transformation ratio of interstage network

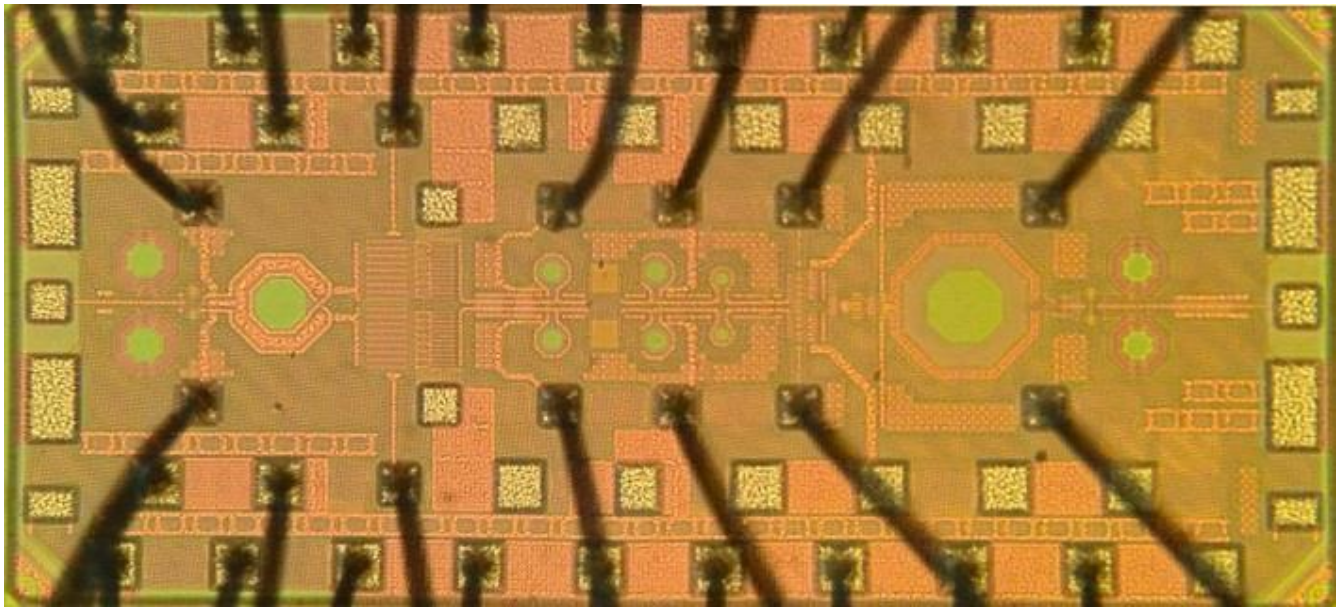


Full-Chip Schematics & Layout





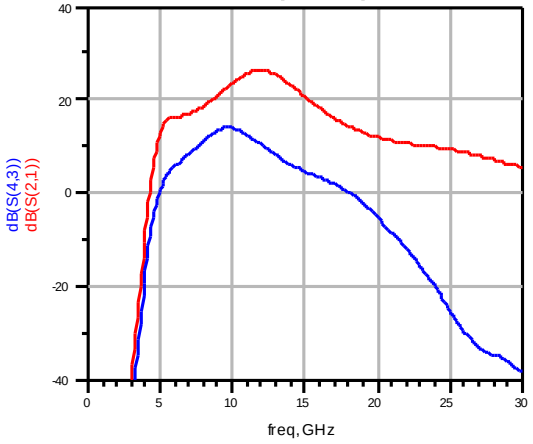
Chip Micrographs



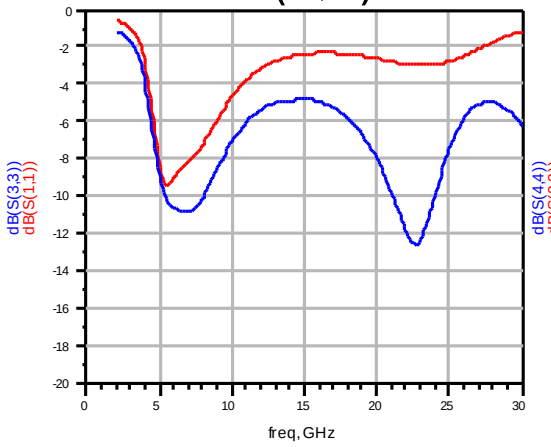
Chip Area:	1614×675 um^2
DC Power Consumption:	2.5V×960 mA

Full Pre-Simulation (red line)
vs.
Measurement (blue line)

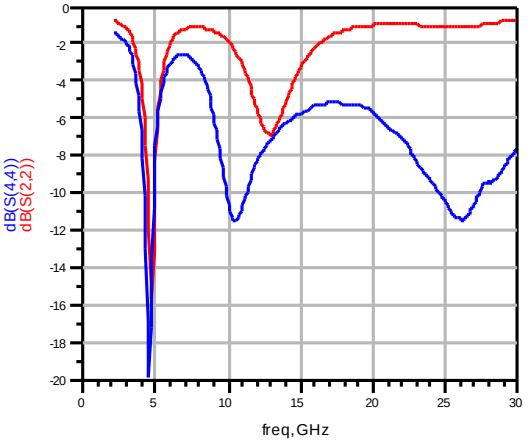
S(2,1)



S(1,1)

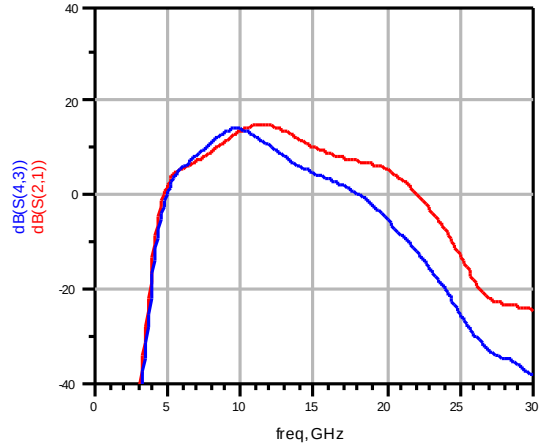


S(2,2)

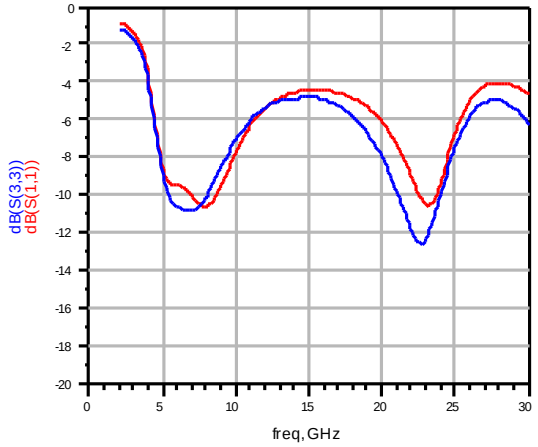


Full Post-Simulation (red line)
vs.
Measurement (blue line)

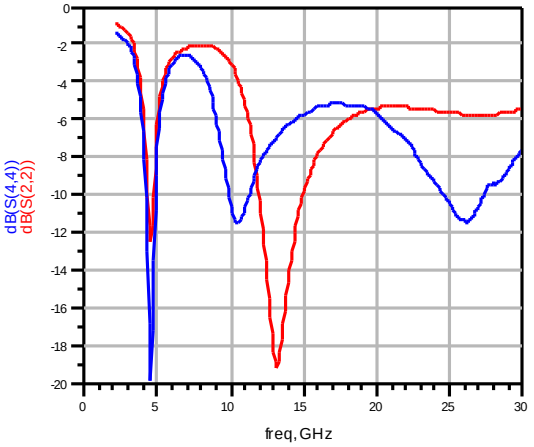
S(2,1)



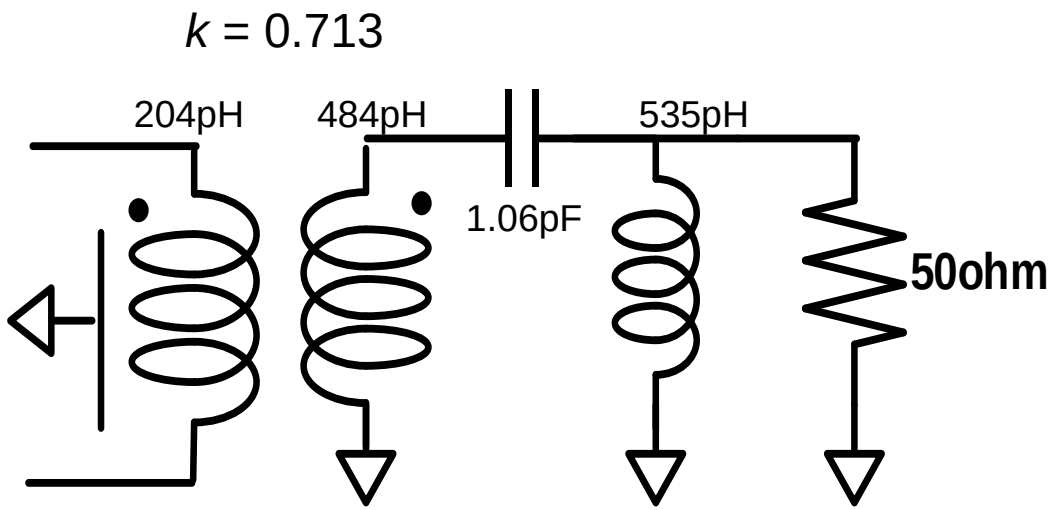
S(1,1)

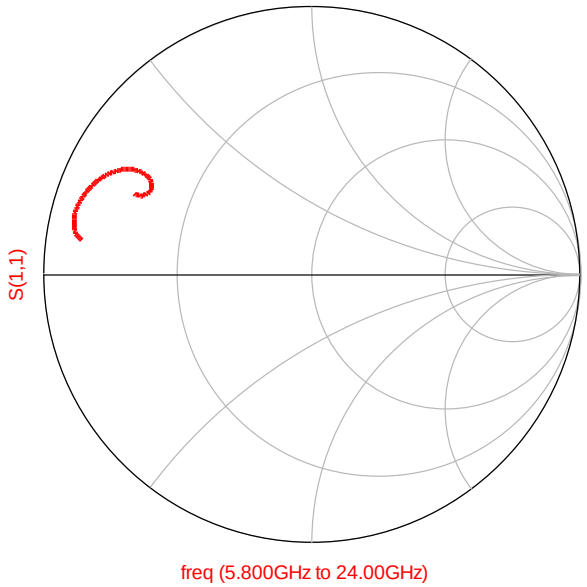


S(2,2)



Output Network





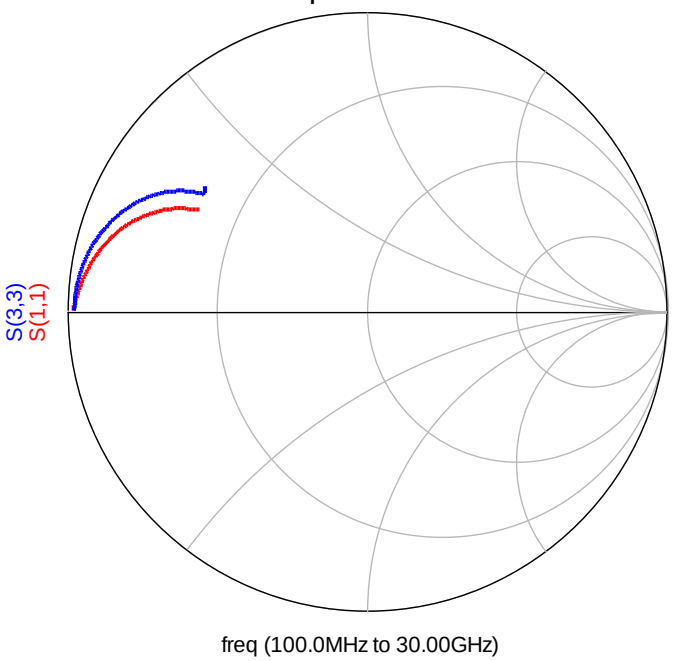
Output Network – Transformer modeling errors

PORT1: Differential Input PORT

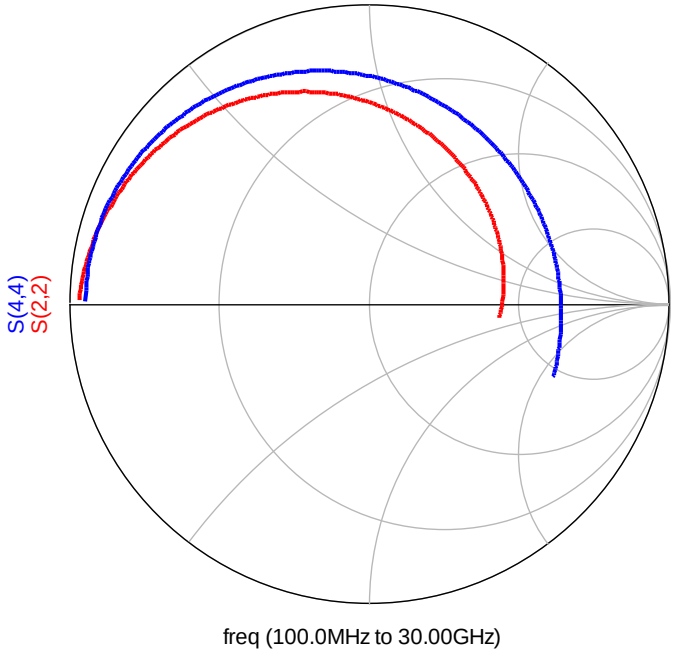
PORT2: Output PORT

Red line: EM S2P

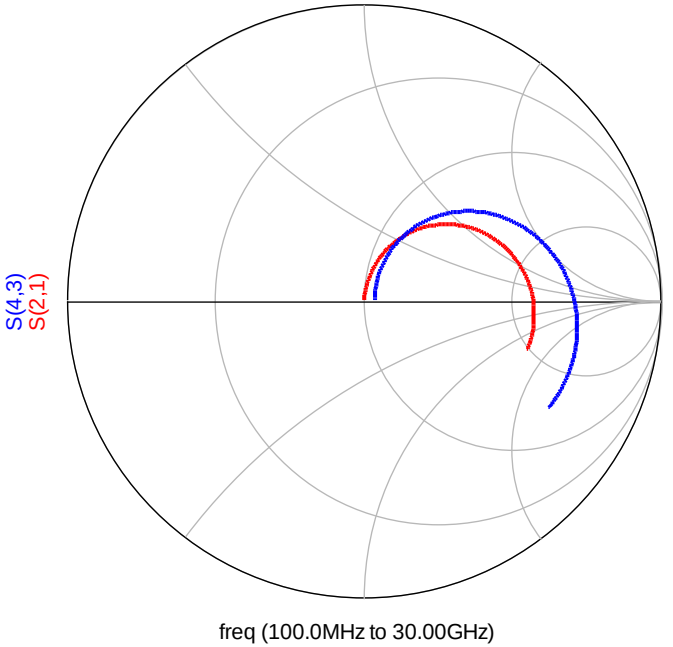
Blue line: Model



S(1,1)



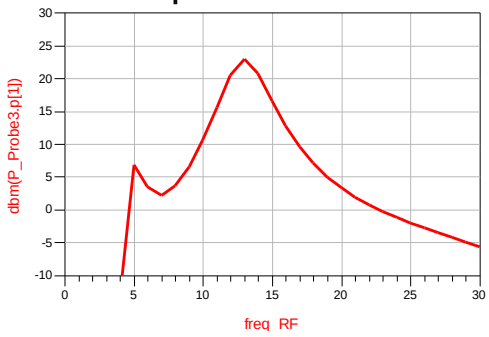
S(2,2)



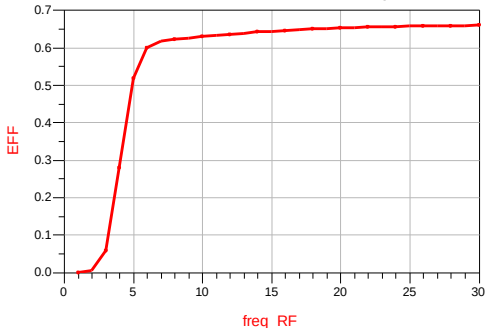
S(2,1)

Output Network

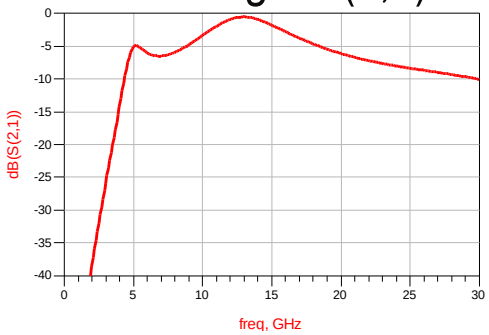
Output Power



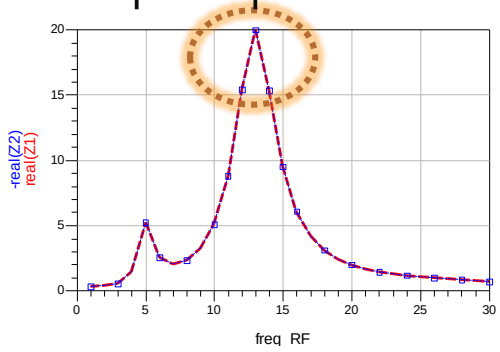
Passive Efficiency

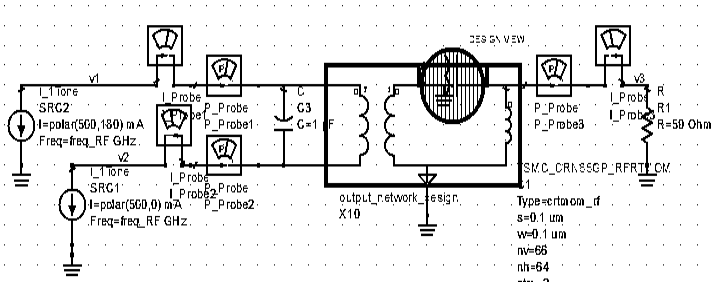


Diff. to single S(2,1)



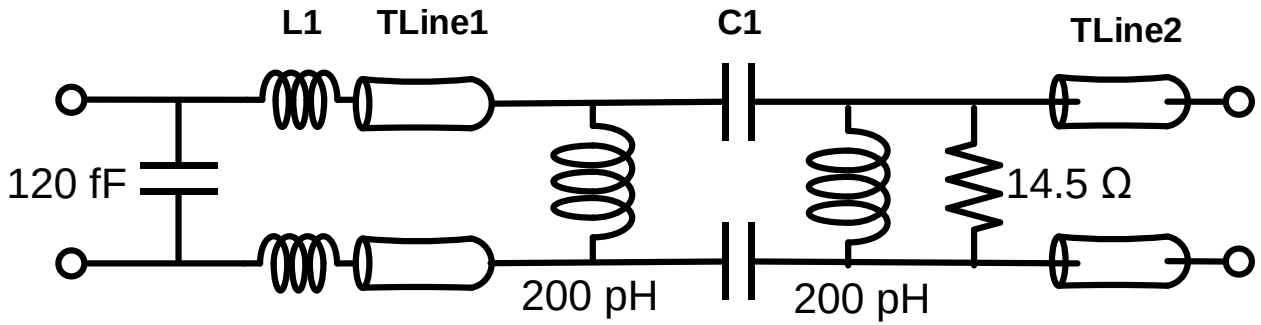
Input Impedance





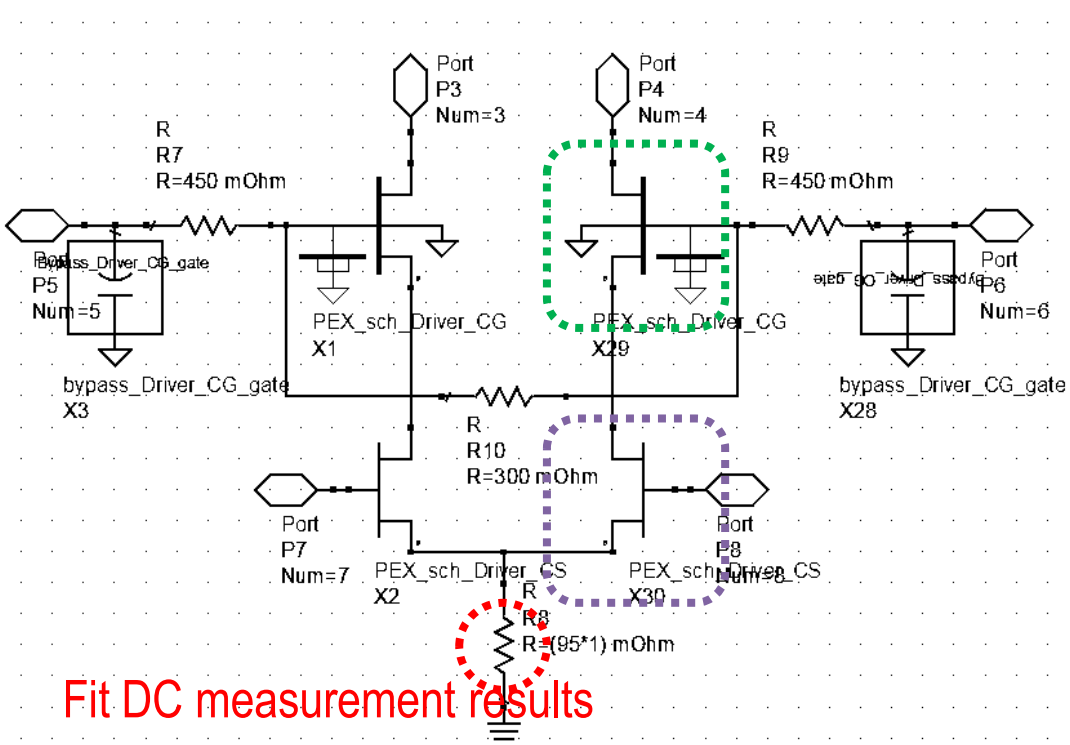
500mA RF current & 2pF device output cap. assumed
Network is designed from 5Ω to 50Ω

Interstage Network

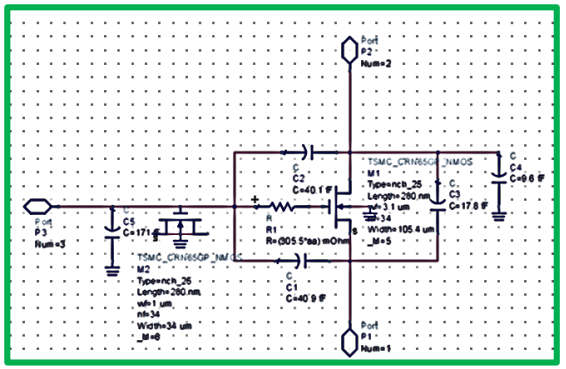


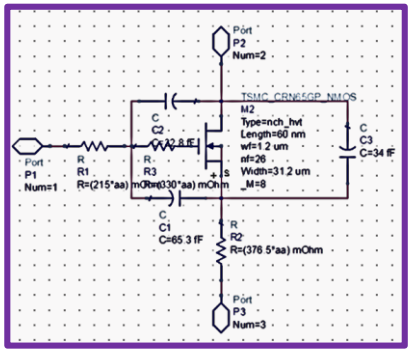
- L1=55pH, which is sensitive to parasitic TLine1
- C1=3.98pF, which has visible parasitic L effect, but not model in network synthesis Model
- CS PA driver input feed lines, parasitic TLine2, change the frequency response of network

Fit Transistor parasitic RC by PEX results



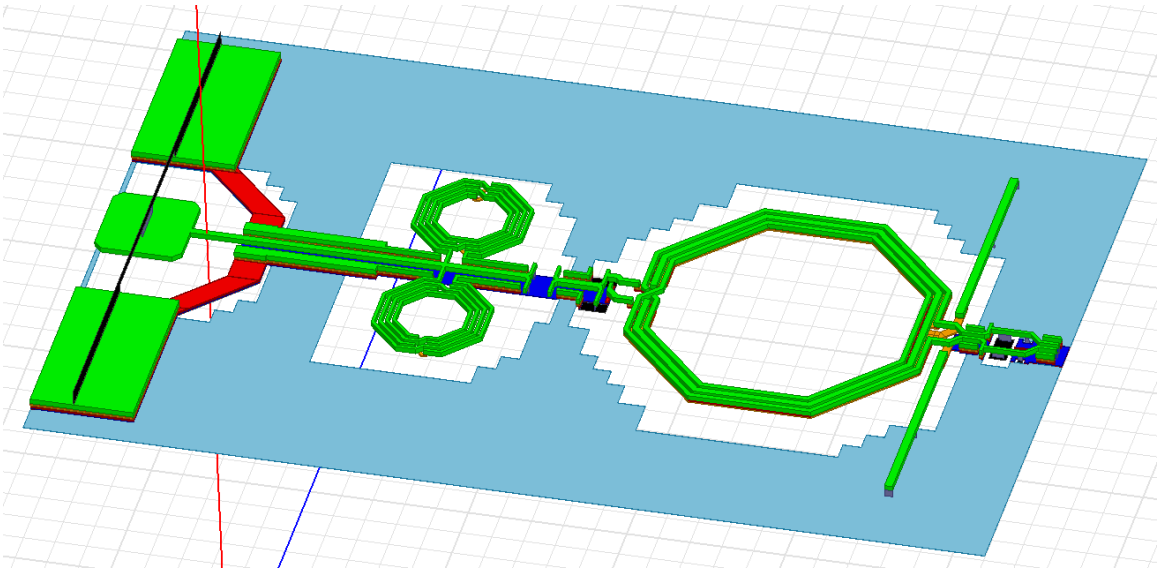
Fit DC measurement results





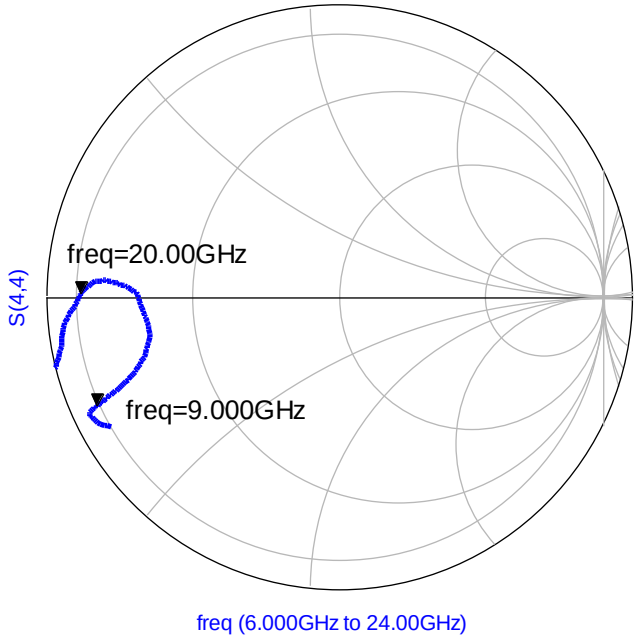
Input Network

- To affect input matching accuracy (XFM model error)
- Tiny effects to S21



Power Transistor Model Accuracy

- De-embed measurement S-parameter with output network EM results
  - Transfer [S] to [T]
  - $[T]_{de\text{-}embed} = [T]_{chip} * [T]^{-1}_{network}$
  - Transfer $[T]_{de\text{-}embed}$ back to [S]
- To model “skin effect” of R
- To model L from EM



My Suggestion to This Work's Future

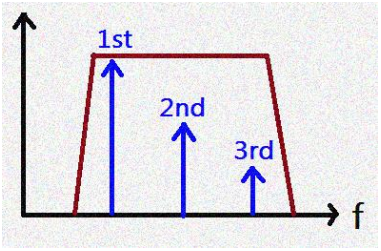
- Target smaller power& use nch to replace nch25
- Thank you.

Appendix

Ultra-Broadband Considerations

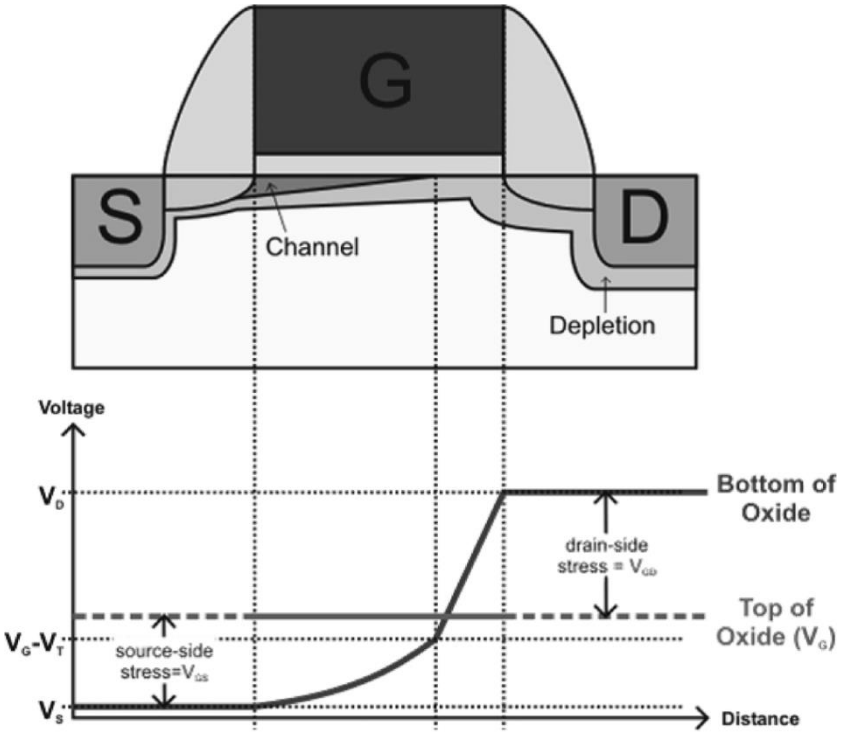
- In-Band Harmonics Problem in Ultra-Broadband Scales
  - At relative low frequency, 2nd and 3rd harmonic tones would be in-band.

  It CANNOT be filtered!!!



  - Broadband push-pull output network cancels 2nd harmonic
  - Broadband poly-phase combining network cancels both 2nd and 3rd harmonics

Gate Oxide Breakdown



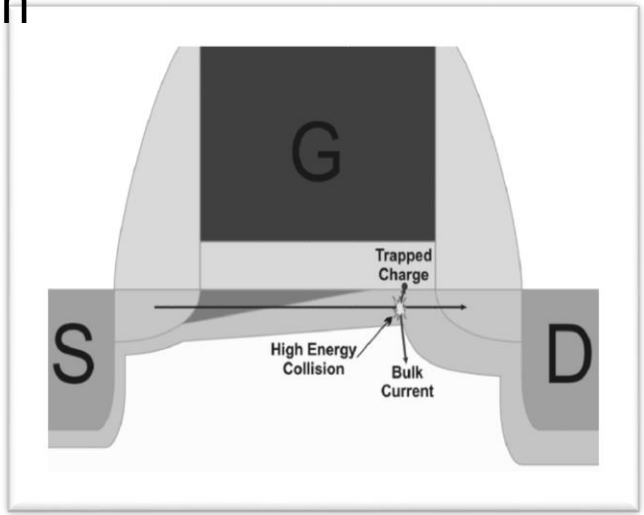
- Catastrophic damage caused by excessive voltage across gate oxide
- Probabilistic: lifetime decreases with voltage and device area
- Determined by oxide thickness and quality

1.0V Core Device (W/L=1.4mm/60nm)	V_{GD} max=1.5V
2.5V I/O Device (W/L=3 mm/280nm)	V_{GD} max=4.5V

Must keep max V_{GD}, V_{GS} within limit for gate oxide breakdown.

V_{DS} Breakdown Mechanism

- Hot Carrier Injection Effect
  - gradual device performance degradation over a period of time
  - necessary to have high drain-source voltage, V_{DS}, and substantial drain current at the same time
  - Max V_{DS} of 1.0V 65nm NMOS: 1.18V
    Max V_{DS} of 2.5V I/O NMOS: 2.70V



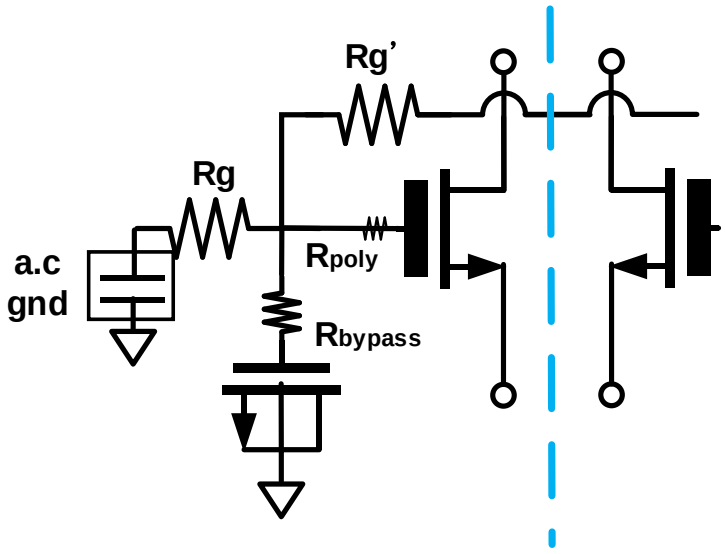
- Punch-Through (V_{DS})

  65nm NMOS=3.0V

Precise Model of Gate Resistor Network

Rg network:

Differential Mode:
symmetric line of layout is A.C ground
Common Mode:
symmetric line of layout is open



$$Rg=4(R_g//R_g'),\quad R_g'=\frac{R_g}{3}$$

$$Z_g(diff)=R_g//\frac{R_g}{3}//Z_{bypass}+R_{poly}$$

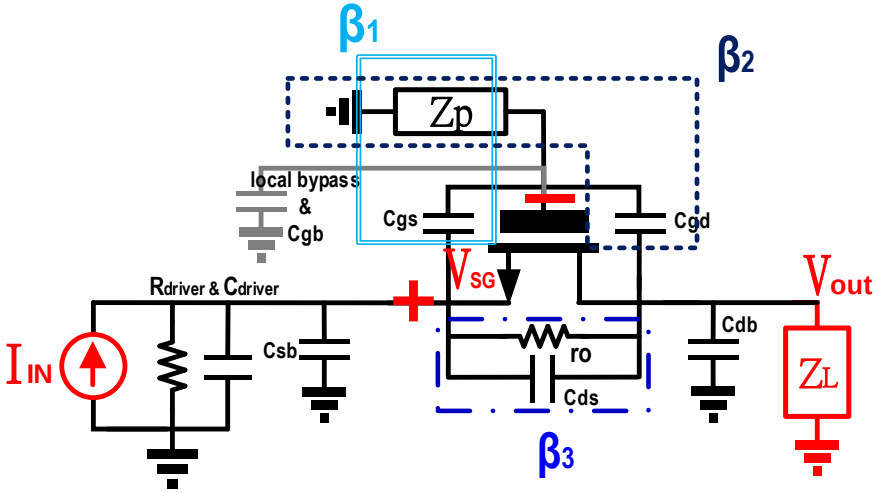
$$Z_g(com)=R_g//Z_{bypass}+R_{poly}$$

Oscillation Conditions in details

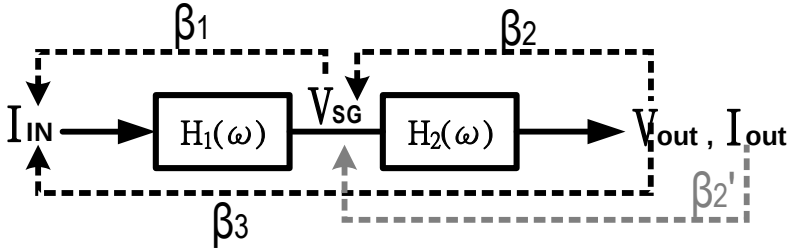
- Feedforward: $s_z = +\frac{G_M}{C_{DS}}$, f_z is larger than 100GHz in 0.28 μm I/O device.
- Positive Feedback:

  β_1 , β_2 : series-shunt feedback

  β_3 : shunt-shunt feedback

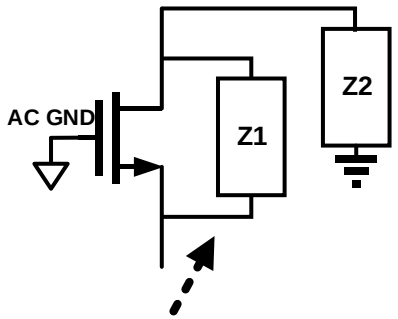


- Insert Local Bypass Caps:
  - $Zp_{new}=Zp//Z_{bypass}$
  - kill β_1 ,$\beta_2$feedback mechanism



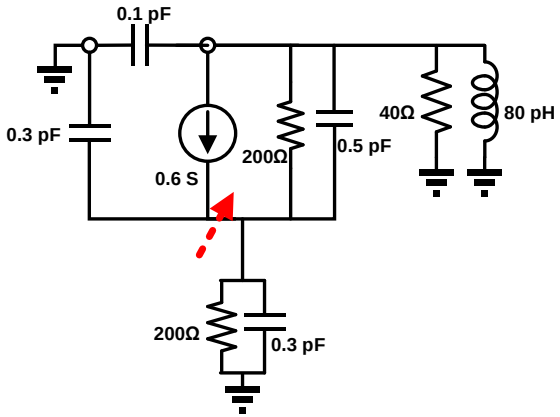
P.S. β_2': series−series feedback, inductive coupling b.t. Z_L & Z_p

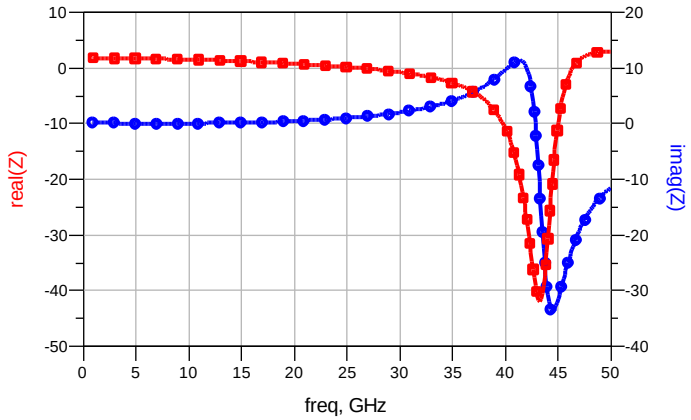
Effective Negative Port Resistance



- If $Z1=\frac{1}{j\omega C_{DS}}$, $Z2=R+j\omega L$, we get $j\omega L \,//\, \frac{1}{G_m}(1-\omega^2 C_{DS} L)$ at high frequency if R is small.
  a) narrow band short-stub matching
  b) XFM common-mode inductor

Example:

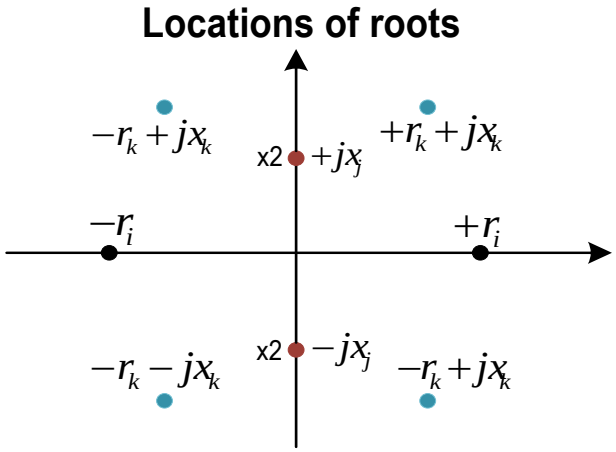


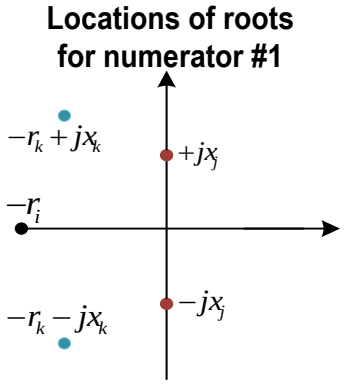


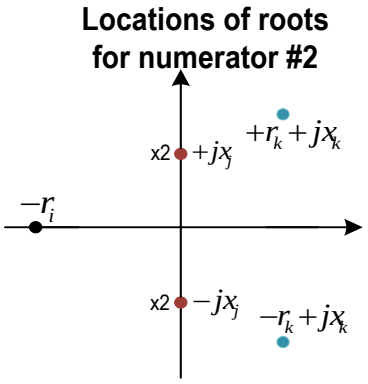
"$|S_{11}|^2 \rightarrow S_{11}$" Enumerations

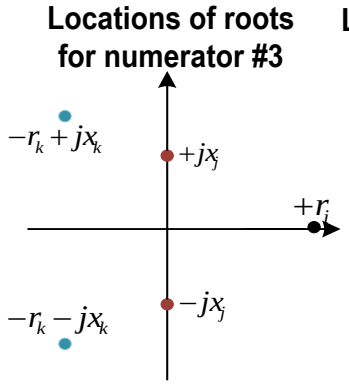
- $|S_{11}|^2 = S_{11}(s)S_{11}(-s) =$

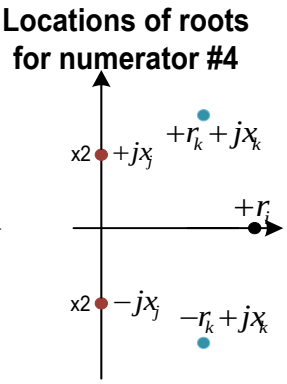
$$\frac{\prod_m (r_{z,m}^2 - s^2)\prod_n (r_{z,n}^2 + s^2)^2 \prod_o (s + r_{z,o} + jx_o)(s + r_{z,o} - jx_{z,o})(s - r_{z,o} + jx_{z,o})(s - r_{z,o} - jx_{z,o})}{\prod_i (r_{p,i}^2 - s^2)\prod_j (r_{p,j}^2 + s^2)^2 \prod_k (s + r_{p,k} + jx_{p,k})(s + r_{p,k} - jx_{p,k})(s - r_{p,k} + jx_{p,k})(s - r_{p,k} - jx_{p,k})}$$

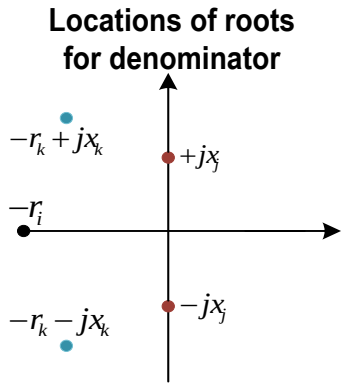








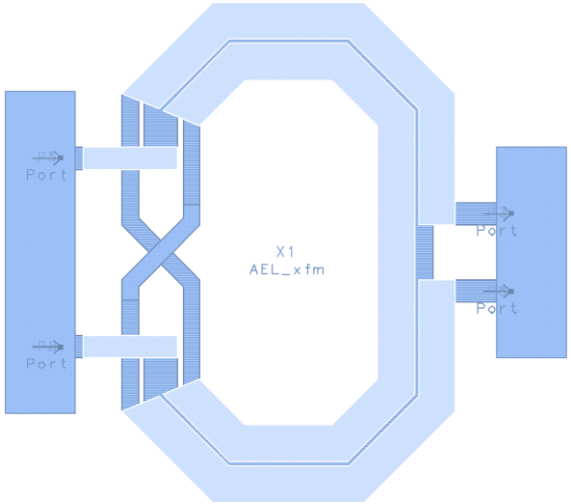


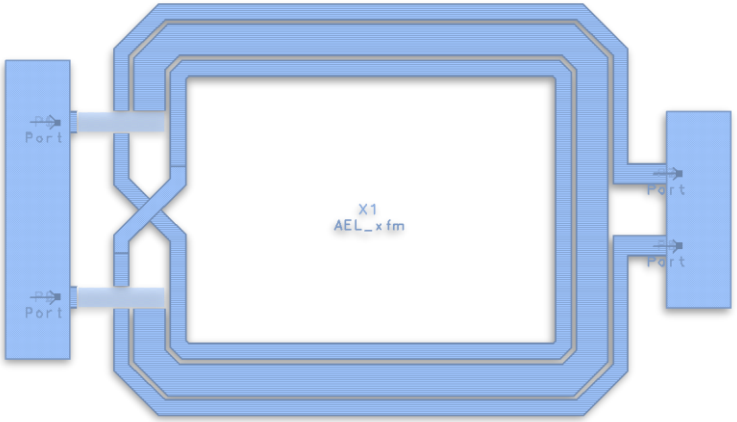


- Roots of numerators can be either Right-Half-Plane(RHP) or Left-Half-Plane (LHP).
- Roots of denominators can only be Left-Half-Plane (LHP) for stability in time-domain.
- **Algorithms:** find all roots, and go through all of them and enumerate recursively based on RHP & LHP, and calculate S_{11} of each root enumeration.

Efforts to Improve Transformer's Model

LAYOUT: more tuning degree of freedom to fit model

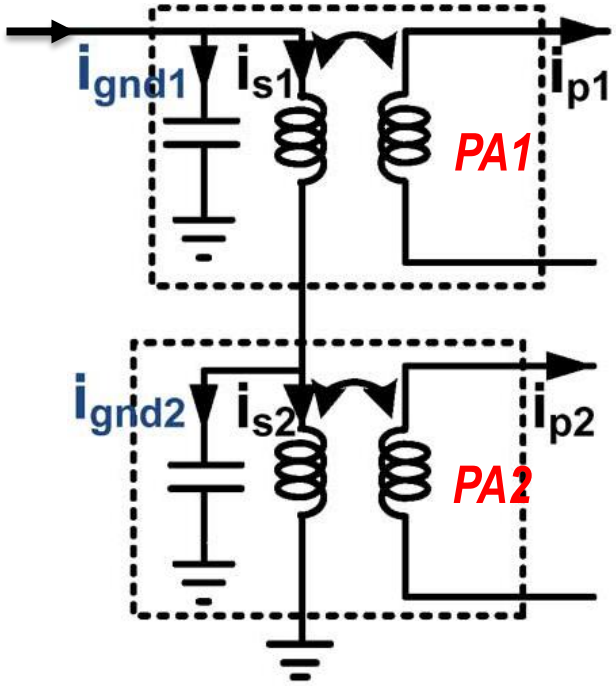




MODEL: parasitic estimation improvement (R,C)

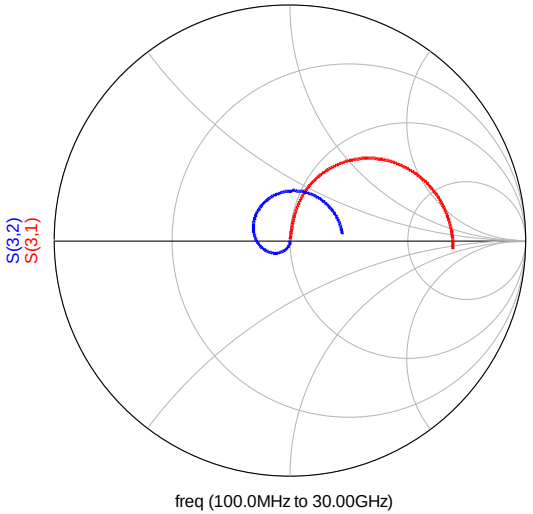
Output Network - Imbalanced Problem

- Transformer unbalanced problems



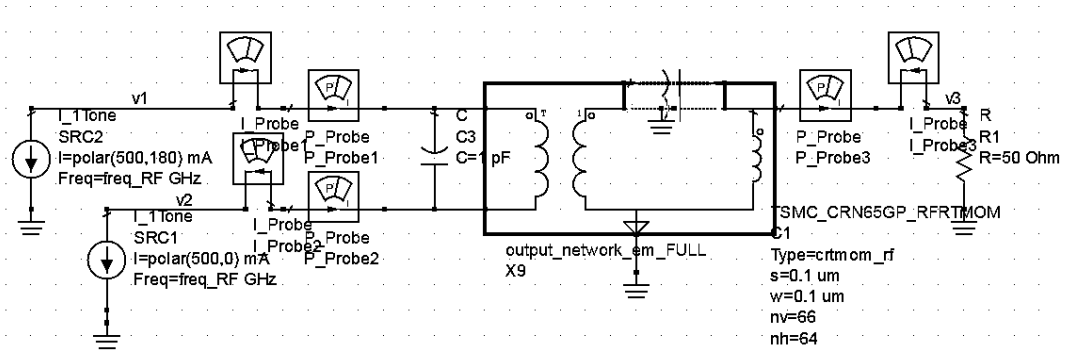
$$i_{S1} = i_{S2} + i_{gnd2}$$

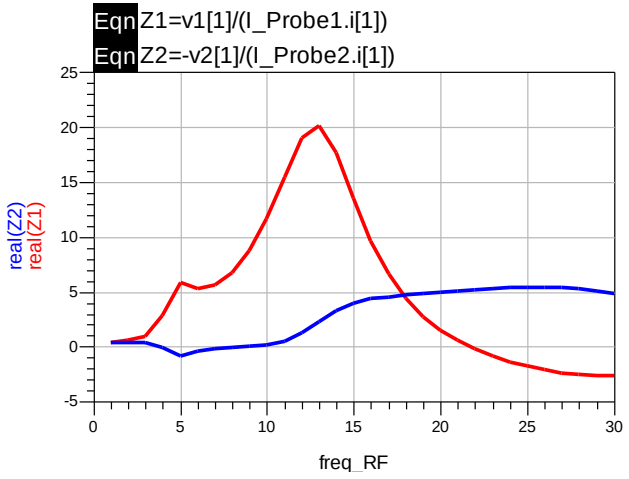
$$i_{p1} \neq i_{p2}$$



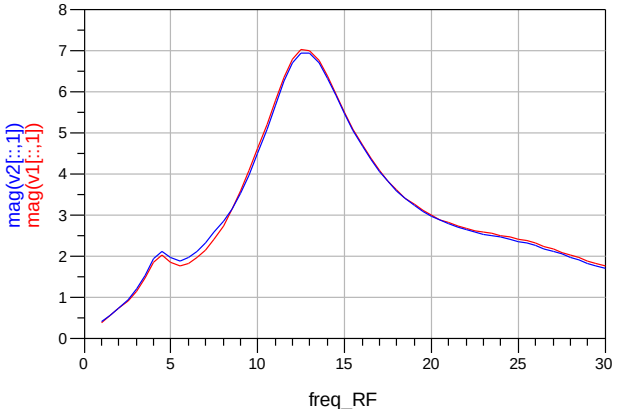
Ref: "Two-Way Current-Combining W-Band Power Amplifier in 65-nm CMOS", Qun Jane Gu, ZhiweiXu, and Mau-Chung Frank Chang

Output Network - Imbalanced Problem





If we put center-tap bypass and effective PA "C_{out}" to GND



Class J - Class AB Using a Capacitive Harmonic Termination

- Fundamental Impedance: loadline impedance R_L
  Second harmonic: $X_{out}/2$
- Trade-off: Larger Peak Voltage at Output Node