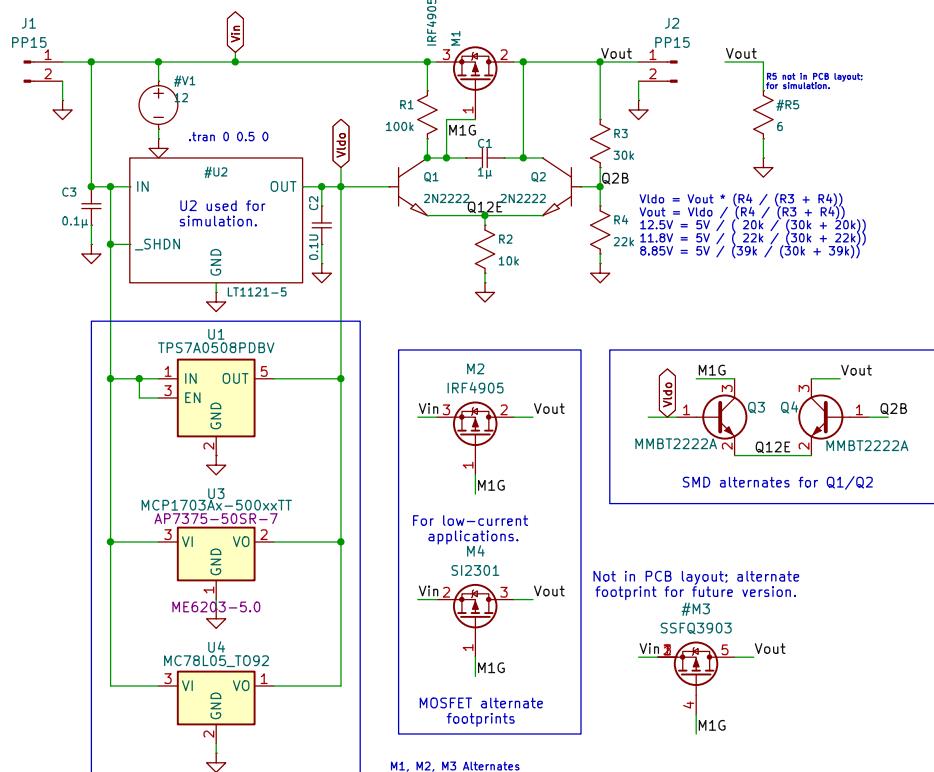


Trise test, Cen-Tech 69465, s/n 364381451
 Vin=13.24, Vout~12V, Iout=2.5A, Q3/Q4=MMBT2222A, U3=ME6203-5.0
 M1=IRF4905, TO-252, no heatsink
 black marked surface, dist., T0=22.0, T30=41.8, T60=52.8, T90=59.1, T120=62.5, T180=62.6, T240=64.4, T300=65.4, T360=66.6
 T30=50.8, T60=41.8, T90=37.8, T120=34.0, T180=29.6, T240=27.0, T300=25.2, T360=24.2
 PCB bottom under TO-263, dist=0.75", T0=20.6, T30=37.8, T60=47.4, T90=53.4, T120=56.8, T180=58.8, T240=60.3, T300=60.3, T360=62.6

ToDo:

- Add test points
- V_{ldo}
- Add solder pads GND, Vin, Vout
- Add LED for power-on
- Add R parallel to either R3, R4 to tweak output volts
- or use adjustable LDO



```

.SUBCKT irf4905 1 2 3
*****
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*****
***** Model generated on Jun 19, 96 *****
* Model Form: SPICE3 *
* Symmetric POWER MOS Model (Version 1.0) *
* External Node Designations *
* Node 1 -> Drain *
* Node 2 -> Gate *
* Node 3 -> Source *
M1 9 8 8 MM L=100u W=100u
* Default values used in MM:
* The voltage-dependent capacitances are
* not included. Other default values are:
* RS=0 RD=LD=0 CBD=0 CBS=0 CGBO=0
.MODEL MM PMOS LEVEL=1 IS=1e-32
+VDS=-3.53713 LAMBDA=0.00549583 KP=23.3701
+CGSO=0.84439e-05 CGDO=1e-11
RD 8 9 0.001265
D1 8 9 MD
.D1 8 9 MD
.MODEL MD D IS=1.29014e-08 RS=0.00297795 N=1.46717 BV=55
+IBV=0.00025 EG=1.2 XT=4 TT=0
+CJO=-3.56968e-09 VJ=1.17553 M=0.500933 FC=0.5
RDS 3 1 2.2e-06
RD 9 1 0.0001
RG 2 7 6
D2 5 4 MD1
* Default values used in MD1:
* RS=0 EG=1.11 XT=3.0 TT=0
* BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=-4.83772e-09 VJ=0.625334 M=0.543532 FC=1e-08
D3 5 0 MD2
* Default values used in MD2:
* EG=1.11 XT=3.0 TT=0 CJO=0
* BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=0.4 RS=3e-06
RL 5 10 1
F12 7 9 VF12 -1
VF12 4 0
EV16 10 0 9 7 1
CAP_11 10 6.08035e-09
F14 11 6 1
VF14 11 6 1
RCAP 6 0 1
D4 6 0 MD3
* Default values used in MD3:
* EG=1.11 XT=3.0 TT=0 CJO=0
* RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=0.4
.ENDS

```

M1, M2, M3 Alternates
 PJD70P03_L2_00001, TO-252AA, <https://www.panjil.com.tw/upload/datasheet/PJD70P03.pdf>
 G4OP03K, TO-252, <https://www.gofordsemi.com/upload/cn/prod/G4OP03K.pdf>
 SSFQ3903, SOP-8, <https://goodarksemi.com/docs/datasheets/mosfets/SSFQ3903.pdf>
 SL4407A, SOP-8, <https://mm.digkey.com/volume0/opasdata/d220001/medias/documents/7181/SL4407A%20SOP-8.PDF>
 MCU6D0P03L-TP, TO-252, [https://www.mccsemi.com/pdf/Products/MCU6D0P03L\(DPAK\).pdf](https://www.mccsemi.com/pdf/Products/MCU6D0P03L(DPAK).pdf)

References:
<https://www.ggrp.com/limiter.jpg>
 via https://groups.io/g/QRPLabs/topic/qmx_battery/111670594
<http://www.nd6t.com/qrp/VLDO.htm>

Based on
[https://www.ggrp.com/limiter.jpg \(G4COL\)](https://www.ggrp.com/limiter.jpg)
<http://www.nd6t.com/qrp/VLDO.htm>
 Artwork (C) 2025, AC8ES

Sheet: /
 File: vldo.kicad_sch

Title: VLDO (Very Low Dropout Regulator)

Size: USLetter Date: 2025-11-16
 KiCad E.D.A. 9.0.6

Rev: 0.1
 Id: 1/1