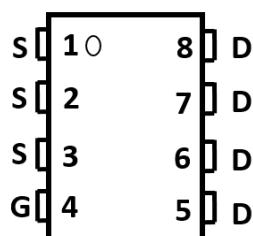
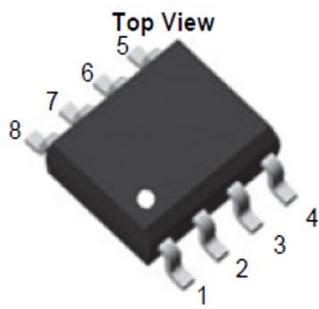
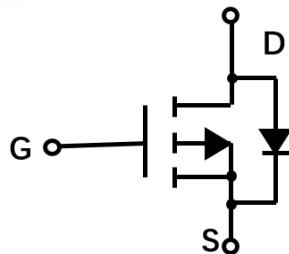


P-Channel Enhancement Mode Field Effect Transistor



SOP-8



Product Summary

- V_{DS} -30V
- I_D -12A
- $R_{DS(ON)}$ (at $V_{GS}=-20V$) <11mohm
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <13mohm
- $R_{DS(ON)}$ (at $V_{GS}=-6V$) <17mohm
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <27mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Power management
- Load switch

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	-30	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	-12	A
Pulsed Drain Current ^A	I_{DM}	-55	A
Single Pulse Avalanche Energy ^B	E_{AS}	105	mJ
Total Power Dissipation @ $T_A=25^\circ\text{C}$ ^C	P_D	3.2	W
Thermal Resistance Junction-to-Ambient @ Steady State ^D	$R_{\theta JA}$	39	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=-30\text{V}, V_{\text{GS}}=0\text{V}, T_c=25^\circ\text{C}$			-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 20\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-1.2	-1.7	-2.8	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=-20\text{V}, I_{\text{D}}=-12\text{A}$		9.0	11	$\text{m}\Omega$
		$V_{\text{GS}}=-10\text{V}, I_{\text{D}}=-10\text{A}$		10.2	13	
		$V_{\text{GS}}=-6.0\text{V}, I_{\text{D}}=-8\text{A}$		12.3	17	
		$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-8\text{A}$		16	27	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=-12\text{A}, V_{\text{GS}}=0\text{V}$		-0.8	-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=-15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		2152		pF
Output Capacitance	C_{oss}			308		
Reverse Transfer Capacitance	C_{rss}			242		
Switching Parameters						
Total Gate Charge	Q_g	$V_{\text{GS}}=-10\text{V}, V_{\text{DS}}=-15\text{V}, I_{\text{D}}=-12\text{A}$		40.1		nC
Gate Source Charge	Q_{gs}			8.4		
Gate Drain Charge	Q_{gd}			8.6		
Reverse Recovery Charge	Q_{rr}	$I_F=-12\text{A}, dI/dt=100\text{A/us}$		7.8		ns
Reverse Recovery Time	t_{rr}			18		
Turn-on Delay Time	$t_{\text{D(on)}}$			8		
Turn-on Rise Time	t_r	$V_{\text{GS}}=-10\text{V}, V_{\text{DD}}=-15\text{V}, I_{\text{D}}=-1\text{A}, R_{\text{GEN}}=2.5\Omega$		19		ns
Turn-off Delay Time	$t_{\text{D(off)}}$			75		
Turn-off Fall Time	t_f			46		

A. Pulse Test: Pulse Width $\leq 300\text{us}$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

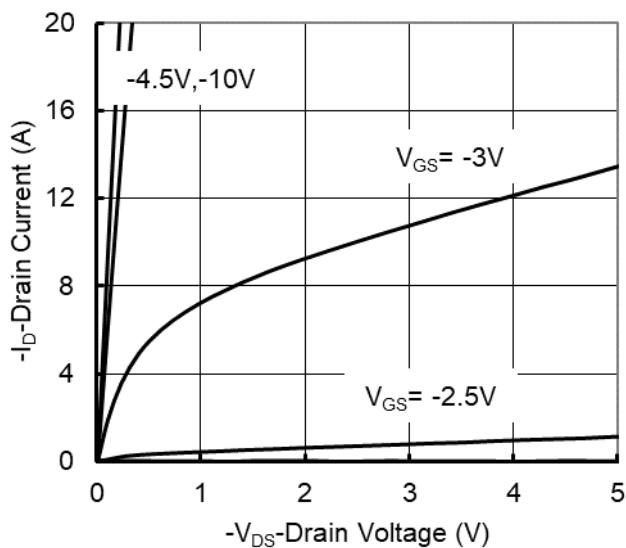


Figure 1. Output Characteristics

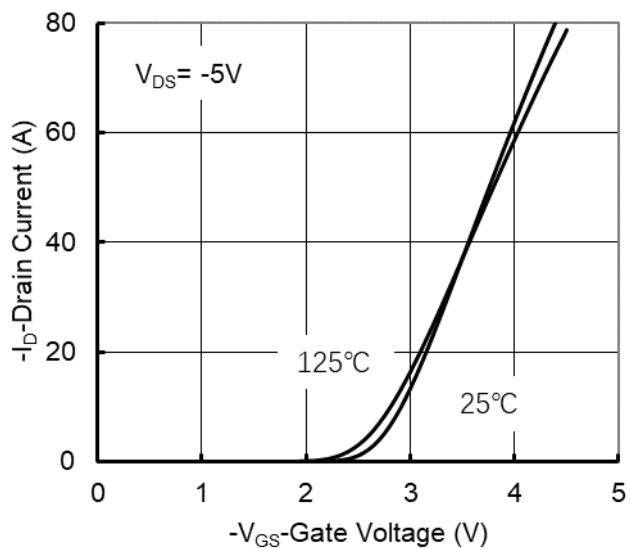


Figure 2. Transfer Characteristics

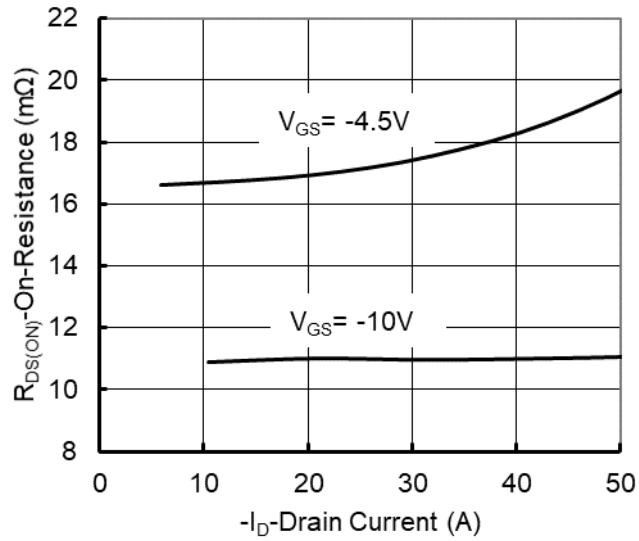


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

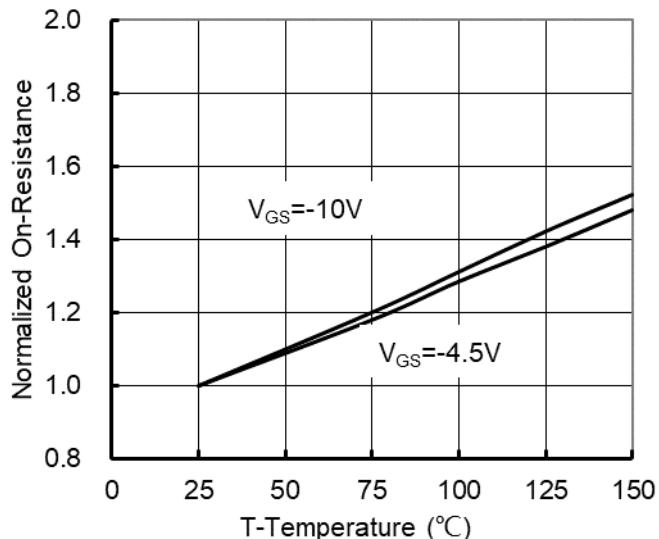


Figure 4. On-Resistance vs. Junction Temperature

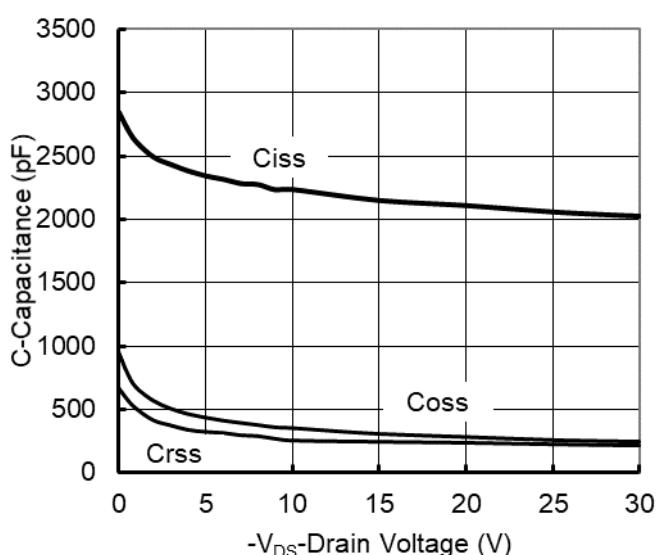


Figure 5. Capacitance Characteristics

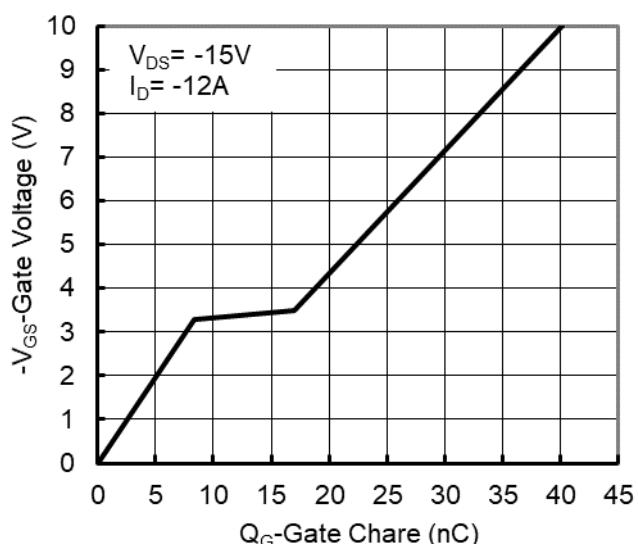


Figure 6. Gate Charge

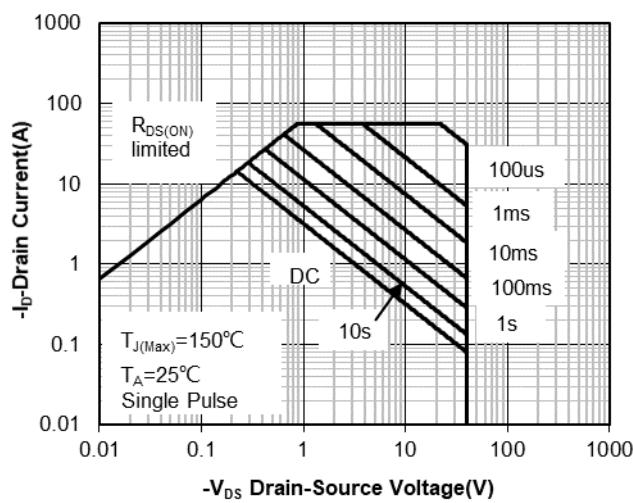


Figure 7. Safe Operation Area

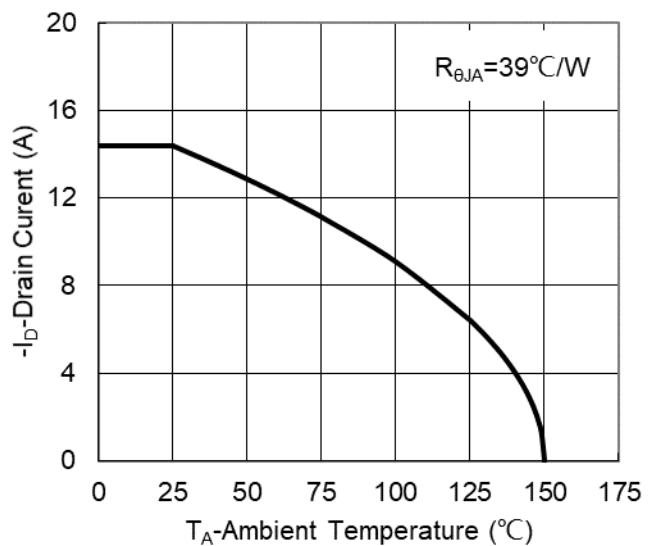


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

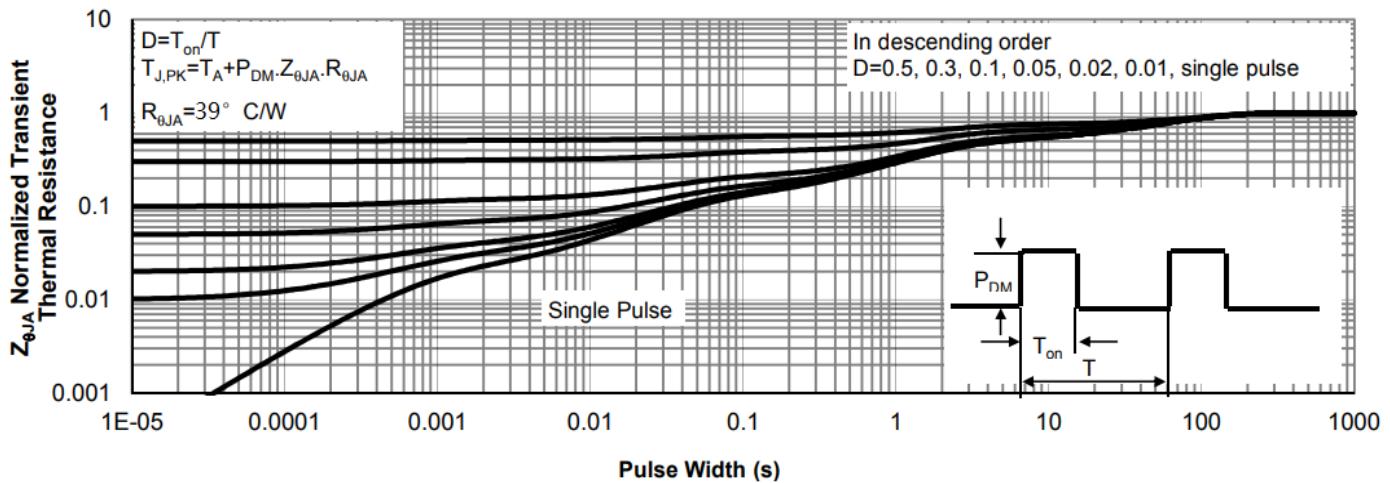
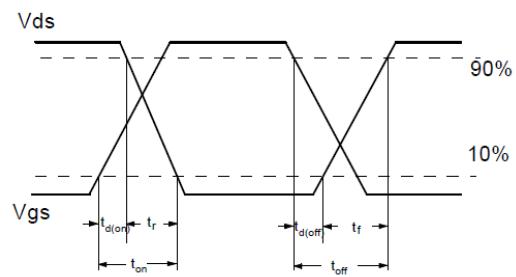
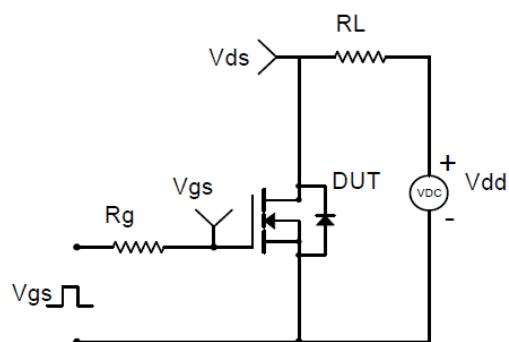
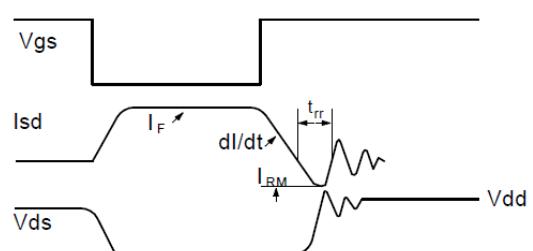
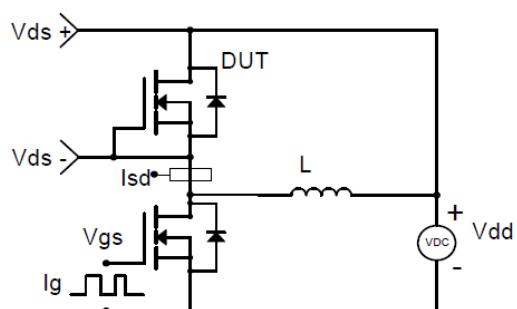


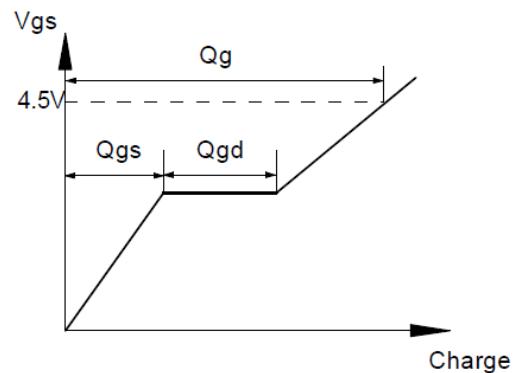
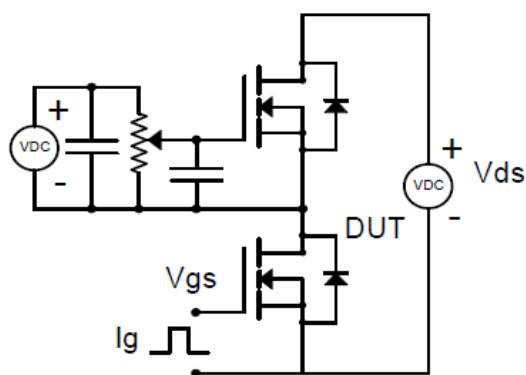
Figure 9. Normalized Maximum Transient Thermal Impedance



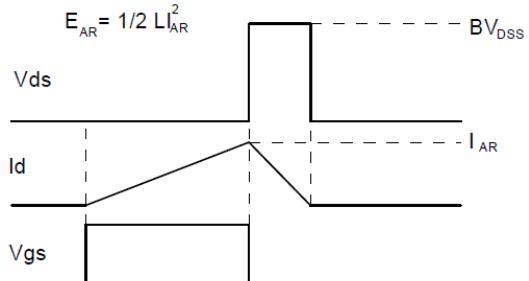
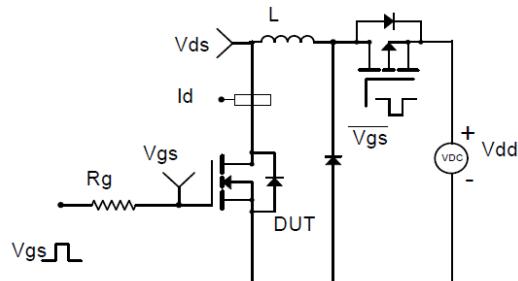
Resistive Switching Test Circuit & Waveforms



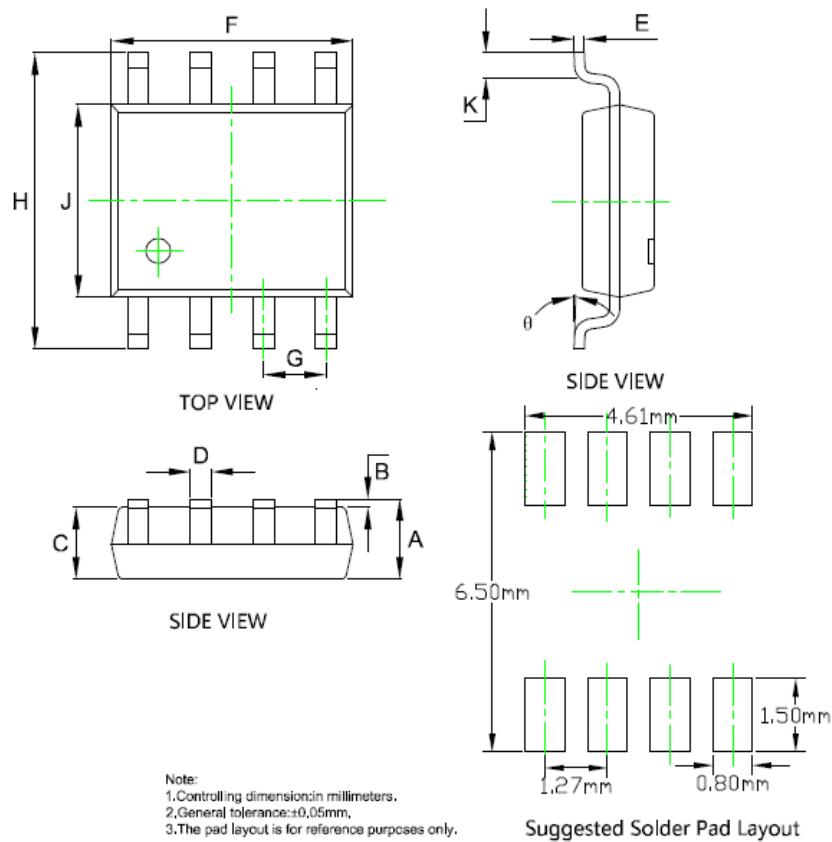
Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

■ SOP-8 Package information

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°