반도체 소자 측정 및 분석기법

Ch.2 Carrier and Doping Density

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2.1 Introduction

- **Measurement of 'carrier density' and 'doping density'**
  - carrier density: C-V, spreading resistance, Hall effect
  - doping density: secondary ion mass spectrometry (SIMS)

2.2 Capacitance-Voltage (C-V)

2.2.1 Differential Capacitance

① **Schottky barrier diode, one-sided junction (p^+n or n^+p)** ← sample type

- C-V technique: width of a reverse-biased space-charge region (scr) depends on the applied voltage
  i.e., dc bias V produces a space-charge region of width W

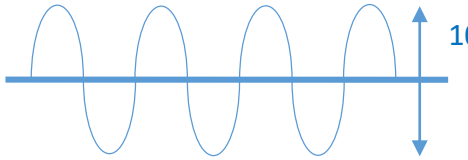
- differential or small signal capacitance in Fig.2.1(b)

$$C = \frac{dQ_m}{dV} = -\frac{dQ_S}{dV} \qquad (2.1)$$

dQ_m: metal charges
dQ_s: semiconductor charges

Small-signal (AC) → response time

DC → operating region



10~20mV@f=10kHz to 1MHz

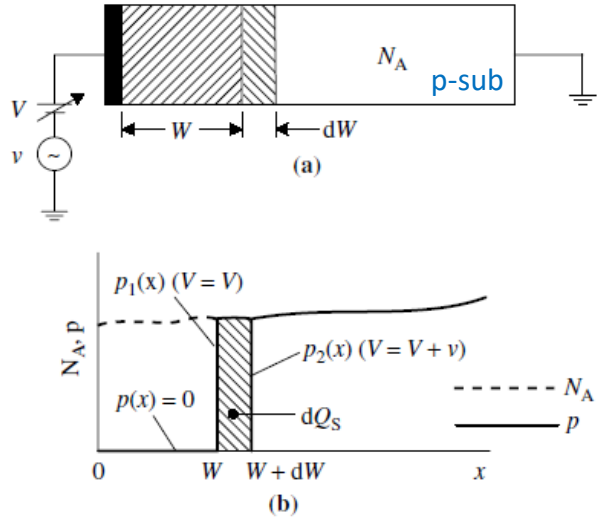


Fig. 2.1 (a) A reverse-biased Schottky diode, and (b) the doping density and majority carrier density profiles in the depletion approximation.

2.2.1 Differential Capacitance

- Semiconductor charge $$Q_s = qA\int_0^W (p - n + N_D^+ - N_A^-)dx \approx -qA\int_0^W N_A dx \qquad (2.2)$$

- From (2.1) and (2.2), $$C = -\frac{dQ_s}{dV} = qA\frac{d}{dV}\int_0^W N_A\,dx = qAN_A(W)\frac{dW}{dV} \quad [\mathrm{F}] \qquad (2.3)$$

- Capacitance of a reverse-biased junction at parallel plate capacitor $$C = \frac{K_S\varepsilon_0 A}{W} \qquad (2.4) \qquad \frac{dC}{dV} = -\frac{K_S\varepsilon_0 A}{W^2}\frac{dW}{dV}$$

- Differentiating (2.4) with V and substituting dW/dV into (2.3)

$$N_A(W) = -\frac{C^3}{qK_S\varepsilon_0 A^2 dC/dV} = \frac{2}{qK_S\varepsilon_0 A^2 d(1/C^2)/dV} \qquad (2.5)$$

→ 'doping density' is obtained from the slope dC/dV of a C-V curve or from the slope $d(1/C^2)/dV$ of $1/C^2$-V curve

② MOS capacitor

- space charge region width, W excluding dielectric capacitance

$$W = K_S\varepsilon_0 A\left(\frac{1}{C} - \frac{1}{C_{ox}}\right) \qquad (2.7)$$

C_{ox}: oxide capacitance

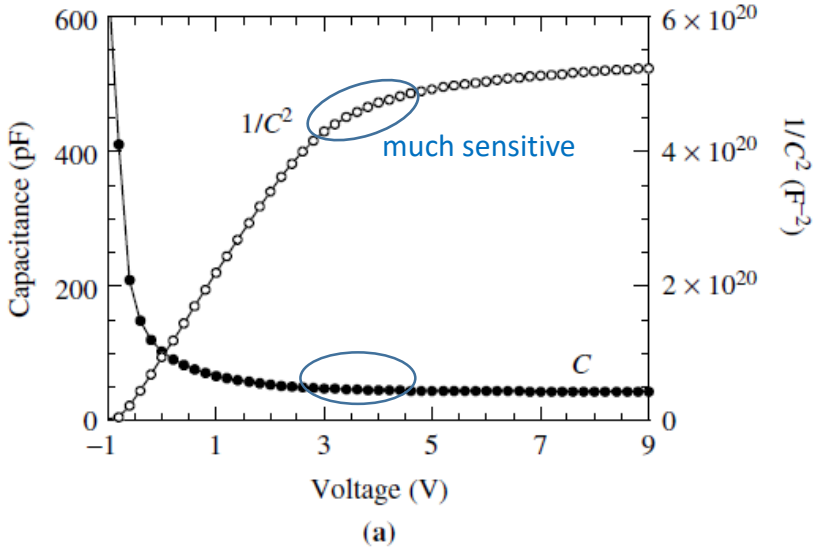
2.2.1 Differential Capacitance

- **'Differential capacitance-voltage profiling technique'** determines the '**carrier density profile'**, not the doping density
  Actually measured is an apparent or effective carrier density

$$p(W) = -\frac{C^3}{qK_S\varepsilon_0 A^2 dC/dV} = \frac{2}{qK_S\varepsilon_0 A^2 d(1/C^2)/dV} \qquad (2.8)$$

$$W = \frac{K_S\varepsilon_0 A}{C} \qquad (2.9)$$

- **d(1/C²)/dV is preferred than dC/dV**
  - at d(1/C²)/dV, it is immediately obvious that the carrier density is not uniform with a discontinuity at around 3V



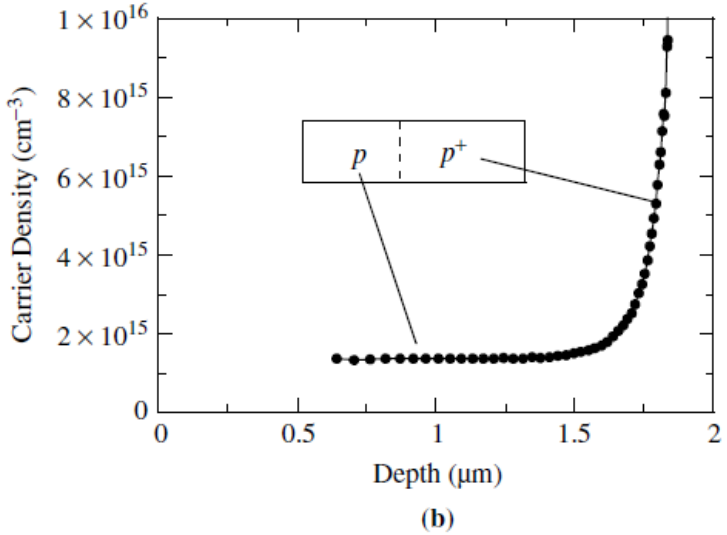


Fig. 2.3 (a) $C-V$ and $1/C^2-V$ curves of a Si n^+p diode, (b) p(x)-W profile.

2.2.1 Debye length L_D

- **Debye length:** the **distance over which a charge imbalance is neutralized by majority carriers** under steady-state or equilibrium conditions

$$L_D = \sqrt{\frac{kTK_S\varepsilon_0}{q^2(p+n)}} \qquad (2.11)$$

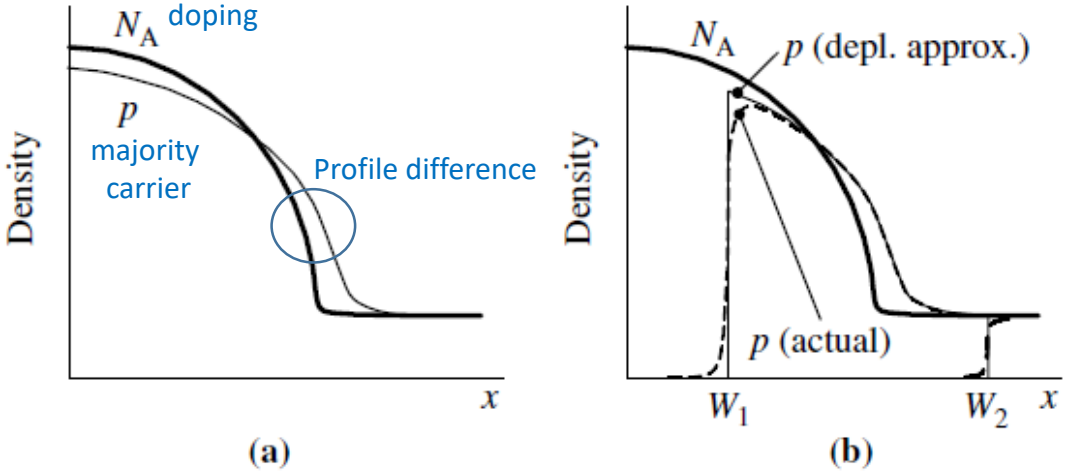


Fig. 2.4 A schematic representation of the doping and majority carrier density profiles of a non-uniformly doped layer. (a) zero-biased junction, (b) reverse-biased junction showing the doping density profile, the majority carrier profiles in the depletion approximation and the actual majority carrier profiles for two reverse-bias voltages.

- Relationship between **the measured majority carrier density** and **the doping density**[16]

$$N_A = p(x) - \frac{kTK_S\varepsilon_0}{q^2}\frac{d}{dx}\left(\frac{1}{p(x)}\frac{dp(x)}{dx}\right) \qquad (2.12)$$

2.2.3 Maximum-Minimum MOS-C Capacitance

- **'Max-min capacitance method'** is useful for '**uniformly doped substrates**' but not accurate for non-uniform doping densities
  - interface traps play no role in this measurement if gate voltage is sufficiently high for the device to be in strong inversion

- **The general MOS-C capacitance**

$$C = \frac{C_{ox}C_s}{C_{ox}+C_s} \qquad (2.15)$$

$C_s = K_s\varepsilon_0 A/W$: semiconductor capacitance

$$W = W_{inv} = \sqrt{\frac{2K_s\varepsilon_0\emptyset_{s,inv}}{qN_A}} \qquad (2.16a)$$

$$W = W_{2\emptyset F} = \sqrt{\frac{2K_s\varepsilon_0 2\emptyset_F}{qN_A}} \qquad (2.16b)$$

$\phi_{s,inv}$: surface potential in strong inversion, $2\phi_F < \phi_{s,inv} < 2\phi_F + 4kT/q$

- (2.15) and (2.16b) lead to

assuming uniform doping

$$N_A = \frac{4\emptyset_F}{qK_s\varepsilon_0 A^2}\frac{C_{2\emptyset_F}^2}{\left(1-C_{2\emptyset_F}/C_{ox}\right)^2} \qquad (2.17)$$

$$N_A = \frac{4\emptyset_F}{qK_s\varepsilon_0 A^2}\frac{C_{inv}^2}{\left(1-C_{inv}/C_{ox}\right)^2} = \frac{4\emptyset_F}{qK_s\varepsilon_0 A^2}\frac{R^2C_{ox}^2}{(1-R)^2} \qquad (2.18)$$

$R = C_{inv}/C_{ox}$

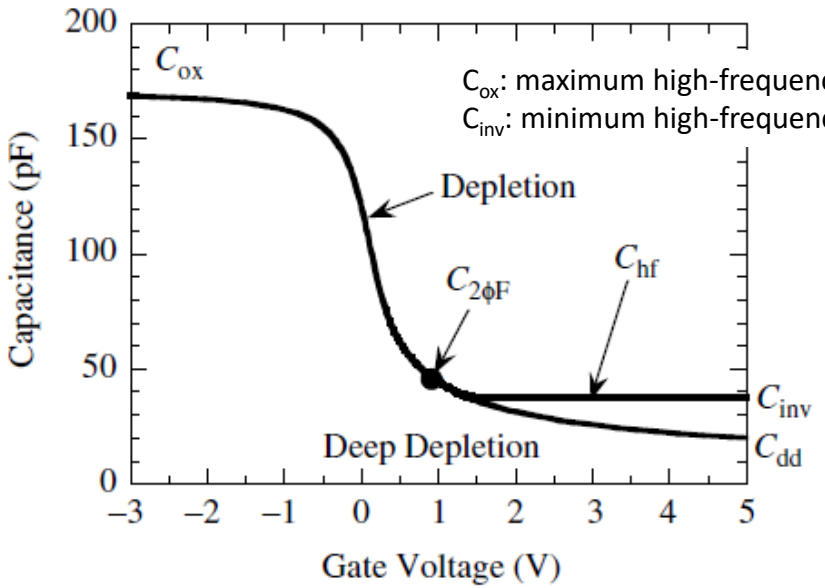
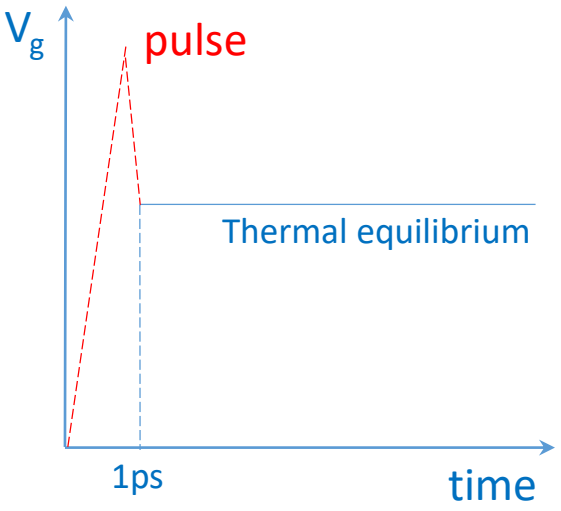


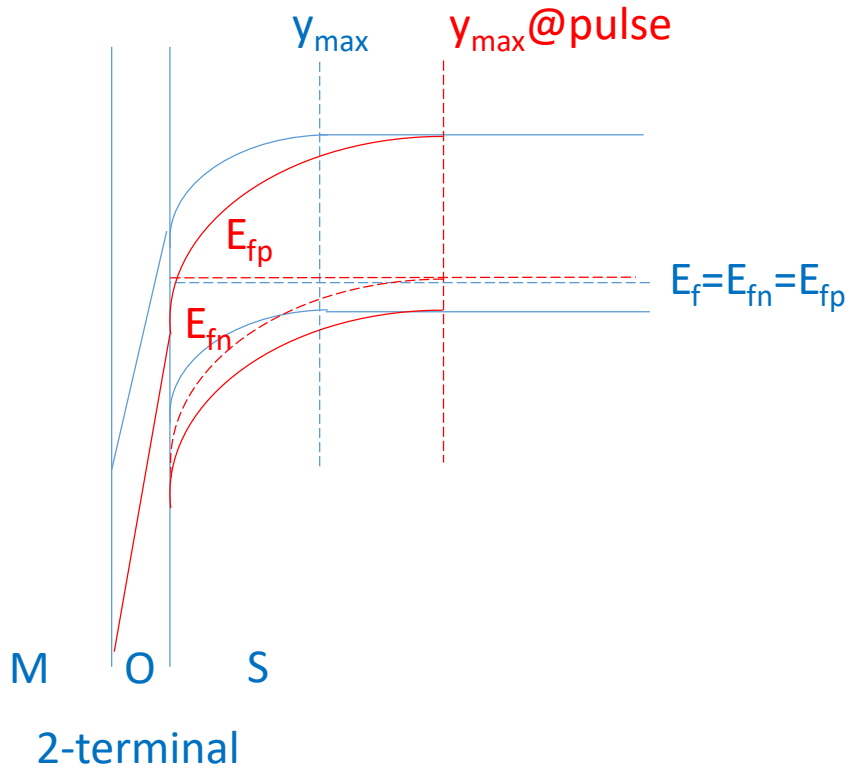
Fig. 2.9 $C-V_G$ curve for an SiO_2/Si MOS capacitor. $N_A = 10^{17}$ cm^{-3}, $t_{ox} = 10$ nm, $A = 5 \times 10^{-4}$ cm^2.

Deep depletion and Quasi-Fermi level

Quasi-Fermi levels, E_{fn} and E_{fp}

- **Definition: the separated Fermi levels for e^- and h^+** due to slow generation-recombination process is inefficient to establish equilibrium between electrons and holes ($pn=n_i^2$).
- The gradient of e^- quasi-Fermi potential drives the electron current, and the gradient of h^+ quasi-Fermi potential drives the hole current.





$$n = n_i e^{(E_{fn}-E_i)/kT}$$

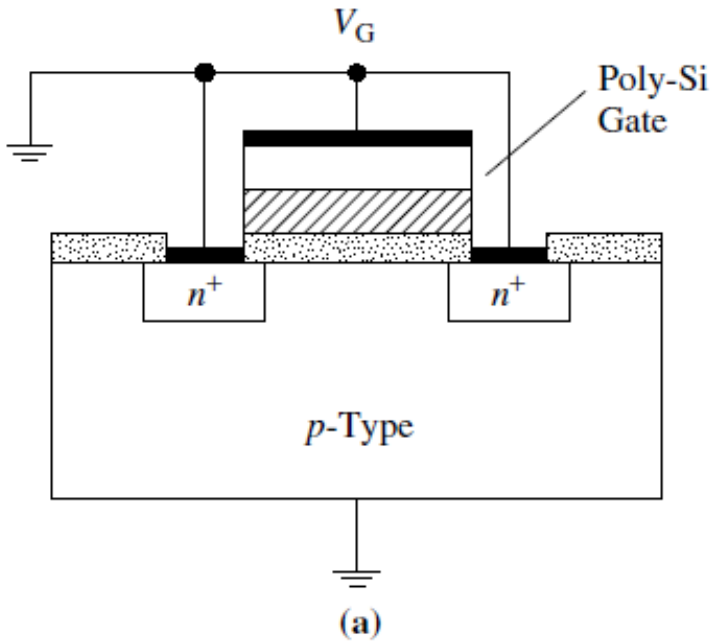
$$p = n_i e^{(E_i-E_{fp})/kT}$$

$$pn = n_i^2 e^{q(\phi_p-\phi_n)/kT} < n_i^2$$

2.2.3 Doping density of Poly-Si gate

- **Doping density of poly-Si gate can be determined by the C_{inv}/C_{max} method**
  - source/drain/substrate form one continuous n-layer (MOSFET → MOSCAP)
  - gate voltage is applied above the threshold voltage

- it takes a **'significant gate voltage'** to invert the gate and the gate oxide may break down before inversion is reached



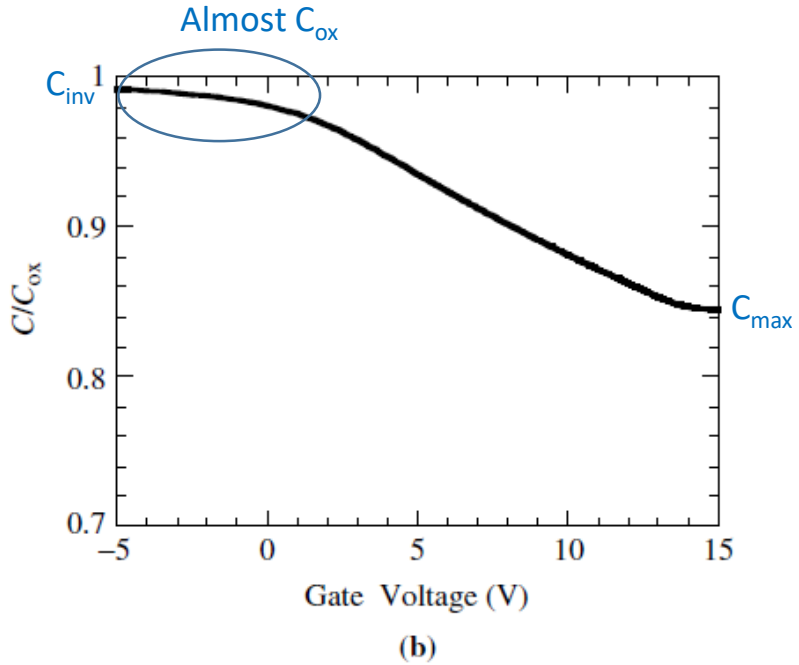


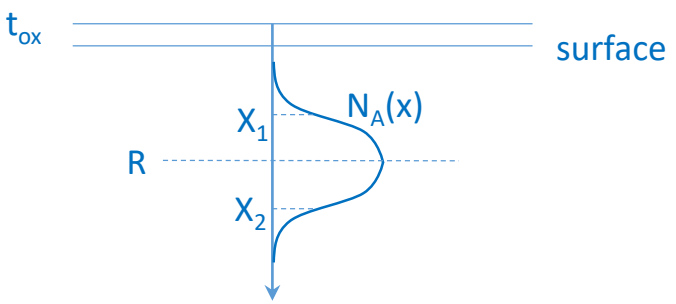
Fig. 2.11 (a) MOSFET connection to determine the doping density of the gate, (b) resulting $C-V$ curve calculated, $N_D = 5 \times 10^{19}$ cm^{-3}, $t_{ox} = 10$ nm.

2.2.4 Integral Capacitance (1/2)

- **'Integral capacitance technique'**[50]
  - integrating a portion of the **pulsed MOS-C C-V** curve to obtain a **'partial implant dose P_Φ'.**
  - chosen dose includes the doping density between $x=x_1$ and $x=x_2$ and contains most of the implanted layer

$$P_\emptyset = \int_{x1}^{x2} N_A(x)dx = \frac{1}{qA}\int_{V_1}^{V_2} C dV \qquad (2.20)$$

$P_\emptyset$: calculated; C: measured; $\int_{V_1}^{V_2} C dV$: Charge difference, ΔQ



- **'projected range R or implant depth'** at the density peak

$$R = t_{ox} + \frac{1}{P_\emptyset}\int_{x1}^{x2} xN_A(x)dx = \frac{K_s\varepsilon_0}{qP_\emptyset}(V_2 - V_1) + (1 - K_s/K_{ox})t_{ox} \qquad (2.21)$$

R: calculated; $P_\emptyset$: calculated

2.2.4 Integral Capacitance (2/2)

- **Another MOS capacitor integral[51] gives the implanted dose (Fig.2.12)**
  - but gap (Fig.2.12(b)) between extracted C-V of deep depletion(**by different C-V including L_D effect**, symbols) vs. simulated C-V(by integral C-V, lines)

→ just **simple integration C-V_G doesn't yield the true doping densities**

- to increase the accuracy of **ΔQ**, **P_Φ** in integral technique

① **ΔQ** is obtained by integrating the **deep depletion** C-V_G curve
- completely eliminating inversion charge effect

② **P_Φ** by integrating the two C-V_G (**ref and test**) curves at the same accumulation capacitances to the same deep-depletion capacitance

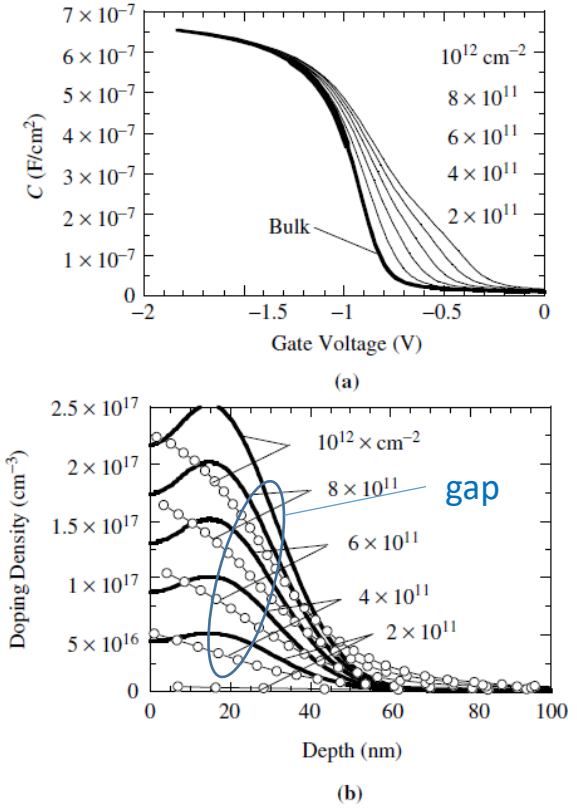


Fig. 2.12 (a) Deep depletion $C-V_G$ curves as a function of boron ion implant dose at 40 keV into p-Si substrates, $t_{ox} = 4.1$ nm, (b) doping profiles determined by conventional $C-V$ profiling (symbols) and simulation (lines). The "bulk" curve in (a) is for the unimplanted substrate. After ref. 51.

2.3 Current-Voltage (I-V)

- **Limitation of differential capacitance(0.1-1 MHz)**
  - small-geometry MOSFETs difficult to measure C-V because the capacitance is extremely small

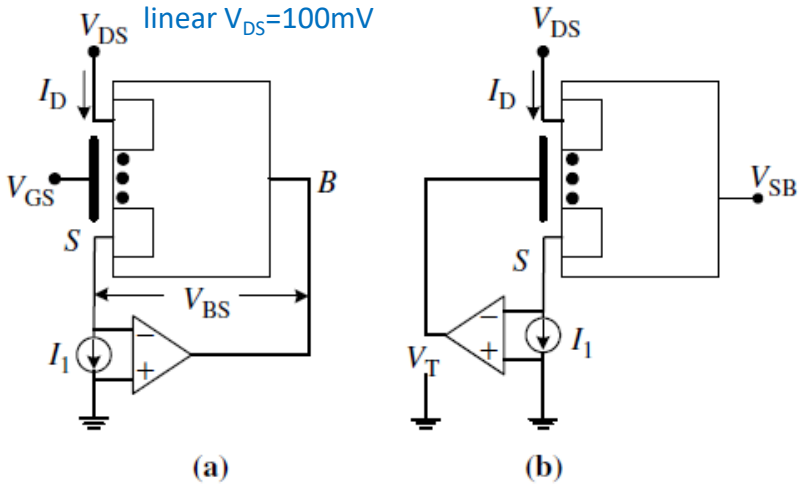
2.3.1 'Substrate voltage(V_{SB})-gate voltage(V_{GS}) method'[66-67]

- V_{SB} forces the space-charge region under the gate to extend into the substrate
- **inversion charge density** is held **constant**, approximated by a constant I_D, by adjusting V_{GS} whenever V_{SB} is changed

$$p(W) = \frac{K_{ox}\varepsilon_0}{qK_s t_{ox}^2}\frac{d^2 V_{SB}}{dV_{GS}^2} \qquad (2.25)$$

$$W = \frac{K_s\varepsilon_0}{C_{ox}}\frac{d\,V_{SB}}{dV_{GS}} \qquad (2.26)$$

When V_{GS} is changed, the op amp adjusts it output voltage (V_{SB}) to maintain I_D=I_1=const.



When V_{SB} is changed, the output of the op amp gives the threshold voltage(V_{GS}) directly. Typically I_1≈1μA=const.

Fig. 2.15 Operational amplifier circuit for (a) the MOSFET substrate/gate voltage method, (b) the MOSFET threshold voltage method.

2.3 Current-Voltage (I-V)

2.3.2 'Threshold voltage method'[73-75]

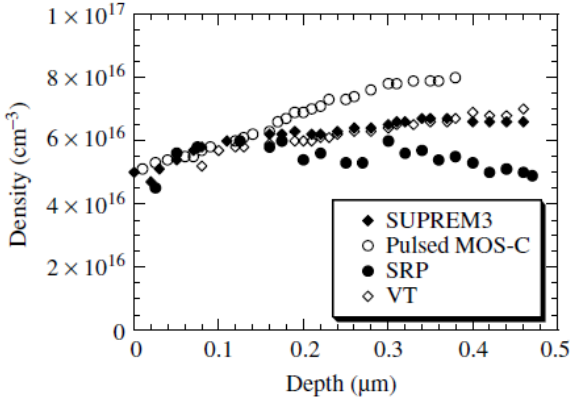
- the threshold voltage is measured as a function of substrate bias($V_{SB} > 0$ for nFET),

$$V_T = V_{FB} + 2\emptyset_F + \frac{\sqrt{2qK_S\varepsilon_0 N_A(2\emptyset_F+V_{SB})}}{C_{ox}} = V_{FB} + 2\emptyset_F + \gamma\sqrt{2\emptyset_F + V_{SB}} \quad (2.27)$$

Function of N_A (in γ) Function of N_A (in $2\emptyset_F$)

$$N_A = \frac{\gamma^2 C_{ox}^2}{2qK_S\varepsilon_0} \quad (2.28)$$

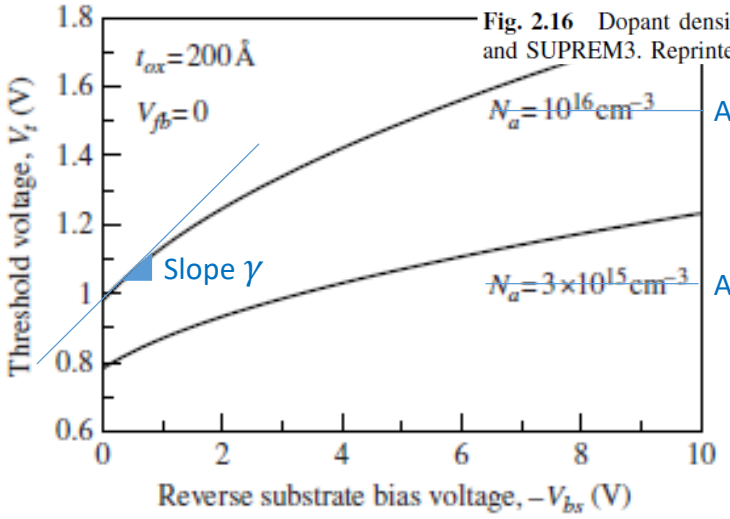
$$\gamma = \sqrt{(2qK_S\varepsilon_0 N_A)}/C_{ox}$$
$$\emptyset_F = (kT/q)\ln(N_A/n_i)$$



- **iteration to obtain doping density N_A profile**
  - ① plot V_T versus $(2\emptyset_F+V_{SB})^{1/2}$ using $2\emptyset_F$=0.6V
  - ② take the slope γ and find N_A
  - ③ find new $\emptyset_F$ → replot ①

- profile depth

$$W = \sqrt{\frac{2K_S\varepsilon_0(2\emptyset_F+V_{SB})}{qN_A}} \quad (2.29)$$



Assuming non-uniform

Assuming non-uniform

[ref] Y. Taur, Fundamentals of Modern VLSI Devices

Fig. 2.16 Dopant density profiles determined by MOSFET threshold voltage, SRP, pulsed $C-V$, and SUPREM3. Reprinted after ref. 73 by permission of IEEE (© 1991, IEEE).

Figure 3.14. Threshold-voltage variation with reverse substrate bias for two uniform substrate doping concentrations.

2.4 Measurement errors and precautions

2.4.1 Debye Length making measurement errors

- Debye Length: 'mobile majority carriers' do not follow the profile of the 'dopant atoms' if the dopant density profile varies spatially over distances less than the Debye length
- majority carriers are more smeared out than the dopant atoms

→ **inability to profile closer than about $3L_D$** from the surface using MOS devices

▪ **Dopant profiling depth limitations**

- W_{BD}: upper profile depth limit by semiconductor bulk breakdown
- W_{0V}: zero-bias scr width of Schottky diodes or pn junction
- $3L_D$: Debye Length limitation from MOSCAP or MOSFET surface

→ providing the dose and energy limits of Si and III-V

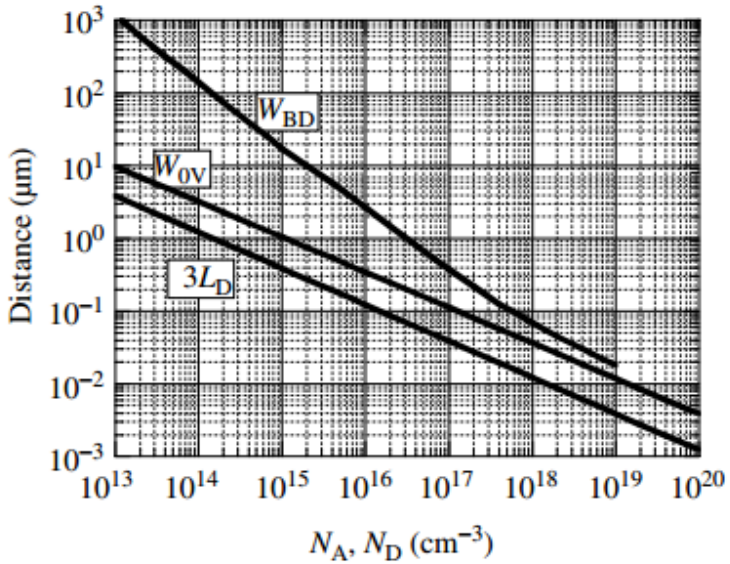


Fig. 2.17 Spatial profiling limits. The "3 L_D" line is the lower limit for conventional MOS-C profiling, the zero bias "W_{0V}" line is the lower limit for pn and Schottky diode profiling, and the "W_{BD}" line is the upper profile limit governed by bulk breakdown.

2.4 C-V measurement equipment

- **Agilent 4284A LCR meter**
  - test frequency range: 20Hz to 1MHz
  - accuracy: ±0.01%

R_s accuracy
When D_x (measured D value) ≤ 0.1

R_s accuracy is given as

$$X_x \times D_e \quad [\Omega]$$

$$X_x = 2\pi f L_x = \frac{1}{2\pi f C_x}$$

where:

X_x = Measured X value [Ω]
C_x = Measured C value [F]
L_x = Measured L value [H]
D_e = Absolute D accuracy
f = Test frequency [Hz]

Relative Accuracy
Relative accuracy includes stability, temperature coefficient, linearity, repeatability, and calibration interpolation error. Relative accuracy is specified when all of the following conditions are satisfied:

1. Warm-up time: ≥ 30 minutes

2. Test cable length: 0 m, 1 m, 2 m, or 4 m (Agilent 16048 A/B/D/E)

For 2 m or 4 m cable length operation, test signal voltage and test frequency are set according to Figure 1-1. (2 m and 4 m cable can only be used when Option 4284A-006 is installed.)

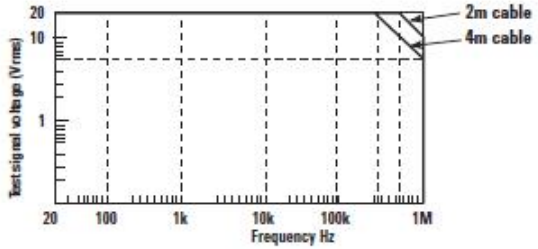


Figure 1-1. Test signal voltage and test frequency upper limits to apply relative accuracy to 2 m and 4 m cable length operation

3. OPEN and SHORT corrections have been performed. calibration

4. Bias current isolation: Off

(For accuracy with bias current isolation, refer to supplemental performance characteristics.)

5. Test signal voltage and DC bias voltage are set according to Figure 1-2.

6. The optimum measurement range is selected by matching the DUT's impedance to the effective measuring range. (For example, if the DUT's impedance is 50 kΩ, the optimum range is the 30 kΩ range.)

Range 1: Relative accuracy can apply.

Range 2: The limits applied for relative accuracy differ according to the DUT's DC resistance. Three dotted lines show the upper limits when the DC resistance is 10 Ω, 100 Ω and 1 kΩ.

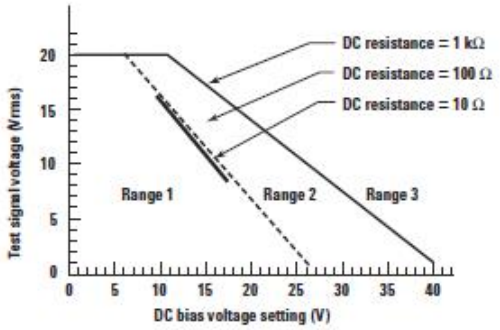


Figure 1-2. Test signal voltage and DC bias voltage upper limits apply for relative accuracy

[ref] Agilent 4284A Data sheet

2.4 C-V measurement equipment

DC Bias Settling Time (DC - operation region)

When DC bias is set to on, add the settling time listed in the following table to the measurement time. This settling time does not include the DUT charge time.

Test frequency (f_m)	Bias current isolation On	Off
20 Hz ≤ f_m < 1 kHz	210 ms	20 ms
1 kHz ≤ f_m < 10 kHz	70 ms	20 ms
10 kHz ≤ f_m ≤ 1 MHz	30 ms	20 ms

Sum of DC bias settling time plus DUT (capacitor) charge time is shown in the following figure.

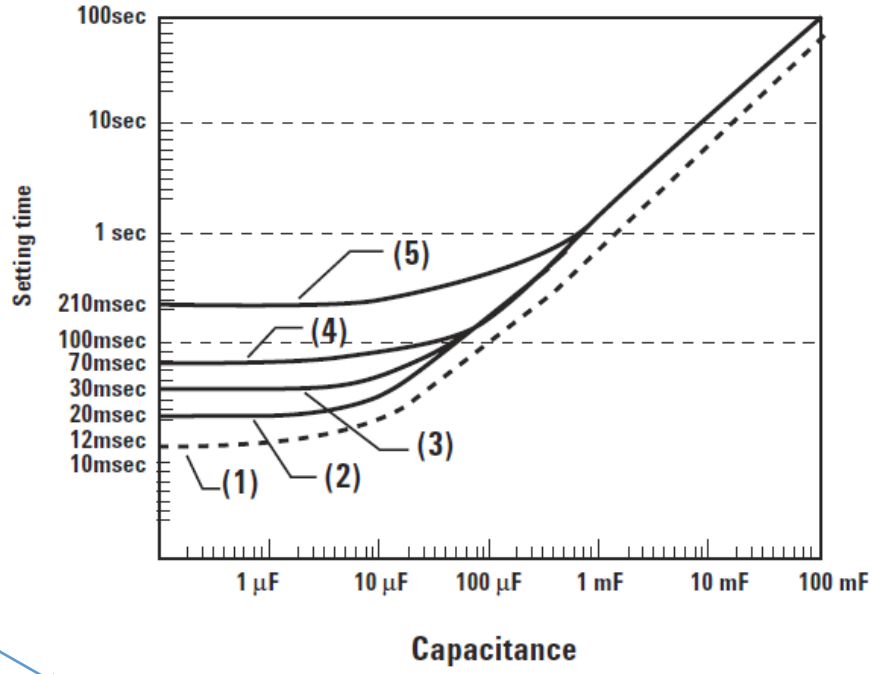
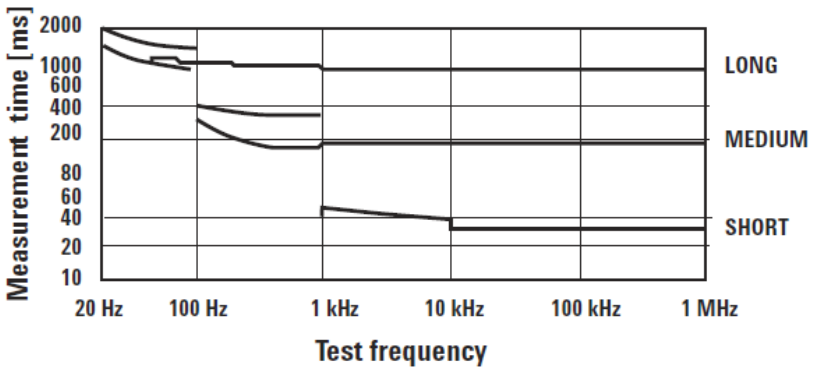


Figure 1-6. Measurement time

Measurement Time (AC - small signal)

Typical measurement times from the trigger to the output of EOM at the handler interface. (EOM: end of measurement)

Integration time	Test frequency 100 Hz	1 kHz	10 kHz	1 MHz
SHORT	270 ms	40 ms	30 ms	30 ms
MEDIUM	400 ms	190 ms	180 ms	180 ms
LONG	1040 ms	830 ms	820 ms	820 ms



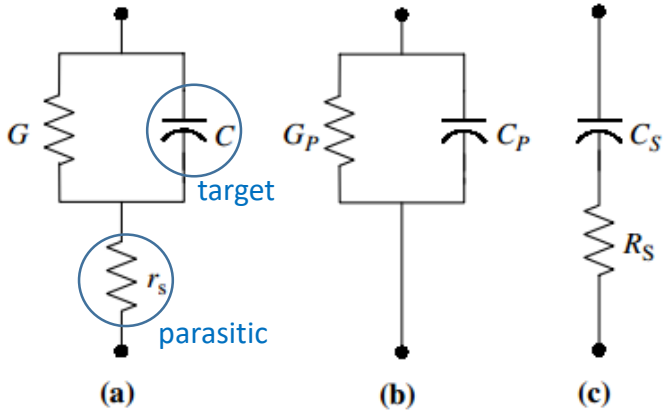
It seems that 4284 is not able to measure deep depletion,
because sum of DC bias settling time and DUT charge time is too slow (>10ms).

[ref] Agilent 4284A Data sheet

2.4 C-V measurement principle (1/2)

2.4.2 Series Resistance

- **'pn or Schottky diode'** consists of a junction capacitance *C*, a junction conductance *G*, and a series resistance r_s
- G governs the junction leakage current
- r_s depends on the bulk wafer resistivity and on the contact resistances



(b) Parallel equivalent circuit (measured, r_s term in C_P), $\omega=2\pi f$

$$C_P = \frac{C}{(1+r_S G)^2+(\omega\, r_S C)^2}; \quad G_P = \frac{G(1+r_S G)+r_S(\omega\, C)^2}{(1+r_S G)^2+(\omega\, r_S C)^2} \qquad (2.32)$$

target

(c) series equivalent circuit (measured, no r_s term in C_S)

$$C_S = C[1+(G/\omega\, C)^2]; \quad R_S = r_S + \frac{1}{G[1+(\omega C/G)^2]} \qquad (2.33)$$

target

Fig. 2.18 (a) Actual circuit, (b) parallel equivalent circuit, and (c) series equivalent circuit for a pn or Schottky diode.

- **Determining C from series connected measurement @ two different frequency**
  - C_{S1} and C_{S2} are the measured capacitance at frequency ω_1 and ω_2

$$C = \frac{\omega_2^2 C_{S2} - \omega_1^2 C_{S1}}{\omega_2^2 - \omega_1^1} \qquad (2.34)$$

2.4 C-V measurement principle (2/2)

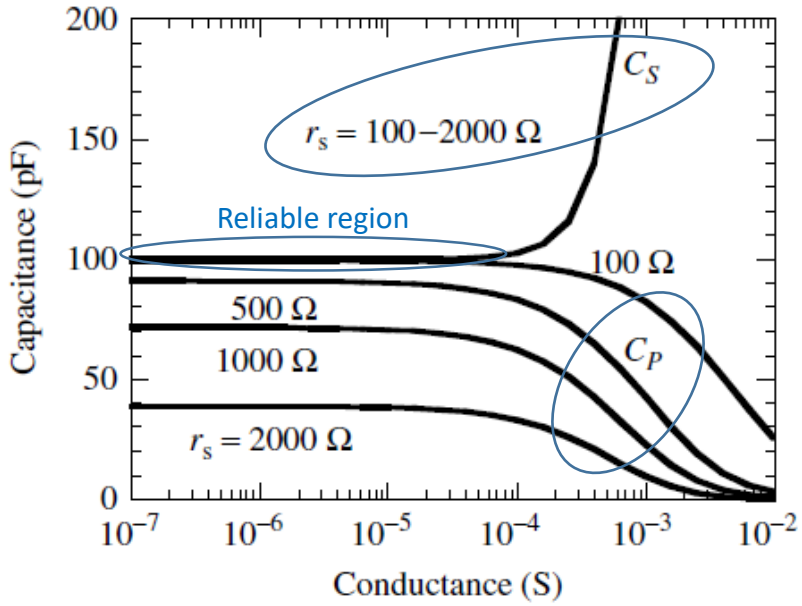


Fig. 2.19 C_S and C_P versus G as a function of r_s. $C = 100$ pF, $f = 1$ MHz.

- **C_S is independent of the series resistance r_s**, whereas **C_P** depends strongly on r_s
  - series equivalent circuit is the one to use for capacitance measurement if r_s is suspected
  - what is the purpose of C_p? Cross-checking r_s existance

- **Quality factor Q** for a parallel circuit defined by ***Q= ωC/G, true capacitance to be measured for Q≥5***
  ex) $Q= \omega C/G \sim 5\times10^{6}\times100\times10^{-12}/10^{-4}=5$

- In MOS structure, however, high gate leakage current distorts measured capacitance C_S or C_P

In real device, series resistance and capacitance (parasitic)

- **PN or Schottky Diode** (**dc** current flow is **necessary**) **vs. MOS-C** (**dc** current flow is **not necessary**)

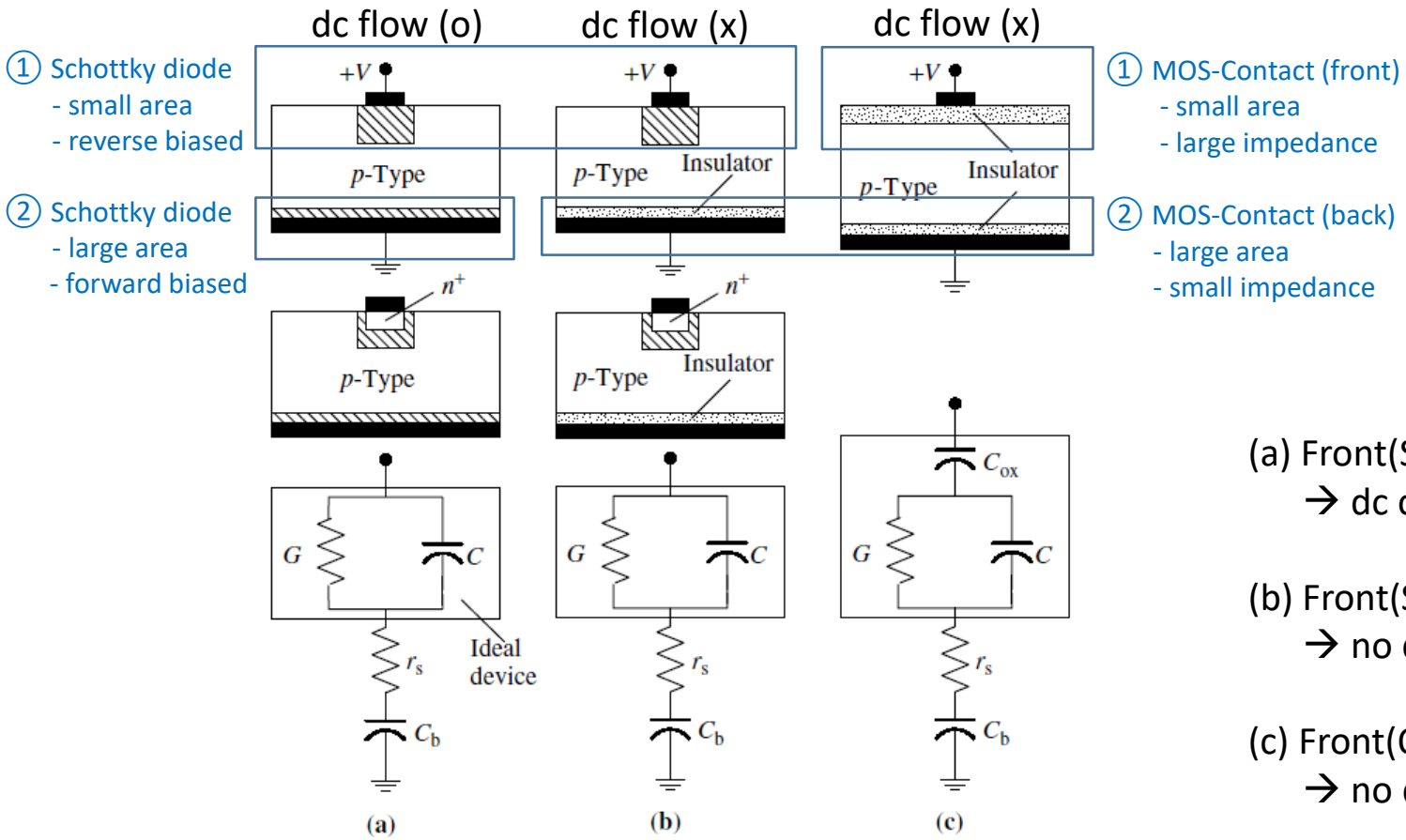


Fig. 2.20 Equivalent circuits with series resistance and capacitance for (a) front and rear Schottky contacts, (b) front Schottky and rear oxide contact, and (c) front and rear oxide contacts. The elements within the rectangles represent the intrinsic device.

(a) Front(Schottky contact)-Rear(Schottky contact)
→ dc current flow → dc doping profile (o)

(b) Front(Schottky contact)-Rear(Oxide contact)
→ no dc current flow → dc doping profile (x)

(c) Front(Oxide contact)-Back(Oxide contact)
→ no dc current flow → C-V doesn't require dc current

In real device, series resistance from back contact

- **Differential capacitance ($1/C^2$ vs. V)** method to obtain **carrier density profile**

- **$1/C^2$ distorted by series resistance(r_s), to reduce r_s …**
  - Fig.2.20(a), np or schottky diode
    : metallic back contact is required, vacuum of chuck to reduced resistance

  - Fig.2.20(c), MOS device
    : leave the oxide on the back surface,
    i.e large-area capacitive back contact ($C_b >> C_{ox}$)

- **Doping profile adjustment[81]**
  - measured density and depth increase with series resistance

target

$$N_{A.meas} = \frac{N_A}{1-(\omega r_s C)^4} \qquad (2.35)$$

target

$$W_{meas} = W[1 + (\omega r_s C)^2] \qquad (2.36)$$

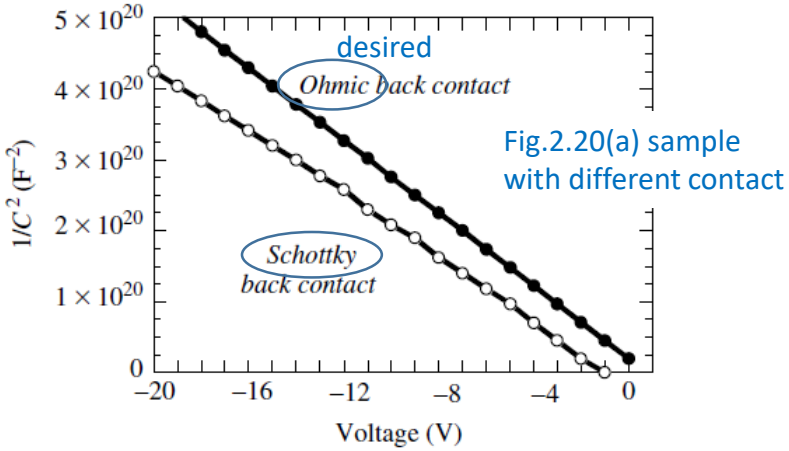


Fig. 2.21 $1/C^2$ versus voltage curves for n-Si wafers with $A = 3.14 \times 10^{-2}$ cm^2, $t = 640$ µm, $N_D \sim 5 \times 10^{14}$ cm^{-3}. Curve (a): front and back Al Schottky contacts, (b): front Au/Pd Schottky and back Au/Sb ohmic contacts. After Mallik et al., ref. 80.

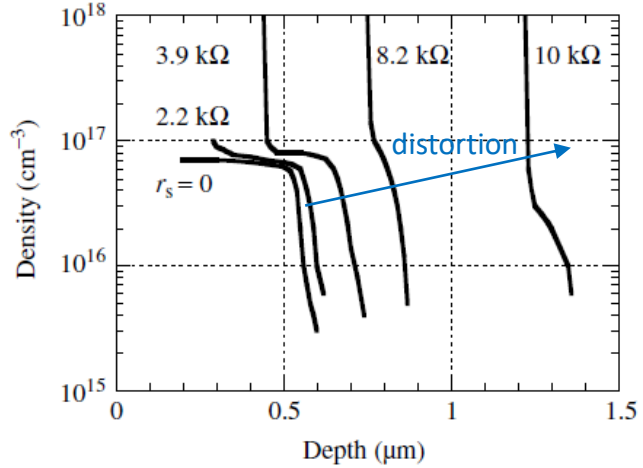
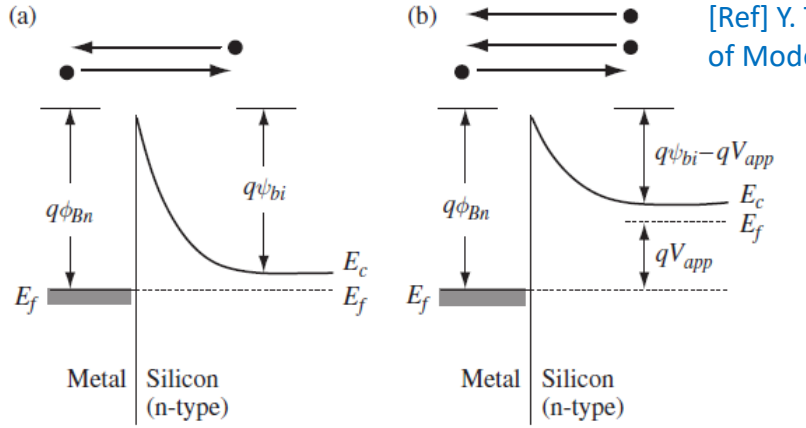


Fig. 2.22 Measured dopant profiles for a GaAs epitaxial layer on a semi-insulating substrate. The series resistance was obtained by placing resistors in series with the device. Reprinted after ref. 81 by permission of IEEE (© 1975, IEEE).

2.4.3 Minority Carriers in C-V

- **Minority Carriers**
  on 'reverse-biased Schottky barrier or pn junction diode'
  - scr width remains constant as a function of time
  - thermally generated e^- and h^+ pairs are swept out of scr and leave through the ohmic contact of device
  → probing depth W is **not effected** by minority carrier



[Ref] Y. Taur, Fundamentals of Modern VLSI Devices

Figure 2.55. Schematic energy-band diagrams illustrating the flow of electrons in an n-type Schottky diode. (a) At thermal equilibrium, there is an equal and opposite flow of electrons. (b) At forward bias, there is a net flow of electrons from the silicon into the metal. For simplicity of illustration, barrier-lowering effect is not shown.

- **Minority Carriers**
  on 'deep-depleted MOS capacitance'
  - thermally generated minority carrier drift to form inversion
  - device is unable to remain in deep depletion
  → probing depth W is **effected** by minority carrier
  - Fig.2.23(b) differential capacitance vs. max-min capacitance

  - method to prevent minority carrier generation
  : liquid N_2 and collected by reverse-biased junction

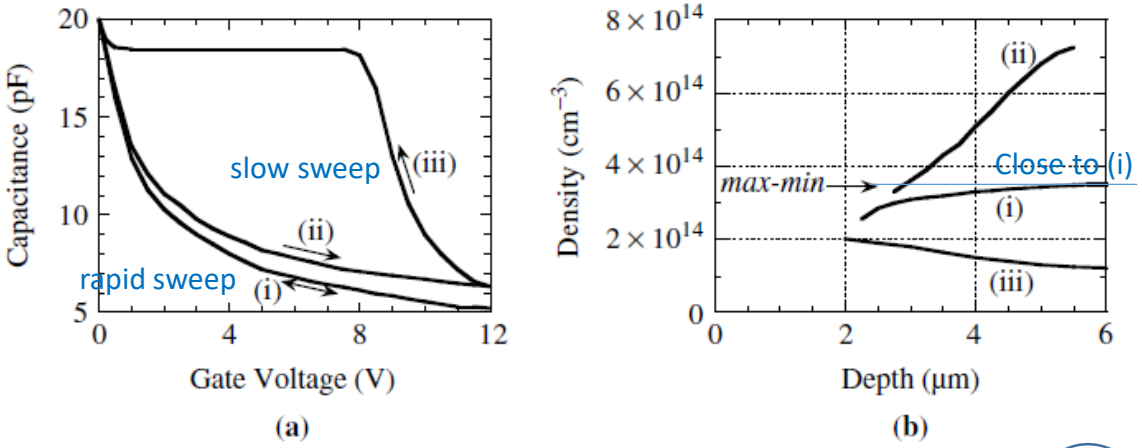


Fig. 2.23 (a) Equilibrium $C-V_G$ curve of an MOS-C, (b) deep-depletion curves for (i) 5 V/s and (ii), (iii) 0.1 V/s sweep rates, (c) the carrier density profiles determined from (b). $C_{ox} = 98$ pF, $t_{ox} = 120$ nm. Courtesy of J.S. Kang, Arizona State University.

2.4.3 Interface Traps in MOSCAP C-V

- **'C-V stretched out' by interface trap**
- Doping profiling can be corrected[85]
  by measuring the 'high-frequency capacitance C_{hf}' and the 'low-frequency capacitance C_{lf}'

$$N_{A.corr} = \frac{1-C_{lf}/C_{ox}}{1-C_{hf}/C_{ox}} N_{A.uncorr} \qquad (2.37)$$

- Method to mitigate interface traps effecting on 'stretched out'
  ① pulsed MOS-C doping density profile technique,
  suggested modulation frequency of 30MHz
  ② device freeze-out

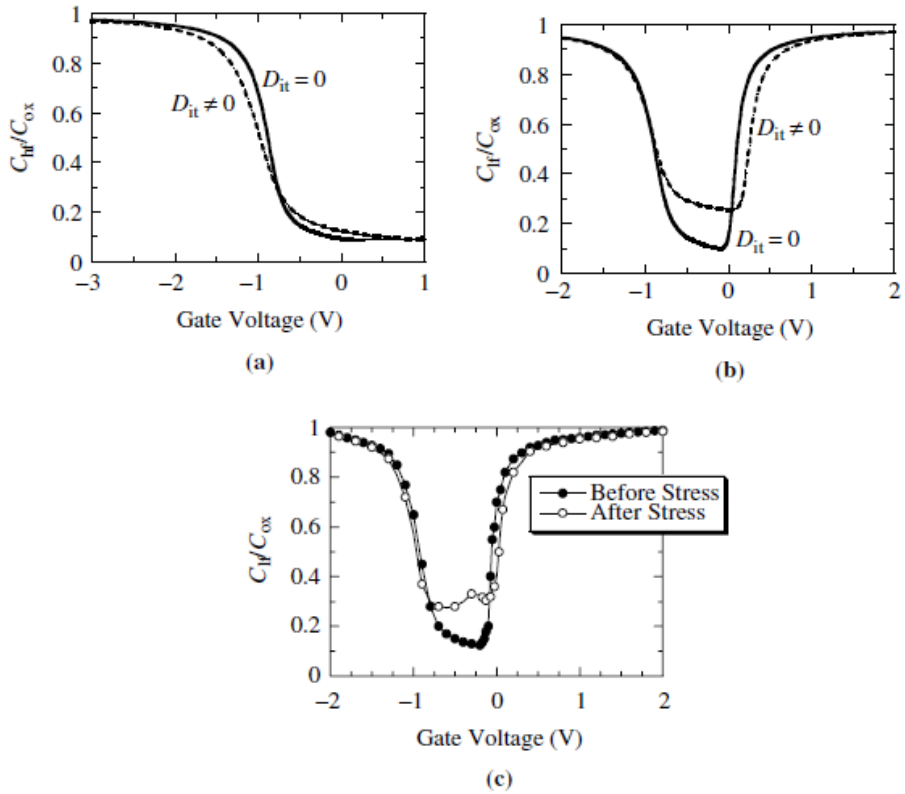


Fig. 6.21 Effect of D_{it} on MOS-C capacitance-voltage curves. (a) Theoretical high-frequency, (b) theoretical low-frequency and (c) experimental low-frequency curves. Gate voltage stress generated interface traps.

2.4.6 Deep Level Dopants/Traps

- The 'contribution of traps' is a complicated function of
  density, energy level of trap, sample temperature, frequency of ac voltage

- **Traps is able to respond** to sufficiently **slowly changed** reverse bias **dc voltage**

- Assuming
  - **deep-lying dopant atoms not fully ionized** at the measurement temperature
  - reverse bias V_1 has been applied for a sufficiently long time
  - **emission time constant,** τ_e

$$\tau_e = \frac{\exp(\Delta E/kT)}{\sigma_p v_{th} N_v} \qquad (2.42)$$

σ_p: capture cross-section
v_{th}: thermal velocity
N_v: effective density of states in the valence band

$\tau_e < 1/\omega$: holes emitted
$\tau_e > 1/\omega$: insufficient time to emit holes

$\omega = 2\pi f$: ac cycle

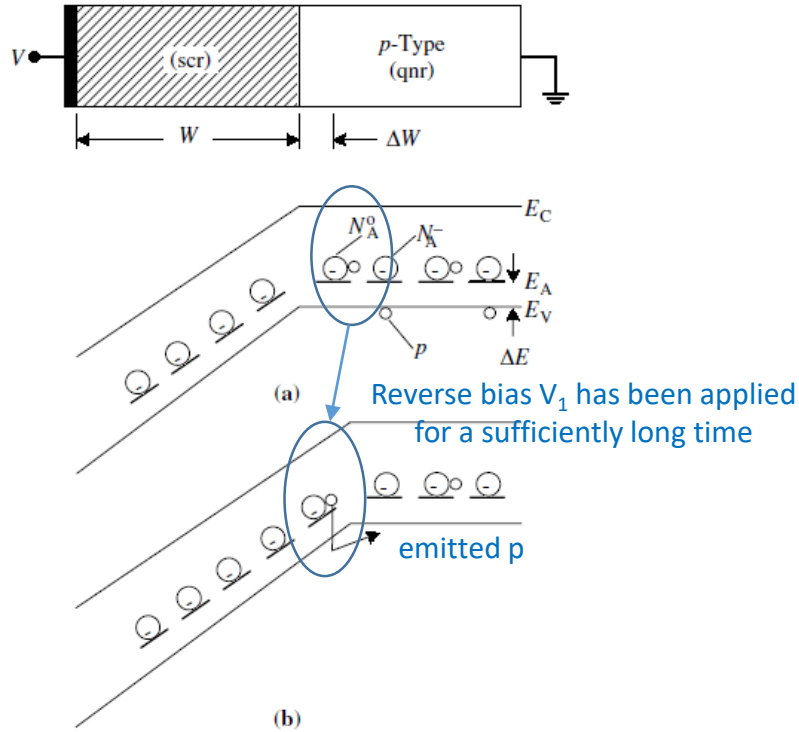


Fig. 2.24 Band diagram of a reverse-biased Schottky diode showing complete ionization in the space-charge region (scr) but only partial ionization in the quasi-neutral region (qnr). (a) $V = V_1$, (b) $V = V_1 + \Delta V$.

2.5 Differential Hall Effect for carrier density

- The **key feature of Hall measurements** is the ability to determine **carrier density, carrier type, and mobility**

- **Hall coefficient R_H**[95] definition

$$R_H = \frac{r(p-b^2n)}{q(p+bn)^2} \qquad (2.45)$$

r: scattering factor ($1 < r < 2$), usually 1
b: μ_n/μ_p

① p-type with p >> n,

$$R_H = \frac{r}{qp} \qquad (2.47)$$

② n-type with n >> p,

$$R_H = -\frac{r}{qn} \qquad (2.48)$$

③ Hall coefficient determined by experiment

$$R_H = \frac{tV_H}{BI} \qquad (2.46)$$

t: sample thickness, V_H: Hall voltage, B: magnetic field, I: current

- **Differential Hall Effect (DHE)**[103]
  - sheet Hall coefficient '$R_{Hsh}=V_H/BI$', and sheet conductance '$G_{Hsh}=1/R_{Hsh}$' must be measured repeatedly

$$p(x) = \frac{r(dH_{Hsh}/dx)^2}{qd(R_{Hsh}G_{Hsh}^2)/dx} \qquad (2.54)$$

2.7 Secondary Ion Mass Spectrometry (SIMS)

- **SIMS** for **'dopant profiling'**
  - removal of material from a solid by **'sputtering'** and on **'analysis of the sputtered ionized species'**
  - **only the ionized atoms can be analyzed** by passing them through an energy filter and a mass spectrometer
  - **highest sensitivity:** can detect all elements having **dopant densities as low as 10^{14} cm^{-3}**
  - **depth resolution of 1 to 5nm,** and can give lateral surface characterization on a scale of several microns

  - converting **"secondary ion signal vs. time"** to **"impurity density vs. depth"**
    ① standards of known dopant profile obtained from uniform impurity sample
    ② time x sputtering rate = depth

  - SIMS determines the **total, not the electrically active** impurity density

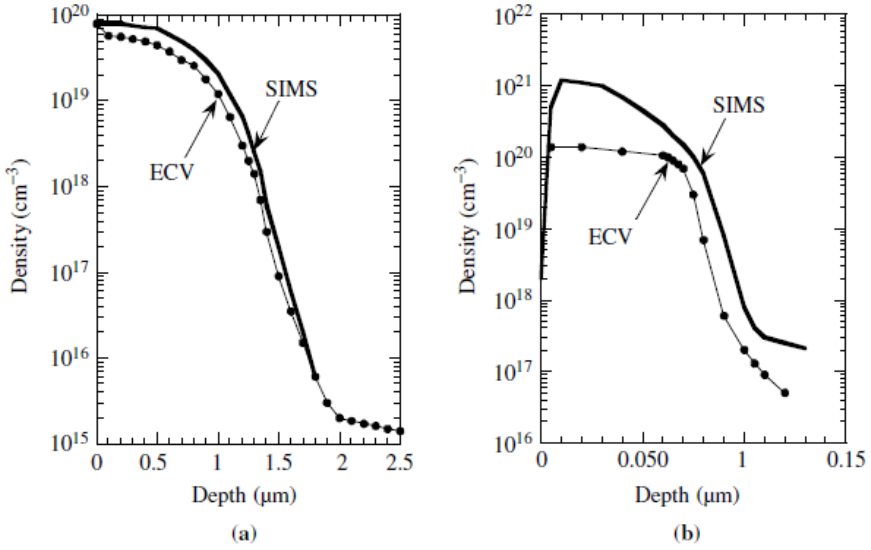


Fig. 2.14 Profiles obtained with the ECV profiler and with SIMS. (a) $p^+(B)/p(B)$ Si and (b) n^+ (As)/$p(B)$ Si. Reprinted after Peiner et al., Ref. 64 by permission of the publisher, the Electrochemical Society, Inc.

2.10 Strengths and Weaknesses

Dopant/Carrier profiling	Strengths	Weaknesses
Differential Capacitance	- Giving carrier density profile with little data processing - Non-destructive, well-commercialized	- Limited profile depth by 'zero-bias scr width' and depth by voltage 'breakdown' of heavily doped region
Max-Min MOS-C Capacitance	- Simplicity - Just high-frequency C-V required	- Inability to provide a density profile - only average value
Integral Capacitance	- providing a value for an 'implant dose' and 'depth' - Accurate (monitoring ion implant uniformities of 1%)	- Inability to provide a density profile
MOSFET Current-Voltage	- Applicable for small sample	- Not found wide application - Good interpretation(Short & Narrow CE removal) required
Spreading Resistance	- Well known method in Si Semiconductor industry - No depth limit - Large doping density range from 10^{13} cm^{-3} to 10^{21} cm^{-3}	- Complexity of sample preparation and interpretation (need a mobility values)
Hall Effect	- Utilized for profiling, but not a routine for profiling - Providing average values of carrier density and mobility	- Inconvenience of providing repeated layer removal
Secondary Ion Mass Spectrometry (SIMS)	- Commonly used - Dopant(not carrier) density profiling - High spatial resolution - can be used for any semiconductor	- Complexity of equipment - Most sensitive for B in Si, sensitivity reduction for all other impurities -reference standard must be used for quantitative interpretation

Homework #1 (due Oct 16th)

Chapter 1

#1.4
#1.5
#1.7
#1.15
#1.16
#1.24
#1.25

Chapter 2

#2.3
#2.4
#2.16

Backup

2.5 Hall Effect and activation energy E_A

- For a **p-type semiconductor** of doping density N_A, compensated with donors of density N_D
  - the hole density is determined from the equation[100]

$$\frac{p(p+N_D)-n_i^2}{N_A-N_D-p+n_i^2/p} = \frac{N_v}{g}\exp(-E_A/kT) \qquad (2.49)$$

① At low temperature where $p << N_D$, $p << (N_A-N_D)$, and $n_i^2/p \approx 0$

$$p \approx \frac{(N_A-N_D)N_v}{gN_D}\exp(-E_A/kT) \qquad (2.50)$$

② When N_D is negligibly small

$$p \approx \sqrt{\frac{(N_A-N_D)N_v}{g}}\exp(-E_A/kT) \qquad (2.51)$$

③ At higher temperature where $p >> n_i$

$$p \approx N_A - N_D \qquad (2.52)$$

④ At still higher temperature, where $n_i >> p$

$$p \approx n_i \qquad (2.53)$$

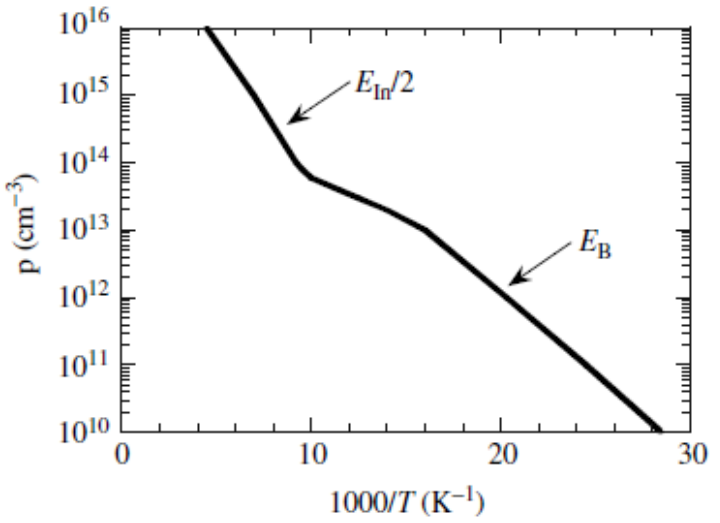


Fig. 2.26 Carrier density vs. reciprocal temperature for Si:In with Al and *B* contamination. $N_{In} = 4.5 \times 10^{16}$ cm^{-3}, $E_{In} = 0.164$ eV, $N_{Al} = 6.4 \times 10^{13}$ cm^{-3}, $E_{Al} = 0.07$ eV, $N_B = 1.6 \times 10^{13}$ cm^{-3}, $N_D = 2 \times 10^{13}$ cm^{-3}. Reprinted after ref. 101 by permission of IEEE (© 1980, IEEE).