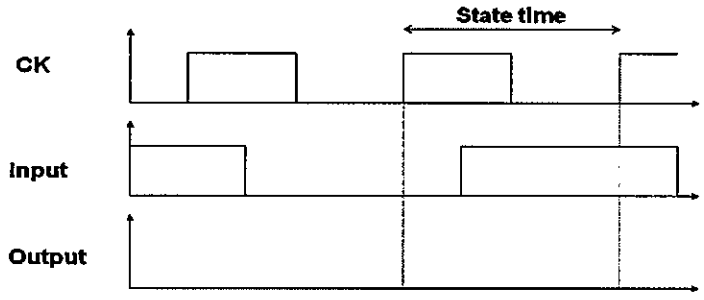
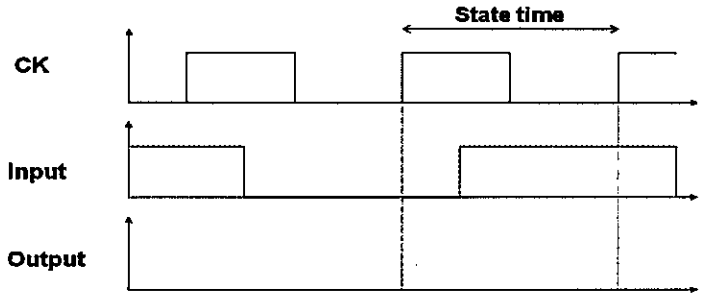
Digital/μ-Processor 박사 과정 입학 시험 (2010년)

Digital System Design (총 50점)

1. (10점) Multi-input single-output K-map에서 EPI (Essential Prime Implicant)를 찾는 법을 설명하라.
2. (15점) End-around carry란 무엇이며, 언제 발생하는가?
3. (10점) F/F의 synchronization failure가 무엇인가 설명하고, 이에 대응하기 위한 설계 방안에 대하여 설명하라.
4. (15점) Mealy machine과 Moore machine의 출력이 나오는 output time을 그리고, 두 machine의 출력이 나오는 output time을 비교, 차이를 설명하라. 두 시스템 모두 positive edge-triggered F/F을 사용한다. Moore machine의 어느 기간의 oputput이 Mealy machine의 어느 기간의 output에 해당하는지 설명하라. 문제지가 아닌, 답안지에 그림을 그리고 설명하기 바람.



Moore machine



Mealy machine

Microprocessor

1. Explain the following addressing modes: immediate, direct, register indirect, register relative. [10 points]

2. What is a stack? List the sequence of operations executed for an Intel x86 architecture "PUSH AX" instruction and a "POP AX" instruction. [15 points]

3. Draw a basic computer system that include three building blocks and three buses connecting blocks. Don't forget to label buses. [10 points]

4. Explain the differences between the real mode and the protection mode. [15 points]

2009 QE [Computer Eng]

Digital

1. Use Boolean Algebra (not the Karnaugh Map) to simplify: (10)

$(a+b)(a+c)(bc+d)(bc+\bar{d})=$

2. Explain overflow in addition or subtraction. When does it occur ? (10)

3. Simplify f(A,B,C,D) using the K-Map. (15)

AB \ CD	00	01	11	10
00	1	1	1	0
01	0	0	1	0
11	0	0	0	0
10	1	1	1	0

4. Complete the following input excitation table for 3 types of Flip-Flops. (15)

Q	Q+	D input for a D FF	T input for a T FF	J input for a JK FF	K input for a JK FF
0	0				
0	1				
1	0				
1	1				

Microprocessors

1. The 3 types of system bus are _____, _____, _____. [10]

2. Explain the following three addressing modes: immediate, register indirect and register relative. [10]

3. How do we address a large address space (example: 0x12345678) using a small number of address bits (e.g., 16 bits) efficiently? [10]

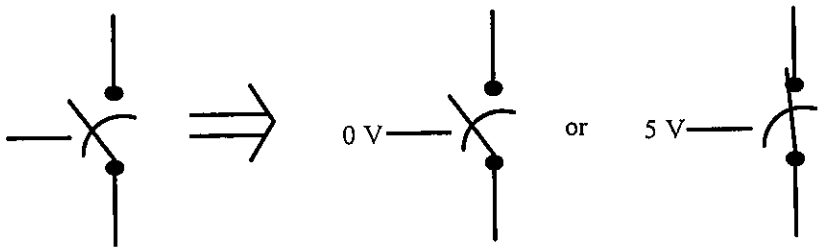
4. Compare subroutine and interrupt. [10]

5. What is system-on-chip (SoC)? Compare SoC and micro-controller. [10]

2008 QE (Computers)

Part 1: Digital Systems

1. (10 points) Show the design for a 2-input NOR gate designed from electromechanical switches like the one shown below.



* Note: Logic 1 = 5 V and Logic 0 = 0 V

2. (10 points) Given the binary bit sequence 100110010110, what is the value being represented if (a) unsigned binary, (b) 1's complement, (c) 2's complement, (d) sign-magnitude, and (e) excess-2047 notation is being used?

3. (15 points) Show how an 8:1 MUX can be connected to implement the function

$$g(A, B, C, D) = \Sigma (0, 1, 4, 5, 7, 9, 13, 14, 15)$$

4. (15 points) Discuss the "metastability" problem and methods for avoiding or minimizing the probability of metastable values.

Part 2: Microprocessors

5. What is the difference between **von Neumann architecture** and Harvard architecture?
6. Name the 3 **buses** and explain them in terms with directions.
7. Name 3 differences between **real mode** and **protection mode** and explain them.
8. Explain 2 differences between **processes** and **threads**.
9. Name 3 different **addressing modes** and explain them.
10. Explain the internal structures of microprocessors **as much as you know.** (Drawing recommended. The more the better.)

컴퓨터 공학 분야 박사 과정 자격 시험

(PH.D. Qualifying Examination in Computer Engineering)

(2007. 8.)

NOTE

본 시험은 디지털 시스템 설계(50 점)와 마이크로프로세서 (50 점)의 2 개 분야로 나누어져 있음.

This qualifying examination is divided into two parts of digital system design (50 points) and microprocessor (50 points).

Digital System Design Part of COMPUTER ENGINEERING

1. (10 points) For the following state table, show equations for the next state and the output in the minimum S-O-P forms.

	Q1+ Q2+		Z	
Q1 Q2	X=0	X=1	X=0	X=1
0 1	0 0	0 1	1	0
1 1	1 1	0 1	0	1
0 0	1 1	0 0	1	0

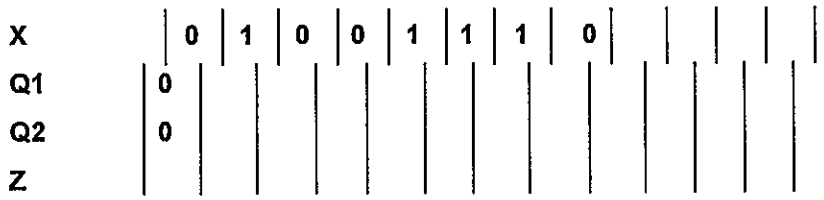
2. (10 points) Show the state table for a Mealy system that produces a 1 output (Z) *if and only if* there have been four or more consecutive 1 inputs or two or more consecutive 0 inputs.

X (input) 0 1 1 0 0 1 0 0 1 1 1 1 1 0 0 0 1

Z (output) ? 0 0 0 1 0 0 1 0 0 0 1 1 0 1 1 0 0

3. (15 points) For the following state table, show a state diagram and complete the timing trace as far as possible (even after the input is no longer known). For the output Z, ignore the false output in completing the timing trace.

	Q1+ Q2+		Z	
Q1 Q2	X=0	X=1	X=0	X=1
00	00	10	0	1
01	00	00	0	0
10	11	01	1	1
11	10	10	1	0

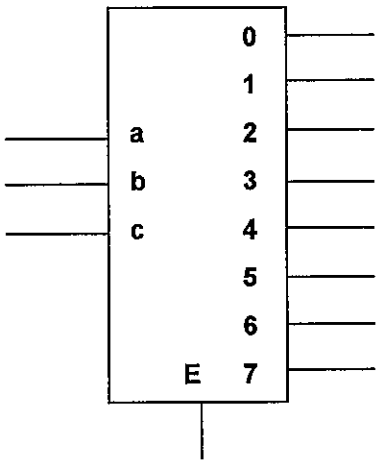


4. (15 points) Professor Kim computes grades as follows: He uses only the first digit (that is, 9 for averages between 90 and 99). He never has an average of 100. He gives a P (pass) to anyone with an average of 60 or above and an F to anyone with an average below 60. Now, Professor Kim needs a combinational circuit that gives the output

P=1, *if and only if* his student passes the subject he taught. Design the combinational circuit that Professor Kim needs. For your design, assume that the first digit is decoded in the 8421 code (that is, straight binary, 5 as 0101, for example); these are inputs w, x, y, and z. You have one 6-input OR gate, one inverter, and two of the decoders with active high outputs and an active high enable E, shown below. You don't need to use all components you have.

You will get 15 points (max.) if you use only one decoder, and 12 points (max.) if your use two decoders.

E	a	b	c	0	1	2	3	4	5	6	7
0	X	X	X								
1	0	0	0	1							
1	0	0	1		1						
1	0	1	0			1					
1	0	1	1				1				
1	1	0	0					1			
1	1	0	1						1		
1	1	1	0							1	
1	1	1	1								1



Microprocessor Part of COMPUTER ENGINEERING

2007 QE [Computer Eng - Microprocessors]

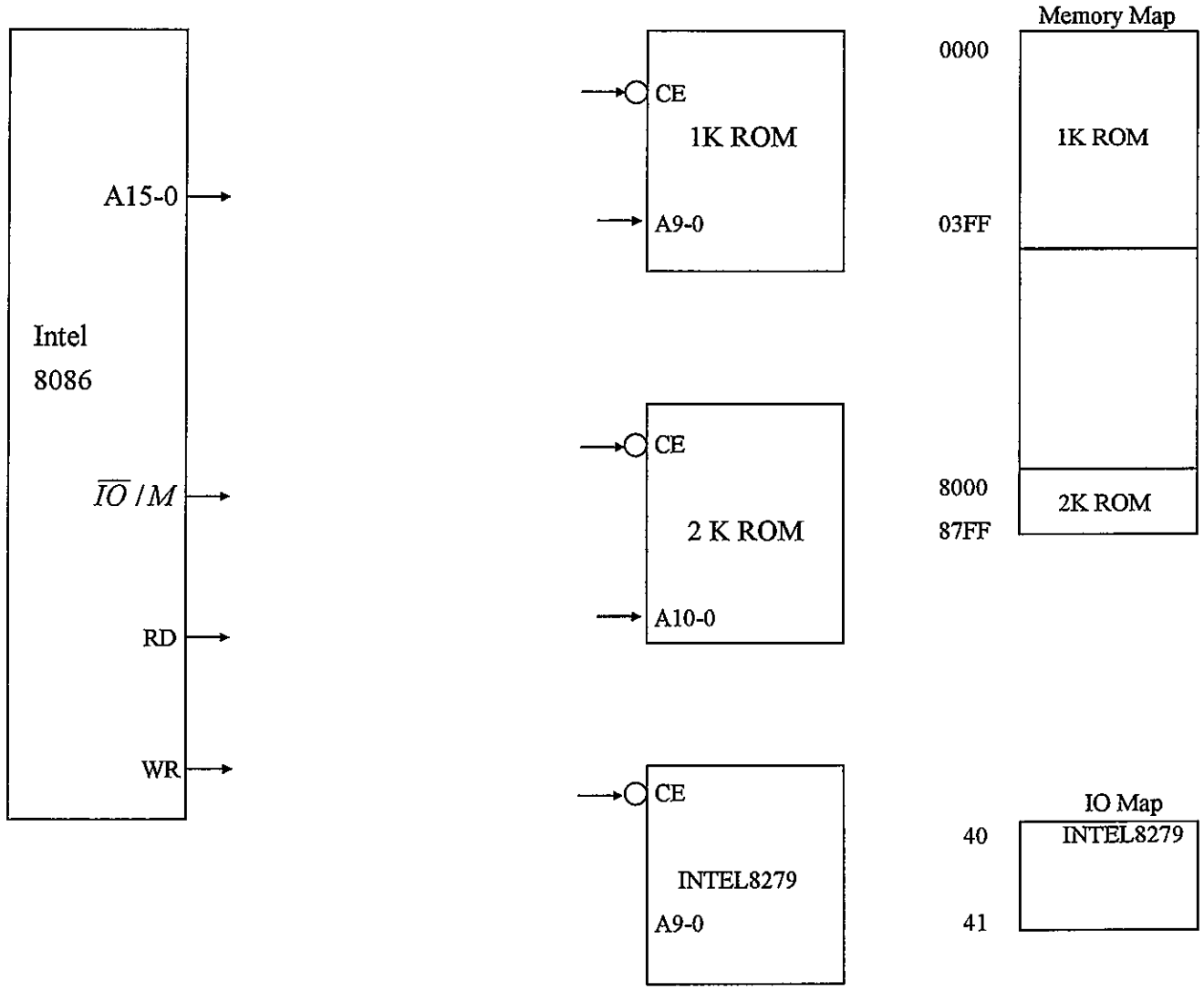
1. The 3 types of system bus are _____, _____, _____ .[5]

2. Define the programming model of a CPU. [5]

3. What is the functional difference between a general digital system and a computer?
   What kinds of hardware are present in a computer that does not exist in a general digital system? [10]

4. What is a bus cycle and a T-state in an Intel CPU? What kinds of operations (list all the major operations in a CPU) take place within a bus cycle and within a T-state? What is the first machine cycle of any instruction?
Which initiates this bus cycle? [15]

5. Design a simple address decoding circuitry and then make appropriate connections in the following diagram. Partial decoding is allowed. Use the memory map as a guide. (10)



POHANG UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department of Electrical Engineering

Computer Engineering

2006 Qualifying Exam for PhD Program

Name:

Digital System

1. (15 points) For the logic equation f = (a b' c + a d') c + a' c' d
   (a) Draw a Karnaugh-Map (K-map).
   (b) Derive a minimal sum-of-products (SOP) expression using the above K-map.
   (c) Show a logic implementation using only 2-input NAND gates (either the minimized SOP expression or the original expression can be used).

2. (20 points) Use the finite state machine (FSM) method to design a synchronous sequential circuit that implements the following pseudocode algorithm.

   Pseudocode:

   Step 0: Initialization (can use RESET' signal):
   toggle ← 0 ;
   req ← 0 ;
   Step 1: *req* ← *toggle'* ;
   wait until *ack* = *toggle'* ;
   Step 2: *toggle* ← *toggle'* ;
   go to Step 1;

3. (15 points) Is an 8:1 multiplexer (MUX) a universal logic device? Prove your answer. Next, use an 8:1 MUX to implement the logic equation of Problem 1 (the original, unsimplified equation).

4. (10 points) For the following assembly program, determine the values of flags after the operation.

```
0000 B5 22        MOV CH,22H
0002 80 ED 44     SUB CH,44H
```

5. (10 points) Explain the memory management methods, segmentation, paging, and hybrid in terms with the size and fragmentation. Fill in the blanks with the terms: variable, fixed, internal and external.

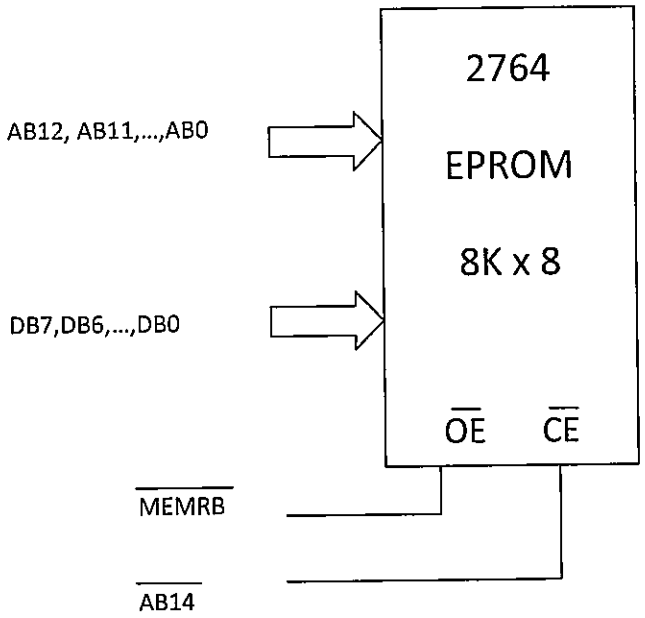
	Segmentation	Paging	Hybrid
Size			
Fragmentation			

6. (20 points) Explain the following concepts in protection mode.
   (a) Memory management

   (b) Protection

   (c) Task switching

7. (10 points) The following is an EPROM memory storing 8Kx8 bits. For the given address decoding as shown, determine the memory map. (Hints. XXXXH-YYYYH)



2005. 10. 26

컴퓨터 공학 분야 박사 과정 자격 시험

(2005. 10.)

NOTE

1. **Digital system design** 과 **Microprocessor** 의 **2** 개 분야로 나누어져 있음.
2. 분야 당 배점은 각 **50** 점임.

Digital System Design Part of COMPUTER ENGINEERING

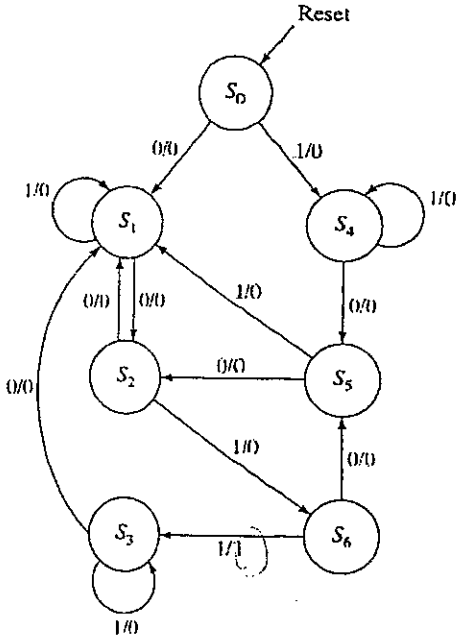
1. (15 points) Consider the function.

$$F(A,B,C,D) = \Sigma m(1,5,7,8,9,13,15) + \Sigma d(4,12,14)$$

   A. (5 points) Ignoring the don't care terms, write the above function as a Boolean expression in canonical maxterm form. i.e., write the canonical maxterm form for $F(A,B,C,D) = \Sigma m(1,5,7,8,9,13,15)$

   B. (10 points) Find the minimum sum of products form. Show your process of getting the minimum form.

2. (15 points). Given the state diagram, draw the fully reduced state diagram. Show the process of state reduction.



3. (10 points) Explain Consensus theorem, and give the consensus term of the following expression. F = ABC + A'D+B'D

4. (10 points) Explain which static hazard can happen for the following system, static 0 hazard, static 1 hazard, none, or both, and explain why. F = AB + A'BC + BD +ACD + BCDD'

2005QE [Microprocessors]

1. [22]

1) For high speed of I/O transfer, a DMA controller takes charge of the I/O instead of the CPU. Here, the hardware performs the I/O and thus instead of the _____ involving the CPU. The major source of time saving comes from no need to accesss the _____ for instructions.

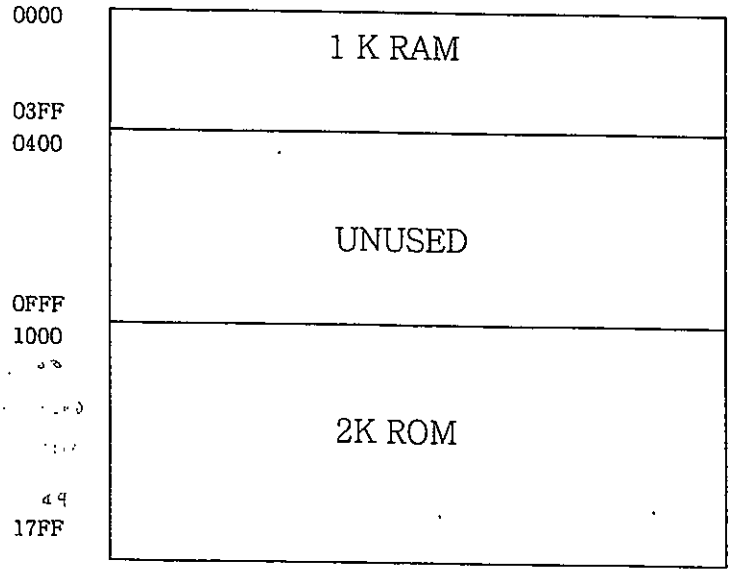
2) If a CPU does not have the multiply or divide instructions in the instruction set, then four instructions such as _____, _____, _____, _____ are needed to multiply or divide integers.

3) The Last-In-First-Output type of data structure is called a _____ and is used to execute _____, _____ instructions or to handle hardware _____.

2. When might an instruction come from an I/O device ? [8]

3. List and briefly explain all data transfer types of operations. There must be at least five of them. [10]

4. Given the following memory map, implement a memory interface that realizes this map. Show all the devices and signals along with their connections involved. Hint: Use a decoder and NAND gates. [10]

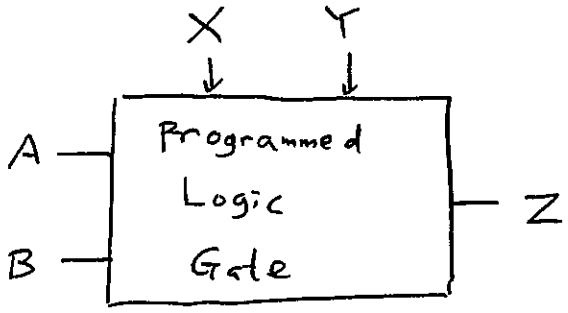


2004. 11. 3

QE 2004 Computer Eng. – Digital

1. Given the following Programmed Logic Gate hardware and its Programmed Function Below:

If XY = 00, then Z = 0
If XY = 01 then Z = AB
If XY = 10 then Z = 1
If XY = 11 then Z = A + B



Find a Minimal Sum of Product expression for the Output Z (A, B, X, Y). (15)

2. A multiplexer can implement any logic. Right or Wrong ? (5)

3. Design a 3-bit counter that counts in the following sequence:

000, 010, 111, 100, 110, 011, 001, 000.
Design the counter using D flip-flops and gates. Minimize the hardware. (30)

QE 2004 Computer Eng. – Microprocessors

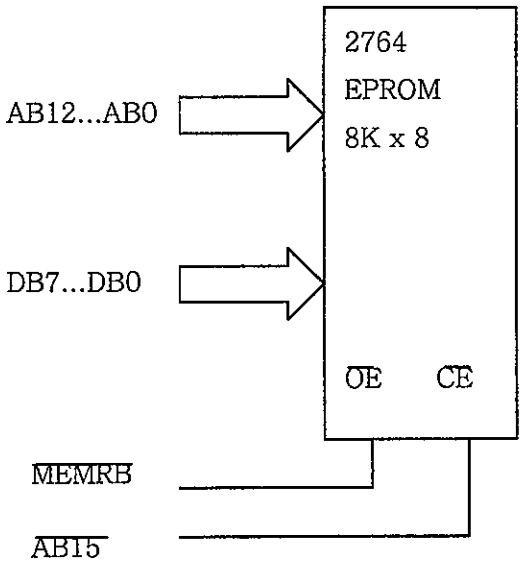
4. Determine the flags CF, PF, AF, ZF, SF, OF for the following operation.

   ADD 7F,1

5. Explain the memory management methods: segmentation, paging, and hybrid, in terms with the size and the fragmentation.

6. Explain the differences between the real mode and the protection mode.

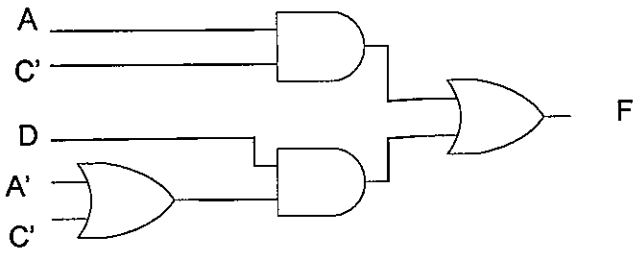
7. Derive the memory map for the following memory interface.



2003년도 QE (Digital System)

이름:

1. (총 20점) 다음과 같이 A, B, C, D의 4개 변수를 입력으로 갖는 논리회로에 대하여 아래 물음에 답하라.

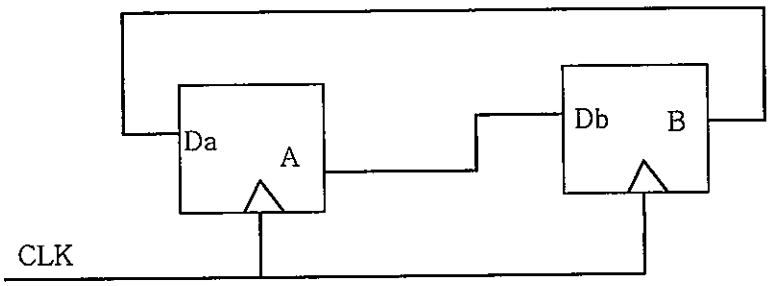


A. (5점) 위 논리 회로의 레벨은 얼마인가?

B. (10점) Static 1 hazard가 있는가? 있다면 있는 경우를 보이고, 없다면 없는 이유를 설명하라.

C. (5점) Static 0 hazard가 있는가? 있다면 있는 경우를 보이고, 없다면 없는 이유를 설명하라.

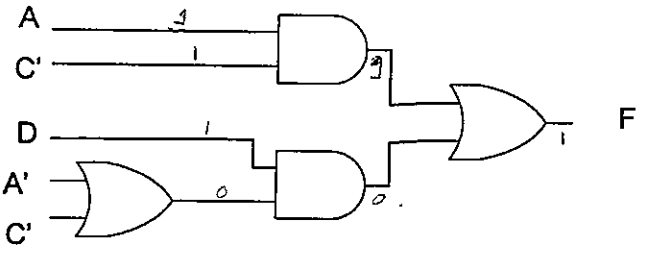
2. (총 5점) 다음 counter의 sequence를 적으라. 초기 조건은 AB (00) 이다.



2003년도 QE (Digital System)

이름:

1 (총 20점) 다음과 같이 A, B, C, D의 4개 변수를 입력으로 갖는 논리회로에 대하여 아래 물음에 답하라.



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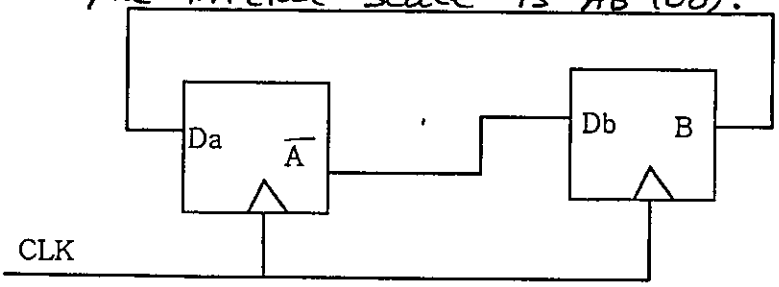
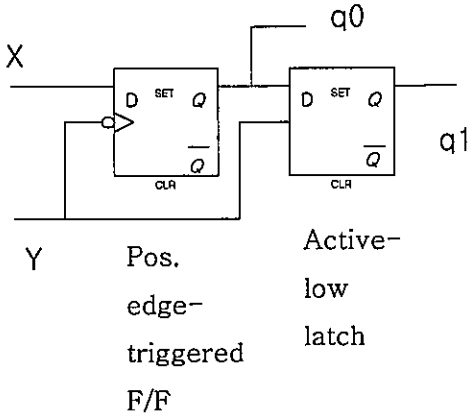
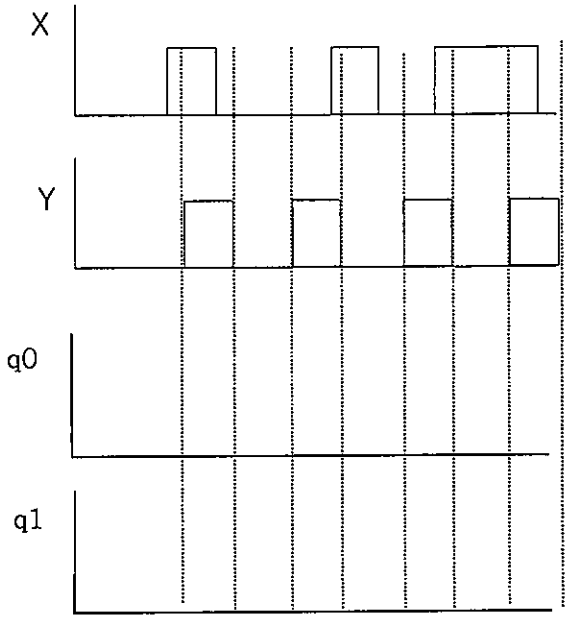


3. (총 5점) 아래 회로에서 q0와 q1의 타이밍 다이아그램을 그려라. F/F과 latch의 딜레이는 없다고 가정하라. 또 q0와 q1의 초기 값은 zero (0)이다.





4. (10점) Combinational logic과 sequential logic의 차이를 설명하라

5. (10점) Moore machine과 Mealy machine의 블록 다이아그램을 그리고, neg. edge triggered F/F을 사용하는 시스템들의 output이 변화하는 time point의 차이를 설명하라.

2003 QE (Microprocessors)

6. (10 points) What is a stack? List the sequence of operations executed for an Intel x86 architecture "PUSH DX" instruction and a "POP DX" instruction.

7. (15 points) Show how the "vectored interrupt" method can be used to branch to address 0x003C (the hexadecimal address 3C) using an external interrupt. What I/O pins of the microprocessor are used, and in what sequence?

8. (15 points) Show the pseudocode or flowchart of the operation of a basic computer system. For full credit, you should also include a mechanism for handling interrupts.

9. (10 points) Draw a block diagram for a basic computer system. For full credit, include and label the three main busses used. Hint: It consists of three blocks with connections between those blocks.

2003 Qualifying Exam (Computer Engineering)

1. $F = \square(0, 4, 6, 9, 13, 14) + d(1, 7, 12)$. Implement F using a single 8:1 MUX

Don't Care Terms

2. Use the Finite State Machine (FSM) Method to design a sequence detector for the sequence 110011.

3. Draw a timing diagram showing all modes of operation for a positive edge-triggered D flip-flop. In the last portion of your timing diagram, show how a metastable output can be produced.

4. Determine the carry, sign, overflow, and zero flags for the following operation:

781FH SUB 82B1H

where SUB denotes "subtraction" and H denotes "Hexadecimal."

5. Explain the 3 I/O interfacing methods.

6. Explain the segmentation and paging modes.

7. Explain the write-back and write-through in cash operations.

8. A 8Kx8 EPROM has 13 address input pins and 8 data output pins. The address bus lines AB0-AB12 are connected to the address pins and the data bus lines DB0-DB7 are connected to the data pins. Also, AB14 and AB15 are connected to the CE (negative logic) via a XOR(exclusive-OR) gate. Draw the memory map of the 16-bit address space.

컴퓨터 공학 분야 박사 과정 자격 시험

(2001. 10. 31.)

NOTE

1. **Digital system design** 과 **Microprocessor** 의 **2** 개 분야로 나누어져 있음.
2. 분야 당 배점은 각 **50** 점임.

Digital System Design Part of COMPUTER ENGINEERING

1 (10 points) 2's complement Number system:

1.1 (5 points) 6 bit 를 사용하는 2's complement number system 에서 표현이 가능한 수의 범위를 나타내시오.

1.2 (5 points) 6 bit 를 사용하는 2's complement number system 에서 001111 + 100101 의 10 진수 상의 의미를 설명하시오.

2 (10 points) Flip-flop 의 setup time 과 hold time 이 무엇인지 설명하시오.

3 (10 points) Finite state machine 의 state reduction 방법에 있어서 row matching method 와 implication chart method 의 차이점을 설명하시오.

4 (10 points) Machine equivalence:

Implication chart method 를 사용한 state reduction 을 통하여 아래에 보인 두 FSM (finite state machine)의 state table 을 보고 FSM 1 과 FSM 2 가 같은 equivalent machine 인지, 아닌지를 밝히시오.

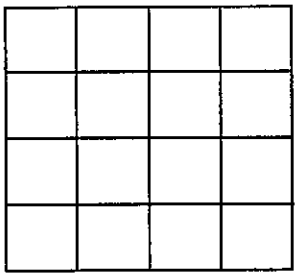
[Hint] Machine equivalence 를 확인하기 위해서는 아래의 참고도 1 과 같은 형태의 implication chart 를 사용하여 machine 1 의 각 state 에 대하여 machine 2 에 1:1 으로 matching 이 되는 equivalent state 가 있는지 확인하여야 함.

PS	NS X=0	NS X=1	Output X=0	Output X=1
A	B	A	0	0
B	C	D	0	1
C	A	C	0	1
D	C	B	0	0

FSM 1 의 state table

PS	NS X=0	NS X=1	Output X=0	Output X=1
S0	S3	S1	0	1
S1	S3	S0	0	0
S2	S0	S2	0	0
S3	S2	S3	0	1

FSM 2 의 state table



참고도 1

5. (10 points) Moore machine & Mealy machine

Moore machine 과 Mealy machine 의 block diagram 을 그리고, negative F/F 을 사용하는 Moore machine 과 Mealy machine 의 경우 output 이 valid 한 영역에 대하여 설명하시오 (F/F 과 gate 들의 딜레이는 zero 로 가정).

Microprocessor Part of COMPUTER ENGINEERING

1. List any five addressing modes of the INTEL 8086 and also find the number of memory accesses including the instruction fetch access. (15)

addressing modes	# memory accesses

2. List three advantages of memory-mapped I/O and isolated (or I/O mapped) I/O. (15)

Memory-mapped	Isolated

3. List the hardware structures or devices affected by the subroutine CALL instructions in INTEL 8086. Here, "affected" means "changed." (10)

4. What is the role of the READY input to the CPU? Which CPU state does it generate? When is it used? (10)

컴퓨터 공학 분야 박사 과정 자격 시험 (2000. 10. 27.)

분야 당 배점은 50 점임.

Digital System Design

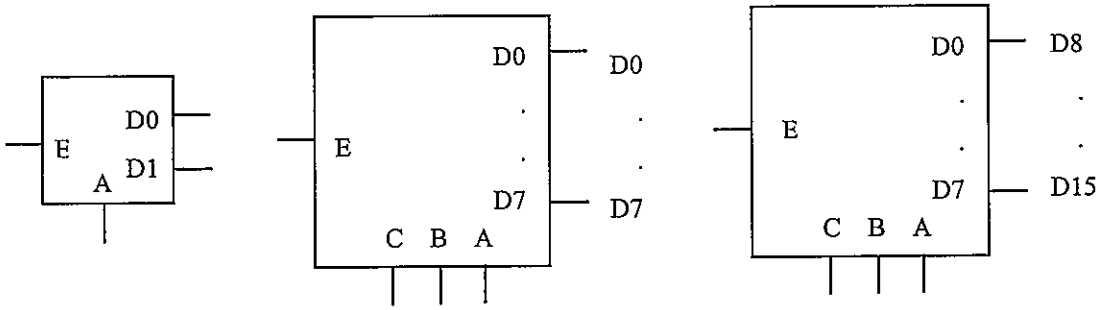
1. (20 점, 각 10 점) Implement the following functions using AND-OR-Inverter gates in the minimum form:

   1.1 (10 점) $f(A, B, C) = A \oplus B \oplus C$

   1.2 (10 점) $f(A, B, C, D) = \Sigma m\,(1, 3, 5, 7, 9) + \Sigma d\,(6, 12, 13)$

2. (10 점) Implement the following specification of the Boolean function in a minimum form and in a hazard-free manner: $F(A, B, C) = BC' + A'C$

3. (10 점) Show how to implement a 4:16 decoder using generic 1:2 decoder x 1 and 3:8 decoder x 2, where A of the control signals A, B, C ,.. is LSB. (Hint: Decoder is conceptually the reversal of the mulitplexer).



4. (10 점) A sequential circuit has one input (X) and one output (Z). Draw a Mealy state diagram of the circuit when the circuit is Z=1 if and only if the total number of 1's received is divisible by 3 (for example, 0, 3, 6, ...).

Microprocessor

1. Give an example (assembly instruction) and a brief description for the use of each of the following addressing modes: immediate, direct, indirect, register direct, indexed.

2. Using diagrams and short examples, show how the stack operations "PUSH CX" and "POP CX" are implemented, where "CX" is a 16-bit register.

2000 QUALIFIYING EXAM - COMPUTER ENGINEERING

99-10-29

Digital Systems

1. Using Consensus Theorem: xy + yz + x'z = xy + x'z, simplify

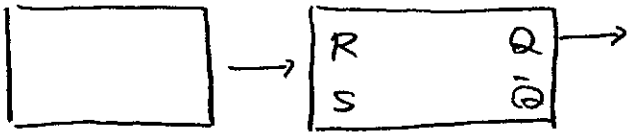
F = a'b'c + bc'd' + a'cd + ab'd' + bcd + ac'd'. (10)
USE BOOLEAN ALGEBRA. DO NOT USE KARNAUGH MAPS.

2. Consider a programmed logic gate that performs the following:

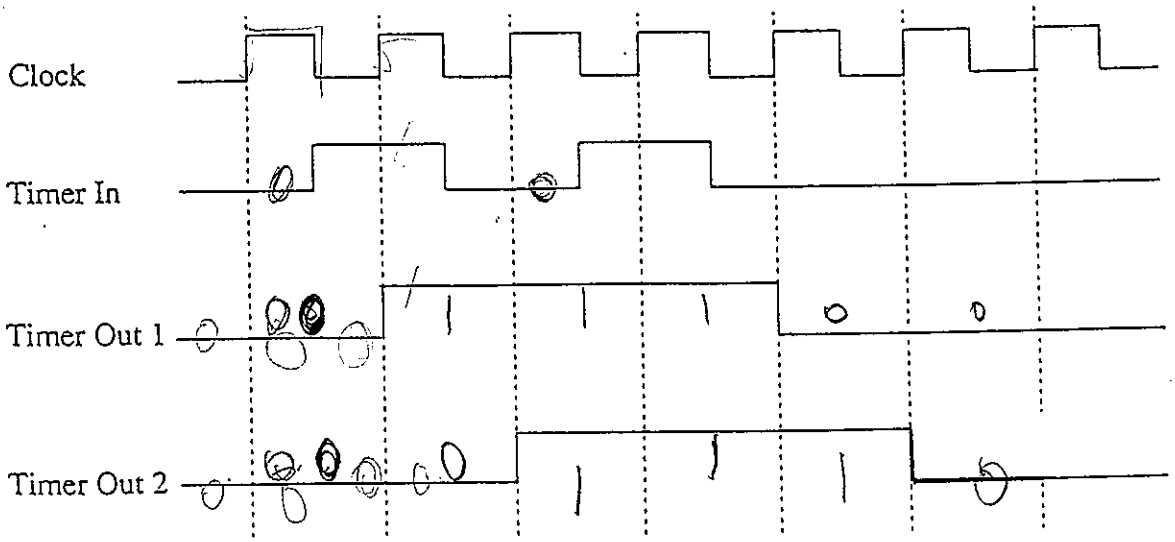
If XY = 00 then Z = 0
If XY = 01 then Z = AB
If XY =10 then Z = 1
If XY =11 then Z = A + B.

Derive a minimal product of sum expression for Z(X,Y,A,B) using the Karnaugh map. [15]

3. Show the additional circuitry that converts an RS flip-flop into a JK flip-flop.[10]



4. Draw an ASM chart and the circuitry for a timer which generates the following two outputs as shown below. Use an internal counter for internal timing as the circuitry. The chart should generate all the output signals needed by the internal counter. [15]



POHANG UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department of Electrical and Electronic Engineering
Qualifying Examination, Oct. 29, 1999
Computer Engineering (Microprocessors)

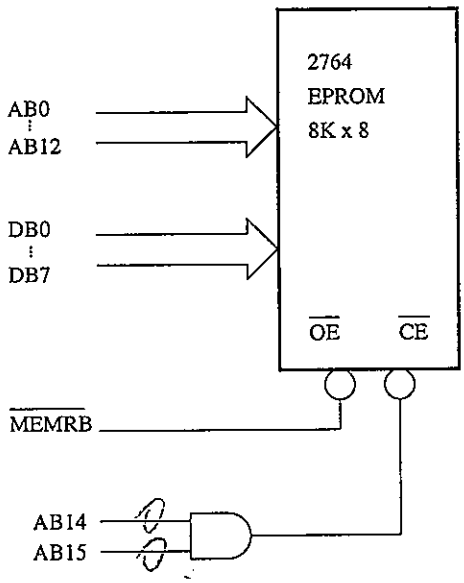
[5] Determine the carry, sign, overflow, and zero flags for the following operation:

791FH SUB 82A1H

where SUB denotes "subtraction" and H denotes "Hexadecimal numbers".

[6] I/O interface 방식 3가지에 대해 설명하시오.

[7] Draw the memory map of the 16 bit address space for the following memory circuit.



[8] real-mode memory addressing과 protected-mode memory addressing의 차이점을 설명하시오.

컴퓨터 공학 분야 박사 과정 자격 시험

(1998. 10)

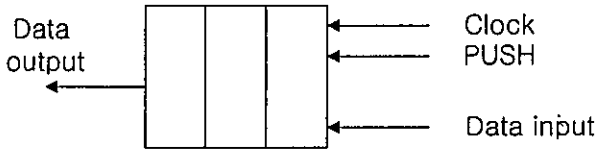
NOTE

1. Digital system design 과 Microprocessor 의 2 개 분야로 나누어져 있음.
2. 분야당 배점은 각 50 점임.

Qualifying Exam 98

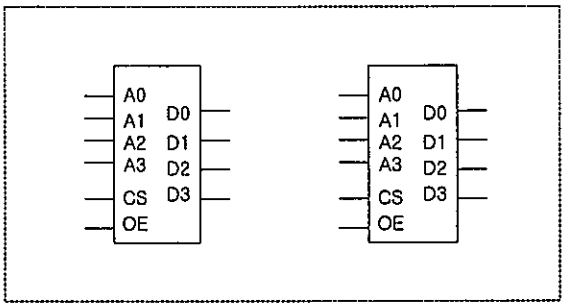
(Digital System Design)

1. (10 점) Design a 3 ***word*** by 1 ***bit*** LIFO (last in, first out) stack such that most recently pushed data is the first to be popped. The block diagram is given below. Here, ***word*** means the length of the stack and ***bit*** means the number of input bits in parallel. The popped data (output) must be held unless a new pop signal is applied. Draw your schematic, indicating the components used. To simplify the design, assume that POP=PUSH' and do not implement the ***LIFO empty*** and ***LIFO full*** signals.

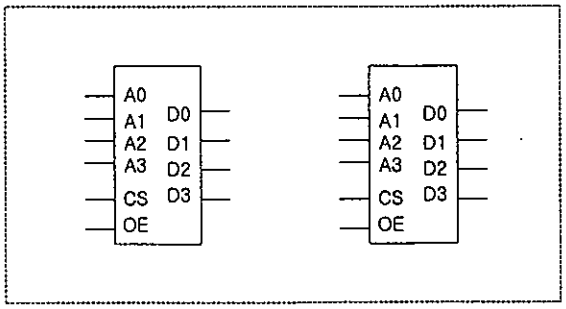


2. (총 10 점, 각 5 점) I have two ROM chips with 4 address lines (A3:A0) and 4 data lines (D3:D0), whose output is driven only if the chip is selected and the output is enabled.

2.1 Show that how to make a ROM with 5 address lines (A4:A0) and 4 data lines (D3:D0). Specify the address and data names in your design (dotted box).



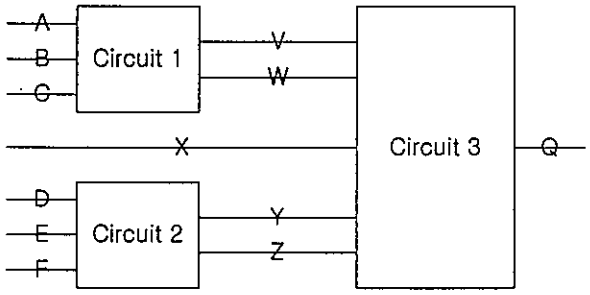
2.2 Show that how to make a ROM with 4 address lines (A3:A0) and 8 data lines (D7:D0). Specify the address and data names in your design (dotted box).



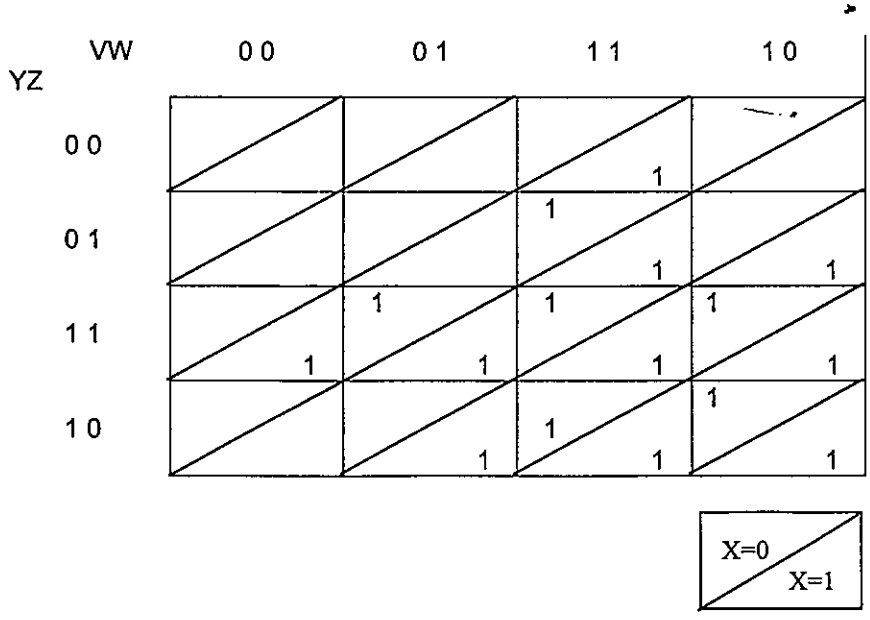
3. (10 점) A Moore machine has two inputs (X1, X2) and one output (Z). Draw the minimized state diagram for the machine, given the following specification. The output remains a constant value unless one of the following input sequences occurs.
   - The Reset causes the output to become 0.
   - The input sequence X1 X2 = 00, 11 causes the output to become 0.
   - The input sequence X1 X2=01, 11 causes the output to become 1.
   - The input sequence X1 X2=10, 11 causes the output to change the value of Z.

4. (총 20 점) You are to implement a seven-input majority function, which will assert its output whenever four or more of its inputs are asserted. The block diagram is given below, where circuits 1 and 2 tally the number of their inputs that are asserted and provide the count in binary on the outputs (V, Y are MSBs; W,Z are LSBs). Based on these second-level inputs, Q determines if more than four or more of the original inputs are 1. Note: tally = 세다.

4.1 (10 점) find the minimized sum of products form for circuits 1 (circuit 2 is identical). The functions V and W look familiar. Explain the function of circuit 1.



4.2 (10 점) After some work with the Truth table for Q, I found the following K-map to implement circuit 3. Circle prime implicants on the K-map and find the minimum sum of products form.



Qualifying Exam 98

(Microprocessor)

5. (15 pts) Draw the timing waveforms and label the important time parameters for a memory write access (an SRAM can be assumed).

6. (15 pts) What is Direct Memory Access (DMA)? Describe how DMA can be implemented in a computer system using a block diagram.

7. (20 pts) Show how to interface an input device to a microprocessor so that it responds by putting data on the data bus when the microprocessor executes the following assembly instruction: "IN 01234H". Be sure to show the resulting circuit diagram down to the gate level.

Qualifying Exam: Digital Problems

1. (10 points) A logic circuit has five inputs: A2, A1, B2, B1, and E. If E = 0, the output Z = 0. If E = 1, the output Z = 1 if and only if A2 = B2 and A1 + B1 = 1. Derive and simplify the expression for Z directly from the problem statement. Be sure to show the derivation procedure.

2. (20 points) The logic diagram shown below, Fig. 1, has an input "x" and clock pulse "clk" as shown. Assume that the flip-flop changes state at the trailing edge of the clock. Draw the timing diagram of x, x', A, A', R, S, and y. Start by assuming that the flip-flop is initially in the set state and later justify your assumption. What is the function of this circuit?

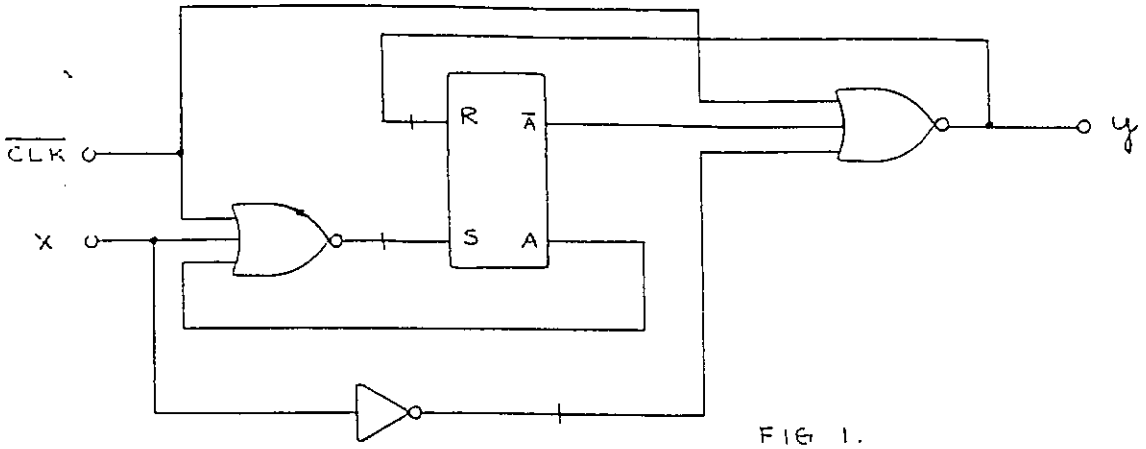


FIG 1.

TIMING DIAGRAM.

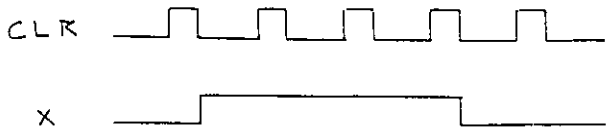


FIG. 1.

3. (20 points) Given the Mealy machine in Figure Ex8.7, implemented with one toggle flip-flop and one D flip-flop,k with single input I and single output Z, draw its complete state diagram.

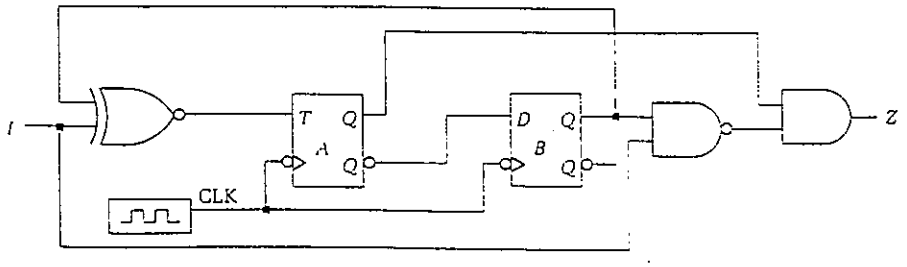


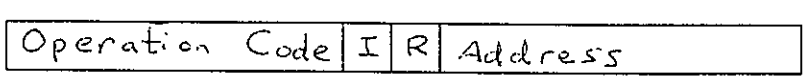
Figure Ex8.7 Mealy machine implementation.

4. (20 points) Design an 8 Mbyte memory starting at address 00000000H using several 16 Mbit (4M x 4) SRAM chips. Design the memory so that it interfaces to a typical 32-bit microprocessor with 32 address lines.

(a) How many SRAM chips are necessary ?
(b) What is the highest memory address used ?
(c) Show the resulting memory map.

(d) Show the memory interface design including all important control signals and the connections to all of the 32 address lines.

5. (20 pts) A machine has the following memory reference instruction format:



The accumulator is the implied source/destination operand. The available addressing modes are:

I = 0 R = 0 Direct
I = 0 R = 1 PC Relative [Effective Address is the sum of the updated PC and the address field]
I = 1 R = 0 Indirect
I =1 R =1 PC Relative Indirect [Indirect mode after PC Relative mode]

The following lists the four PC - final operand address pairs. For each, what type of address calculation require the least amount of memory access given the PC values ? Answer this by finding the values of I, R bits and the address field. All addresses are in decimal.

a) PC 500 OP 200

b) PC 500 OP 400

c) PC 503 OP 236

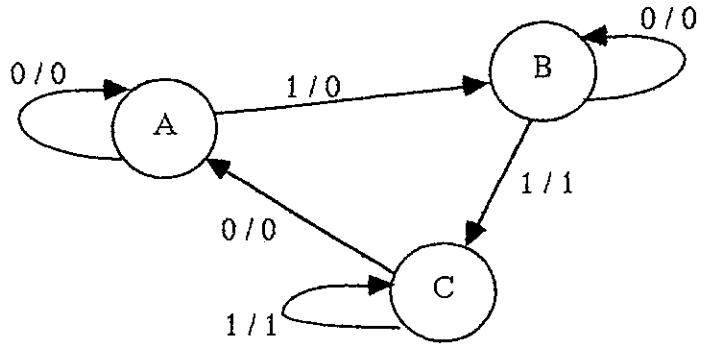
d) PC 2160 OP 2220

6. (10 pts) What are the similarities and differences between subroutine and interrupt ?

컴퓨터 분야

Qualifying Exam (1994.10) : Digital Design Problems

1. (20 points) Design the finite state machine corresponding to the following state diagram (use J-K flip-flops for full credit or D flip-flops for partial credit).



2. (10 points) Show the gate-level design for a master-slave D flip-flop (use only 1-4 input NAND, NOR, AND, OR and INVERTER gates).

3. (10 points) Simplify the following logic expression using a Karnaugh Map.

$$F = xy + x'z + wyz' + wxy + wz' + wx$$

4. (10 points) Redesign the state diagram of problem 1 as a Moore Machine.
(NOTE: Show the new state diagram ONLY.)

1990 년도

전자전기공학과 박사과정 자격시험 문제집

1990 1.22

성 명 : _____

학 번 : _____

QE
MICROPROCESSORS

정 홍

[1] 마이크로컴퓨터의 Three-bus system architecture에서 Bus의 종류를 말하고 그 기능과 데이타의 방향(uni/bidirectional)을 설명하시오.

[2] 마이크로컴퓨터와 I/O device 간에 데이타를 전송하는 대표적인 3가지 방법을 설명하시오.

[3] 다음 3개의 메모리 칩으로 구성된 마이크로컴퓨터 시스템의 memory map을 그리시오. 여기서 address는 memory map 상의 address를 나타낸다.

1. 12K ROM, 최종 address FFFFH
2. 24K RAM, 시작 address 0000H
3. 8K EEPROM, 시작 address 8000H.

[4] What is the difference between
1) Polled and daisy chain
2) Maskable and nonmaskable interrupts
3) Standard and memory-mapped programmed I/O
4) Internal and external interrupts.

[5] What is meant by a 16-bit microprocessor and a 32-bit microprocessor?

컴퓨터공학 분야

1. 반복된 binary sequence (0 1 2)를 발생하는 binary counter를 J-K flip-flop을 써서 설계하여 다음의 회로를 combinational circuit를 써서 완성하라. 여기서 상태는 AB, 즉, AB = (00,01,10).

2 (a) Memory-mapped Input/Output 을 Standard 혹은 Isolated Input/Output 와 비교하라.

(b) PLA 와 ROM 의 차이를 기술하라.

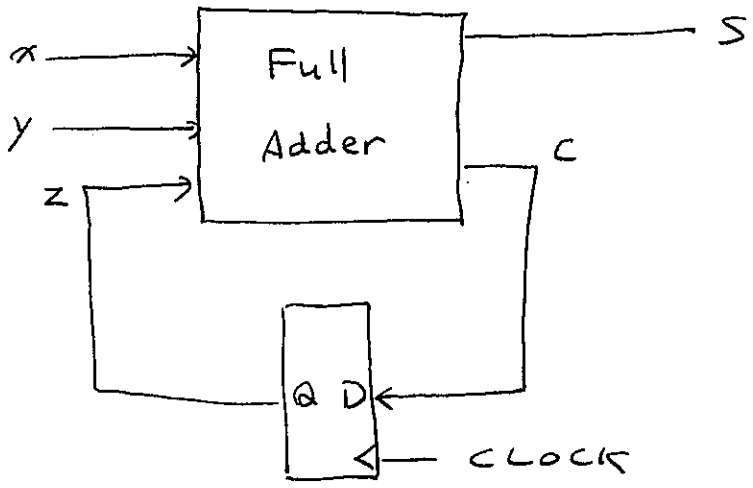
(c) 컴퓨터와 컴퓨터가 정보를 주고 받을때 어떤 Signal 을 사용하여 어떤 Protocol (규약)에 의하여 통신하는지 간략히 기술하라.

가) Parallel Communication 일 경우

나) Asynchronous Serial Communication 으로 나누어 기술하라.

[2] Given the Boolean function: F = xy + x'y' + y'z, implement it with only OR and NOT gates.

[3] Obtain the state table and state diagram of the following sequential circuit:

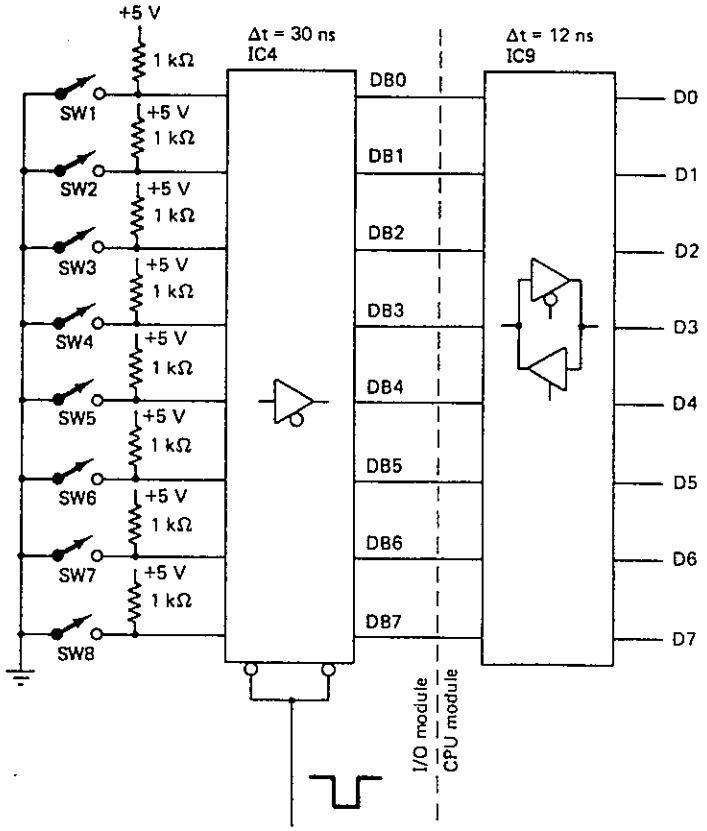


전산기 공학 컴퓨터 구조 분야

5. 한 줄에 alphabet 80자, 24줄을 쓸 수 있는 video display terminal 이 9600 baud rate 인 asynchronous serial I/O port에 물려있다. 화면 가득히 글자로 채울 때 걸리는 시간은? (1 start bit, 2 stop bit을 가정) (10점)

6. interrupt가 발생하면 이를 처리하기 위해 해당 interrupt service routine (ISR)이 있는 address로 jump 해야한다. 이를 위한 세가지 방법을 각각 설명하라. (20점)

7. 아래의 그림과 같이 8 개의 DIP switch의 상태를 Z80 에서 IN A, (74H) 명령문을 써서 읽으려한다. tristate buffer (IC4)를 active low로 control 하는 회로를 그려라. 참고로 Z80에서 system control signal에는 $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$ 가 있다. (20점)



DIGITAL SYSTEMS

[1] 다음을 간단히 답하라.

1) zx + zx'y 를 단순화하라.

2) Exclusive OR 게이트를 어떻게 Inverter 로 쓸 수있나 ?

3) 다수 게이트는 다수의 입력이 1 일때만 출력이 1 이다. Karnaugh Map 을 그리고 단순화하라.

4) Combinational 과 Sequential 회로의 차이점은 ?

5) Decoder 로 모든 Logic 을 구현할 수 있는가 ? 있다면 어떻게 ?

6) 2-input Exclusive OR 게이트를 어떻게 Inverter 로 쓸 수 있나 ?

7) Tri-State Logic 의 정의와 용도는 ?

[박사자격시험] QUALIFYING EXAM - Computer Engineering

November 7, 1993

Name [ ] GRADE [ ]

Digital Design

1. An Exclusive OR (XOR) gate is a 2-input gate whose output is 1 if and only if exactly one of its inputs is 1. (20)

(a) Draw a truth table for the XOR gate and show the minimum sum-of-products form for the XOR function.

(b) Implement the XOR function using 2-input NOR gates only.

2. Design a 3-bit modulo-6 binary counter (the counting sequence is 000, 001, 010, 011, 100, 101, 000, 001, ...) (30)

(a) using edge-triggered D flip-flops.
(b) using edge-triggered J-K flip-flops.

Microcomputers

3. Answer briefly the following using keywords.

1) What is a bus ? Why are they needed ? What are the three types of buses ? (5)

2) Which addressing mode is necessary for position independent coding (PIC) ? In PIC, the program may be loaded anywhere in memory for proper execution. (5)

3) _____ interrupt has been implemented if the interrupting device indicates the starting address of the routine used to service the interrupt. (5)

4) What is handshaking ? Why is it needed ? (5)

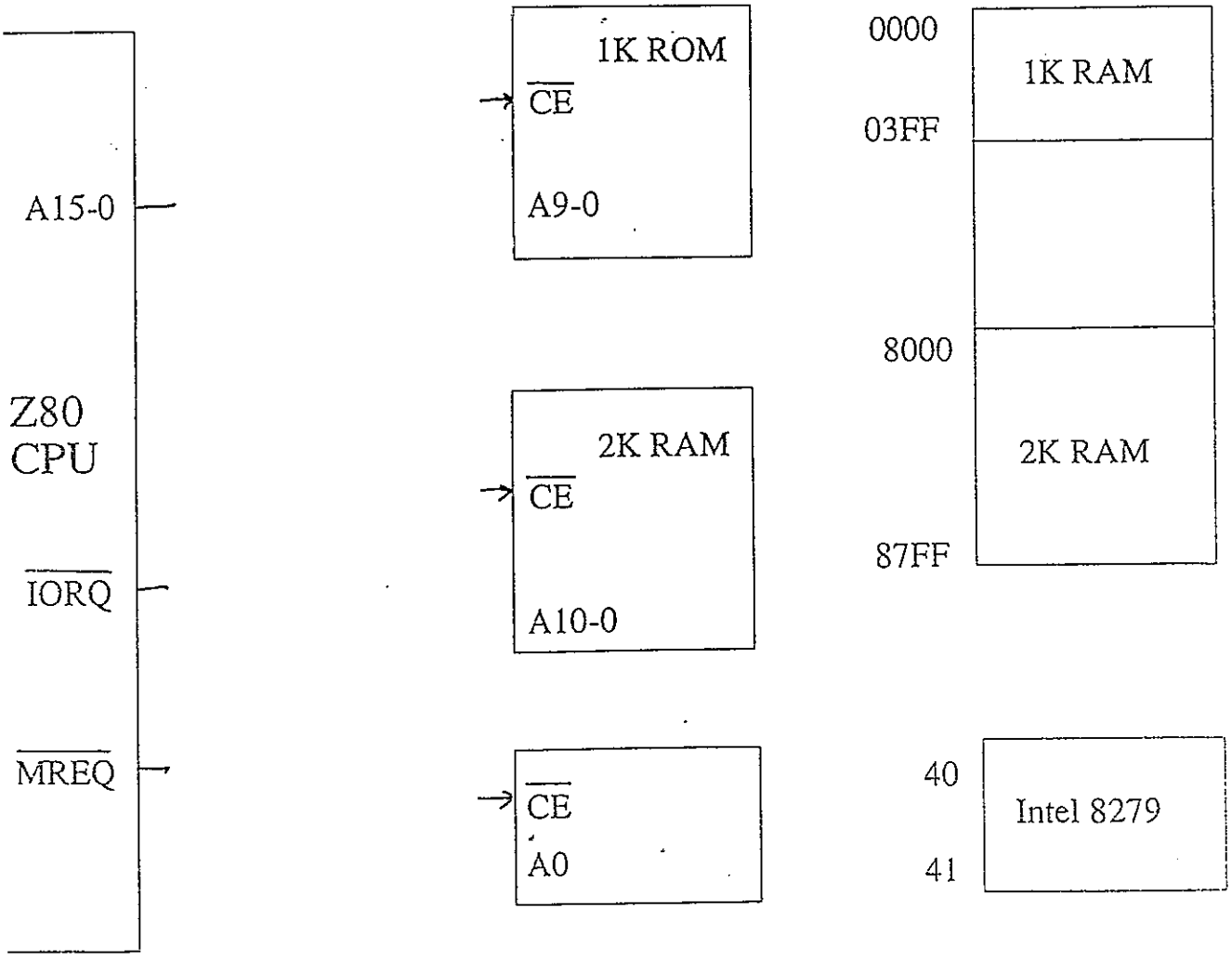
5) List two advantages and disadvantages of memory-mapped I/O compared with I/O mapped I/O. (5)

4. Consider the following program:

```
START: LD DE, 469FH ; load DE with 469FH
       LD HL, 2050H
       LD SP, 20C8H ; SP is the stack pointer
       PUSH HL ; PUSH pushes onto the stack
       EX DE, HL ; EX (1), (2) exchanges the contents of (1) and (2)
       EX [SP], HL; [SP] is the memory location pointed by SP
       RET
```

To what address does the RET instruction send the PC ? (10)

5. Design a simplest address decoding circuitry (circuit that drives the three CE signals) and then make appropriate connections in the following diagram. Partial decoding is allowed. Use the memory map as a guide. (15)



QUALIFIYING EXAM - COMPUTER ENGINEERING

OCTOBER 19, 1994

Name _____ Grade _____

1. A processor can address up to 64 K bytes of memory. How can it address 128 K bytes of memory ? (5)

2. List three reasons of interfacing the CPU to I/O ports, instead of directly interfacing to I/O devices. (5)

3. Compare and contrast polling and interrupt. (8)

4. Show the interconnection diagram that connects two registers to the bus so that each register can read from and write to the other one. Name the hardware and relevant control signals. (7)

5. A "decimal adjust" operation is used to adjust the result of an 8-bit binary addition so that the result is the same as that of a decimal addition. For instance

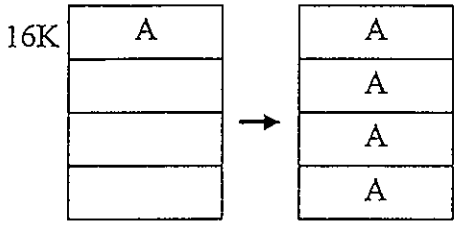
57			57		
+) 33			+) 49		
8A	--- binary addition		A0	--- binary addition	
90	--- after decimal adjust		1 06	--- after decimal adjust	

Write down a flowchart of the algorithm that does this decimal adjust. (7)

6. A 16-bit address microprocessor has the LDIR instruction which performs the following steps of operations:

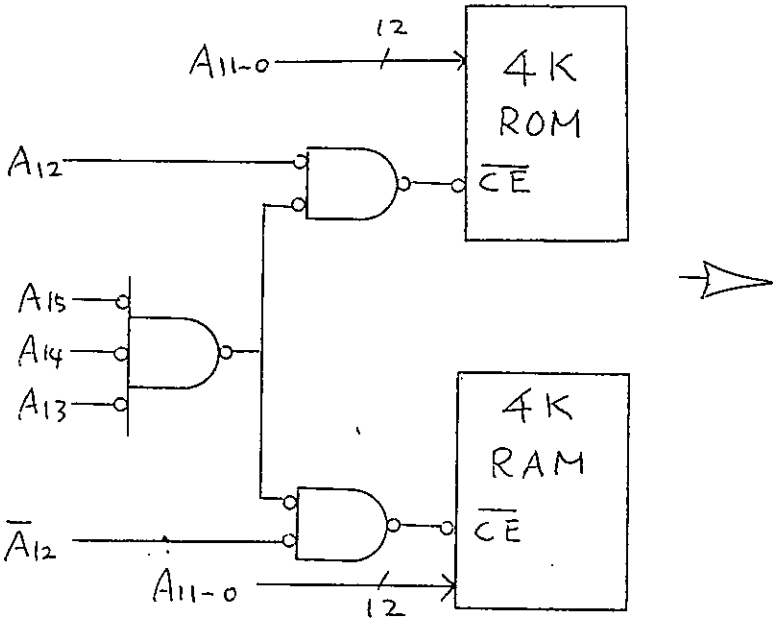
(HL) → (DE)
HL → HL + 1
DE → DE + 1
BC → BC + 1
REPEAT UNTIL BC = 0.

It essentially moves a block of memory data from one area to another.
Write a program for the following transfer using only LDIR and LD instructions:



LD (register pair), constant
loads the register pair (HL, DE, BC etc.)with a constant.

7. Redesign the memory interface in the following to cover the address range 4000 - 5FFFH.



COMPUTER ENGINEERING (DIGITAL SYSTEMS)

이름:_____ 점수:_____

1. (10 점) 디지탈 시스템은 COMBINATIONAL 이나 SEQUENTIAL 네트워크의 형태를 갖는다. 이 두가지 네트워크의 차이점을 설명하라.

2. (10점) SEQUENTIAL 네트워크는 ASYNCHRONOUS 시스템과 SYNCHRONOUS 시스템으로 나눌 수 있다. 이 두 시스템의 차이점을 기술하라.

3. (총 20점) MOORE 및 MEALY MACHINE MODELS:

3-1. (10점) SYNCHRONOUS 시스템에는 MOORE MACHINE 과 MEALY MACHINE 의 두가지 모델이 있다. 이 두 모델을 그린후, 동작을 설명하라.

3-2. (10점) MOORE MACHINE 과 MEALY MACHINE 의 STATE TRANSITION GRAPH 의 차이점을 기술하라.

4. (10점) 4-BIT 2'S COMPLEMENT NUMBER SYSTEM 에서 -5 는 어떻게 표현되는가?

Qualifying Exam: Digital Design Problems

1. (25 points) Design a logic circuit that detects a binary string "1100" from a continuous stream of binary signals. The circuit should use a minimum number of logic elements. An example of the response of the circuit is given below:

Input: 11001010110001101100110
Output: 00010000000100000001000

2. (total of 25 points):
   (b) (15 pts) Implement the logic function F, shown below, using 2-input NAND gates only (do NOT simplify the logic function for this part).
   (a) (10 pts) Produce the minimal sum-of-products form for the logic function F.

$$F = A'(B + C + D) + ACD$$

QUALIFYING EXAMINATION (DIGITAL SYSTEM)

(SPRING 1992)

학번: _____ 이름: _____ 점수: / 50

[1] (30 points)
다음의 각 서술이 올바르면 TRUE, 그렇지 아니하면 FALSE 라고 적고, FALSE 의 경우에는 서술을 바르게 고치든가 justify 를 하시오 (그렇지 않으면 무효임). 맞으면 각 2 점, 틀리면 감점 1 점 임.

1. Combinational circuit 의 출력값은 현재와 과거의 입력값에 의존한다. ( )

2. Asynchronous system 내의 신호의 흐름은 설계의 편의를 위해서 clock 으로 조절한다. ( )

3. Switching function 이 product-of-sums 형태로 나타나면 이는 다수개의 OR gate 와 1개의 AND gate 로 구현 될수있다. ( )

4. Switching function f(X1, .., Xn, 0, 1, +, .)의 dual 은 f(X1',..,Xn', 1, 0, ., +) 이다. ( )

5. Sum-of-products 형태의 switching function 을 얻으면 NAND gate 만으로 이를 구현할수 있다. ( )

6. K-map 에서 min. sum-of-products 을 구해 내면 그 expression 은 적어도 1개 이상의 essential prime implicant 를 포함하고 있다. ( )

7. Positive logic 에서 AND 기능을 하는 gate 는 negative logic 에서는 NAND 기능을 한다. ( )

8. PAL 은 user-programmable OR gate 와 non-programmable AND gate 들로 구성된다. ( )

9. ROM 을 설계할때 silicon 면적을 효율적으로 사용하기 위해서는 logic minimization 을 잘하는것이 중요하다. ( )

10. 일반적으로 parallel multiplier 가 serial multiplier에 비하여 연산 속도가 빠르다. ( )

11. Mealy machine 과 Moore machine 은 false output period 를 지난후 출력이 안정이 된다. ( )

12. Sequential circuit 중에는 global clock signal 을 필요로 하지 않는 회로도 있다. ( )

13. n-input XOR gate의 논리함수를 sum-of-product 형태로 나타내면 모든 product term 들은 minterm 이다. ( )

14. 3-input EQ gate와 3-input XOR gate의 논리기능은 같다. ( )

15. Hamming distance가 2인 code로는 1bit error의 correction이 가능하다. ( )

[2] (5 points)
Diode 를 사용하여 다음 함수를 구현하는 PLA (Prgrammable Logic Array) 회로를 그리시오.

out1 = AB' + BC, out2 = A'C' + BC, out3 = A'C' + AB'

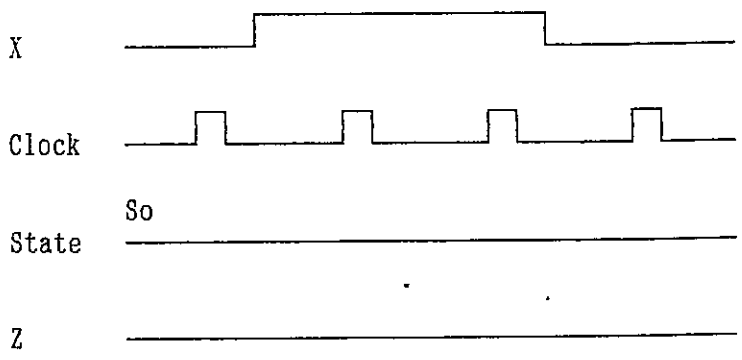
[3] (3 points) On a five-variable map (A,B,C,D,E), what are the five minterms adjacent to A'BC'DE ?

[4] (Total 6 points) Consider the following state table.

Present state	Next state X=0	Next state 1	output, Z X=0	output, Z 1
So	So	S1	0	1
S1	S2	S1	1	0
S2	S2	S3	1	0
S3	S0	S3	0	1

a. (2 points) Draw the corresponding state graph.

b. (4 points) Using the state table, complete the following timing diagram for the network, that illustrates the change of state (State) and output (Z). Indicate clearly when the changes occur by using vertical lines. Note that the initial state of the network is So. Assume that the F/F's used are positive edge-triggered type. Ignore any propagation delays.



[5] (Total 6 points) Compute the followings using the 2's complement system. Assume that six bits are used for the representation of the numbers.

a. (3 points) 15 + 18

b. (3 points) 18 - 25

Qualifying Exam: Microprocessors

3. 컴퓨터시스템에서 Bus 를 쓰는 이유는 ? Bus 의 세 가지 유형은 ? (5)

4. Polling 과 Interrupt 를 비교하라. (10)

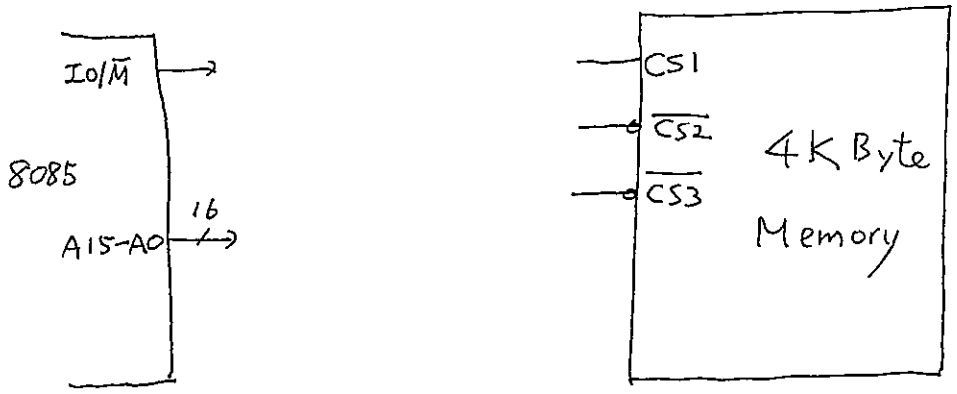
5. Emulation 이란 ? Simulation 과의 차이점은 ? (10)

6. Device 와 Device 간의 Handshaking 은 무엇인가 ? (5)

7. 8085 microprocessor 가 현재 다음과 같은 address map 을 가지고 있다. (20)

address range	decoding 방식
2000 - 2FFF	full
9000 - 9FFF	full

여기서 full decoding 은 16 개의 모든 bit 을 써서 decode 하는 방식이며 partial decoding 은 그렇지 않은 경우를 말한다. 이 시스템에 4KB memory 를 address 1000-1FFF 에 첨가확장하고자 한다. 또 8085 는 IO/$\overline{M}$ =1 일 경우 IO device , IO/$\overline{M}$ = 0 인 경우 memory 를 address 한다. 4 KByte memory 는 CS1 = 1, $\overline{CS2}$ = 0, $\overline{CS3}$=0 일때만 선택된다.



a) partial decoding 이 허용되는 경우 3 개의 chip select 입력으로 외부 gate 를 안쓰고 4K memory 를 addressing 할 수 있는가 ?

b) IO/$\overline{M}$ 와 A0-A15 에서 4K Memory 로 선을 연결하라.

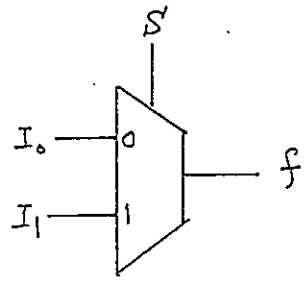
c) $\overline{CS3}$ = 0 로 둘 경우 CS1 와 $\overline{CS2}$ 만 연결하여 충분히 address decoding 이 되겠는가 ?

d) CS1 = 1 으로 둘 경우 $\overline{CS2}$ 와 $\overline{CS3}$ 만 가지고 충분히 address decoding 이 되겠는가 ?

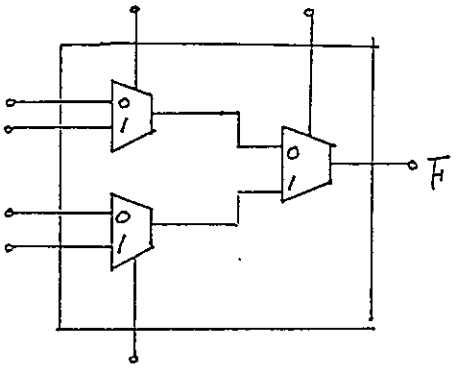
1. (총 15점) MUX를 사용하는 gate array logic module

1a) (5점) 아래 2-to-1 MUX의 논리 식을 적으라. 단 MUX는 control 신호가 '0' 일때는 '0' 입력신호가 선택되고, '1' 일때는 '1' 입력이 선택된다.

1b) (10점) 다음과 같은 gate array logic module 하나를 사용하여 논리기능 F = A + B + C 를 구현하라. 사용된 MUX는 위 문제의 MUX와 같은 종류이다. Module의 입력 신호로는 A, B, C만 있으며, complement 신호는 없다. 또, 필요하면 논리 '1' 신호와 '0' 신호는 입력으로 사용할 수 있다.

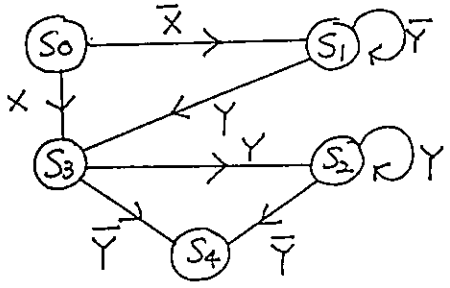


1a 그림

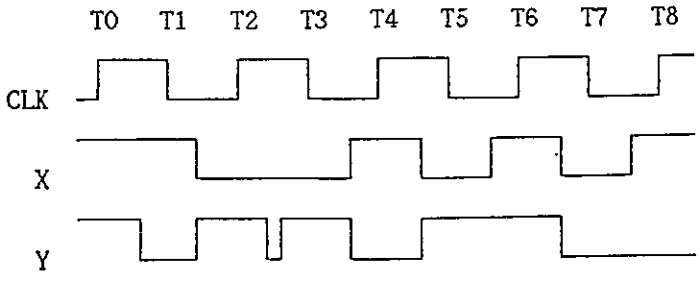


1b 그림

2. (총 10점) 다음 그림은 어떤 controller의 state diagram을 나타 내고 있다.

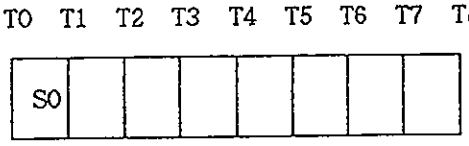


Clock 과 입력 X, Y가 다음과 같이 주어 질때

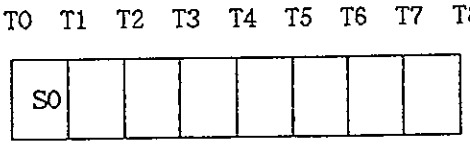


등기소자로 positive edge-triggered F/F을 사용할때와 negative edge-triggered F/F을 사용할때 다음 각 time interval 동안의 controller state를 적으라.
단, T0-T1간의 state는 S0로 가정하라.

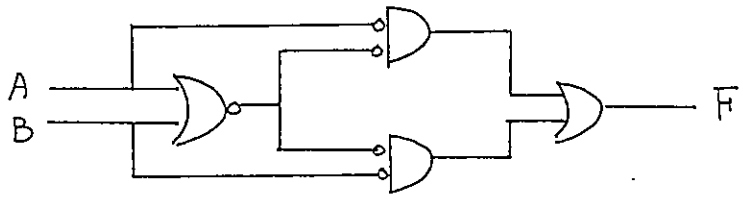
2a) (5점) positive edge-triggered F/F을 사용할때



2b) (5점) negative edge-triggered F/F을 사용할때



3. (총 5점)



3a) (3점) 위 회로의 논리 기능을 AND, OR, NOT 만을 사용하여 multi-level factored form 으로 기술하라.

3b) (2점) 이러한 기능을 가진 gate를 무엇이라고 부르는가?

4. (총20점) 1s' complement number를 2's complement number로 바꾸는 회로를 설계하고자 한다. 사용 bit 수는 sign bit를 포함하여 3 bit를 쓴다고 가정하자.

4a) (5점) 위의 number system에서 1s' complement 와 2's complement 로 표현할 수 있는 수의 범위는 무엇인가?
4b) (5점) 회로의 논리 기능을 truth table로 나타 내어라.
4c) (5점) Karnaugh map을 사용하여 최소화된 논리 식을 sum-of-products 형태로 구하라.
4d) (5점) NAND gate 만을 사용하여 위 논리식을 회로로 구현하라.

[6]. True or False (14 points)

다음의 각 서술이 올바르면 True, 그렇지 않으면 False라 적고, False 의 경우에는 서술을 바르게 고치든가 justify 를 하시오. (그렇지 않으면 무효임). 맞으면 2점, 틀리면 감점 1 점임.

a RAM use an RS flip-flop as the basic storage cell, but ROM use a single MOS capacitor.

b The indexed addressing mode is best suited for accessing sequential data and the register indirect addressing mode is best for nonsequential data.

c. All of the combinational logic of an address decoder can be replaced by a single ROM or PAL chip.

d. When several peripherals are controlled via programmed I/O, the last device polled has highest priority.

e. During a DMA data transfer, the CPU has no control over the system buses.

f. The CPU can always be interrupted by a nonmaskable interrupt.

g. The CPU can not be interrupted during the execution of an interrupt service routine.

[7] (20 points)

다음 질문에 간단히 답하시오.

a. List three ways of locating the address of Interrupt Service Routine.

b. List three ways of handling the priority of interrups in case of multiple interrupts.

c. What is the value of the stack pointer after the following program is run ?

```
LD  SP, 07FFH
CALL SUB
INC A
PUSH AF
PUSH BC
POP BC
HALT
```

d. Calculate the checksum byte for the four hex data bytes 10, 23, 45, and 04

[8] (6 points)

Arrange the following list of events in the order in which they occur as the CPU services an interrupting device.

a. The return address is placed on the stack.

b. The CPU is directed to the ISR by the interrupt vector.

c. The CPU returns to the main program.

d. The ISR is executed.

e. The CPU checks the interrupt disable flag.

f. The return address is put back in the PC.

[9] (10 points)

Calculate the time required for the 8-bit addition program listed below, assuming a 4-MHz Z-80 mivroprocessor is used. Consult the Z-80 instruction set description attached.

```
LD  IX, 0700H
LD A, (IX+0)
ADD A, (IX+1)
LD (IX+2), A
HALT
```

전자전기공학과

Qualifying Examination, April 2, 1994
Computer Engineering (Microprocessors)

[1] (10 점, Stack) What is the value of the stack pointer after the following program is run?

The code is as follows.

```
MOV     SP,07FFH
PUSH    B
CALL    Subroutine
POP     B
ADD     B
PUSH    B
HALT
```

[2] (10 점, Bus) The 74LS00 can source 400 μA in the high state and sink 8 mA in the low state. Based on this information, how many standard TTL loads ($I_{IH} = 40\mu A$ and $I_{OL} = 1.6mA$) can this chip drive? Here, I_{IH} and I_{OL} denote respectively, maximum logic 1 level input sink current and maximum logic 0 level output sink current.

[3] (10점, Memory) 다음 그림을 보고 16 bit 어드레스(AB0-AB15)로 구성된 메모리 맵을 그리시오. (힌트: Partial decoding)

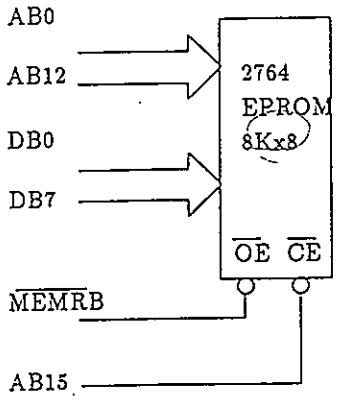


그림 1: 문제 [3]의 그림.

[4] (20 점, 설명)
(a) 마이크로프로세서 Bus 타입 3가지를 들고 차이점을 쓰시오.
(b) Macro와 Subroutine의 차이점을 드시오.

COMPUTER 분야

Qualifying Exam: Digital Design Problems

(10 pts) Problem 1: Assume that we are using an 8-bit 2's complement signed binary code.

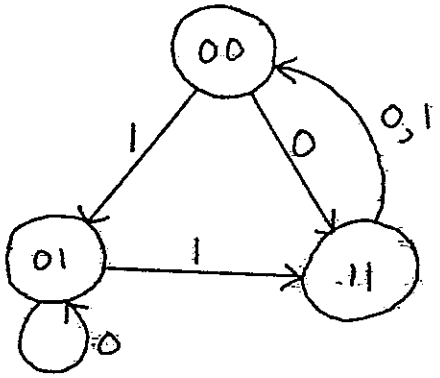
(a) Represent +11 and -29 in 2's complement notation.
(b) Add the above numbers.
(c) Represent the result in hex and in decimal form.
(d) What is the result (in decimal) of adding +59 and +69? Why?

(20 pts) Problem 2: Suppose $F1 = \Sigma(1, 3, 4, 5, 12, 14)$ with don't care conditions $d(6, 7, 13)$.

(a) Draw the Karnaugh-map (K-map) for $F1$.
(b) Using the K-map, write $F1$ in minimal sum-of-products form.
(c) determine the minimal product-of-sums form for $F1$.
(d) implement $F1$ using 2 to 4-input NAND gates only.

(20 pts) Problem 3: For the state diagram shown,

(a) obtain the state transition table.
(b) obtain the next-state equations.
(c) design the circuit using inverters, a 4-1 MUX and D flip-flops.
(d) implement the combinational part of the above circuit using inverters, OR-gates and a 2-4 line decoder with an enable input.



92/2 Qualifying Examination

Computer Engineering Area

92.9.29

Qualifying Exam: Digital Design Problems

1. (25 points) Design a logic circuit that detects a binary string "1100" from a continuous stream of binary signals. The circuit should use a minimum number of logic elements. An example of the response of the circuit is given below:

Input: 1100101011000110110011 0
Output: 0001000000010000000 1000

2. (total of 25 points):

(b) (15 pts) Implement the logic function F, shown below, using 2-input NAND gates only (do NOT simplify the logic function for this part).

(a) (10 pts) Produce the minimal sum-of-products form for the logic function F.

$$F = A'\overline{(B + C + D)} + ACD$$

$A'B + A'C + A'D$

$= A'\overline{B'C'D'}$

$A'B + A'C + A'D + ACD$

Qualifying Exam: Microprocessors

3. 컴퓨터시스템에서 Bus 를 쓰는 이유는 ? Bus 의 세 가지 유형은 ? (5)

4. Polling 과 Interrupt 를 비교하라. (10)

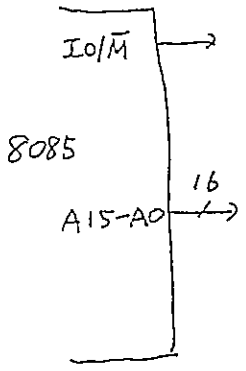
5. Emulation 이란 ? Simulation 과의 차이점은 ? (10)

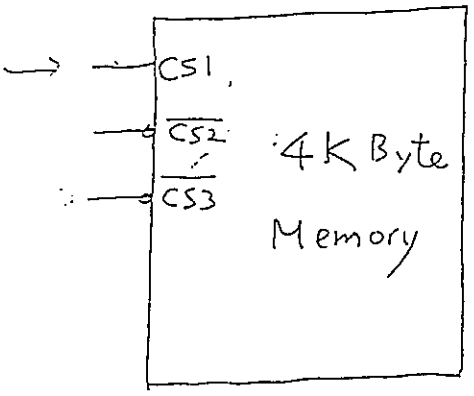
6. Device 와 Device 간의 Handshaking 은 무엇인가 ? (5)

7. 8085 microprocessor 가 현재 다음과 같은 address map 을 가지고 있다. (20)

address range	decoding 방식
2000 - 2FFF	full
9000 - 9FFF	full

여기서 full decoding 은 16 개의 모든 bit 을 써서 decode 하는 방식이며 partial decoding 은 그렇지 않은 경우를 말한다. 이 시스템에 4KB memory 를 address 1000-1FFF 에 첨가확장하고자 한다. 또 8085 는 IO/$\overline{M}$ =1 일 경우 IO device , IO/$\overline{M}$ = 0 인 경우 memory 를 address 한다. 4 KByte memory 는 CS1 = 1, $\overline{CS2}$ = 0, $\overline{CS3}$=0 일때만 선택된다.





0001
1FFF
0010
1001

a) partial decoding 이 허용되는 경우 3 개의 chip select 입력으로 외부 gate 를 안쓰고 4K memory 를 addressing 할 수 있는가 ?

b) IO/$\overline{M}$ 와 A0-A15 에서 4K Memory 로 선을 연결하라.

c) $\overline{CS3}$ = 0 로 둘 경우 CS1 와 $\overline{CS2}$ 만 연결하며 충분히 address decoding 이 되겠는가 ?

d) CS1 = 1 으로 둘 경우 $\overline{CS2}$ 와 $\overline{CS3}$ 만 가지고 충분히 address decoding 이 되겠는가 ?