Large-Scale Photonic Integrated Circuits

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***Abstract*—In this paper, 100-Gb/s dense wavelength division multiplexed (DWDM) transmitter and receiver photonic integrated circuits (PICs) are demonstrated. The transmitter is realized through the integration of over 50 discrete functions onto a single monolithic InP chip. The resultant DWDM PICs are capable of simultaneously transmitting and receiving ten wavelengths at 10 Gb/s on a DWDM wavelength grid. Optical system performance results across a representative DWDM long-haul link are presented for a next-generation optical transport system using these large-scale PICs. The large-scale PIC enables significant reductions in cost, packaging complexity, size, fiber coupling, and power consumption.**

***Index Terms*—Integrated optoelectronics, optical fiber communication, optical receivers, optical transmitters.**

I. Introduction

THE EXPLOSIVE "Moore's Law" growth of integrated electronics [1], along with the similarly explosive growth of the Internet, has contributed to growing demand for communications networks offering greater bandwidth and flexibility at lower cost. Monolithic InP-based photonic integrated circuits (PICs), if able to provide sufficient functionality, performance, and cost reduction, offer compelling solutions for such networks, while also providing the same inherent scalability that has benefited Si-based integrated electronics. However, since the early proposals for photonic integration [2]–[5], progress in InP PIC technology has been relatively slow. Today, large-scale PICs (LS-PICs) with high levels of integration (>50 components/chip) remain confined to the laboratory. There are myriad reasons for this slow rate of maturity. Numerous technological barriers associated with InP semiconductor processing have been one of the strongest inhibitors—including difficulty in achieving the requisite process uniformity and reproducibility—on a manufacturing scale—in such processes as epitaxy, lithography, dry etching, etc. Additionally, monolithically integrating numerous devices and functions, while at the same time minimizing process complexity, has proven challenging from a design standpoint, due to requirements associated with active/active and active/passive transitions, electrical and optical isolation, compromises in discrete device performance, etc. As a result, early versions of LS-PICs, even if successful in demonstrating useful functionality, have fallen short in demonstrating the levels of performance and manufacturability necessary to achieve commercial viability. It is also interesting to note that "industry pull" may have played a role in this slow development path, particularly in the past 10 years. Since all-optical wavelength division multiplexing (WDM) networks based on Erbium doped fiber amplifier (EDFA) technology rose to prominence in the 1990s, meeting the demands of telecommunications bandwidth while in effect circumventing the need for optical-electronic-optical (OEO) conversion, the motivation for commercial development of large scale photonic integration that would enable such approaches was somewhat dampened.

In this paper, we report the design and operating characteristics of the first commercially deployed monolithic large-scale PICs providing transmit and receive functions. These LS-PICs were developed to be consistent with the functionality, cost, and reliability requirements of a new telecommunications network architecture termed a "digital optical network" wherein OEO regeneration and add–drop functionality can be drastically increased throughout the network due to the cost reduction enabled by the integration of ten transmitter channels and ten receiver channels onto photonic integrated circuits. The transmitter (TX) PIC includes over 50 discrete functions integrated monolithically on a single chip, spread over ten channels with an aggregate data capacity of 100 Gb/s. The monolithic receiver (RX) PIC supports a similar aggregate data rate of 100 Gb/s—the first time a matched TX/RX pair operating at this data rate has been produced. The chips are manufactured on InP substrates, leveraging many of the advances in III-V semiconductor processes manufacturing that have arisen in the past decade. This level of integration is more than an order of magnitude greater than previously demonstrated in a commercial system, and thus represents a significant milestone in PIC development.

II. Progression of Photonic Integrated Circuit Development

Recent concurrent trends suggest that the timing may be right for commercial development of LS-PICs, both from the perspective of technological capability and market receptiveness. Steady progress in the InP components field in the last 10 years has led to improved InP process capability, which has

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contributed to not only significant progress in the performance and commercial availability of discrete devices, but also the commercial introduction of the first InP-based PICs, with 2–4 integrated functions. Such progress has helped to lay the groundwork for a LS-PIC technology meeting increasingly aggressive cost requirements, as will be further described in this paper. Additionally, it is increasingly clear that the economics of current WDM networks are optimal only for maximum capacity and reach, and do not scale well to new demands for greater flexibility (e.g., add–drop functionality). As a result, industry acceptance for complex LS-PICs as the enabling foundation technology in new OEO-based telecommunications schemes may prove stronger in the future.

Improvements in InP fabrication/process capability have progressed on multiple fronts, and have had profound impact on technological capability. InP substrate quality has improved consistently over the past 20 years, and now conductive substrates are available to 4 inch diameters with dislocation etch pit densities (EPD) of less that 500 cm^{-2}, rivaling GaAs. Fe-doped semi-insulating substrates have also improved; boules grown using the vertical gradient freeze (VGF) technique and exhibiting EPDs of less than 5000 cm^{-2} have become recently available. Manufacturers are also now reporting availability of substrates up to 6 in in diameter. Metalorganic vapor phase epitaxy (MOVPE) equipment has undergone an even more dramatic revolution. The current generation of manufacturing-capable multiple wafer MOVPE reactors became available in the early 1990s, and with refinements since then, are now capable of consistently producing wavelength uniformities of $1\sigma \sim 3$ nm or better, thickness uniformities of better than $\pm 2\%$, and defect (particle) densities approaching 1 cm^{-2}, on 3- and 4-in InP substrates. These levels of demonstrated performance, along with concurrent improvements in system reliability and increasing use of statistical process control methodologies, have been essential to enabling manufacture of progressively more complex photonic integrated circuits by ensuring a consistent materials baseline from which to build. Developments in the dry etching field, in particular in the areas of improved sidewall roughness and cross-section targeting, have also contributed to overall improvement in InP process capability. Relevant etching techniques include reactive ion etching (RIE), and its more versatile variants: electron cyclotron resonance (ECR) and inductively coupled plasma (ICP) etching, which employ high-density plasmas to achieve high etch rates with good uniformity and reduced damage. Other areas in which improvement has made significant impact on overall InP process capability includes fine-line lithography and interconnect metallization.

Improved InP process capability has led directly to commercial impact with the growing deployment of the first photonic integrated circuits in the optical transport network. The simplest photonic integrated devices are spot size converter (SSC) integrated lasers [6]. Electroabsorption modulated lasers (EMLs), consisting of a continuous-wave (CW) DFB or DBR laser integrated with a passive transition element and an electroabsorption modulator (EAM) to provide modulation bandwidths in excess of 10 Gb/s, were introduced more than a decade ago [7], [8]. The communication data rate possible using the EML exceeds that possible using commercially available directly modulated lasers (DMLs) for long-reach and intermediate reach telecommunications applications [including dense WDM (DWDM) applications]. Commercial tunable lasers, to address sparing and emerging optical add/drop multiplexer (OADM) applications, have taken advantage of integration techniques in a variety of ways. The tunable sampled grating (SG) DBR laser represents one such approach [9], [10], employing a four-section DBR laser with integrated gain, phase, and two tunable grating sections. More recently, single channel DBR and SG-DBR lasers have been integrated with EAMs to provide a tunable 10 Gb/s EML [11], [12] and a single-channel tunable SG-DBR laser with integrated SOA has also been developed [13]. Both of these innovations have resulted in an increase in PIC complexity (in terms of functions/chip) by 2–4 times. Another example of a commercially available PIC developed to address the tunable laser market is the wavelength selectable laser array [14]. This device employs multiple laser (DFB) channels that are combined to a single output, so provide no increase in functionality despite a somewhat more complex integration scheme. All of these small-scale PICs meet the performance, cost and reliability requirements for deployment in the telecommunications network. However, their functionality remains limited with the relatively low level of integration ($\leq$5 integrated functions/chip), and as such they cannot address more complex system needs, such as full-scale OEO conversion in a DWDM system. Higher levels of integration (up to 12 independently addressable channels) have been achieved in data communication using parallel optical arrays of GaAs-based vertical cavity surface emitting lasers operating at 10 Gb/s [15], [16]. However, such devices are currently limited to short-reach applications and cannot provide for sophisticated functions such as OEO conversion.

More complex PICs have been demonstrated in the laboratory, and while this work has not yet proven commercially viable, it has proven crucial in furthering the groundwork for commercial LS-PICs. Multiple wavelength EMLs [17], [18] include an array of DFBs integrated with a multimode interference (MMI) combiner into a single output channel, followed by an SOA and an EAM. Aside from the discrete wavelength steps between channels in the array, continuous wavelength tuning of the entire array is possible using a thermoelectric cooler (TEC). Arrayed waveguide grating (AWG) [also known as a phased array grating (PHASAR)] technology [19] enables more complex frequency-selective integration schemes, and such functionality may be indispensable to LS-PIC design. Demonstrations of AWG integration into transmitter and receiver PICs include multiplexed laser sources [20]–[22] and demultiplexing receiver PICs [23]–[26]. In the latter demonstrations, the AWG is used to demultiplex from a multiwavelength input, into a multiple element array of photodetectors, for channel-level detection. Other uses of AWGs in more complex PIC's include a lossless 16-channel wavelength selector, making use of two AWGs in series with an array of SOAs [27], a 2×2 optical cross-connect using four AWGs in a single chip with Mach–Zehnder Interferometers (MZIs) [28], and a multichannel modulation circuit employing eight channels of SOAs and EAMs with a single AWG with 25-GHz spacing [29].

While crucial in establishing a technological foundation from which to build, these examples provide neither the requisite functionality nor the demonstrated performance and yield/manufacturability upon which to base commercial DWDM carrier network architectures. These failures have several origins. For one, much of the PIC research described in the literature is not closely coupled to a network systems development. As a result, critical functionality required for commercial network operation is missing. Moreover, academic R&D is by nature focused on early-stage demonstration, while largely neglecting manufacturability and reliability concerns that are of principal importance to enabling commercial network deployment of LS-PICs.

That InP device and PIC development has made such significant progress is a testament both to the amenability of this materials system to various integration strategies, and to steady maturation of the underlying process technologies. However, until now the feasibility of producing PICs with a high level of integration ($\gg$10 components), and with performance and yield sufficient to meet the demands of commercial networks, has been generally regarded to be extraordinarily low—and corporate spending toward such development has reflected this notion. Indeed, with the complexities presented by relatively immature InP process technologies, and given the high level of synergy required between PIC design and fabrication on the one hand, and system architectural design and construction on the other, the barrier to demonstrating a commercially relevant and viable large-scale PIC technology has been extraordinarily high.

III. Photonic Integrated Circuit Architecture and Fabrication

A. DWDM Transmitter PIC Architecture

In the "Digital Optical Network," the transmitter (TX) LS-PIC is responsible for electrical to optical conversion, while the paired receiver (RX) PIC is used for complementary optical to electrical conversion. This architecture features a 100 Gb/s (10 channels $\times$ 10 Gb/s) LS-PIC DWDM transmitter, with each channel operating at an aggregate data rate of 10 Gb/s (line rate of 11.1 Gb/s with forward error correction (FEC) overhead) on a 200-GHz International Telecommunication Union (ITU) wavelength grid in the C-band. A schematic of the TX LS-PIC is shown in Fig. 1. In simplest terms, the optical signals in each of the ten monolithic channels originate in an active section, and are multiplexed into a single output channel in a monolithically integrated passive region. The active train of each monolithically integrated channel includes a tunable EML—a tunable DFB laser integrated with an EAM operating at a data rate of 10 Gb/s. The EMLs are individually controlled with DC bias on the DFBs, and 10 Gb/s input on the EAMs. The wavelength is chirped across the monolithically integrated DFB array to yield ten distinct and highly controllable wavelengths that can each be fine-tuned to the ITU grid individually at the channel level. A photodiode is monolithically integrated into the back of each channel, to provide optical power monitoring (OPM) of the DFB over the lifetime of the chip. Control of the output power profile across all channels is enabled with a monolithically integrated variable optical attenuator (VOA), essentially an absorber in the active train light path of each

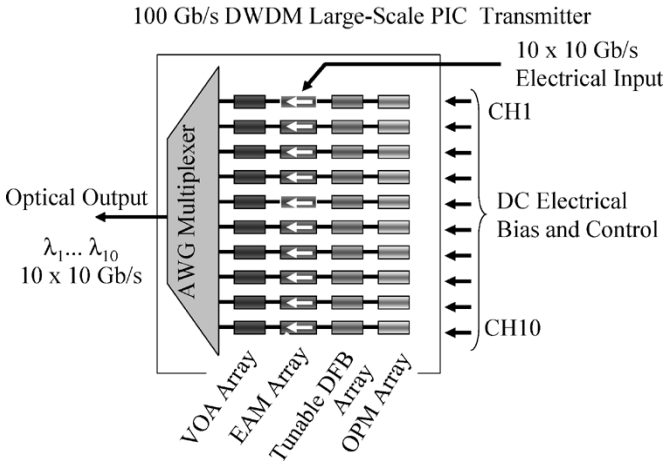

Fig. 1. Schematic of the architecture of the ten-channel LS-PIC transmitter chip. The transmitter PIC incorporates over 50 functions monolithically integrated on a single chip.

channel. Multiplexing the ten wavelengths into a single output channel is accomplished with an AWG router monolithically integrated in the passive section of the chip. The single output channel is terminated in a spot size converter for optimized fiber coupling. AWGs are ideally suited for LS-PICs, given their integrability in InP, high channel count and low insertion loss characteristics. This chip represents the first realization of the combined functionality—10 Gb/s modulated source integrated with continuous tunability, AWG frequency selective multiplexing, and power profiling through the use of VOAs, all operating at performance levels required by commercial class carrier networks (as will be described in detail in subsequent sections of the paper).

B. DWDM Receiver PIC Architecture

The RX PIC is similarly configured. A single input channel is routed into a spot-size converter and subsequently through a polarization independent demultiplexing AWG in the passive section of the chip. Here, the frequency selectivity of the AWG filter is optimized to achieve sufficiently low channel-to-channel crosstalk, as well as acceptably low insertion loss. PIN photodiodes (PDs) are monolithically integrated into the waveguides at the output of the AWG. Key operating characteristics of the PD's include responsivity, modulation bandwidth and dark current. These RX PICs represent the first demonstration of such a combination of integrated functionality and performance—high speed (10 Gb/s) waveguide photodetectors integrated with a 10 channel demultiplexing AWG. Further quantitative details of the operating characteristics of these RX PICs will be described in the following sections of this paper and will demonstrate the viability of such devices in achieving ten-channel DWDM PIC-PIC links with performance consistent with that required for deployment in a carrier-class long-haul telecommunications network.

C. PIC Fabrication and Packaging

The LS-PICs are fabricated using conventional, yet state-of-the-art InP processing techniques. A block diagram of the PIC fabrication flow is show in Fig. 2. The fabrication of the PICs

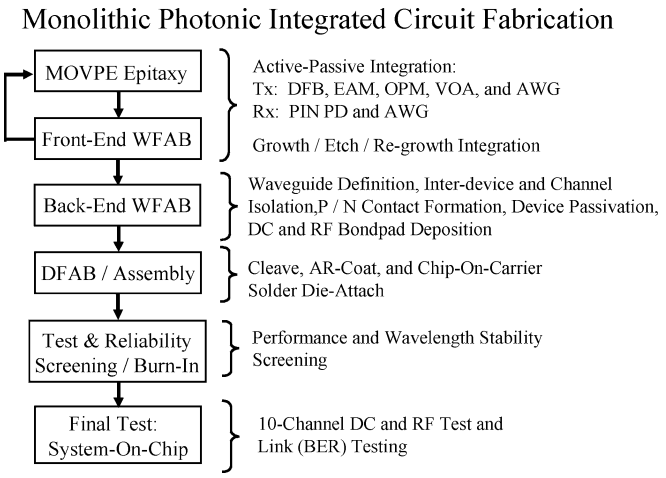

Fig. 2. Process flow for the fabrication of photonic integrated circuits described herein. An array of 10 DFBs, 10 EAMs, 10 OPMs, 10 VOAs, and an AWG are simultaneously monolithically integrated on a single LS-PIC transmitter chip. In addition, 10 PIN PDs and an AWG are simultaneously monolithically integrated on singe PIC receiver chip.

begins with the formation of the multiple epitaxial layer structures required to achieve the simultaneous monolithic integration of the numerous active and passive devices on the PIC chips. The epitaxial layers are grown using MOVPE in multiwafer reactors. The active elements (DFB, EAM, OPM, and VOA) of the monolithic transmitter LS-PIC consist of multiquantum well (MQW) active regions whereas the passive regions (waveguides and AWG) consist of bulk double heterostructure (DH) waveguides. For the Rx PIC chip, the active region of the PIN PD is a bulk DH as are the passive regions (waveguides and AWG). Conventional growth-etch-regrowth techniques (e.g., as described in [5], [30], and [31]) are utilized to monolithically integrate the multiple epitaxial layers. The epitaxial reactors and growth processes require control of compositional, strain, and thickness uniformity (in-wafer, wafer-to-wafer, and run-to-run) similar to or exceeding that required for the growth of vertical cavity surface-emitting lasers [32], making the epitaxy that is employed in the fabrication of the DWDM PICs described in this paper among the mostly highly controlled of any III-V device.

After the epitaxial (re)growths and front-end wafer fabrication (patterning and etching) are complete, the PIC wafers are subjected to a back-end wafer fabrication process sequence. These wafer fabrication processes are similar to that used to form a heterostructure bipolar transistor (HBT) integrated circuits [33], [34], both in complexity and number of mask levels. Specifically, the back-end wafer fabrication is performed to define the active/passive waveguides, form interdevice and channel–channel electrical isolation, contact p and n regions of the active devices, form DC and RF bondpads, and facilitate passivation of the devices, The precise control of critical dimensions (e.g., waveguides) are realized via dry-etching (using both conventional RIE and high-density plasmas). These processes result in a very high degree of control of such parameters as waveguide width, etch depth, sidewall roughness, etc. that are required to achieve the precise control of wavelengths while simultaneously maintaining low loss of all elements within a channel, from channel-to-channel, and between the active and passive regions. Finally, conventional metallizations and dielectric deposition techniques utilized to fabricate III-V optoelectronic devices are employed in the fabrication of the DWDM PIC devices described herein.

After the wafer fabrication steps are complete, the wafers are subjected to a die fabrication sequence wherein they are singulated into individual die (via cleaving) and each die is coated with an antireflection coating. The die are subsequently solder die-attached to a submount. Next, the resultant chip-on-carriers are subjected to a test and reliability screening/burn-in sequence to screen for performance and wavelength stability. Wavelength stability is extremely critical in a monolithic DWDM PIC to ensure that all devices can maintain their requisite performance on the ITU grid over life. The PIC fabrication sequence is completed by a rigorous final test sequence that includes DC and RF testing (including the measurement of the bit-error rate (BER).

Many of the fabrication specifications—from epitaxy to etching—are highly demanding, even using current state-of-the-art processes. The combination of these factors underlies the long-held concern that LS-PIC manufacturing is infeasible from a yield and cost standpoint. However, we have found that through appropriate attention to process development, diligent simplification of the processes and process sequence, and application of rigorous manufacturing process controls, sufficiently high yields are in fact possible to realize large-scale integration with the requisite performance. This will be evidenced by the high degree of uniformity achieved within the LS-PICs reported in Sections IV and V.

Subsequent to the assembly of the DWDM PIC transceiver line cards, the monolithically integrated PIC chip-on-carriers are soldered on a thermoelectric cooler (TEC) and enclosed in a metal package. For the TX LS-PIC, one single mode fiber is optically coupled to the output of the TX multiplexer, and a ten-channel monolithic modulator-driver ASIC array is electrically coupled in a hybrid fashion to the modulators. A photograph and block diagram of the fully packaged TX LS-PIC is shown in Fig. 3. The RX PIC packaging is similar, including a lensed fiber coupling to the input of the RX multiplexer, and a transimpedance amplifier (TIA) array electrically coupled in a hybrid fashion to the PDs on the PIC.

IV. Photonic Integrated Circuit Performance

A. 100-Gb/s DWDM Transmitter PIC Performance

The DFBs have been optimized for high yield manufacturing and integration into the transmitter PIC. A typical light versus current/voltage (L-I-V) plot of the DFB laser array is shown with all ten channels superimposed in Fig. 4. The data was taken using the per channel OPM shown in Fig. 1 as the detector. The lasing threshold (Ith) for all channels ranges from 20–28 mA. A typical voltage at turn on is 1.2 V. The devices exhibit a forward resistance of 5.5 $(+/-0.3)$ Ω and operate in a current range of 60–80 mA, typically. This bias allows the DFBs to deliver sufficient power per channel into the fiber at the output of the integrated transmitter chip to effectively transmit data across all long-haul links encountered in real world networks (see Section IV).

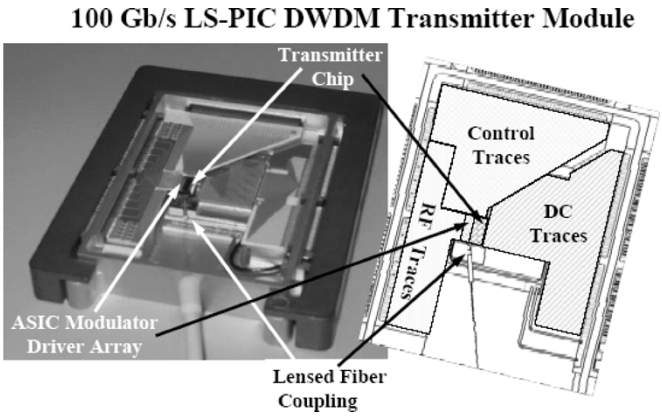

Fig. 3. Photograph and schematic of the 100 Gb/s DWDM LS-PIC transmitter module with the hermetic lid removed.

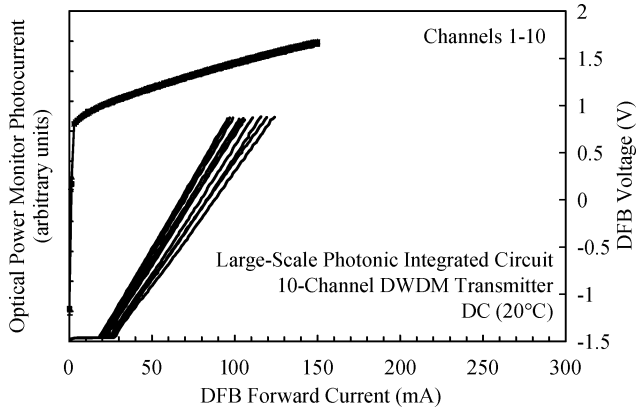

Fig. 4. Typical light-current-voltage (L-I-V) characteristics for the LS-PIC transmitter. The optical power is monitored via the monitor photodiode.

Narrow laser linewidth is critical for a transmission link in which an external modulator is used. A broad linewidth results in signal distortion which degrades the BER performance and optical-signal-to-noise (OSNR) in the link. A typical linewidth spectrum of a single DFB on the LS-PIC transmitter is shown in Fig. 5. The linewidth was measured using a delayed self-heterodyne technique. The DFB is running CW at an operating current of 67 mA ($>3 \times$ Ith), and the light is transmitted through the entire LS-PIC and into the fiber. The data fits well to a Lorentzian curve giving a full-width-half maximum (FWHM) linewidth of 2.3 MHz. Thus, the linewidth performance of the LS-PIC transmitter exceeds the 10-MHz spec of most state-of-the-art commercial standalone DFBs [35]–[37], and the 10 MHz [38] to 20 MHz specification [39] of commercial EMLs.

Data is encoded for optical transmission on each channel of the LS-PIC via electro-absorption modulators (EAMs). The dc transfer characteristic of the modulator is key in minimizing the waveform distortion in the network. A typical transfer function for an EAM on the LS-PIC transmitter is shown in Fig. 6. The modulator is capable of a dc extinction of -19 dB at less than -3 V reverse bias and is representative of the performance of other channels of the array. The maximum extinction as well as the extinction per volt realized in the LS-PIC is comparable to or exceeds the specification of currently sold two-element EMLs [38], [39].

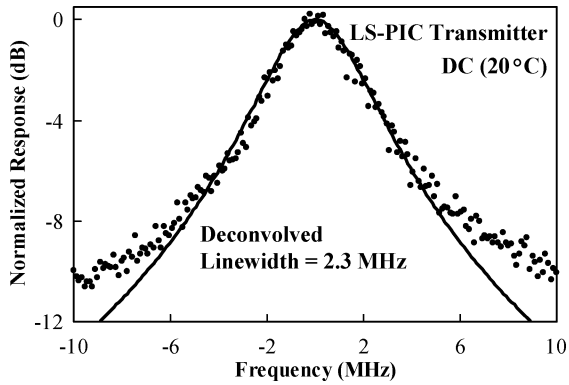

Fig. 5. Linewidth spectrum of a single DFB from a LS-PIC transmitter chip under direct current (DC) operation at 20 °C.

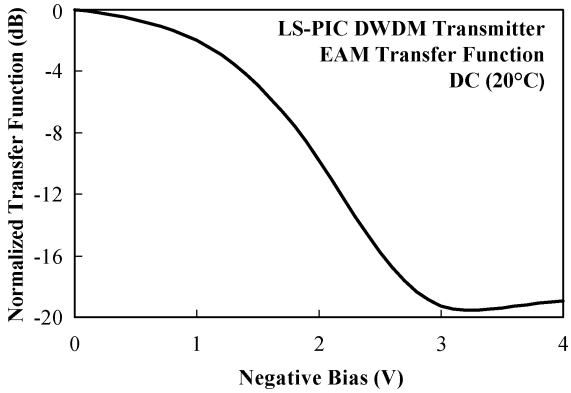

Fig. 6. Power transfer function of the electrabsorption (EA) modulator on the LS-PIC transmitter. Extinction ratio and extinction per volt rival that of the best commercial two-element (single-channel) EMLs.

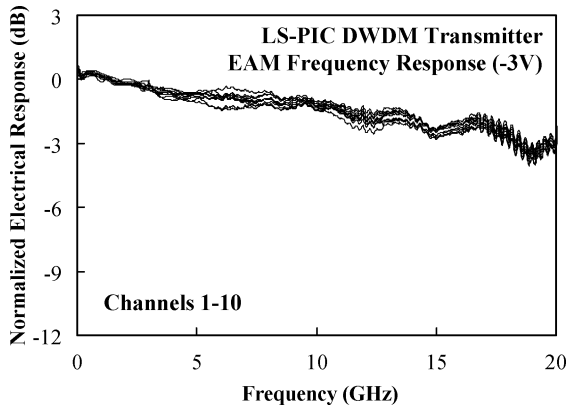

Fig. 7. Small signal frequency response for the EAM of a DWDM LS-PIC transmitter chip.

The small signal frequency response for a chip on carrier was measured using an Agilent 8703B Lightwave Component Analyzer. The response versus frequency curves for all ten channels have been superimposed and are shown in Fig. 7. The -3-dB bandwidth is better than 17 GHz for the worst channel. The variation in frequency response from channel-to-channel is on the order of 0.5 dB and largely due to variation in error of measurement with probe placement. The ripple on the plots is a combination of small electrical reflections from the PIC layout and reflections internal to the probe. This data indicates that the unifor-

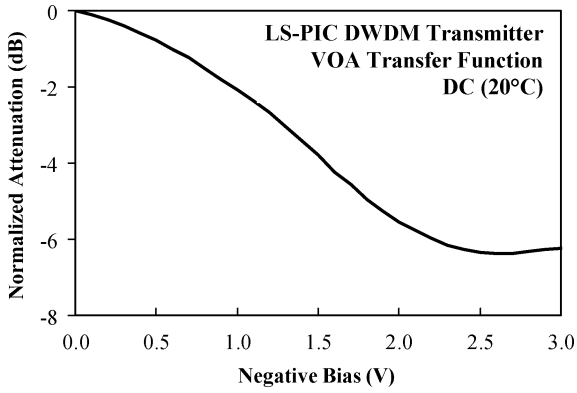

Fig. 8. Power transfer function of a VOA from the DWDM LS-PIC transmitter.

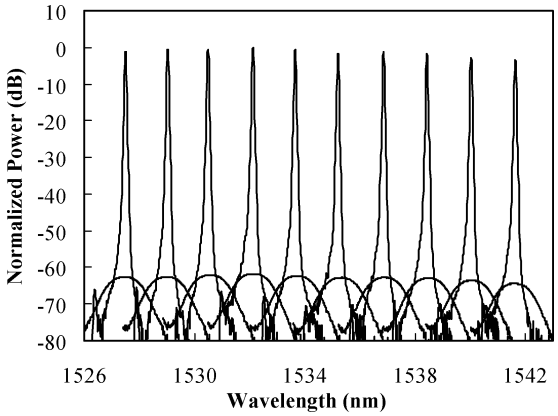

Fig. 9. Superposition of the ten-channel DFB spectrum with the AWG multiplexer transmission function for the ten-channel DWDM LS-PIC transmitter. The DFB and AWG are aligned using the per channel tuning elements with <0.1 dB power loss resulting from misalignment between the AWG and DFB.

mity of the modulator capacitance and the impedance matching of the bond pad configuration across the array is very high.

The variable optical attenuators are used to control the shape of the ten-channel output power spectrum. They are the last element in the transmitter signal chain before multiplexing the signals from all channels via the AWG. This capability is critical to flattening the transmitter power spectrum before it is launched into the fiber as we will show in Section IV. In addition the VOAs can be used to compensate for any small differences in output power between the DFBs over their lifetime. The dc transfer function for a typical VOA element is shown in Fig. 8. An attenuation range of 5.5 dB is possible by employing between 0 and -2 V reverse bias.

In Fig. 9, we superimpose the DFB spectrum with the AWG multiplexer transmission function. This is achieved by forward biasing the EAMs to produce an spontaneous emission source to map the AWG passbands. The center position of the AWG passband comb is tuned using the TEC in the packaged module to match the ITU grid. Each DFB is subsequently individually thermally tuned onto the ITU grid as well. The tunable DFBs are further employed to account for small frequency drifts to maintain the frequency of each channel to within $+/-3$ GHz over life. The tuning range of the DFBs exceeds 300 GHz (data not shown). Control of the relative channel spacing aperiodicity on the 200 GHz grid for the AWG passbands is better than $+/-4$ GHz (one sigma of a normal distribution). The loss penalty due to misalignment of any AWG passband to the ITU grid for the transmitter is less than 0.1 dB.

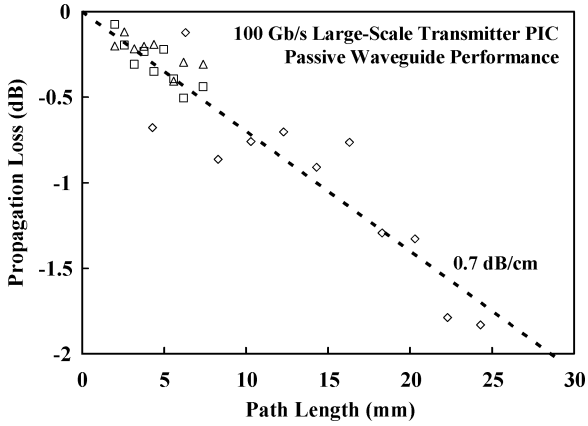

Fig. 10. Propagation loss measured using a series of waveguides of varying lengths for the passive waveguide structure employed in the DWDM transmitter PIC. The best fit to the data indicates a propagation loss of ~0.7 dB/cm.

Another point highlighted by the data in Fig. 9 is the tight manufacturing tolerance needed to maintain accurate alignment of the DFB and AWG arrays to the ITU grid over life. The AWGs are low loss but require precise epitaxial control in thickness and composition as well as tight waveguide width tolerances to ensure uniform passband spectra and high yield to alignment of the center channel to the ITU grid at a predetermined initial chip temperature. The DFB arrays must be fabricated to emit over a narrow range of initial wavelengths across all 10 channels in order to allow enough margin for the tuning elements to maintain the wavelength on the ITU grid over life. This alignment implies excellent manufacturing control of the DFB grating pitch, waveguide width, coupling length, epitaxial thickness and composition during both growth and regrowth. Commercial viability requires this manufacturing accuracy where per channel power leveling, absolute power output, and wavelength drift over life are essential to achieve the requisite performance for use in an optical telecommunications network.

A key element to large scale integration is low loss passive waveguides to link the individual elements in a PIC. The total power loss from straight sections of passive waveguides of different lengths is plotted in Fig. 10. A linear least-squares-fit to the data, provides a propagation loss value of ~0.7 dB/cm for the integrated waveguide structure in a TX LS-PIC. This propagation loss value for the transmitter waveguide competes with the best wet etched rib loaded slab structures at 0.2 dB/cm [40], and is superior to the more typical 1.5–2 dB/cm for dry etched ridge waveguides [40]–[42].

B. 100 Gb/s DWDM Receiver PIC Performance

The receiver PIC consists of a wavelength demultiplexer monolithically integrated with an array of high speed photodetectors (PD). The demultiplexer is an AWG and the PDs are each a waveguide PIN diode. Like the transmitter PIC the channel spacing is 200 GHz in the receiver. There are several reports of AWG/PIN integrated receiver chips in the literature;

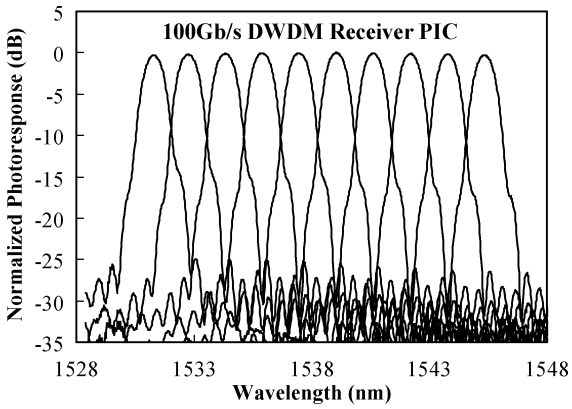

Fig. 11. Normalized photoresponse of the 100 Gb/s (10 × 10 Gb/s) DWDM receiver PIC.

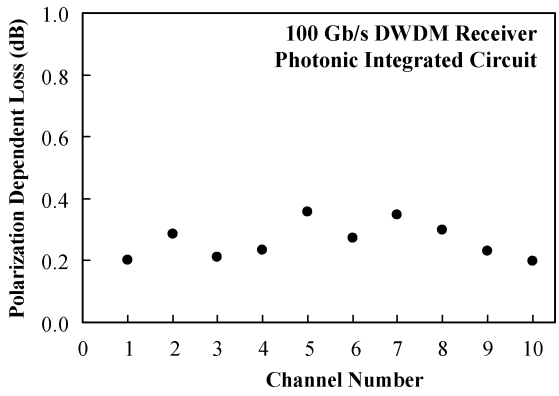

Fig. 12. Polarization dependent loss as a function of channel number for the 100 Gb/s (10 × 10 Gb/s) DWDM receiver PIC.

a ten-channel device operating at 2.5 Gb/s per channel [43] has been reported, and a four-channel device operating at 10 Gb/s per channel is also commercially available.[1] As far as we know, this is the first report of an integrated receiver optical device with ten channels operating successfully at 10 Gb/s per channel for an aggregate data throughput of 100 Gb/s.

Fig. 11 shows the normalized photoresponse of the receiver. In the test setup, the input to the device is from a tunable laser. The output is measured as the dc photocurrent at the PIN array. The nominal fiber coupled responsivity of the integrated device is sufficient to effectively transmit data across all long-haul links encountered in real world networks (see Section IV) and compares favorably with currently available discrete combinations of commercial components.

Standalone commercial PIN receiver modules for OC-192 applications have a typical responsivity of 0.8 A/W (including fiber coupling losses).[2] Standalone fiber coupled, Gaussian type, Silica AWG modules (flat top types have higher losses), have insertion losses between 3 dB (ultralow loss version) and 5 dB (normal version).[3] Silica based AWGs have larger fabrication tolerances (commensurate with the optical mode index which is less than half of that in InP) and, hence, are easier to fabricate, and have lower fiber coupling losses (similar mode index and better mode matching to glass fiber).

Unlike the transmitter PIC, the integrated receiver PIC chip needs to be polarization independent. To determine the polarization dependent loss (PDL) and polarization dependent wavelength shift (PDWS) of the receiver PIC, the maximum and minimum photoresponse is measured as the polarization state of the input light is varied. Fig. 12 shows the nominal PDL of the receiver as a function of channel number. The per-channel PDL is less than 0.5 dB for all ten channels with a median of 0.3 dB. For the single polarization spectrum shown in Fig. 11, the flatness (which affects the dynamic range of the receiver) is better than 0.4 dB. The median PDWS for all 10 channels is 14 GHz (the minimum value is 12 GHz and the maximum value is 17 GHz).

[1]ThreeFive Photonics, Argo A4D10, The Netherlands.

[2]JDS Uniphase, ERM 568XCX, 10 Gb/s SONET/SDH, PIN-TIA High Gain, Optical Receiver Modules, U.S.; NEL, NLK2C1B1KC, High Speed Photodiodes, Japan; Bookham, PT10G, 10 Gb/s PIN Preamp Receiver, U.K.

[3]NEL, AWG Multi/Demultiplexer, Japan.

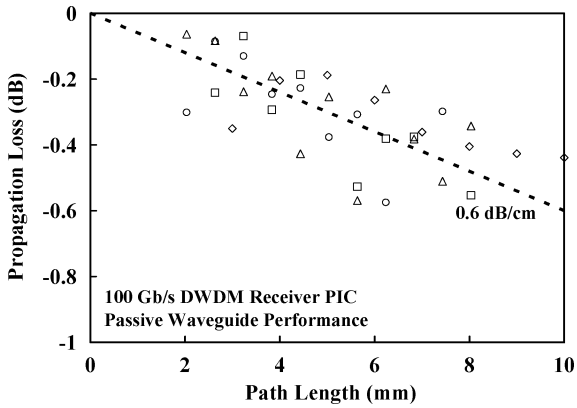

Fig. 13. Propagation loss measured using a series of waveguides of varying lengths for the passive waveguide structure employed in the DWDM receiver PIC. The best fit to the data indicates a propagation loss of ∼0.6 dB/cm.

To realize low insertion loss in the receiver PIC, it is critical to fabricate waveguides with very low propagation loss. Fig. 13 shows the waveguide propagation loss measured on the receiver PIC. This is done by measuring the insertion loss of waveguides of multiple lengths and plotting the data as a function of propagation distance. This method gives the average insertion loss over multiple lengths of the waveguide, and also eliminates the fiber coupling loss as a source of measurement uncertainty. The average propagation loss is 0.6 dB/cm which is amongst the best performance reported to date for InP waveguides [41]. These waveguides were defined via dry etching. Dry etching is required for precise and reproducible fabrication of the AWG in InP. Since the performance of the AWG is phase sensitive, fabrication errors of the order of a fraction of the propagation wavelength have a deleterious effect on AWG performance [44]. Dry etched InP waveguides are generally reported to have an order of magnitude higher propagation losses compared to wet etched waveguides [41]. Typical propagation loss reported in literature for dry etched InP waveguides is 1.5–2 dB/cm [40]–[42].

The adjacent channel crosstalk is lower than −25 dB for all ten channels with the median value of −26 dB. This accounts for adjacent channel crosstalk variation over all polarization states (including the effects of both PDL and PDWS). The total crosstalk is the sum of the effects of all the adjacent channels.

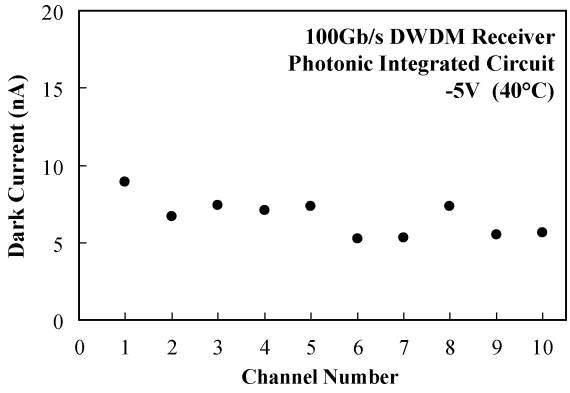

Fig. 14. Reverse bias dark current of the high-speed PIN photodiode array at 40 °C and −5-V bias voltage as a function of channel number for the DWDM receiver PIC.

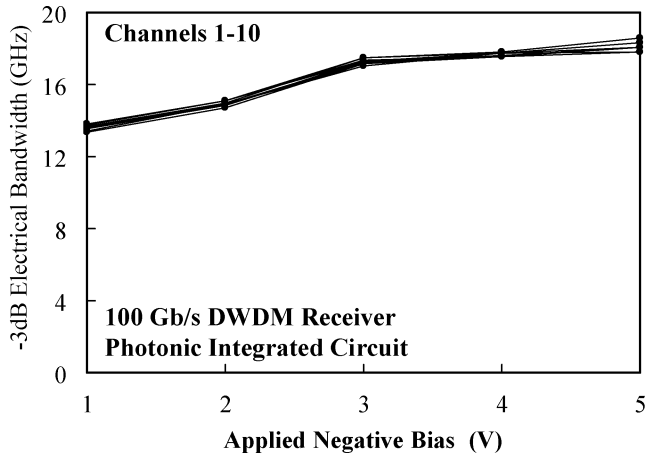

Fig. 15. Electrical modulation bandwidth for all ten channels of the high-speed photodiode array in the DWDM receiver PIC as a function of reverse bias voltage.

The worst case total crosstalk is better than −20 dB with a median value of −21.3 dB.

The high-speed PIN diodes were also designed to have very low dark current. Fig. 14 shows the dark current measured at 5-V reverse bias and 40 °C across all 10 channels. The dark currents are all nominally under 10 nA. This is comparable to the performance of commercial high speed PIN photodiodes for 10 Gb/s applications . The 40 °C higher temperature screen is used to ensure that the device will be robust in the field and allows for the temperature tuning of the AWG up to 40 °C to allow for variations in the AWG center frequency resulting from manufacturing deviations encountered in PIC fabrication.

Fig. 15 shows the small signal bandwidth of the ten-channel high-speed PIN array as a function of bias voltage. The bandwidth was measured using an Agilent 8703B Lightwave Component Analyzer. The small signal bandwidth is about 18 GHz at a reverse bias of 5 V. The channel to channel variation in bandwidth is very small, well within the measurement error of the instrument, attesting to the fabrication uniformity of the PD array. Across all ten channels, the median parasitic capacitance is 200 fF and median series resistance is 15 Ω. Even at reverse bias voltages as low as −1 V, the bandwidth is about 14 GHz, and is sufficient for 10 Gb/s operation. The performance shows that we have not sacrificed bandwidth for responsivity which is a common tradeoff in many commercial high-speed photodetector designs.

V. System Performance Utilizing DWDM Photonic Integrated Circuits

A. Module and Back-To-Back Performance

The transmitter and receiver PICs were built into DWDM transceiver line cards for implementation in an optical transport system. The features of the transmitter and receiver PIC were optimized to ensure good overall system level performance, including link margin to cover spans with loss >30 dB in a network as well as sufficient controls and reliability to maintain performance over 20 years of life. The ten-channel LS-PIC DWDM transceiver cards result in over a 30-times reduction in the number of fiber-couplings compared to a conventional system comprised of discrete optical components. The drastic reduction in fiber connections results in a drastic reduction in packaging and system hardware costs as well as reliability issues associated with the many fiber couplings in traditional systems. Furthermore, the space occupied by a system based on DWDM LS-PIC's is >3 times less than that of a conventional optical transport system, conserving valuable floor space in the central office.

Although integrated transmitters and receivers have been demonstrated previously, there are a several reasons, in addition to the many obvious advantages of integration, why the current design is uniquely suited for real world deployment. First, there is the use of an EAM to encode the data. Also, the use of an AWG (its frequency discrimination properties) together with an EML, which can provide concurrent modification of the output power and chirp characteristics of the transmitter PIC. Second, there is the use of on-PIC VOAs to enable output power flattening. Third, the use of an AWG wavelength combiner with a DFB array requires an array of integrated tuning elements to keep the DFB array aligned to the AWG. The tuning elements deployed here also are used to compensate for the small errors in the stringent manufacturing tolerances of the transmitter PIC. Fourth, the on-PIC VOA also compensates for over life power degradation of all elements on the PIC. Finally, the integrated back facet OPM provides an independent DFB power monitor over life. No other PIC reported to date has demonstrated the level of integration of the ten-channel DWDM LS-PIC transmitter reported herein while maintaining sufficient performance and reliability required for deployment in a carrier-class telecommunications network.

Similarly, for the 100-Gb/s DWDM receiver PIC, the fabrication of a ten-channel high-speed photodetector array and polarization insensitive AWG meeting all the performance specifications related to crosstalk, responsivity, dark current, dynamic range, and polarization independence simultaneously is extremely challenging, but achievable.

There are several advantages achieved in the integration of the electroptic elements in a DWDM TX LS-PIC. The first advantage relates to the integrated EAMs. During EAM fabrication, its operating wavelength can be uniquely matched to the operating wavelength of the DFB for optimum performance. The second advantage is that the EAM can be biased appropriately

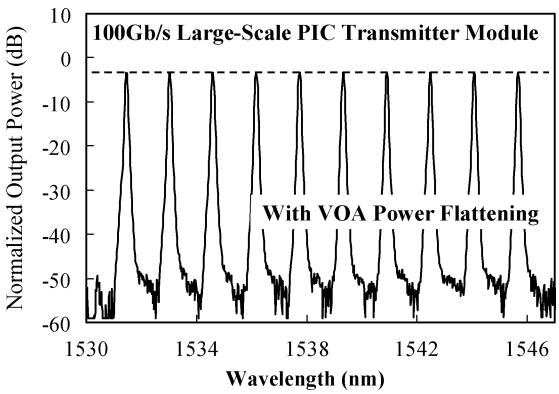

Fig. 16. Output optical spectrum from the DWDM LS-PIC transmitter module using the on-PIC VOA for power flattening.

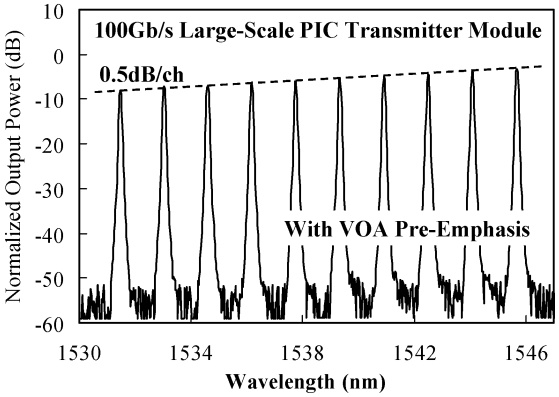

Fig. 17. Output optical spectrum from the DWDM LS-PIC transmitter module in Fig. 16 showing the on-PIC capability to customize the power spectrum. In this case, a linear grade of 0.5 dB per channel is demonstrated.

to modify its chirp to suit the dispersion properties of the transmission fiber [45]. Conventional DWDM systems primarily deploy Lithium Niobate-based MZ modulators and these have a higher insertion loss, and fixed chirp properties [46], [47]. In contrast, the EAM chirp can be easily varied by appropriate dc biasing. InP MZ modulators come in two varieties. The conventional design operates solely based on the electro-optic effect and has fixed chirp properties like the Lithium Niobate devices. InP MZ modulators, which use the electroabsorption effect to realize an index change, also have the bias dependent variable chirp property [48]. In our system, the EAM is typically biased to provide negative chirp. Under optimized bias conditions, its modulated signal is capable of transmission over 100 km of uncompensated SMF-28 fiber.[4]

The third advantage is the availability of on-PIC power flattening capability. The individual channels are spaced at 200 GHz and locked to the ITU grid. At power-up, the roll-off in power in the outer channels often follows the classic roll-off in the AWG output spectrum. Fig. 16 shows how power flattening can be achieved using the per-channel VOA integrated on the transmitter PIC. Power flattening is critical for EDFA-based links. Fig. 17 shows that we can actually achieve any desired "shaping" of the powers in the output spectrum. The figure shows a 0.5-dB/channel tilt for a total of 4.5-dB tilt across all ten channels. A tilt or some variation thereof may be desired to compensate for nonlinearities in the installed fiber base or the gain flatness of the EDFA.

Fig. 18 shows the output eye diagram for all the ten channels from the DWDM LS-PIC transmitter module measured using an Agilent 86 100A Infinium Digital Communication Analyzer (DCA) with a 86 109A 30-GHz optical bandwidth plug-in. The data rate is set at 11.1 Gb/s to accommodate the FEC overhead for the implementation of a 10 Gb/s data transmission. The eye diagrams are very uniform over all ten channels demonstrating a robust design and a high degree of control in manufacturing. The minimum extinction ratio for all ten channels shown is in excess of 13 dB. The minimum 10%/90% rise time is better than 34 ps and the 90%/10% fall time is better than 37 ps. The maximum peak-to-peak jitter for all ten channels is less than 12 ps.

B. Transmission Performance

A PIC-based transport system can be configured in two different ways. The first option is to regenerate the data at every network node. This also allows for all or some part of the data traffic to be dropped and added at will. In addition, situations exist where the traffic is only required to be expressed through to the next node, and there is sufficient OSNR margin present. Thus, the second option for transport system design is to simply insert an optical amplifier at the express nodes. The PIC's must be designed with sufficient performance margin to elegantly handle both options.

One of the system test setups used to characterize the line cards is shown in Fig. 19. This particular configuration has five spans of 75-km fiber each with an EDFA [also referred to as an optical amplifier module (OAM)] after every span. Fig. 20 shows the back-to-back Q measurement, i.e., for zero dispersion. The data is plotted as $20\log(Q)$ as a function of OSNR. For reference, a Q value of 15.6 dB is required for an uncorrected BER of 10^{-9} and 16.9 dB for 10^{-12}. In Fig. 20, the Q values for OSNR higher than about 17 dB are test time limited and, hence, the curves "appear" to rollover. This is not as the result of a back-to-back noise floor limit. An excellent discussion on the definition of Q, its practical applications, and its experimental determination may be found in a publication by Bergano, *et al.*, [49].

Many terrestrial systems for telecommunication applications these days employ an FEC scheme to reduce the Q requirement for error free transport of data [50], [51]. Until just a few years ago, FEC was utilized solely in high-end submarine transmission systems. There are several FEC schemes that have been demonstrated to date, and most of them are proprietary. Recently, the ITU has approved G.975.1 (02/2004) the implementation of FEC in DWDM systems. Our system employs a proprietary FEC code. Fig. 21 shows the link performance across five spans of 75-km fiber spools for all ten channels of the system. These measurements are useful to characterize the number of skip sites possible with a particular system configuration. The system sensitivity limit is $<$12 dB-0.1 nm of OSNR. Even after five spans there is significant OSNR margin in the system. The Q values of the individual channels tend to spread as the number of skips increases. This is a function of the residual gain flatness

[4]Registered trademark of Corning, Inc.

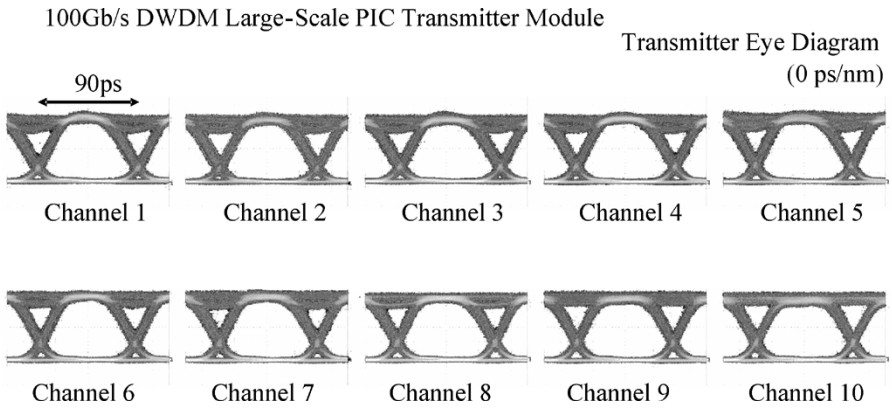

Fig. 18. Ten-channel output eye diagram from the 100 Gb/s DWDM LS-PIC transmitter module. Modulation is achieved via a variable chirp EAM array.

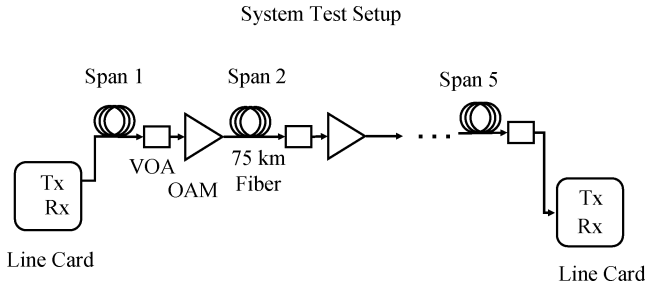

Fig. 19. Schematic of the system test bed utilized for evaluating the performance of the DWDM transceiver PIC-based line cards over multiple fiber spans.

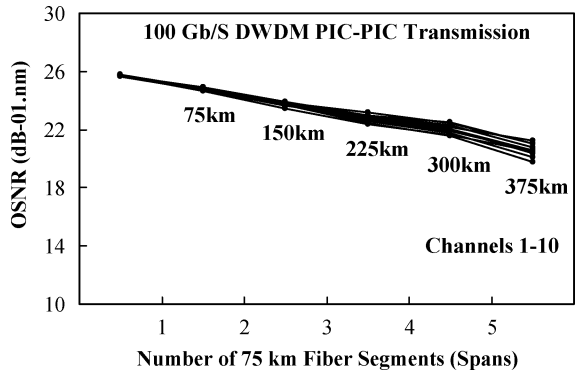

Fig. 21. OSNR as a function of number of 75-km fiber segments in an amplified system utilizing DWDM PIC-transceiver line cards at the terminals of the link.

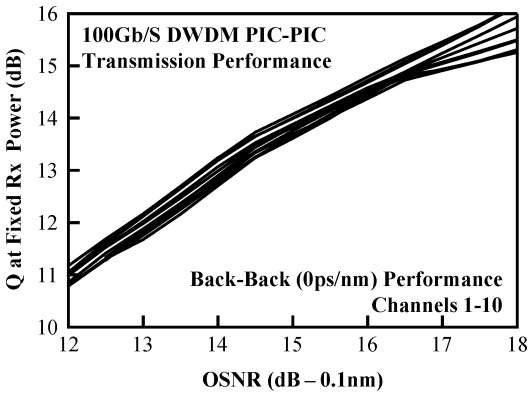

Fig. 20. Back-to-back Q versus OSNR performance of a DWDM PIC-based transmitter-receiver module pair on a system line card.

variation of the EDFA chain in the transmission link and not attributable to the PIC's themselves. The on-PIC VOA allows one to correct, within limits, for a large part, but not all, of the imperfections in gain flatness of an EDFA chain. The demonstrated uniformity in transmission performance over five fiber segments is only possible with a very tight control of the chirp and other modulation properties of the EAM. This, is turn, is enabled by precise controls realized during PIC fabrication.

This is the first-ever demonstration of a transmission system to carrier level specifications based on transmitter and receiver multichannel photonic integrated circuits.

VI. Scaling of Photonic Integrated Circuits

The development of the first transistor [52] marked the beginning of the semiconductor electronics revolution. A little over a decade later, the integrated circuit (IC) was invented [53], [54]. During this time, the commercial scaling of the IC proceeded at a staggering pace, advancing from a discrete device circa 1949 [55] to >50 components/chip in 1965 [1] to >42 000 000 transistors/chip for a Pentium 4 device in 2000 [56]. This progression was predicted by Moore [1] and has driven the scaling of electronic devices to be a self-fulfilling prophecy.

The commercial development and scaling of optoelectronic devices and photonic integrated circuits in the telecommunications network has occurred at a substantially slower rate. The first semiconductor-based light-emitting diode (LED) transmitters were reported in 1960 [57], [66] followed shortly thereafter by the demonstration of the first semiconductor lasers [58]–[61]. However, the first telecommunications networks utilizing such devices were not deployed until 1980 for LEDs [62] and 1984 for lasers [63]. The incubation period from development to commercial deployment was thus ~20 years for optoelectronic discrete devices (compared to ~10 years for the transistor). The scaling of photonic integrated circuits versus time in the telecommunication network is shown in Fig. 22 for the most advanced PIC technology (transmitter devices). The first commercial deployment of a semiconductor transmitter occurred in 1980 (LED-based), followed by the deployment of networks utilizing DMLs [63]. For over the next 10 years,

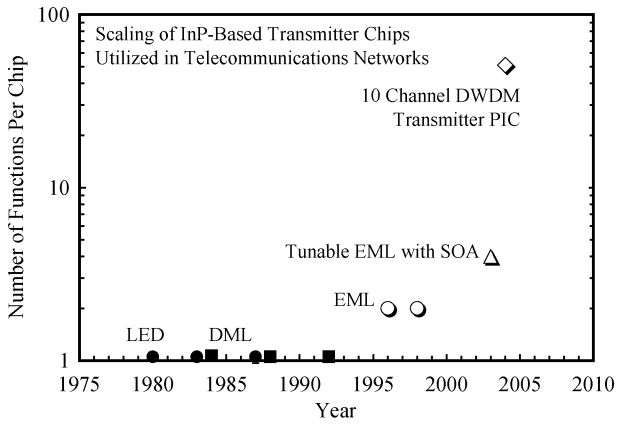

Fig. 22. Progression of scaling of the number of functions/chip for InP-based transmitter chips utilized in commercial telecommunications networks. The 100 Gb/s DWDM transmitter PIC's described in this work represent over an order magnitude increase in scale compared to existing commercial devices.

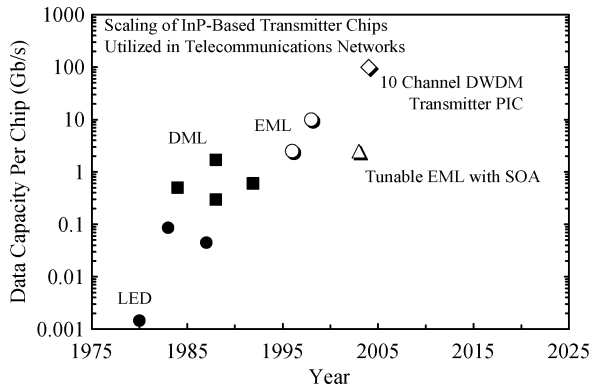

Fig. 23. Scaling of the data capacity/chip for InP-based transmitter chips utilized in commercial telecommunications networks. Over the last 25 years, the data capacity per chip has doubled an average of every 2.2 years. The 100 Gb/s DWDM transmitter PIC's described in this work represent an order of magnitude increase in data capacity per chip compared to existing commercial devices.

commercial implementations focused on incrementally higher data rates in discrete devices. The first integrated device, the EML, consisting of two functions on a single chip, was first deployed in 1996 at 2.5 Gb/s and in 1998 at 10 Gb/s in long-haul terrestrial networks [64]. This was followed by the integration of two additional functions (tuning and amplification), resulting in a transmitter consisting of a tunable EML with an SOA [13] which was first deployed in a telecommunications network in 2003.

The scaling of the PIC has thus been substantially slower than the corresponding electronic IC, requiring 24 years to scale by 4 times (the corresponding scaling for electronic ICs was ~5,000 times in the same period [56]). The most important contributors to the retardation in the scaling rate of PICs have been the immaturity of the existing network infrastructure and the inability for the cost of the integration to be recouped in value delivered by the integrated device. The optimal integration level was highlighted by both Moore [1] and Noyce [65] to be a balance of increased chip cost per function (which increases for increased scaling) and reduced assembly cost per function (which decreases with increased scaling). The resultant value of the device depends on the network architecture and implementation. To date, the increased chip cost (due to immaturity of the III-V optoelectronic device and process technology) and the value derived in the network have been insufficient to drive PIC scaling at a rate consistent with Moore's Law. The large-scale ten-channel DWDM transmitter PICs reported in this work results in an inflection point in this progression, scaling by over an order of magnitude to >50 functions/chip. This PIC scaling is driven by dramatic improvements in III-V device and process technology as well as the ability for such devices to enable new network architectures (wherein OEO regeneration and add–drop functionality are pervasive in the network).

The scaling of the data capacity per chip for transmitter devices employed in the telecommunications network is shown in Fig. 23. Unlike the PIC scaling shown in Fig. 22, the scaling of the data rate per chip is exponential and shows a doubling every ~2.2 years, which is ~65% of the rate of progression of Moore's Law. The large-scale ten-channel transmitter PIC reported in this work represents an order of magnitude improvement in data capacity per chip compared to existing commercial devices. The transition in scaling of data rate from discrete devices (solid symbols) to integrated devices (open symbols) has been driven by the presence of performance impairments in the network that arise at higher bit rates making discrete scaling less cost effective than that of integrated devices. In order to continue the progression of data capacity per chip at its historical rate, further improvements in PIC scaling will be required. Thus, the rates of the scaling of functions per chip (Fig. 22) and data capacity per chip (Fig. 23) are expected to become more closely related over time.

VII. Conclusion

Large-scale photonic integrated circuits with performance and capability sufficient for commercial deployment have been demonstrated. These devices represent an order of magnitude or more improvement in number of functions per chip and data capacity per chip compared to previous generation devices, using >50 functions to provide a chip operating at an aggregate data rate of 100 Gb/s. Further, we have shown the first use of such PICs in a complete optical transport system operating across a representative DWDM long-haul network link. The use of such LS-PICs will enable significant reductions in the cost of optical transport systems, while also enabling new simplified network architectures that make maximum use of the ability to implement low-cost OEO conversions more frequently in the network. Compared to existing DWDM systems, such "Digital Optical Network" architectures offer the promise to enable simplified add/drop, easier optical network engineering, automated end-end circuit provisioning, and reduced operational difficulties in such areas as system deployment and turn-up, performance monitoring and trouble-shooting.

Acknowledgment

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REFERENCES

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114–117, Apr. 19, 1965.

[2] S. E. Miller, "Integrated optics: An introduction," *Bell Syst. Tech. J.*, vol. 48, pp. 2059–2069, 1969.

[3] R. C. Alferness, "Guided wave devices for optical communication," *IEEE J. Quantum Electron.*, vol. QE-17, no. 6, pp. 946–959, Jun. 1981.

[4] O. Wada, T. Sakurai, and T. Nakagami, "Recent progress in optoelectronic integrated circuits (OEICs)," *IEEE J. Quantum Electron.*, vol. QE-22, no. 6, pp. 805–823, Jun. 1986.

[5] T. L. Koch and U. Koren, "Semiconductor photonic integrated circuits," *IEEE J. Quantum Electron.*, vol. QE-27, no. 3, pp. 641–653, Mar. 1991.

[6] I. Moerman, P. P. Van Daele, and P. M. Demeester, "A review on fabrication technologies for the monolithic integration of tapers with III-V semiconductor devices," *IEEE J. Select. Topics Quantum Electron.*, vol. 3, no. 6, pp. 1308–1320, Nov. 1997.

[7] Y. Kawamura, K. Wakita, Y. Yoshikuni, Y. Itaya, and H. Asahi, *IEEE. J. Quantum Electron.*, vol. QE-23, no. 6, pp. 915–918, Jun. 1987.

[8] H. Soda, M. Furutsu, K. Sato, N. Okazaki, Y. Yamazaki, H. Nishimoto, and H. Ishikawa, "High-power and high-speed semi-insulating BH structure monolithic electroabsorption modulator/DFB laser light source," *Electron. Lett.*, vol. 26, pp. 9–10, 1990.

[9] T. L. Koch, U. Koren, R. P. Gnall, C. A. Burrus, and B. I. Miller, "Continuously tunable 1.5 μm multiple-quantum-well InGaAs/InGaAsP distributed-Bragg-reflector lasers," *Electron. Lett.*, vol. 24, pp. 1431–1432, 1988.

[10] B. Mason, G. A. Fish, S. P. DenBaars, and L. A. Coldren, "Ridge waveguide sampled grating DBR lasers with 22-nm quasicontinuous tuning range," *IEEE Photon. Technol. Lett.*, vol. 10, no. 10, pp. 1211–1213, Oct. 1998.

[11] ——, "Widely tunable sampled grating DBR laser with integrated electroabsorption modulator," *IEEE Photon. Technol. Lett.*, vol. 11, no. 11, pp. 638–640, Nov. 1999.

[12] J. E. Johnson, L. J.-P. Ketelsen, J. A. Grenko, S. K. Sputz, J. Vandenberg, M. W. Focht, D. V. Stampone, L. J. Peticolas, L. E. Smith, K. G. Glogovsky, G. J. Przybylek, S. N. G. Chu, J. L. Lentz, N. N. Tzafaras, C. L. Reynolds, L. A. Gruezke, R. People, and M. A. Alam, "Monolithically integrated semiconductor optical amplifier and electroabsorption modulator with dual-waveguide spot-size converter input," *IEEE J. Select. Topics Quantum Electron.*, vol. 6, no. 1, pp. 19–25, Jan. 2000.

[13] B. Mason, J. Barton, G. A. Fish, S. P. DenBaars, and L. A. Coldren, "Design of sampled grating DBR lasers with integrated semiconductor optical amplifiers," *IEEE Photon. Technol. Lett.*, vol. 12, no. 7, pp. 762–764, Jul. 2000.

[14] B. Pezeshki, E. Vail, J. Kubicky, G. Yoffe, S. Zou, J. Heanue, P. Epp, S. Rishton, D. Ton, B. Faraji, M. Emanuel, X. Hong, M. Sherback, V. Agrawal, C. Chipman, and T. Razazan, "20-mW widely tunable laser module using DFB array and MEMS selection," *IEEE Photon. Technol. Lett.*, vol. 14, no. 10, pp. 1457–1459, Oct. 2002.

[15] D. Kuchta, Y. Kwark, C. Schuster, C. Baks, C. Haymes, J. Schaub, P. Pepeljugoski, L. Shan, R. John, D. Kucharski, D. Rogers, and M. Ritter, "120 Gb/s VCSEL-based parallel optical link and custom 120 Gb/s testing station," in *Proc. 54th Electronic Components Technology Conf.*, Las Vegas, NV, June 1–4, 2004, pp. 1003–1011.

[16] J. Simon, L. Buckman Windover, S. Rosenau, K. Giboney, B. Law, G. Flower, L. Mirkarimi, A. Grot, C.-K. Lin, A. Tandon, G. Rankin, and R. Gruhlke, "Parallel optical interconnect at 10 Gb/s per channel," in *Proc. 54th Electronic Components Technology Conf.*, Las Vegas, NV, June 1–4, 2004, pp. 1016–1023.

[17] M. G. Young, U. Koren, B. I. Miller, M. A. Newkirk, M. Chien, M. Zirngibl, C. Dragone, B. Tell, H. M. Presby, and G. Raybon, "A 16 $\times$ 1 wavelength division multiplexer with integrated distributed Bragg reflector lasers and electroabsorption modulators," *IEEE Photon. Technol. Lett.*, vol. 5, no. 8, pp. 908–910, Aug. 1993.

[18] K. Kudo, K. Yashiki, T. Sasaki, T. Y. Yokoyama, K. Hamamoto, T. Morimoto, and M. Yamaguchi, "1.55-μm wavelength-selectable microarray DFB-LDs with monolithically integrated MMI combiner, SOA, and EA-modulator," *IEEE Photon. Technol. Lett.*, vol. 12, no. 3, pp. 242–244, Mar. 2000.

[19] M. K. Smit and C. van Dam, "PHASAR-based WDM-devices: principles, design and applications," *IEEE J. Select. Topics Quantum. Electron.*, vol. 2, no. 2, pp. 236–250, Jun. 1996.

[20] M. Zirngibl and C. H. Joyner, "A 12 frequency WDM laser source based on transmissive waveguide grating router," *Electron. Lett.*, vol. 30, pp. 700–701, 1994.

[21] A. M. Staring, L. H. Spiekman, J. J. M. Binsma, E. J. Jansen, T. van Dongen, P. J. A. Thijs, M. K. Smit, and B. H. Verbeek, "A compact nine-channel multiwavelength laser," *IEEE Photon. Technol. Lett.*, vol. 8, no. 9, pp. 1139–1141, Sep. 1996.

[22] S. Menezo, A. Talneau, F. Delorme, S. Grosmaire, F. Gaborit, and S. Slempkes, "10-wavelength 200-GHz channel spacing emitter integrating DBR lasers with a PHASAR on InP for WDM applications," *IEEE Photon. Tech. Lett.*, vol. 11, no. 7, pp. 785–787, Jul. 1999.

[23] M. R. Amersfoort, C. R. de Boer, B. H. Verbeek, P. Demeester, A. Looyen, and J. J. G. M. van der Tol, "Low-loss phased-array based 4-channel wavelength demultiplexer integrated with photodetectors," *IEEE Photon. Tech. Lett.*, vol. 6, no. 1, pp. 62–64, Jan. 1994.

[24] M. Zirngibl, C. H. Joyner, and L. W. Stulz, "WDM receiver by monolithic integration of an optical preamplifier, waveguide grating router and photodiode array," *Electron. Lett.*, vol. 31, pp. 581–582, 1995.

[25] C. A. M. Steenbergen, C. van Dam, A. Looijen, C. G. P. Herben, M. de Kok, M. K. Smit, J. W. Pedersen, I. Moerman, R. G. F. Baets, and B. H. Verbeek, "Compact low-loss 8 $\times$ 10 GHz polarization independent WDM receiver," in *Proc. 22nd Eur. Conf. Optical Communication*, Oslo, Norway, Sept. 15–19, 1996, pap. Mo C4.1, pp. 129–132.

[26] M. Kohtoku, H. Sanjoh, S. Oku, Y. Kadota, and Y. Yoshikuni, "Packaged polarization insensitive WDM monitor with low loss (7.3 dB) and wide tuning range (4.5 nm)," *IEEE Photon. Tech. Lett.*, vol. 10, no. 11, pp. 1614–1617, Nov. 1998.

[27] R. Mestric *et al.*, "Sixteen-channel wavelength selector monolithically integrated on InP," in *Proc. Optical Fiber Conf.*, Baltimore, MD, 2000, paper TuF6, pp. 81–83.

[28] S. Oei and M. K. Smit, "Photonic integrated circuits for multiwavelength networks," in *Proc. Int. Conf. Applications of Photonic Technology, SPIE Proc.*, vol. 3491, 1998, pp. 74–79.

[29] Y. Suzaki, K. Asaka, Y. Kawaguchi, S. Oku, Y. Noguchi, S. Kondo, R. Iga, and H. Okamota, "Multi-channel modulation in a DWDM monolithic photonic integrated circuit," in *Proc. 14th Indium Phosphide and Related Materials Conf.*, 2002, pp. 681–683.

[30] E. J. Thrush, J. P. Stagg, M. A. Gibbon, R. E. Mallard, B. Hamilton, J. M. Jowett, and E. M. Allen, "Selective and nonplanar epitaxy of InP/GaInAs(P) by MOCVD," *Mat. Sci. Eng.*, vol. B21, pp. 130–146, 1993.

[31] R. J. Deri, "Monolithic integration of optical waveguide circuitry with III-V photodetectors for advanced lightwave receivers," *J. Lightw. Technol.*, vol. 11, no. 8, pp. 1296–1313, Aug. 1993.

[32] R. P. Schneider Jr and Y. M. Houng, "Epitaxy of vertical cavity lasers," in *Vertical Cavity Surface Emitting Lasers: Design, Fabrication, Characterization and Applications*, Y. M. Wilmsen, Y. M. Temkin, and Y. M. Coldren, Eds. Cambridge, U.K.: Cambridge Univ. Press, 1999.

[33] M. Sokolich, M. Y. Chen, R. D. Rajavel, D. H. Chow, Y. Royter, S. Thomas III, C. H. Fields, B. Shi, S. S. Bui, J. C. Li, D. A. Hitko, and K. R. Elliott, "InP HBT integrated circuit technology with selectively implanted subcollector and regrown device layers," *IEEE Solid-State Circuits*, vol. 39, no. 10, pp. 1615–1621, Oct. 2004.

[34] S. Chandrasekhar, B. C. Johnson, E. Tokumitsu, A. G. Dentai, C. H. Joyner, A. H. Gnauck, J. S. Perino, and G. J. Qua, "A monolithic long wavelength photoreceiver using heterojunction bipolar transistors," *IEEE J. Quantum Electron.*, vol. 27, no. 3, pp. 773–777, Mar. 1991.

[35] D2587P-Wavelength Selected High-Power Isolated DFB Laser Modules Data Sheet, Agere. (2001, Jul. 2). *http://www.agere.com/partah.html* [Online]

[36] 1935 LMI High Power CW Laser, Alcatel. (2001, Sep.). *http://www.photonics.com/spectra/newprods/XQ/ASP/newprodidl.4716/QX/read.htm* [Online]

[37] Nortel Networks. (2001, Nov.) LC155CDC-20 continuous wave fixed wavelength laser -20 mW, publication # 84 084.02/11-01 [Online], vol (5)http://www2.hs-harz.de/~ufischerhirchert/liste/sonstiges/download/papers_pdf/Nortel%20locker.pdf

[38] Marconi, TM10N-1000 10 Gbps integrated transmitter, no. 1, 2001.

[39] Nortel Networks, EA10EW-21-10 Gb/s electro-absorption modulator and laser with optional etalon stabilization-PB0118 , no. 24, Oct. 2000.

[40] C. R. Doerr, "Planar lightwave devices for WDM," in *Optical Fiber Telecommunications*, I. Kaminow and T. Li, Eds. San Diego, CA: Academic, 2002, vol. IVA, pp. 405–476.

[41] C. G. M. Vreeburg *et al.*, "A low-loss 16 channel polarization dispersion compensated PHASAR demultiplexer," *IEEE Photon. Technol. Lett.*, vol. 10, no. 3, pp. 382–384, Mar. 1998.
[42] L. H. Spiekman, M. R. Amersfoort, A. H. De Vreede, F. P. G. M. van Ham, A. Kuntze, J. W. Pedersen, P. Demeester, and M. K. Smit, "Design and realization of polarization independent phased array wavelength demultiplexers using different array orders for TE and TM," *J. Lightw. Technol.*, vol. 14, no. 6, pp. 991–995, Jun. 1996.
[43] Y. Yoshikuni, "Semiconductor arrayed waveguide gratings for photonic integrated devices," *IEEE J. Select. Topics Quantum Electron.*, vol. 8, no. 6, pp. 1102–1114, Dec. 2002.
[44] C. D. Lee, W. Chen, Q. Wang, Y. J. Chen, W. T. Beard, D. Stone, R. F. Smith, R. Mincher, and I. R. Stewart, "The role of photomask resolution on the performance of arrayed-waveguide grating devices," *J. Lightw. Technol.*, vol. 19, no. 11, pp. 1726–1733, Nov. 2001.
[45] M. Matsuda, K. Morito, K. Yamaji, T. Fujii, and Y. Kotaki, "A novel method for designing chirp characteristics in electroabsorption MQW optical modulators," *IEEE Photon. Technol. Lett.*, vol. 10, no. 3, pp. 364–366, Mar. 1998.
[46] E. L. Wooten, K. M. Kissa, A. Yi-Yan, E. J. Murphy, D. A. Lafaw, P. F. Hallemeier, D. Maack, D. V. Attanasio, D. J. Fritz, G. J. McBrien, and D. E. Bossi, "A review of lithium niobate modulators for fiber-optic communications systems," *IEEE J. Select. Topics Quantum Electron.*, vol. 6, no. 1, pp. 69–82, Jan. 2000.
[47] A. Mahapatra and E. J. Murphy, "Electrooptic modulators," in *Optical Fiber Telecommunications*, I. Kaminow and T. Li, Eds. San Diego, CA: Academic, 2002, vol. IVA, pp. 258–294.
[48] J. C. Cartledge, "Multiple-quantum-well Mach-Zehnder modulators: Comparison of calculated and measured results for modulator properties and system performance," *IEEE J. Select. Topics Quantum Electron.*, vol. 9, no. 3, pp. 736–746, May 2003.
[49] N. S. Bergano, F. W. Kerfoot, and C. R. Davidsion, "Margin measurements in optical amplifier system," *IEEE Photon. Technol. Lett.*, vol. 5, no. 3, pp. 304–306, Mar. 1993.
[50] F. Kerfoot and H. Kidorf, "Forward error correction for optical transmission systems," in *Proc. Optical Fiber Conf.*, 2002.
[51] P. V. Kumar, M. Z. Win, H. F. Lu, and C. N. Georghiades, "Error-control coding techniques and applications," in *Optical Fiber Telecommunications*, I. Kaminow and T. Li, Eds. San Diego, CA: Academic, 2002, vol. IVB, pp. 902–964.
[52] J. Bardeen and W. H. Brattain, "The transistor, a semi-conductor triode," *Phys. Rev.*, vol. 74, pp. 230–232, July 1948.
[53] J. S. Kilby, "Minaturized electronic circuits," U.S. Patent 3 138 743, Jun. 23, 1964.
[54] R. N. Noyce, "Semiconductor device-and-lead structure," U.S. Patent 2 981 877, Apr. 25, 1961.
[55] J. Morton, "Report on transistor development," AT&T, July 1949.
[56] G. E. Moore, "No exponential is 'forever': But 'forever' can be delayed!," presented at the *IEEE International Solid State Circuits Conf.*, San Francisco, CA, Feb. 9–13, 2003, Paper 1.1.
[57] R. J. Keyes and T. M. Quist, "Unpublished paper," presented at the *IRE Solid State Device Research Conf.*, Durham, NH, 1962.
[58] R. N. Hall, G. E. Fenner, J. D. Kingsley, T. J. Soltys, and R. O. Carlson, "Coherent light emission from GaAs junctions," *Phys. Rev. Lett.*, vol. 9, pp. 366–368, Nov. 1, 1962.
[59] M. I. Nathan, W. P. Dumke, G. Burns, F. H. Dill Jr., and G. Lasher, "Stimulated emission of radiation from GaAs p-n junctions," *Appl. Phys. Lett.*, vol. 1, pp. 62–64, Nov. 1962.
[60] N. Holonyak Jr. and S. F. Bevacqua, "Coherent (visible) light emission from $Ga(As_{1-x}P_x)$ junctions," *Appl. Phys. Lett.*, vol. 1, pp. 82–83, Dec. 1962.
[61] T. M. Quist, R. H. Rediker, R. J. Keyes, W. E. Krag, B. Lax, A. L. McWhorter, and H. J. Zeiger, "Semiconductor maser of GaAs," *Appl. Phys. Lett.*, vol. 1, pp. 91–92, Dec. 1962.
[62] R. C. Alferness and A. Glass, "Bell labs technology trends and developments," *Bell Labs Tech. J.*, vol. 2, no. 2, pp. 1–15, 1988.
[63] D. C. Gloge and I. Jacobs, *Optical Fiber Telecommunications II*, 1st ed. San Diego, CA: Academic, 1988, p. 857.
[64] S. Grubb, private communication, July 12, 2004.
[65] R. N. Noyce, "Large-scale integration: what is yet to come?," *Science*, vol. 195, pp. 1102–1106, Mar. 18, 1977.
[66] R. J. Keyes and T. M. Quist, "Recombination radiation emitted by gallium arsenide," *Proc. IRE*, vol. 50, pp. 1822–1823, Aug. 1962.

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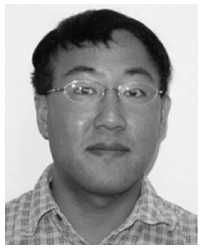

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