반도체 소자 측정 및 분석기법

Ch.1 Resistivity

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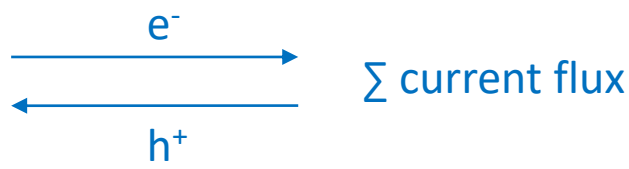
1.1 Introduction

- **Resistivity, ρ**
  - contributes to the Series-Resistance, Capacitance, Vt, Hot carrier degradation, Latch up of CMOS
  - locally controlled by ‘dopant diffusion’ and ‘ion implantation’
  - not truly uniform in grown ingot due to variability and segregation
  - very uniform in epitaxial growth
  - ρ=1/σ=1/conductivity

- **Resistivity calculation**
  - need to measure ‘carrier density’ and ‘mobilities’

$$\rho = \frac{1}{q(n\mu_n + p\mu_p)}$$

free electron and hole densities *n* and *p*
electron and hole mobility μ_n and μ_p



- unfortunately, carrier densities and mobilities are generally not known
  → Contactless, temporary contact, and permanent contact technique

1.2 Two-Point vs. Four-Point probe (principle)

- **Two-Point probe**
  - easier to implement, because only two probes need to be manipulated
  - 1 path: same path for voltage and current
  - difficult interpretation

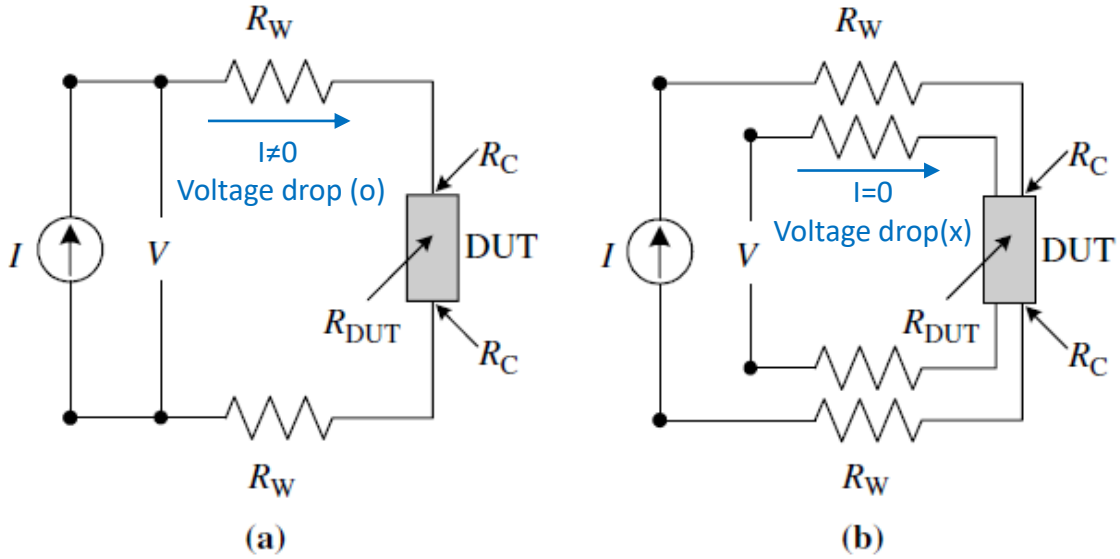
$$R_T = V/I = 2R_W + 2R_C + R_{DUT} \qquad (1.2)$$

R_W: wire or probe resistance
R_C: contact resistance
R_{DUT}: resistance of DUT

Usually R_w, $R_c < R_{DUT}$

- **Four-Point probe (Kelvin measurements)**
  - standard
  - commonly used to measure the semiconductor resistivity
  - 2 path: voltage path and current path
  - negligible voltage drop across the DUT
  - Kelvin measurement (Load Kelvin)

$$R_T = V/I = R_{DUT}$$



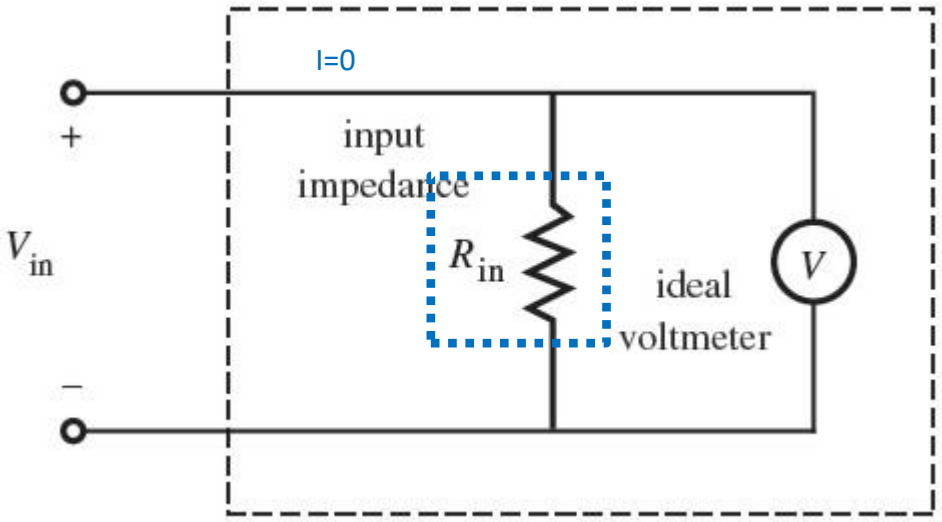
I=0
High input impedance of voltmeter
(> 10^{12} Ω)

Fig. 1.1 Two-terminal and four-terminal resistance measurement arrangements.

Voltage and current meter (ideal)

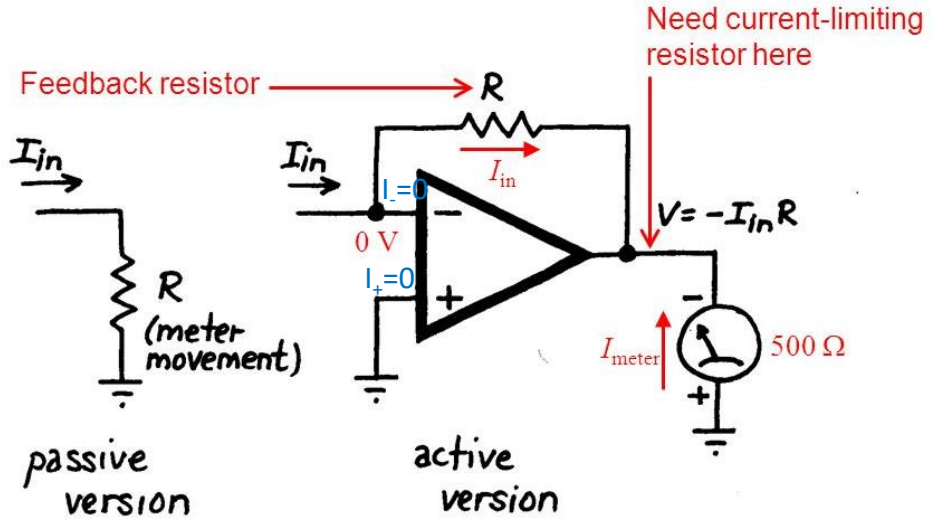
- **Voltage meter**

how to measure V=Vin ?
→ I=0



High input impedance of voltmeter
(> 10^{12} Ω)

- **Current meter**



* Student manual for The Art of Electronics, Hayes and Horowitz, 2nd edition)

1.2 Two-Point vs. Four-Point probe

- **Transconductance (I_D-V_G) curve of MOSFET**

w/o parasitic R_W and R_C

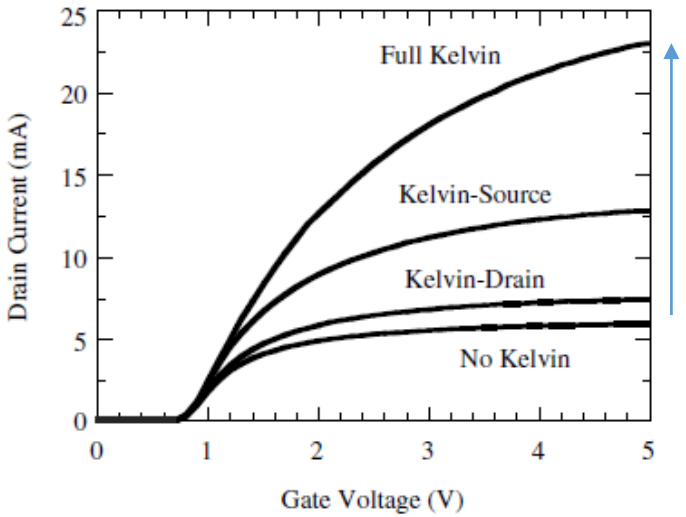


Fig. 1.2 Effect of contact resistance on MOSFET drain current. Data courtesy of J. Wang, Arizona State University.

- **Two-point probe and parasitic resistance**
  - probe resistance (R_P)
  - contact resistance (R_C)
  - spreading resistances(R_{SP})

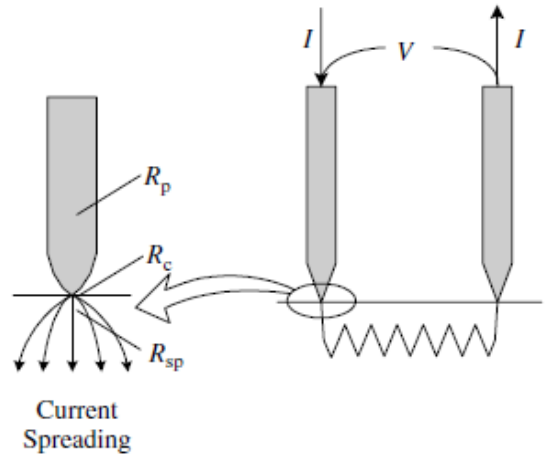
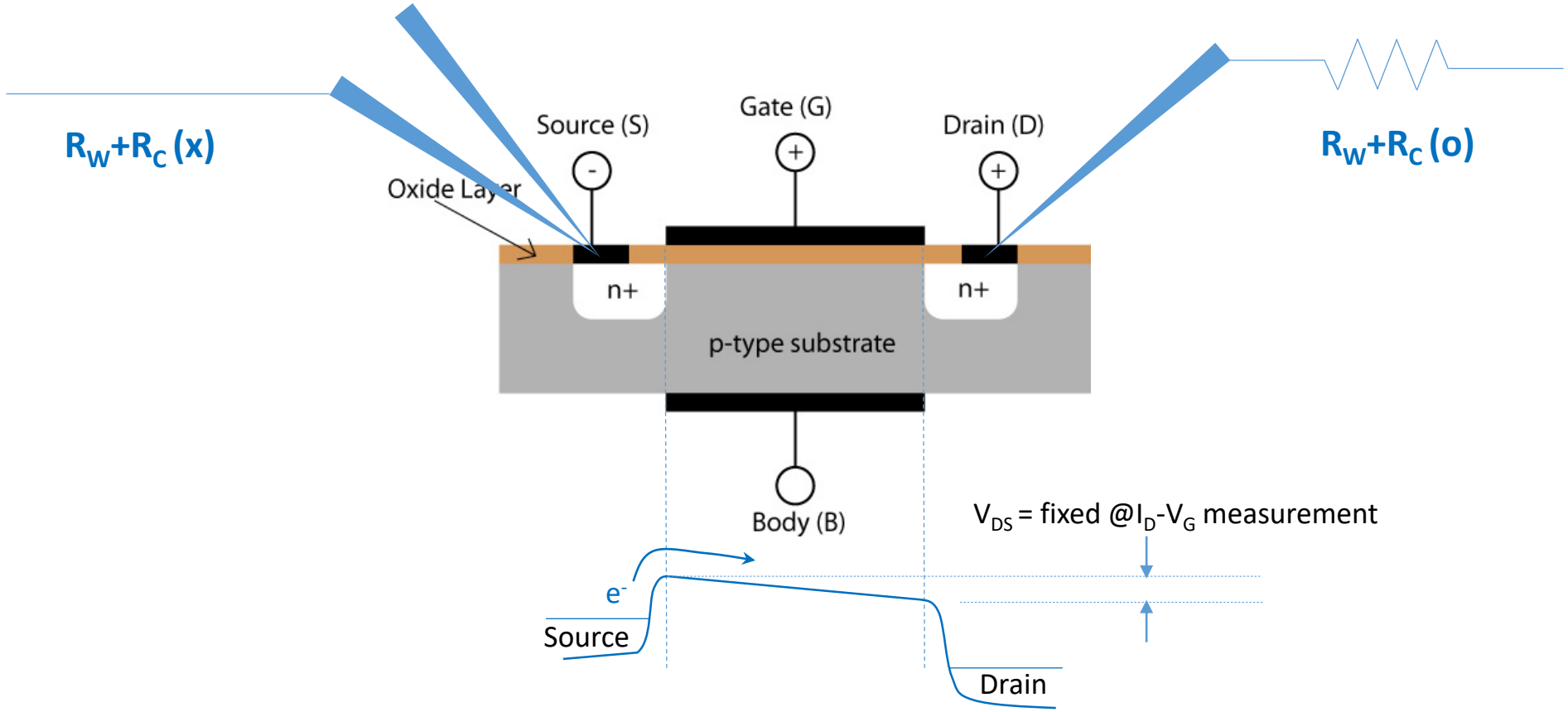


Fig. 1.3 Two-point probe arrangement showing the probe resistance R_p, the contact resistance R_c, and the spreading resistance R_{sp}.

1.2 Kelvin-Source vs. Kelvin-Drain

- **Kelvin technique** eliminates contact(R_c) and wire resistance(R_p)
- R_W+R_C reduction in Source side by **Kelvin-Source is effective than that in Drain side**
  - because current is determined by number of carriers which overcome the energy barrier of Source side



[Kelvin-Source configuration]

(Ex 1.1) Four-point probe equation (ideal)

- **Figure 1.4(a)**
  - ε: electric field, J: current flux, ρ: resistivity

$$\varepsilon = J\rho = -\frac{dV}{dr};\quad J = \frac{I}{2\pi r^2} \qquad (1.3)$$

  - voltage at point P at a distance r from the probe

$$\int_0^V dV = -\frac{I\rho}{2\pi}\int_0^r \frac{dr}{r^2} \Rightarrow V = \frac{I\rho}{2\pi r} \qquad (1.4)$$

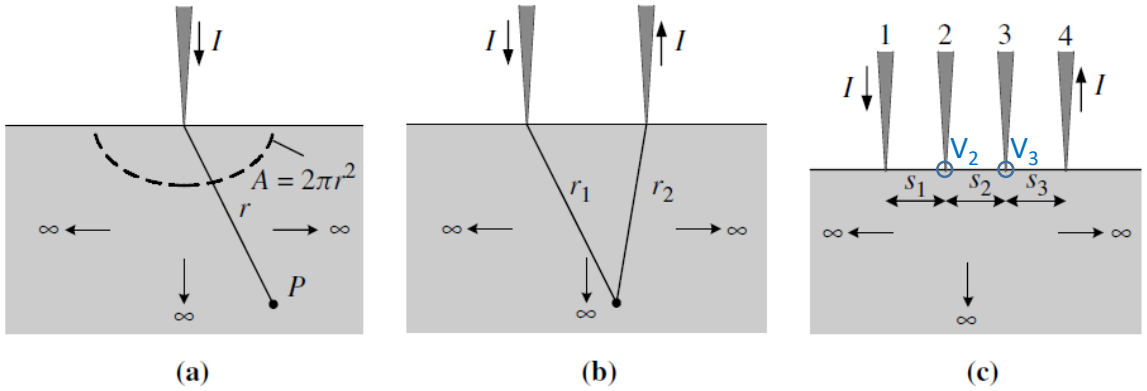


Fig. 1.4 (a) one-point probe, (b) two-point, and (c) collinear four-point probe showing current flow and voltage measurement.

- **Figure 1.4(b)** $V = \frac{I\rho}{2\pi r_1} - \frac{I\rho}{2\pi r_2} = \frac{I\rho}{2\pi}\left(\frac{1}{r_1} - \frac{1}{r_2}\right)$ (1.5)

- **Figure 1.4(c), $V=V_{23}=V_2-V_3$** (V_2 & V_3: voltage at surface)

$$V_2 = \frac{I\rho}{2\pi}\left(\frac{1}{s_1} - \frac{1}{s_2+s_3}\right) \qquad (1.6) \qquad V_3 = \frac{I\rho}{2\pi}\left(\frac{1}{s_1+s_2} - \frac{1}{s_3}\right) \qquad (1.7)$$

target

$$V = \frac{I\rho}{2\pi}\left(\frac{1}{s_1} - \frac{1}{s_2+s_3} - \frac{1}{s_1+s_2} + \frac{1}{s_3}\right) \qquad (1.8)$$

when $s=s_1=s_2=s_3$

$$\rho = 2\pi s\frac{V}{I}\ [\Omega cm] \qquad (1.10)$$

added

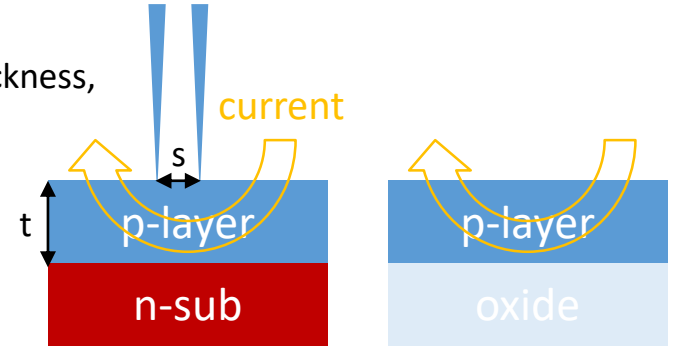
$$\rho = 2\pi s F\frac{V}{I} \qquad (1.11)$$

- Typical probe radii: 0.03~0.5 mm
- Probe spacing(s) range: 0.5~1.5 mm
  s depends on sample THK, sample diameter, temperature and probe placement (s → F: correction factor)

1.2.1 Correction Factors, F_1

- **Correction factors, $F=F_1F_2F_3$** (1.12)
  - F_1: sample thickness
  - F_2: lateral sample dimensions
  - F_3: placement of the probes relative to the sample edge

t: sample (wafer or layer) thickness,
s: probe spacing



① **F_{11}: non-conducting bottom (common)**
- semiconductor wafers are not infinitely thick, i.e finite thickness
- non-conducting bottom is necessary: n-layer on p-sub, p-layer on n-sub, BOX, SOI
  → sufficiently insulating to confine the current to the layer

$$F_{11} = \frac{\text{new factor } (t/s)}{2\ \ln\{[\sinh(t/s)]/[\sinh(t/2s)]\}} \qquad (1.13)$$

② **F_{12}: conducting bottom surface**
- difficult to achieve, there is no perfect conducting bottom due to contact R

$$F_{12} = \frac{(t/s)}{2\ \ln\{[\cosh(t/s)]/[\cosh(t/2s)]\}} \qquad (1.14)$$

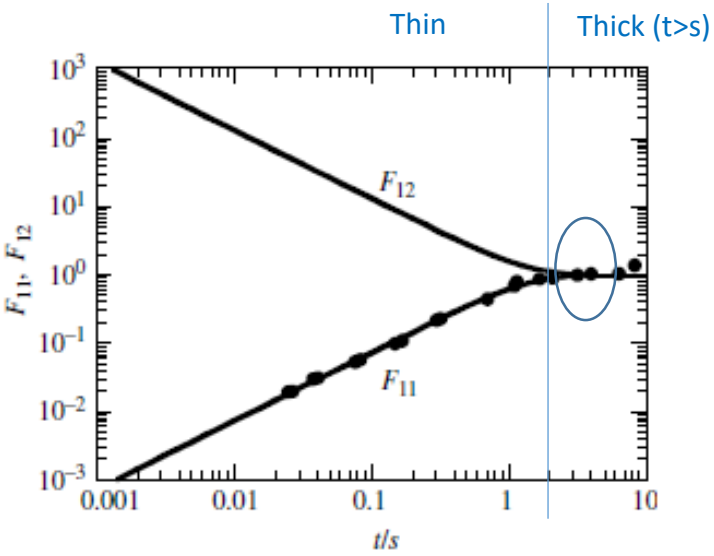
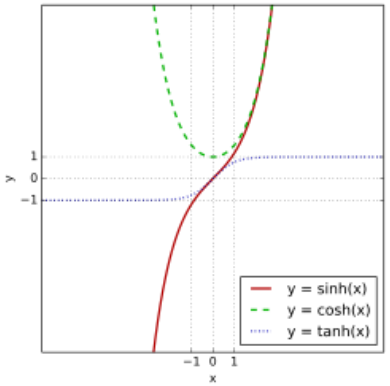


Fig. 1.5 Wafer thickness correction factors versus normalized wafer thickness; t is the wafer thickness, s the probe spacing. The data points are taken from ref. 15.
(Measurement with same doping concentration, but different sample THK)

1.2.1 Correction Factors, F_1



- For thin sample (t/s < 1/2), sinh(t/s) ≈ t/s and (1.13) reduces to From (1.11), (1.12), and (1.15)

$$F_{11} = \frac{t/s}{2\ln(2)} \qquad (1.15)$$

$$\rho = \frac{\pi}{\ln(2)} t \frac{V}{I} = 4.532 t \frac{V}{I} \quad [\Omega\text{cm}] \quad (1.16)$$

$$\frac{V}{I} = \rho\,(ln2)/\pi t = \rho_{sh}(ln2)/\pi \sim \rho_{sh}0.22 \qquad (1.17)$$

→ valid for 'very thin' and 'wide' planar sample

- **Sheet resistance or resistivity, ρ_{sh} in MOSFET**
  - application: diffusion or ion-implant layer, epitaxial films, polycrystalline layer, and metallic conductors
  - the resistance of a uniform conductor of length L, width W, and thickness t is given by

$$R = \rho \frac{L}{Wt} = \rho_{sh} \frac{L}{W} \ [\Omega]$$

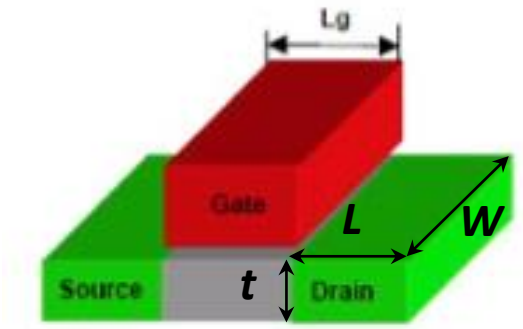
→ valid for uniform doping resistance

- sheet resistance ρ_{sh} [Ω/□] in S/D region

is the 'indicator of achievable resistivity in certain technology'

# of sqaure L/W: device size dependence

t: junction depth of S/D doping, process dependence



Conventional Planar FET

1.2.1 Correction Factors, F_2

- F_2: lateral sample dimensions

$$F_2 = \frac{\ln(2)}{\ln(2)+\ln\{[(D/s)^2+3]/[(D/s)^2-3]\}} \qquad (1.20)$$

new factor

D: sample width or diameter,
s: probe spacing

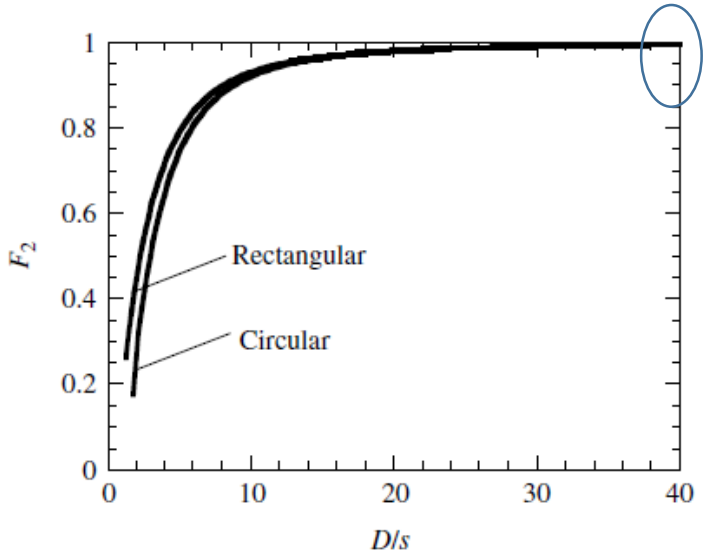


Fig. 1.6 Wafer diameter correction factors versus normalized wafer diameter. For circular wafers: D = wafer diameter; for rectangular samples: D = sample width, s = probe spacing.

- F_3: placement of the probes relative to the sample edge
  - probe positioning, distance from edge, and boundary material
  - correction factors F31 to F34 only become important for small samples

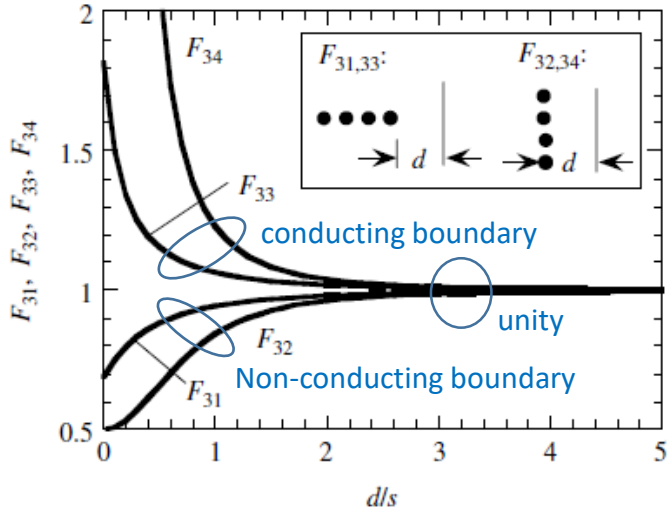


Fig. 1.7 Boundary proximity correction factors versus normalized distance d (s = probe spacing) from the boundary. F_{31} and F_{32} are for non-conducting boundaries, F_{33} and F_{34} are for conducting boundaries.

1.2.2 Resistivity of Arbitrarily Shaped Samples

- **'Non-collinear' type four-point probe (Van der Pauw's method)**
  - more commonly used as contacts to square semiconductor samples
  - required small sample size than 4-point Kelvin

- **conditions of conformal mapping technique** by van der Pauw
  (1) contacts are at the circumference of the sample
  (2) contacts are sufficiently small → not realistic
  (3) sample is uniformly thick
  (4) surface of the sample is singly connected, i.e no isolated holes

$$R_{12,34} = \frac{V_{34}}{I_{12}} \qquad (1.24)$$

$$\rho = \frac{\pi}{\ln(2)} t \frac{(R_{12,34}+R_{23,41})}{2} F \qquad (1.25)$$

- F is function of $R_r=R_{12,34}/R_{23,41}$

$$\frac{R_r-1}{R_r+1} = \frac{F}{In(2)} arcosh\left(\frac{\exp[\frac{\ln(2)}{F}]}{2}\right) \qquad (1.26)$$

(when $R_r=1$, F=1, i.e symmetric sample)

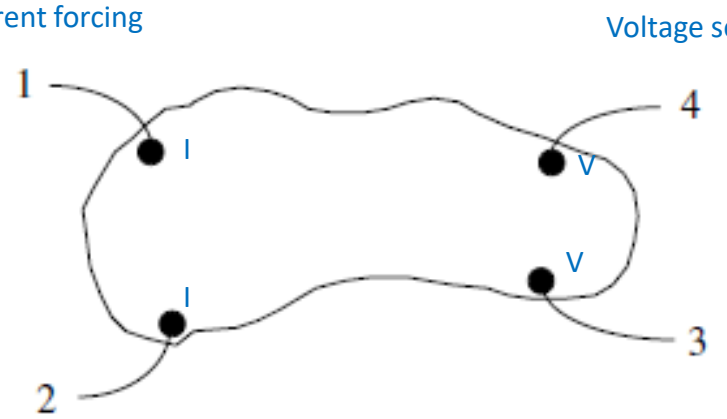
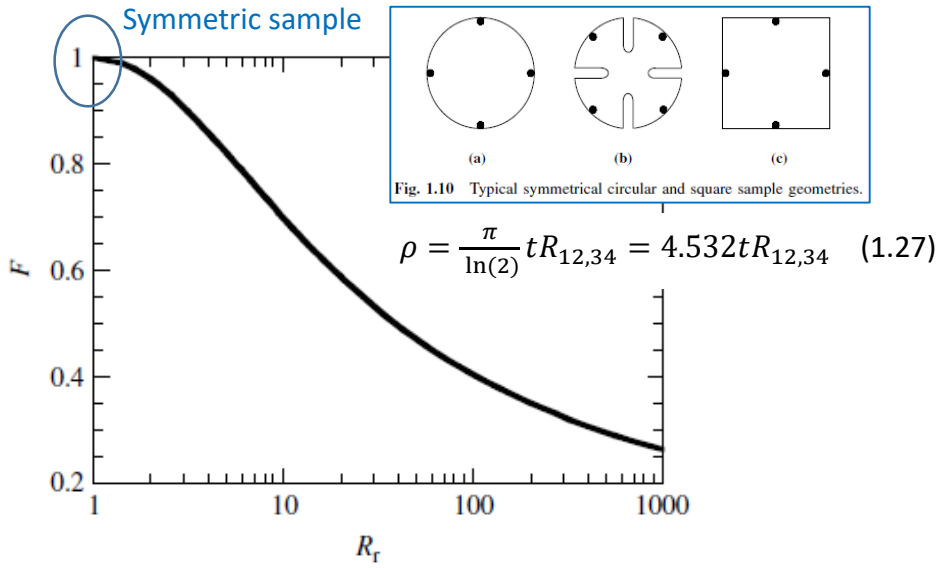


Fig. 1.8 Arbitrarily shaped sample with four contacts.



$$\rho = \frac{\pi}{\ln(2)} t R_{12,34} = 4.532 t R_{12,34} \qquad (1.27)$$

Fig. 1.9 The van der Pauw correction factor F versus R_r.

1.2.2 Resistivity of Arbitrarily Shaped Samples

- **Contact size correction factor, C**
  - depending on 'contact size/sample size=d/l'
  - depending on 'contact location': center or corner
  - to eliminate contact size effect, d/l < 10%

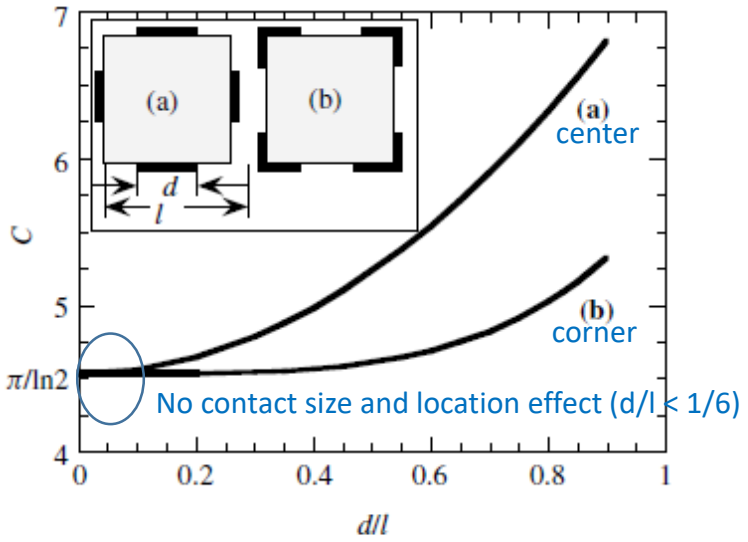


Fig. 1.11 Correction factor C versus d/l for contacts at the center and at the corners of the square. Data after ref. 25.

- **Fig.1.10 shows patterns independent on contact location**
  - (b) cloverleaf: complicate and undesirable
  - (a) circular or (c) square sample is commonly used

$$\rho = CtR_{12,34};\ \ R_{sh} = CR_{12,34} \qquad (1.29)$$

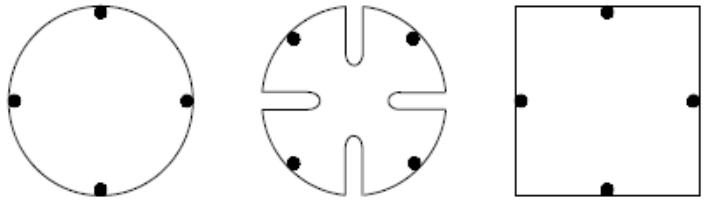


Fig. 1.10 Typical symmetrical circular and square sample geometries.

1.2.2 Cross-bridge structure (in reality)

- **Greek cross structure**
  - possible to make it very small
  - place many on a wafer for uniformity check
  - For L=W, d ≤ L/6 should be acquired

d: distance of the contact from the edge

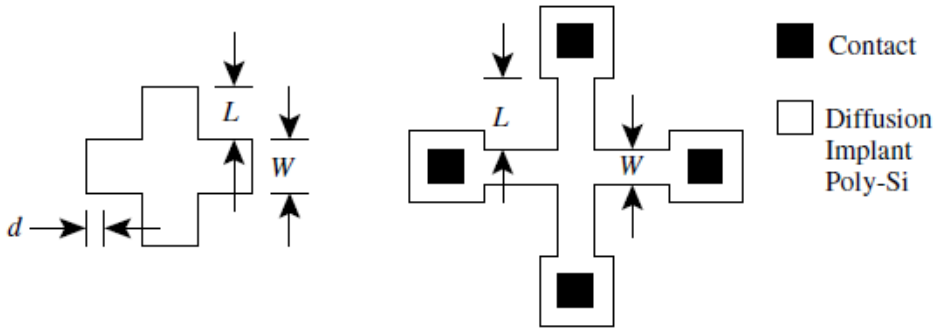


Fig. 1.12 A Greek cross sheet resistance test structure. d = distance of contact from edge.

- **Cross-bridge structure**

① 'sheet resistance'

$$R_{sh} = \frac{\pi}{\ln(2)} \frac{V_{34}}{I_{12}} \qquad (1.30)$$

$V_{34}=V_3-V_4$, I_{12}: current flowing into contact 1 and out of 2

② bridge resistor to determine 'line width W'

$$V_{45} = \frac{R_{sh} L I_{26}}{W} \qquad (1.31)$$

$$W = \frac{R_{sh} L I_{26}}{V45} \qquad (1.32)$$

determined by (1.30)

$V_{45}=V_4-V_5$, I_{26}: current flowing into contact 1 and out of 2

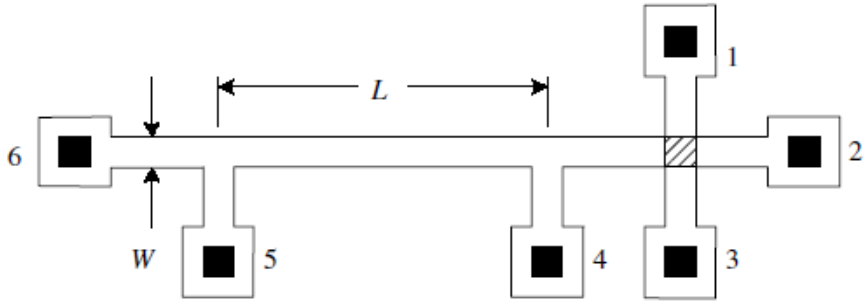


Fig. 1.13 A cross bridge sheet resistance and line width test structure.

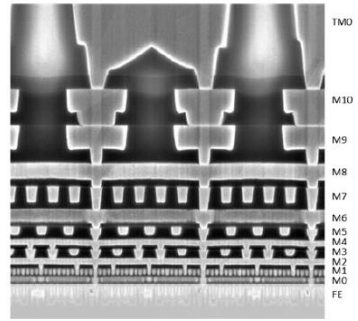
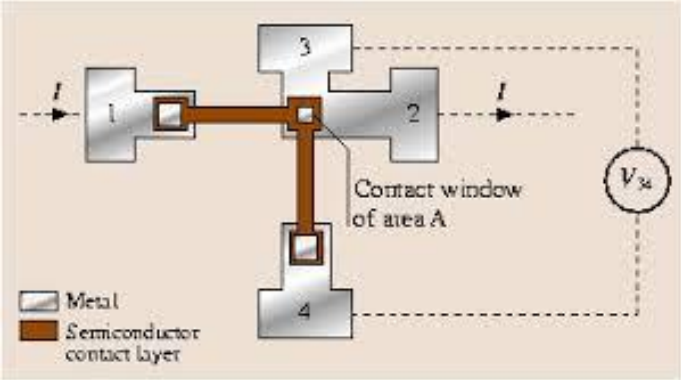


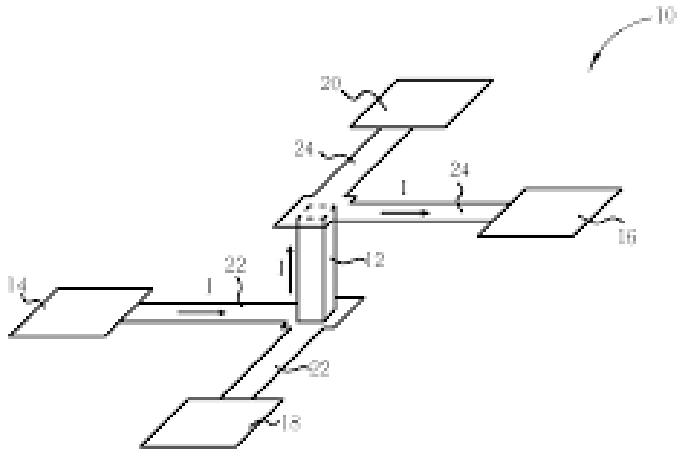
Figure 13: Interconnect Stack

- used to characterize "dishing" during CMP of semiconductor wafers, **monitoring metal line thinning effect by CMP**, especially soft metal such as copper

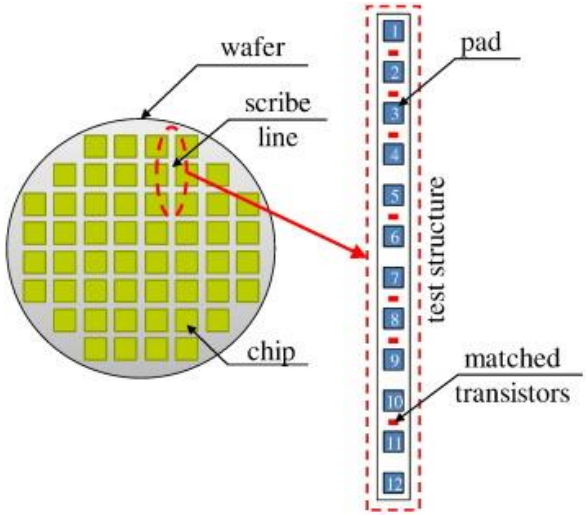
Kelvin structure (in reality)

- **Kelvin structure for vertical DUT**

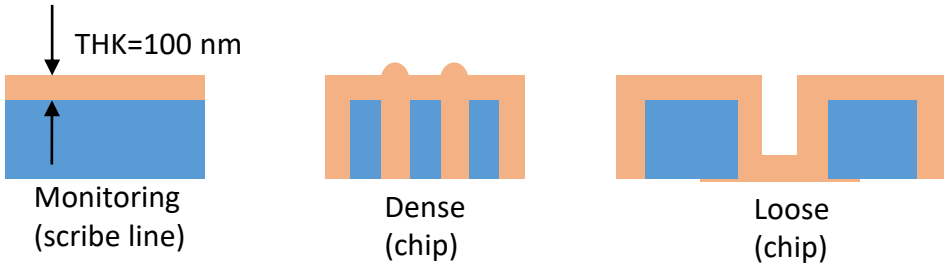




- **Monitoring TEG in scribe line**
  - area saving
  - pattern density effect checking
  - process condition feedback



ex) oxide or nitride deposition, target=100nm



1.3 Wafer mapping

- **Wafer mapping**
  - originally developed to characterize ion implantation uniformity
  - measured at many locations across a sample → two-dimensional or three-dimensional contour map
  - used for **resistivity**(ion implant), **thickness**(poly-Si film), **alignment**(patterning), **warpage**(diffusion)
  - today, highly automated systems are used with several samples → **tolerance and excursion check**

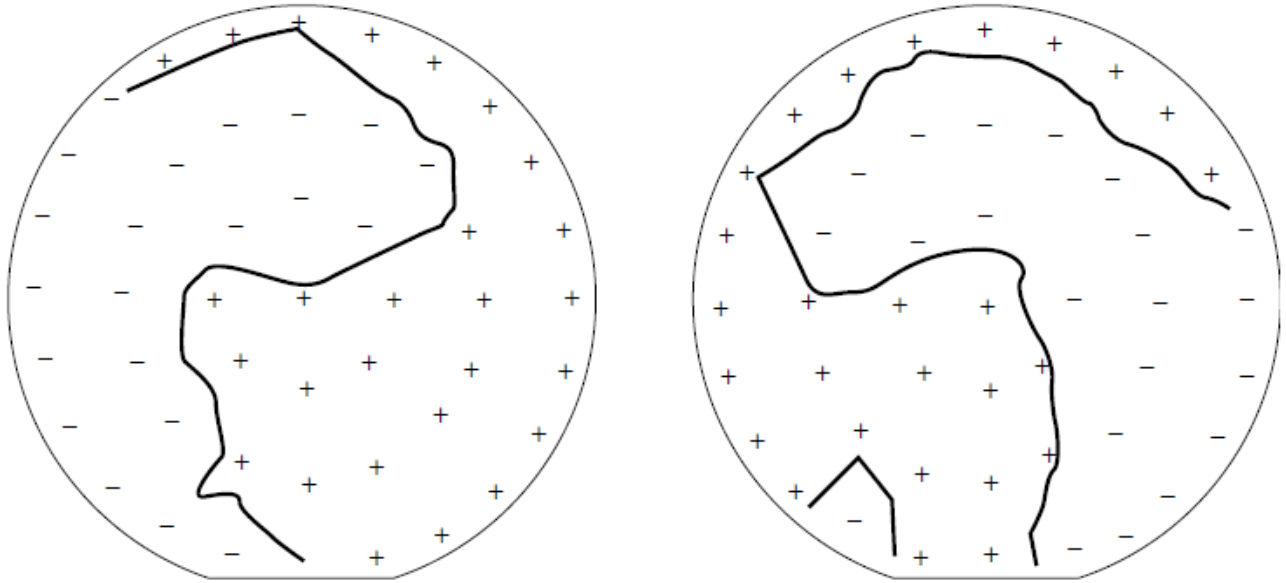


Fig. 1.16 Four-point probe contour maps; (a) boron, 10^{15} cm^{-2}, 40 keV, R_{sh}(average) = 98.5 ohms/square; (a) arsenic, 10^{15} cm^{-2}, 80 keV, R_{sh}(average) = 98.7 ohms/square; 1% intervals. 200 mm diameter Si wafers. Data courtesy of Marylou Meloni, Varian Ion Implant Systems.

1.4 Resistivity profiling

- **Non-uniformly doped layer in reality**
  - sheet resistance measurement averages the resistivity over the sample thickness
  - dopant density profile is desired to get resistivity profile
  - method: differential Hall effect(DHE), spreading resistance, C-V, V_T and secondary ion mass spectrometry(SIMS)

1.4.1 Differential Hall Effect (DHE)

- (measuring the resistivity + removing a thin layer of the sample) x several times
- sample having depth dependent carrier densities and mobilities
- sheet resistance is measured by the Hall effect or four-point probe

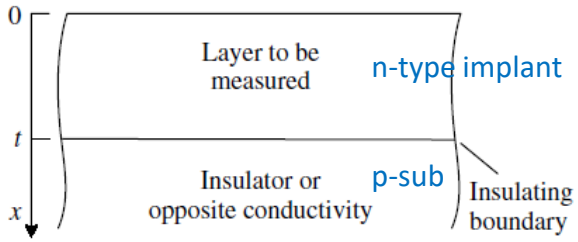


Fig. 1.19 Sample geometry with measurement proceeding from the surface into the sample.

1.4.1 Differential Hall Effect

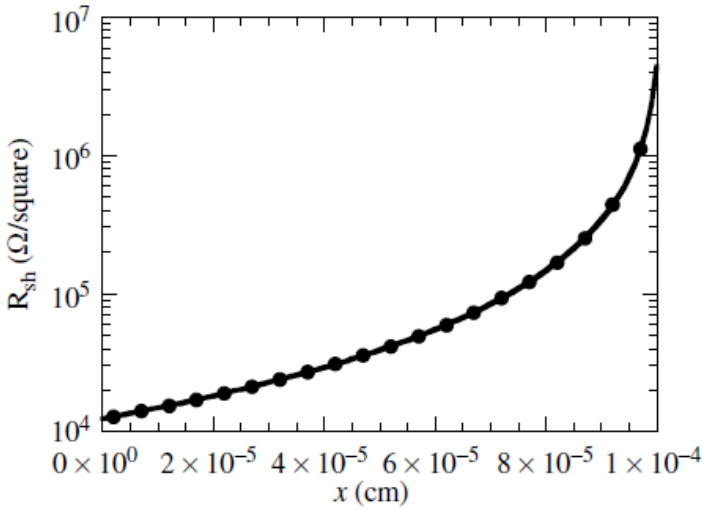
measured

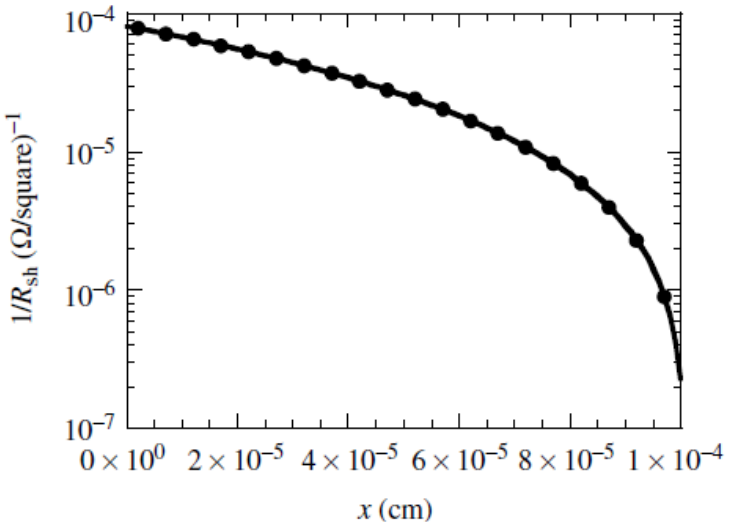
$$R_{sh} = \frac{1}{q\int_x^t [n(x)u_n(x)+p(x)u_p(x)]dx} \quad (1.36)$$

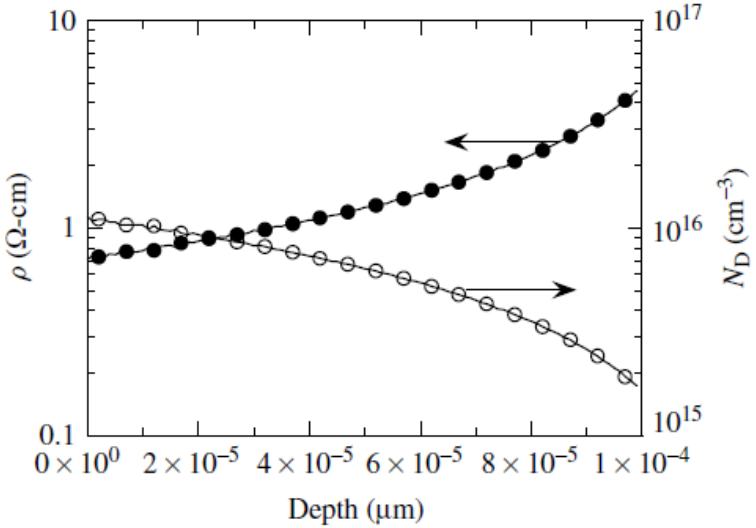
$$\frac{d[1/R_{sh}(x)]}{d_x} = -q\left[n(x)u_n(x) + p(x)u_p(x)\right] = -\sigma(x) \quad (1.38)$$

target

$$\rho(x) = \frac{1}{d[1/R_{sh}(x)]/dx} = \frac{R_{sh}^2(x)}{dR_{sh}(x)/dx} = \boxed{\frac{R_{sh}(x)}{d[\ln(R_{sh}(x))]/dx}} \quad (1.40)$$







1.4.2 Spreading Resistance Profiling (SRP)

1.4.2 Spreading Resistance Profiling (SRP)

- insulating coating (oxide or nitride): oxide provides a sharp corner at the bevel, clearly defines the start of the beveled surface because the spreading resistance of the insulator is very high
- sub micrometer (μm) implants or epi layer: 100-150 data points
- sub 100 nm implants or epi layer: 20-25 data points

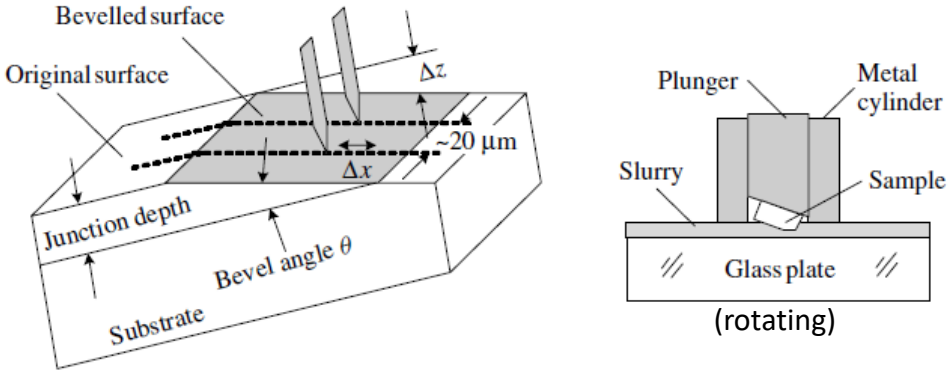


Fig. 1.21 Spreading resistance bevel block and the beveled sample with probes and the probe path shown by the dashed line.

$$R = 2R_p + 2R_c + 2R_{sp} \quad (1.41)$$

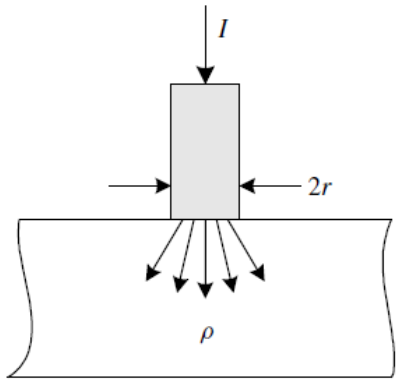
R_p: probe resistance
R_c: contact resistance
R_{sp}: spreading resistance

- **Spreading resistance (cylindrical contact)**
  - semi-infinite sample

$$R_{sp} = \frac{\rho}{4r} ohms \quad (1.42a)$$

  - hemispherical

$$R_{sp} = \frac{\rho}{2\pi r} ohms \quad (1.42b)$$



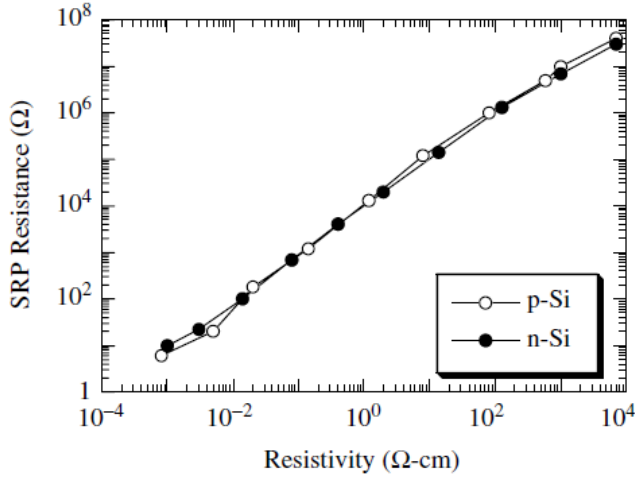


Fig. 1.23 Calibration curves for conventional SRP measurements. After ref. 63.

Back up

About class

- **강의 시간: 화,목 (11:00-12:15), LG102호, office hour: 화,목(PM 4:00-5:30), LG215호**

- **강의 목표**
  반도체 엔지니어로서, 제작된 반도체 소자를
  1) 실제 측정하는 방법과 (→ 측정 구성 및 원리)
  2) 이를 기반으로 물리적 파라미터를 추출하고 (→ 물리적 이론 습득)
  3) 소자의 전기적 특성을 정량적으로 비교 분석하는 방법을 습득한다. (→ 실제 소자에 적용 및 벤치마킹)

- **선수과목:** 반도체 전자공학I or 반도체 전자공학II

- **성적평가:** 중간30%, 기말40%, 숙제: 20%, 출석10% (결석은 최대 2번까지 허용),

- **교재 (Ch01. XXXX.180904)**
  1) Semiconductor Material and Device Characterization (D. K. Schroder) → will be shared
  2) Speaker's materials

Schedules (2nd semester, 2018)

W01 - Ch01. Resistivity (1.2/1.4)
W02 - Ch02. Carrier and Doping Density (2.2/2.3)
W03 - Ch02. Carrier and Doping Density (2.4/2.5)
W04 - Ch03. Contact Resistance and Schottky Barriers (3.2/3.3/3.4)
W05 - Ch03. Contact Resistance and Schottky Barriers (3.5/3.6)
W06 - Ch04. Series Resistance, Channel Length and Width, and Threshold Voltage (4.6/4.8) → IV
W07 - Ch04. Series Resistance, Channel Length and Width, and Threshold Voltage (4.6/4.8)
W08 - (중간고사)

W09 - Ch05. Defects (5.6) → CV
W10 - Ch06. Oxide and Interface Trapped Charges, Oxide Thickness (6.2/6.3) → LFN/RTS/Charge pumping
W11 - Ch06. Oxide and Interface Trapped Charges, Oxide Thickness (6.4)
W12 - Ch07. Carrier Lifetime (7.2/7.3)
W13 - Ch07. Carrier Lifetime (7.5/7.6)
W14 - Ch08. Mobility (8.6/8.7)
W15 - Ch12. Reliability and Failure Analysis (12.2/12.4) → Hot carrier/BTI
W16 - (기말고사)

*theory, real measurement

2017 World #1 in SEMICONDUCTOR INDUSTRY

Top 10 Worldwide Semiconductor Sales Leaders
(Excluding Foundries, $B)

Rank	1993		2000		2006		2016		1H17	
1	Intel	7.6	Intel	29.7	Intel	31.6	Intel	57.0	Samsung	29.2
2	NEC	7.1	Toshiba	11.0	Samsung	19.7	Samsung	44.3	Intel	28.8
3	Toshiba	6.3	NEC	10.9	TI	13.7	Qualcomm (1)	15.4	SK Hynix	11.4
4	Motorola	5.8	Samsung	10.6	Toshiba	10.0	Broadcom (1)	15.2	Micron	10.6
5	Hitachi	5.2	TI	9.6	ST	9.9	SK Hynix	14.9	Broadcom (1)	8.4
6	TI	4.0	Motorola	7.9	Renesas	8.2	Micron	13.5	Qualcomm (1)	7.7
7	Samsung	3.1	ST	7.9	Hynix	7.4	TI	12.5	TI	6.6
8	Mitsubishi	3.0	Hitachi	7.4	Freescale	6.1	Toshiba	10.9	Toshiba	6.0
9	Fujitsu	2.9	Infineon	6.8	NXP	5.9	NXP	9.5	NXP	4.5
10	Matsushita	2.3	Philips	6.3	NEC	5.7	MediaTek (1)	8.8	Infineon	3.9
Top 10 Total ($B)		47.2		108.1		118.2		202.1		117.1
Semi Market ($B)		108.8		218.6		265.5		365.6		201.8
Top 10 % of Total Semi		43%		49%		45%		55%		58%

Source: IC Insights

(1) Fabless

What's happened in KOREA? (ex. SAMSUNG)

(Source: Google images)

What’s happened in KOREA? (ex. SAMSUNG)

삼성바이오로직스 3공장 준공…2020년 본격 생산 시작

송고시간 | 2017/11/30 15:33

"30일 준공 관련 절차 완료"...세계 최대 생산규모 확보

(서울=연합뉴스) 김잔디 기자 = 삼성바이오로직스[207940]가 단일 바이오의약품 생산 공장으로는 세계 최대 규모인 제3공장을 준공했다.

삼성바이오로직스 관계자는 30일 "3공장의 기계적 준공에 관한 모든 절차는 완료했다"며 "이날 중으로 담당 관청인 인천경제자유구역청(IFEZ) 사용 승인까지 나올 것으로 예상한다"고 말했다.

삼성바이오로직스의 3공장은 지상 4층 규모의 면적 11만8천618㎡로, 서울 월드컵경기장 두 배에 달한다. 연간 생산 능력은 18만ℓ다.

특히 3공장에 삼성바이오로직스가 기존에 보유하고 있던 1공장(3만ℓ), 2공장(15만ℓ)을 합하면 연간 36만ℓ의 생산 능력을 갖추게 된다. 경쟁 바이오의약품 위탁생산(CMO) 업체인 스위스의 론자(26만ℓ)나 독일의 베링거인겔하임(24만ℓ)을 뛰어넘는 세계 최대 규모다.

삼성바이오로직스의 3공장은 이후 1년간 생산 설비의 적절성 및 유효성 등을 검증하는 '밸리데이션' 작업을 마친 뒤 2년간의 시제품 생산에 들어간다. 이에 따라 3공장에서 본격적인 생산이 시작되는 시점은 2020년 후반께가 될 것으로 회사는 내다봤다.

현재 삼성바이오로직스는 10개 제약사와 총 15개 제품에 대한 위탁생산 계약을 체결했다. 지금까지 수주 금액은 약 33억달러(한화 3조6천억원) 정도다.

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