

## N- and P-Channel 40 V (D-S) MOSFET

### PRODUCT SUMMARY

	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
N-Channel	40	0.024 at V <sub>GS</sub> = 10 V	8 <sup>e</sup>	6.5
		0.026 at V <sub>GS</sub> = 8 V	8 <sup>e</sup>	
		0.027 at V <sub>GS</sub> = 4.5 V	8	
P-Channel	- 40	0.027 at V <sub>GS</sub> = - 10 V	- 8 <sup>e</sup>	21.7
		0.028 at V <sub>GS</sub> = - 8 V	- 8 <sup>e</sup>	
		0.034 at V <sub>GS</sub> = - 4.5 V	- 7.5	

### FEATURES

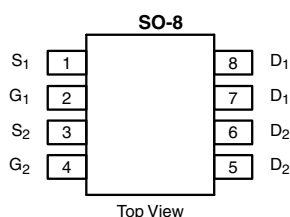
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



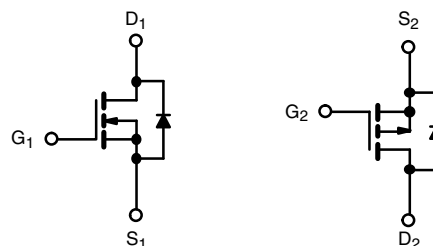
**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Motor Drive



Ordering Information:  
Si4554DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V <sub>DS</sub>	40	- 40	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	8 <sup>e</sup>	- 8 <sup>e</sup>	A
		6.8	- 6.8	
		6.8 <sup>b, c</sup>	- 6.6 <sup>b, c</sup>	
		5.4 <sup>b, c</sup>	- 5.3 <sup>b, c</sup>	
Pulsed Drain Current (10 μs Pulse Width)	I <sub>DM</sub>	40	- 40	
Source-Drain Current Diode Current	I <sub>S</sub>	2.6	- 2.6	
		1.6 <sup>b, c</sup>	- 1.6 <sup>b, c</sup>	
Pulsed Source-Drain Current	I <sub>SM</sub>	40	- 40	
Single Pulse Avalanche Current	L = 0.1 mH I <sub>AS</sub>	10	- 20	
Single Pulse Avalanche Energy	E <sub>AS</sub>	5	20	mJ
Maximum Power Dissipation	P <sub>D</sub>	3.1	3.2	W
		2	2.1	
		2 <sup>b, c</sup>	2 <sup>b, c</sup>	
		1.28 <sup>b, c</sup>	1.28 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s R <sub>thJA</sub>	50	62.5	47	62.5	°C/W
Maximum Junction-to-Foot (Drain)	Steady State R <sub>thJF</sub>	30	40	29	38	

Notes:

a. Based on T<sub>C</sub> = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under steady state conditions is 120 °C/W (n-channel) and 110 °C/W (p-channel).

e. Package limited.

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions		Min.	Typ. <sup>a</sup>	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	N-Ch	40			V	
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	P-Ch	- 40				
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	N-Ch		40		mV/°C	
		I <sub>D</sub> = - 250 μA	P-Ch		- 34			
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	N-Ch		- 4.1			
		I <sub>D</sub> = - 250 μA	P-Ch		5			
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	1		2.2	V	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	P-Ch	- 1.2		- 2.5		
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	N-Ch			± 100	nA	
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	P-Ch			± 100		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V	N-Ch			1	μA	
		V <sub>DS</sub> = - 40 V, V <sub>GS</sub> = 0 V	P-Ch			- 1		
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	N-Ch			10		
		V <sub>DS</sub> = - 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	P-Ch			- 10		
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	N-Ch	20			A	
		V <sub>DS</sub> = - 5 V, V <sub>GS</sub> = - 10 V	P-Ch	- 20				
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6.8 A	N-Ch		0.020	0.024	Ω	
		V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 8 A	P-Ch		0.021	0.027		
		V <sub>GS</sub> = 8 V, I <sub>D</sub> = 6.7 A	N-Ch		0.021	0.026		
		V <sub>GS</sub> = - 8 V, I <sub>D</sub> = - 6.5 A	P-Ch		0.022	0.028		
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.6 A	N-Ch		0.022	0.027		
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 5 A	P-Ch		0.027	0.034		
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 6.8 A	N-Ch		27		S	
		V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 6.7 A	P-Ch		25			
Dynamic <sup>a</sup>								
Input Capacitance	C <sub>iss</sub>	N-Channel V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz  P-Channel V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz	N-Ch		690		pF	
			P-Ch		2000			
Output Capacitance	C <sub>oss</sub>		N-Ch		115			
			P-Ch		240			
Reverse Transfer Capacitance	C <sub>rss</sub>	N-Ch		41				
		P-Ch		202				
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	N-Ch		13.3	20	nC	
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10 A	P-Ch		41.5	63		
		N-Channel V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A	N-Ch		6.5	10		
			P-Ch		21.7	33		
Gate-Source Charge	Q <sub>gs</sub>	P-Channel V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 10 A	N-Ch		2.3			
			P-Ch		5.6			
Gate-Drain Charge	Q <sub>gd</sub>		N-Ch		1.7			
			P-Ch		9.8			
Gate Resistance	R <sub>g</sub>	f = 1 MHz	N-Ch	0.3	1.3	2.6	Ω	
			P-Ch	1.3	6.4	12.8		



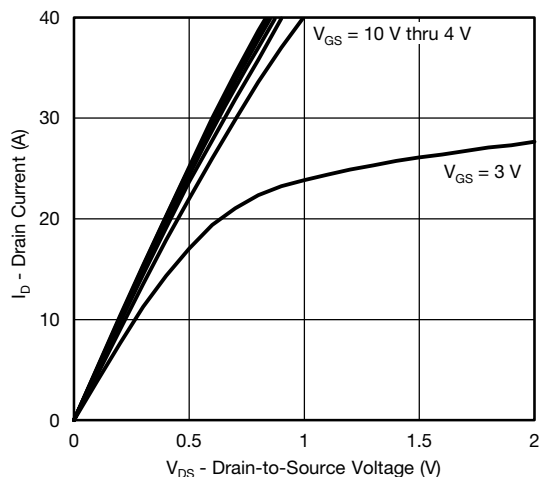
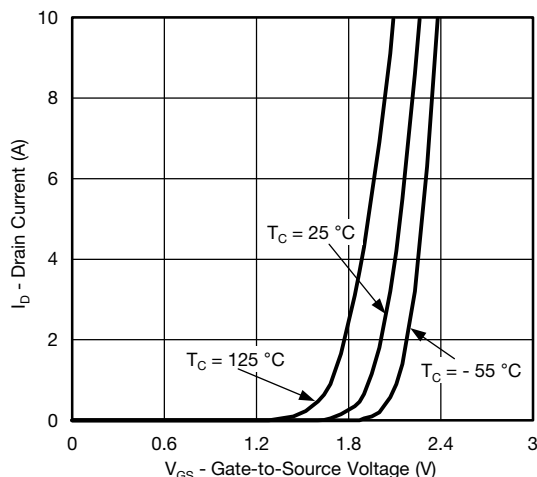
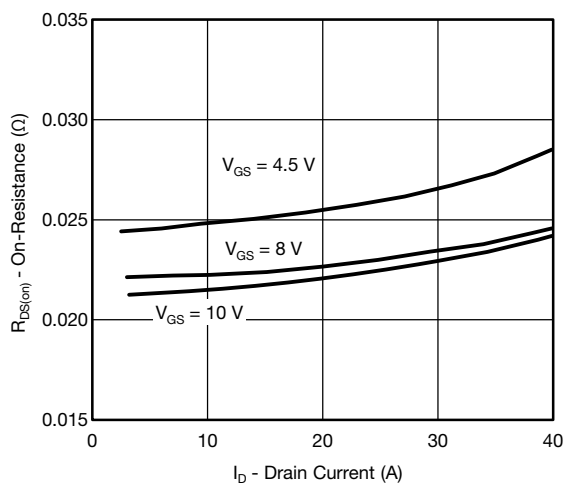
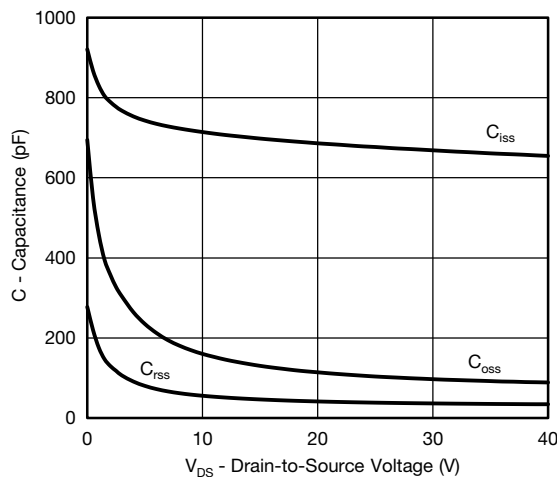
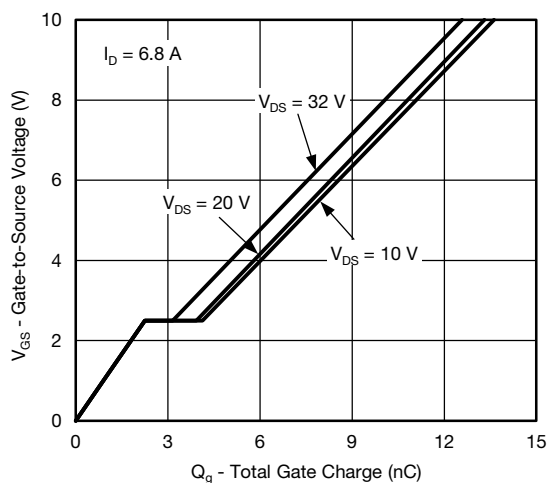
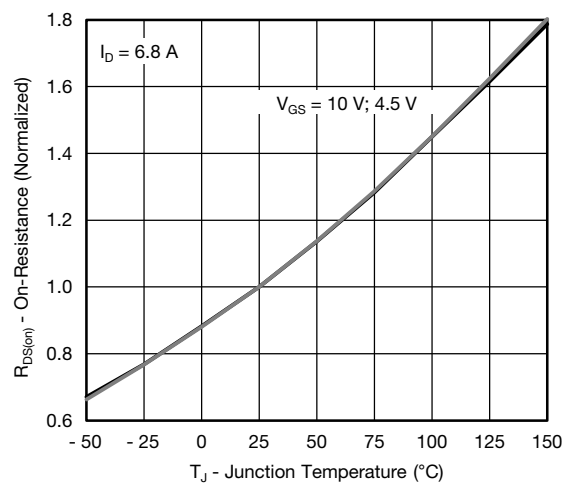
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions		Min.	Typ. <sup>a</sup>	Max.	Unit
Dynamic <sup>a</sup>							
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 20 V, R <sub>L</sub> = 3.7 Ω I <sub>D</sub> ≅ 5.4 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	N-Ch		5	10	ns
			P-Ch		10	20	
Rise Time	t <sub>r</sub>		N-Ch		10	20	
			P-Ch		9	18	
Turn-Off Delay Time	t <sub>d(off)</sub>	P-Channel V <sub>DD</sub> = - 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω	N-Ch		16	25	
			P-Ch		50	90	
Fall Time	t <sub>f</sub>		N-Ch		7	14	
			P-Ch		13	26	
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 20 V, R <sub>L</sub> = 3.7 Ω I <sub>D</sub> ≅ 5.4 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	N-Ch		11	22	ns
			P-Ch		42	75	
Rise Time	t <sub>r</sub>		N-Ch		12	22	
			P-Ch		40	70	
Turn-Off Delay Time	t <sub>d(off)</sub>	P-Channel V <sub>DD</sub> = - 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω	N-Ch		17	26	
			P-Ch		40	70	
Fall Time	t <sub>f</sub>		N-Ch		7	14	
			P-Ch		18	35	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	N-Ch			2.6	A
			P-Ch			- 2.6	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>		N-Ch			40	
			P-Ch			- 40	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 5.4 A	N-Ch		0.81	1.2	V
		I <sub>S</sub> = - 2 A	P-Ch		- 0.77	- 1.2	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	N-Channel I <sub>F</sub> = 5 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C	N-Ch		17	34	ns
			P-Ch		41	80	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	P-Channel I <sub>F</sub> = - 5 A, dI/dt = - 100 A/μs, T <sub>J</sub> = 25 °C	N-Ch		10	20	nC
			P-Ch		32	65	
Reverse Recovery Fall Time	t <sub>a</sub>		N-Ch		10		ns
			P-Ch		15		
Reverse Recovery Rise Time	t <sub>b</sub>	N-Ch		7			
		P-Ch		26			

Notes:

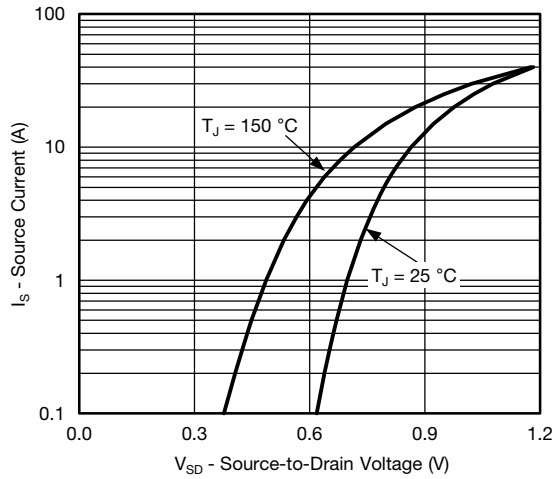
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

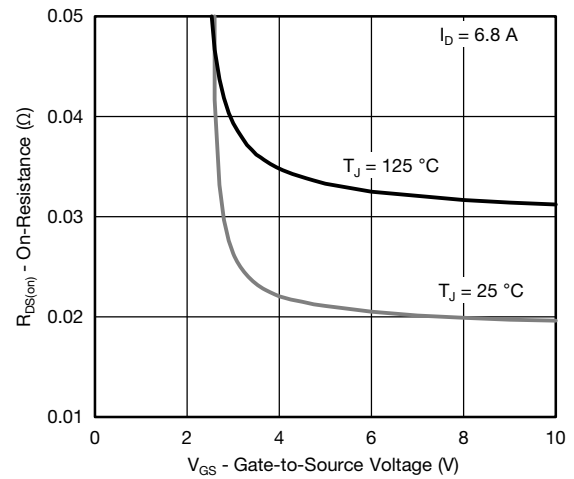
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**N-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

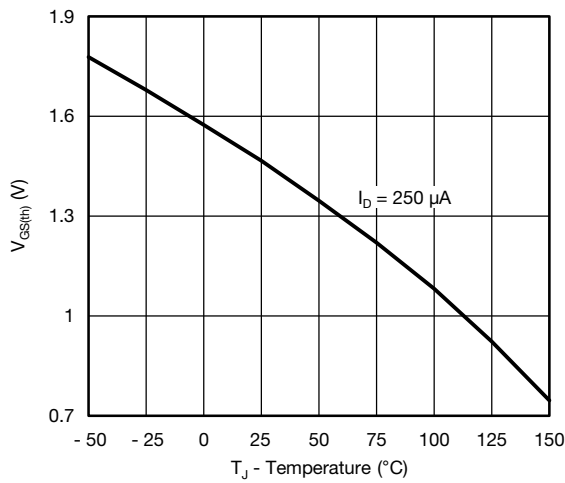
## N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



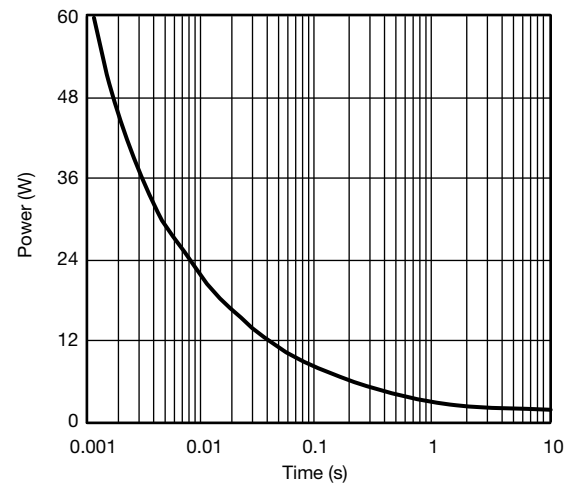
Source-Drain Diode Forward Voltage



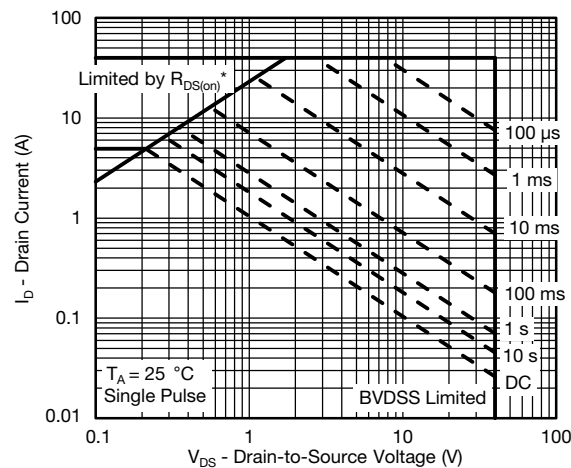
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

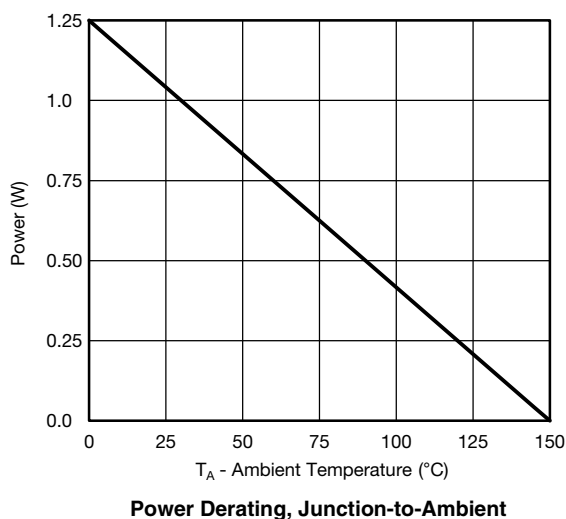
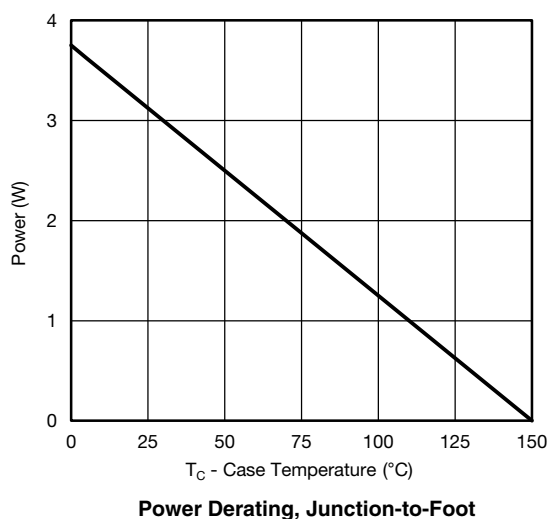
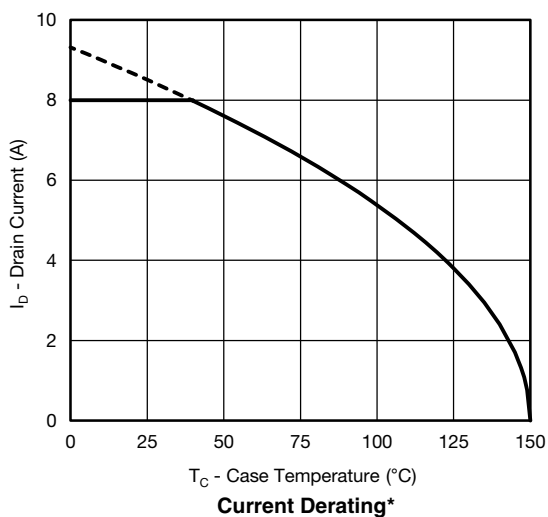


Single Pulse Power, Junction-to-Ambient



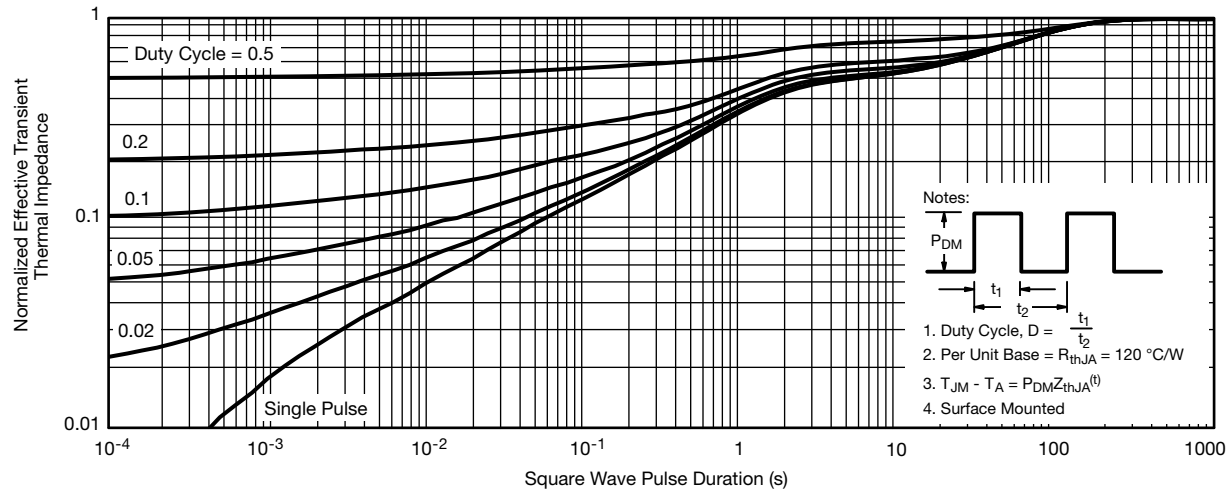
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

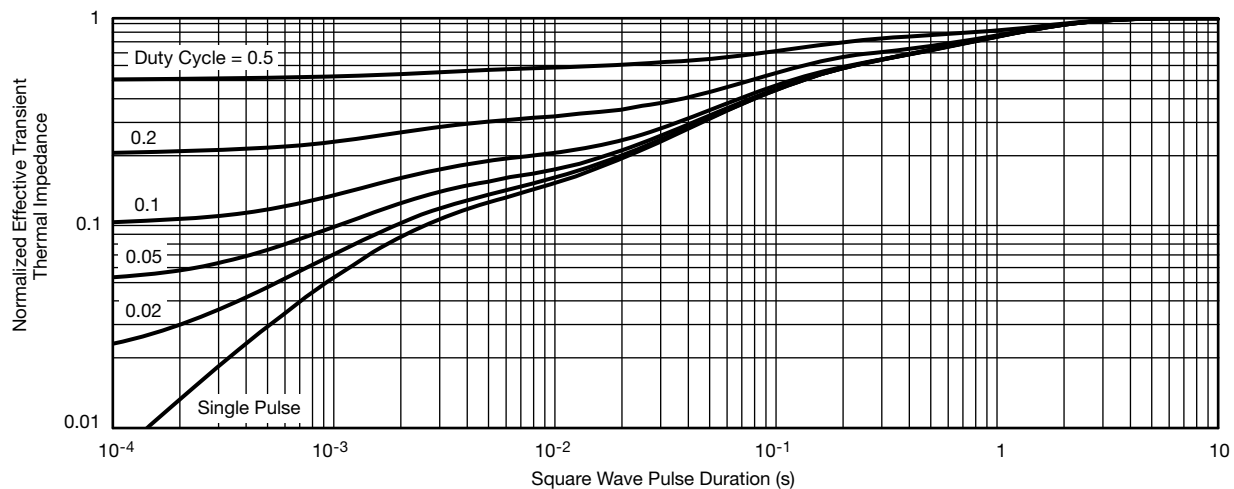
**N-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

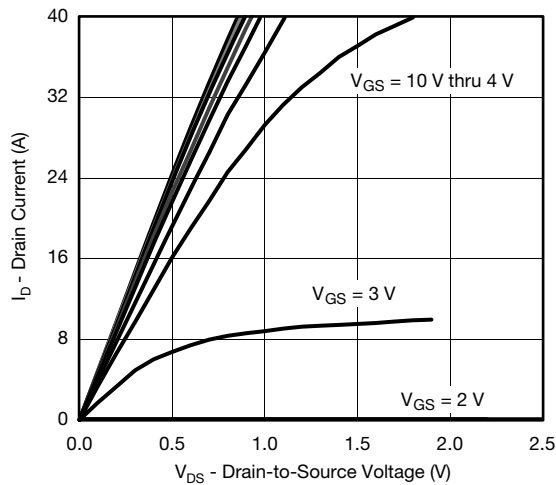
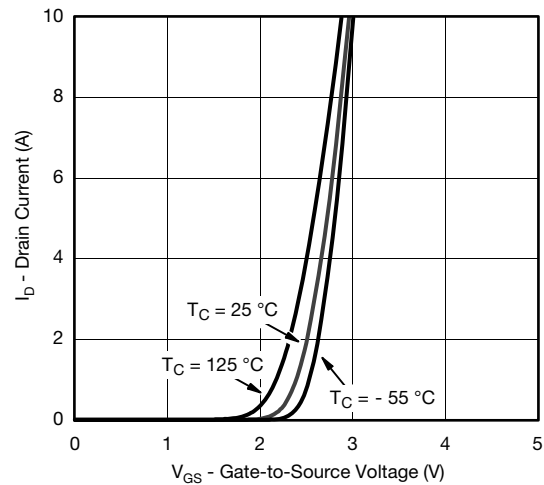
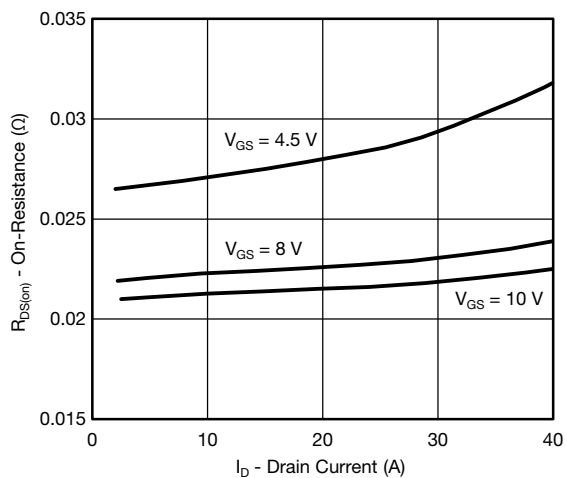
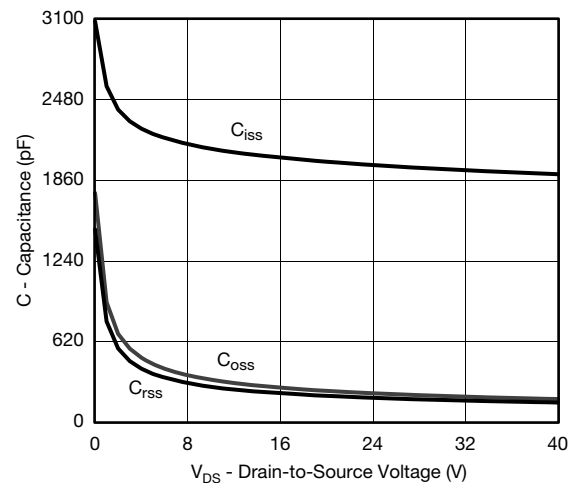
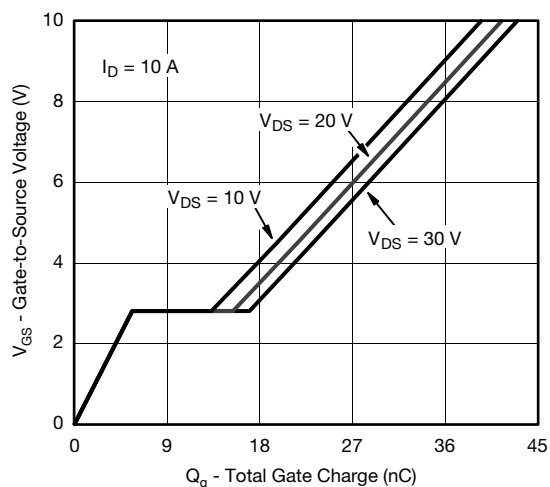
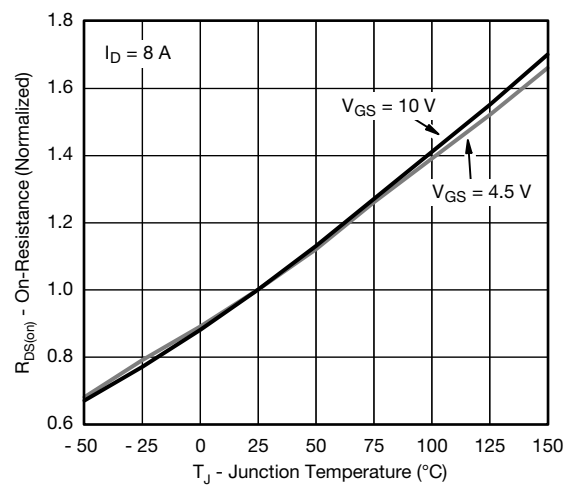
**N-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

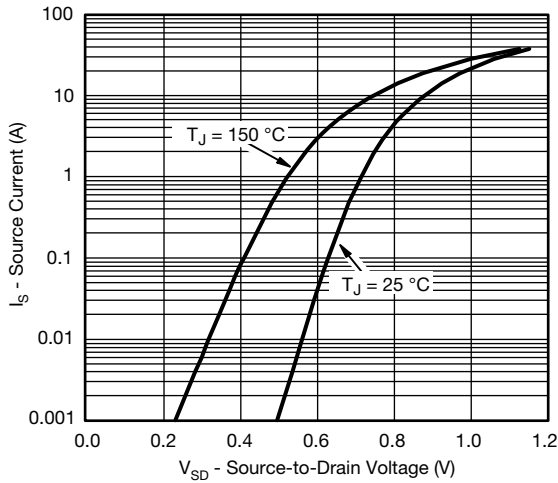


**Normalized Thermal Transient Impedance, Junction-to-Foot**

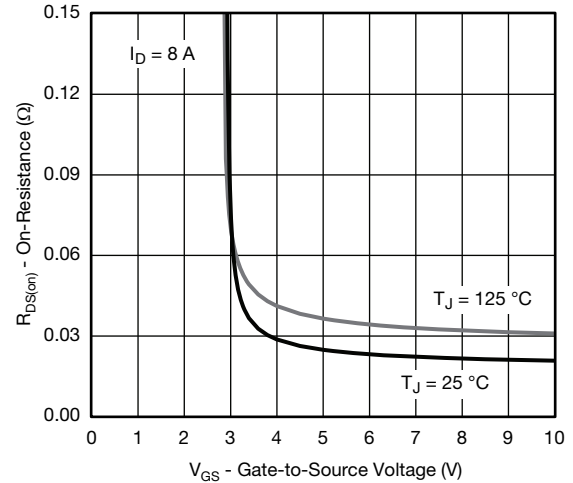
**P-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**



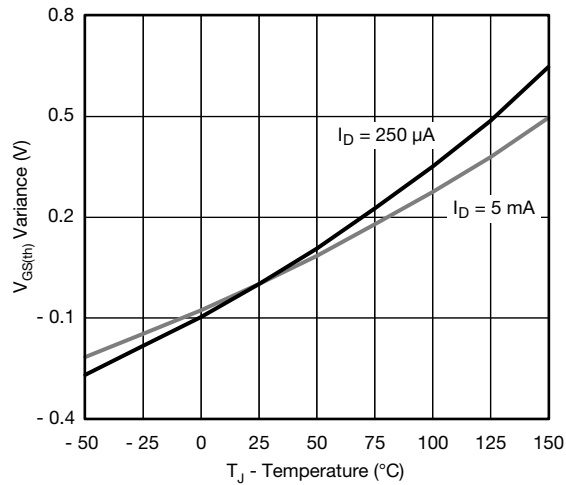
## P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



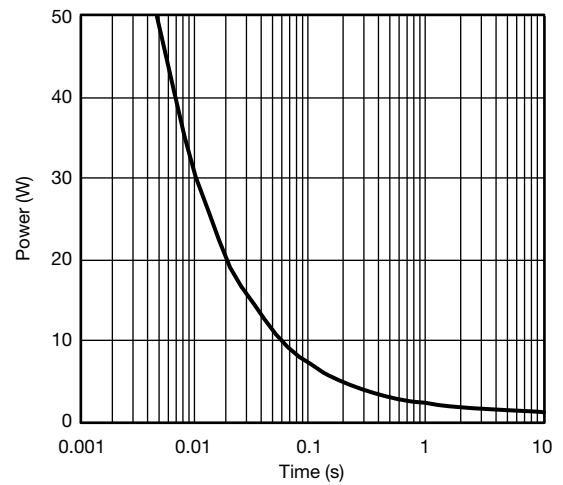
Source-Drain Diode Forward Voltage



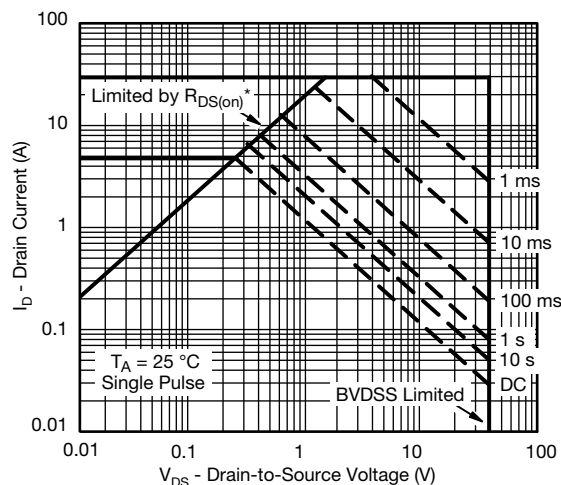
On-Resistance vs. Gate-to-Source Voltage



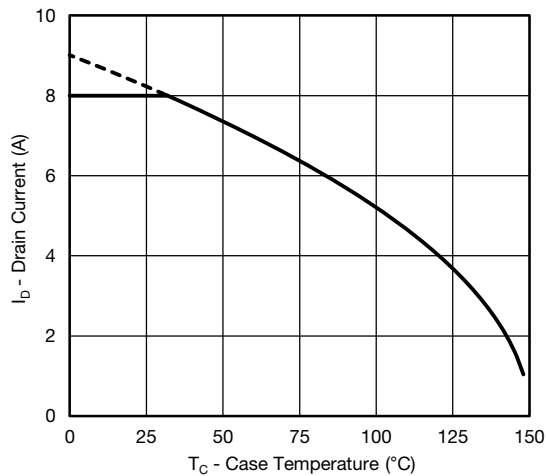
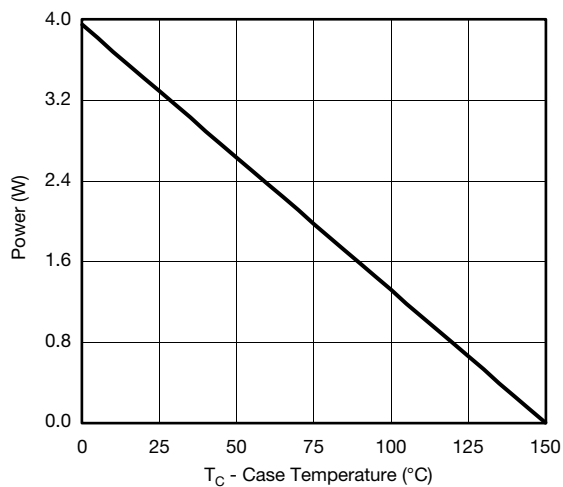
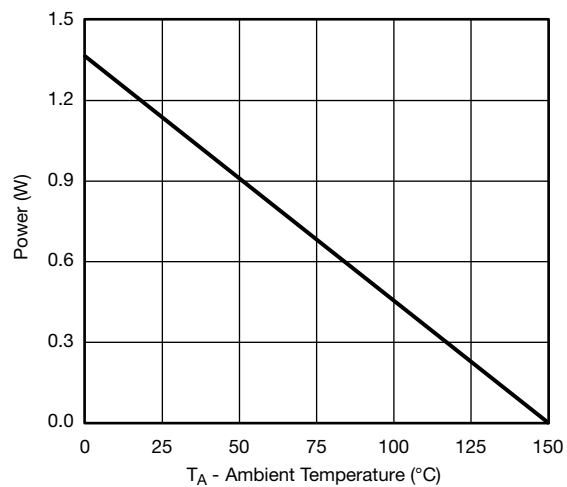
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

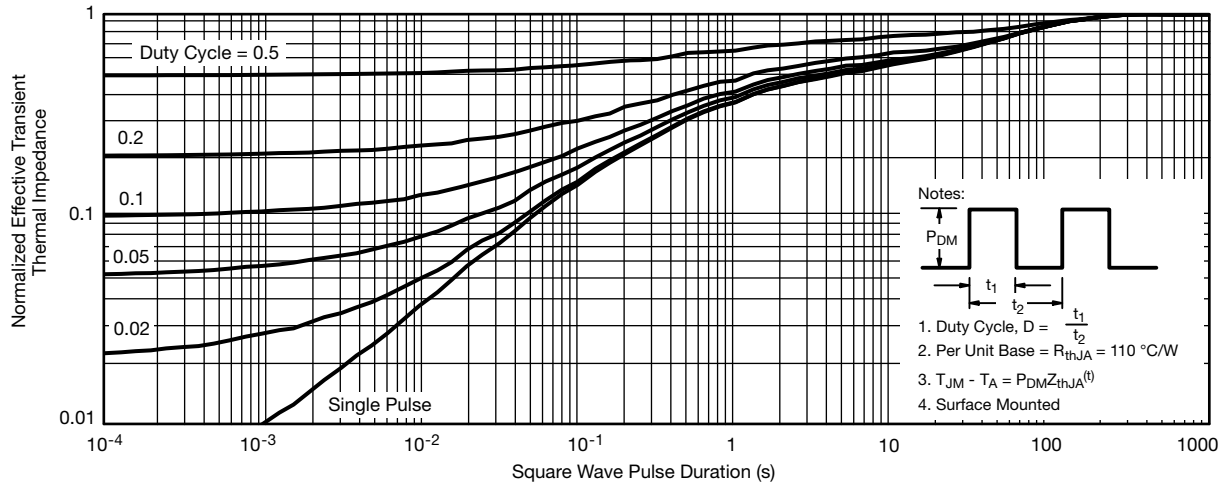


Safe Operating Area, Junction-to-Ambient

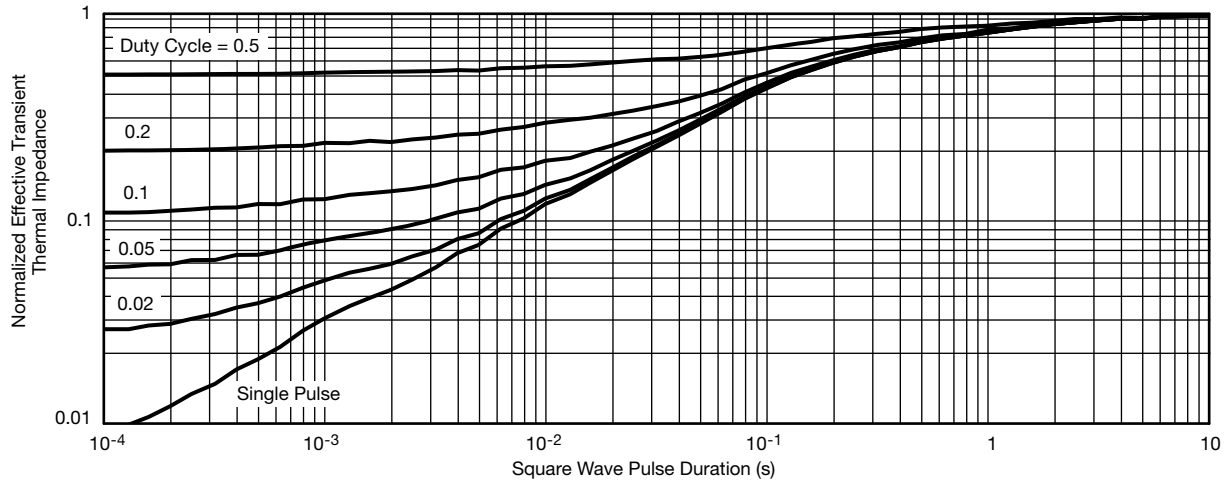
**P-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Current Derating\***

**Power Derating, Junction-to-Foot**

**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**P-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

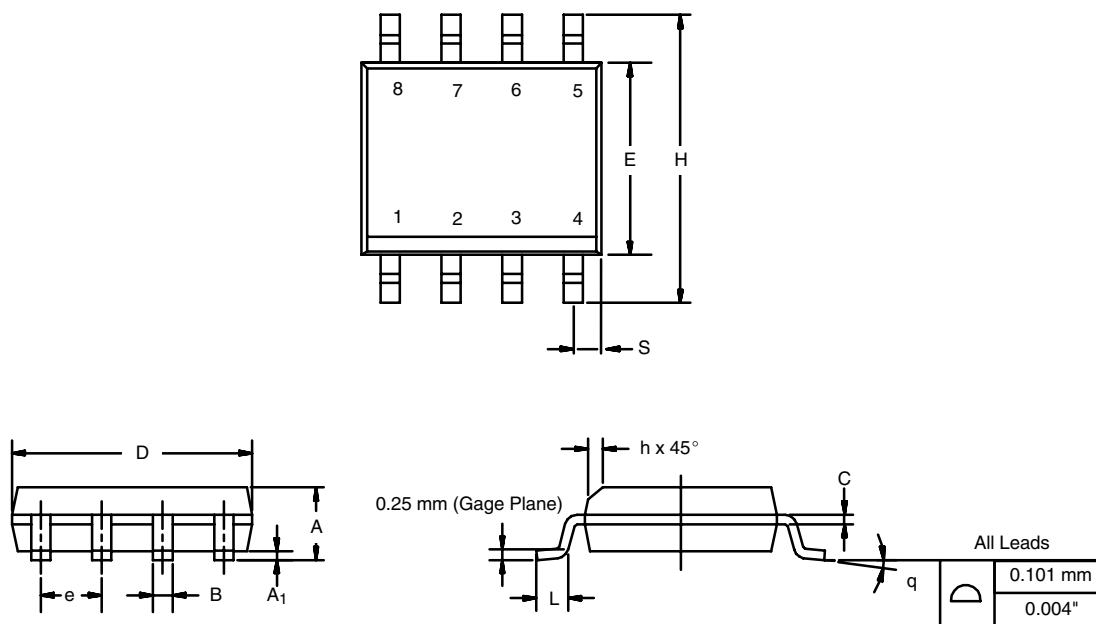


**Normalized Thermal Transient Impedance, Junction-to-Foot**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?63660](http://www.vishay.com/ppg?63660).

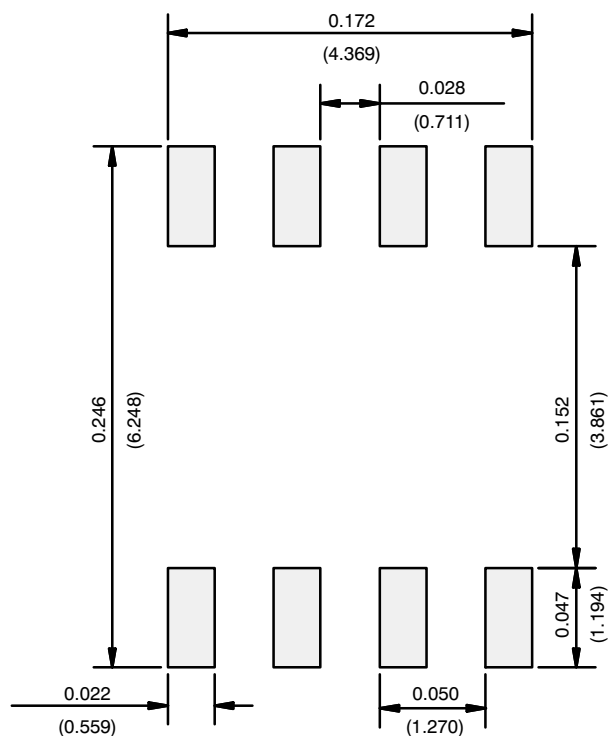
## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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