

JEFFREY GOEDERS

Associate Professor
Department of Electrical and Computer Engineering
Brigham Young University
450J Engineering Building
Provo, UT 84602

jgoeders@byu.edu
github.com/jgoeders
801-422-3499

EDUCATION

- Sep 2012 to Oct 2016** **The University of British Columbia**, *Ph.D., Computer Engineering*
- Sep 2010 to Sep 2012** **The University of British Columbia**, *M.A.Sc., Computer Engineering*
- Sep 2007 to Apr 2010** **University of Toronto**, *B.A.Sc. w/ Honors, Computer Engineering*

PROFESSIONAL EXPERIENCE

- Sep 2022 to Present** **Brigham Young University**, *Associate Professor*
Department of Electrical and Computer Engineering
- July 2016 to Aug 2022** **Brigham Young University**, *Assistant Professor*
Department of Electrical and Computer Engineering

PUBLICATIONS

Book Chapters

1. **Jeffrey Goeders**, Graham M. Holland, Lesley Shannon, and Steven J.E. Wilton, "Systems-on-Chip on FPGAs", in *FPGAs for Software Programmers*, Springer, 2016.
2. Andrew Canis, Jongsok Choi, Blair Fort, Bain Syrowik, Ruo Long Lian, Yu Ting Chen, Hsuan Hsiao, **Jeffrey Goeders**, Stephen Brown, and Jason Anderson, "LegUp high-level synthesis", in *FPGAs for Software Programmers*, Springer, 2016.

Peer-Reviewed Journal Articles

3. Daniel Hutchings, Adam Taylor, and **Jeffrey Goeders**, "Toward FPGA Intellectual Property (IP) Encryption from Netlist to Bitstream", in *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 2024.
4. Nathan Harris, Wesley Stirk, Dolores Black, Jeff Black, Michael Wirthlin, and **Jeffrey Goeders**, "Dynamic Testing of a Commercial FRAM Device Under Gamma Ray Dose and Neutron Beam", in *IEEE Transactions on Nuclear Science (TNS)*, 2024.

5. Wesley Stirk, Dolores A. Black, Jeffrey D. Black, Matthew Breeding, Roy P. Cuoco, Mike Wirthlin, and **Jeffrey Goeders**, “The Effects of Gamma Ray Integrated Dose on a Commercial 65-nm SRAM Device”, in IEEE Transactions on Nuclear Science (TNS), Jun 2023.
6. Wesley Stirk, Evan Poff, Jackson Smith, **Jeffrey Goeders**, and Michael Wirthlin, “Comparison of Neutron Radiation Testing Approaches for a Complex SoC”, in IEEE Transactions on Nuclear Science (TNS), Jan 2023.
7. Hayden Cook, Jacob Arscott, Brent George, Tanner Gaskin, **Jeffrey Goeders**, and Brad Hutchings, “Inducing Non-Uniform FPGA Aging Using Configuration-Based Short Circuits”, in ACM Transactions on Reconfigurable Technology and Systems (TRETs), vol. 15, no. 4, pp.1-33, Jun 2022.
8. Eli Cahill, Brad Hutchings and **Jeffrey Goeders**, “Approaches for FPGA Design Assurance”, in ACM Transactions on Reconfigurable Technology and Systems (TRETs), vol. 15, no. 3, pp.1-29, Dec 2021.
9. Benjamin James, Michael Wirthlin, and **Jeffrey Goeders**, “Investigating How Software Characteristics Impact the Effectiveness of Automated Software Fault Tolerance”, in IEEE Transactions on Nuclear Science (TNS), vol. 68, no. 5, pp. 1014-1022, Apr 2021.
10. Al-Shahna Jamal, Eli Cahill, **Jeffrey Goeders**, and Steven JE Wilton, “Fast Turnaround HLS Debugging using Dependency Analysis and Debug Overlays”, in ACM Transactions on Reconfigurable Technology and Systems (TRETs), vol. 13, no. 1, pp. 1-26, Feb 2020.
11. Benjamin James, Heather Quinn, Michael Wirthlin, and **Jeffrey Goeders**, “Applying Compiler-Automated Software Fault Tolerance to Multiple Processor Platforms”, in IEEE Transactions on Nuclear Science (TNS), vol. 67, no. 1, pp. 321-327, Jan 2020.
12. Matthew Bohman, Benjamin James, Michael Wirthlin, Heather Quinn, and **Jeffrey Goeders**, “Microcontroller Compiler-Assisted Software Fault Tolerance”, in IEEE Transactions on Nuclear Science (TNS), vol. 66, no. 1, pp. 223-232, Jan 2019.
13. **Jeffrey Goeders**, and Steven J.E. Wilton, “Signal-Tracing Techniques for In-System FPGA Debugging of High-Level Synthesis Circuits”, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 36, no. 1, pp. 83-96, Jan 2017.
14. **Jeffrey Goeders** and Steven J.E. Wilton, “Power Aware Architecture Exploration for Field Programmable Gate Arrays”, in Journal of Low Power Electronics (JOLPE), vol. 10, no. 3, pp. 297-312, Sep. 2014.
15. Jason Luu, **Jeffrey Goeders**, Michael Wainberg, Andrew Somerville, Thien Yu, Konstantin Nasartschuk, Miad Nasr, Sen Wang, Tim Liu, Nooruddin Ahmed, Kenneth B Kent, Jason Anderson, Jonathan Rose, and Vaughn Betz, “VTR 7.0: Next Generation Architecture and CAD System for FPGAs”, in ACM Transactions on Reconfigurable Technology and Systems (TRETs), vol 7, no. 2, pp. 6:1–30, Jul 2014.

Peer-Reviewed International Conference Publications

16. Reilly McKendrick, Keenan Faulkner, and **Jeffrey Goeders**, “Assuring Netlist-to-Bitstream Equivalence using Physical Netlist Generation and Structural Comparison”, in International Conference on Field Programmable Technology (FPT), Dec 2023.
17. Dallin Dahl, Corey Simpson, Keenan Faulkner, Brent Nelson, and **Jeffrey Goeders**, “IPRec and Isoblaze: Fuzzy Subcircuit Isomorphism for IP Detection in Physical Netlists”, in Physical Assurance and Inspection of Electronics Conference (PAINE), 26-32, Oct 2023.
18. Hayden Cook, Zephram Tripp, Brad Hutchings, and **Jeffrey Goeders**, “Improving the Reliability of FPGA CRO PUFs”, in International Conference on Field-Programmable Logic and Applications (FPL), 311-316, Sep 2023.
19. Reilly McKendrick, Keenan Faulkner, and **Jeffrey Goeders**, “Assuring Netlist-to-Bitstream Equivalence using Physical Netlist Generation and Structural Comparison”, in International Conference on Field-Programmable Technology (FPT), Dec 2023.
20. Hayden Cook, Jonathan Thompson, Zephram Tripp, Brad Hutchings, **Jeffrey Goeders**, “Cloning the Unclonable: Physically Cloning an FPGA Ring-Oscillator PUF”, in International Conference on Field-Programmable Technology (FPT), 1-10, Dec 2022.
21. Reilly McKendrick, Corey Simpson, Brent Nelson, and **Jeffrey Goeders**, “Leveraging FPGA Primitives to Improve Word Reconstruction during Netlist Reverse Engineering”, in International Conference on Field-

- Programmable Technology (FPT), 1-5, Dec 2022.
22. Benjamin James, and **Jeffrey Goeders**, “Automated Software Compiler Techniques to Provide Fault Tolerance for Real-Time Operating Systems”, in Design, Automation and Test in Europe Conference (DATE), Feb 2021.
 23. Tanner Gaskin, Hayden Cook, Wesley Stirk, Robert Lucas, **Jeffrey Goeders**, and Brad Hutchings, “Using Novel Configuration Techniques for Accelerated FPGA Aging”, in International Conference on Field-Programmable Logic and Applications (FPL), Aug 2020.
 24. Matthew Ashcraft and **Jeffrey Goeders**, “Synchronizing On-Chip Software and Hardware Traces for HLS-Accelerated Programs”, in International Conference on Field Programmable Technology (FPT), Dec 2019.
 25. Wesley Stirk and **Jeffrey Goeders**, “Implementation and Design Space Exploration of a Turbo Decoder in High-Level Synthesis”, in International Conference on Reconfigurable Computing and FPGAs (ReConFig), Dec 2019.
 26. Daniel Holanda Noronha, Ruizhe Zhao, Zhiqiang Que, **Jeffrey Goeders**, Wayne Luk and Steve Wilton, “An Overlay for Rapid FPGA Debug of Machine Learning Applications”, in International Conference on Field Programmable Technology (FPT), Dec 2019.
 27. Daniel Holanda Noronha, Ruizhe Zhao, **Jeffrey Goeders**, Wayne Luk, and Steven J.E. Wilton, “On-chip FPGA Debug Instrumentation for Machine Learning Applications”, in International Symposium on Field-Programmable Gate Arrays (FPGA), pp. 110-115, Feb 2019.
 28. Matthew Ashcraft and **Jeffrey Goeders**, “Unified On-Chip Software and Hardware Debug for HLS-Accelerated Programs”, in International Conference on Field Programmable Technology (FPT), pp. 354-357, Dec 2018.
 29. Al-Shahna Jamal, **Jeffrey Goeders** and Steve Wilton, “An FPGA Overlay Architecture Supporting Rapid Implementation of Functional Changes during On-Chip Debug”, in International Conference on Field Programmable Logic and Applications (FPL), Aug 2018.
 30. **Jeffrey Goeders**, Tanner Gaskin, and Brad Hutchings, “Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ”, in International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2018.
 31. Al-Shahna Jamal, **Jeffrey Goeders**, and Steven J.E. Wilton, “Architecture Exploration for HLS-Oriented FPGA Debug Overlays”, in International Symposium on Field-Programmable Gate Arrays (FPGA), Feb 2018.
 32. Pavan Kumar Bussa, **Jeffrey Goeders**, and Steven JE Wilton, “Accelerating in-system FPGA debug of high-level synthesis circuits using incremental compilation techniques”, in International Conference on Field Programmable Logic and Applications (FPL), Sep 2017.
 33. **Jeffrey Goeders**, “Enabling Long Debug Traces of HLS Circuits Using Bandwidth-Limited Off-Chip Storage Devices”, in International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2017.
 34. **Jeffrey Goeders**, and Steven J.E. Wilton, “Quantifying observability for in-system debug of high-level synthesis circuits”, in International Conference on Field Programmable Logic and Applications (FPL), pp. 1–11, Aug 2016.
 35. **Jeffrey Goeders**, and Steven J.E. Wilton, “Using Round-Robin Tracepoints to Debug Multithreaded HLS Circuits on FPGAs”, in International Conference on Field Programmable Technology (FPT), Dec 2015.
 36. **Jeffrey Goeders**, and Steven J.E. Wilton, “Using Dynamic Signal-Tracing to Debug Compiler-Optimized HLS Circuits on FPGAs”, in International Symposium on Field-Programmable Custom Computing Machines (FCCM), pp. 127-134, May 2015. **Best Paper Award**.
 37. **Jeffrey Goeders**, and Steven J.E. Wilton, “Effective FPGA Debug for High-Level Synthesis Generated Circuits”, in International Conference on Field Programmable Logic and Applications (FPL), pp. 1-8, Sep 2014.
 38. Eddie Hung, **Jeffrey Goeders**, and Steven J.E. Wilton, “Faster FPGA Debug: Efficiently Coupling Trace Instruments with User Circuitry”, in International Symposium on Applied Reconfigurable Computing (ARC), pp. 73-84, Apr 2014.
 39. **Jeffrey Goeders**, and Steven J.E. Wilton, “VersaPower: Power Estimation for Diverse FPGA Architectures”, in International Conference on Field Programmable Technology (FPT), pp. 229-234, Dec 2012.
 40. Jonathan Rose, Jason Luu, Chi Wai Yu, Opal Densmore, **Jeffrey Goeders**, Andrew Somerville, Kenneth B. Kent, Peter Jamieson, and Jason Anderson, “The VTR Project: Architecture and CAD for FPGAs from

Verilog to Routing”, in International Symposium on Field Programmable Gate Arrays (FPGA), pp. 77-86, Feb 2012.

41. **Jeffrey Goeders**, Guy Lemieux, and Steven J.E. Wilton, “Deterministic Timing-Driven Parallel Placement by Simulated Annealing Using Half-Box Window Decomposition”, in International Conference on Reconfigurable Computing and FPGAs (ReConFig), pp. 41-48, Dec 2011.

Peer-Reviewed International Workshop Publications

42. Adam Hastings, Sean Jensen, **Jeffrey Goeders**, and Brad Hutchings, “Using Physical and Functional Comparisons to Assure 3rd-Party IP for Modern FPGAs”, in International Verification and Security Workshop (IVSW), Jul 2018.

Peer-Reviewed International Oral Presentations

43. Wesley Stirk, **Jeffrey Goeders**, Michael Wirthlin, Jeff Black, Dolores Black, and Roy Cuoco., “The Effects of Gamma Ray Integrated Dose on a Commercial 65nm SRAM Device”, in Radiation Effects on Components and Systems (RADECS), Oct 2022.
44. Benjamin James, Michael Wirthlin, and **Jeffrey Goeders**, “Understanding How Software Properties Impact the Effectiveness of Automated Software Fault Tolerance”, in Nuclear and Space Radiation Effects Conference (NSREC), Dec 2020.
45. Benjamin James, Michael Wirthlin, Heather Quinn, and **Jeffrey Goeders**, “Applying Compiler-Automated Software Fault Tolerance to Multiple Processor Platforms”, in Nuclear and Space Radiation Effects Conference (NSREC), Jul 2019.

CITATIONS

Citations: 1362

h-index: 14

i10-index: 17

PROFESSIONAL ACTIVITIES

Senior Member, IEEE

Senior Member, ACM

Workshop Organizer

Workshop on Security for Custom Computing Machines (SCCM) - 2019, 2022, 2023, 2025

Publicity Chair

International Workshop on LLM-Aided Design (LAD) - 2024

International Conference on LLM-Aided Design (LAD) - 2025

Short Course Speaker

IEEE Nuclear & Space Radiation Effects Conference (NSREC) - 2025

Sponsorship Chair

International Symposium on Field-Programmable Custom Computing Machines (FCCM) - 2025

Workshop Chair

International Symposium on Field-Programmable Custom Computing Machines (FCCM) - 2024

Information Director

ACM Transactions on Reconfigurable Technology and Systems (TRETs) - 2018 to Present

Contest Organizer

Design Automation Conference (DAC) System Design Contest - 2020 to 2023

Technical Program Committee (TPC) Member

International Symposium on Field-Programmable Gate Arrays (FPGA) - 2017 to Present

International Conference on Field-Programmable Technology (FPT) - 2016 to 2019

International Conference on Field-Programmable Custom Computing Machines (FCCM) - 2018, 2020 to Present

Reviewer

ACM Transactions on Reconfigurable Technology and Systems (TRETs) - 2016 to Present

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) - 2016 to Present

IEEE Transactions on Nuclear Science (TNS) - 2018 to Present

IEEE Transactions on Computers (TC) - 2019 to 2020

ACM Transactions on Architecture and Code Optimization (TACO) - 2017

International Journal of Reconfigurable Computing - 2016

GRANTS

2025 to 2025	Mike Wirthlin and Jeffrey Goeders , "LLM-aided Design of High-Level Synthesis Circuits" <i>AMD</i> , \$30,000
2023 to Present	Jeffrey Goeders and Michael Wirthlin, "Investigation of radiation effects and development of testing capabilities on Complex ICs in a radiation environment" <i>Sandia National Laboratories</i> , \$200,000
2022 to 2025	Jeffrey Goeders , "FPGA Bitstream-level Equivalence Checking: Securing the FPGA 'Digital Fab'" <i>Office of Naval Research (ONR)</i> , \$291,897
2022 to 2025	Jeffrey Goeders , "GramaTech: FPGA Bitstream Analysis" <i>GramaTech, Office of Naval Research (ONR)</i> , \$267,050
2020 to 2026	Michael Wirthlin and Jeffrey Goeders , "Interaction of Ionizing Radiation with Matter, University Research Alliance (IIRM-URA)" <i>Defense Threat Reduction Agency (DTRA)</i> , \$1,095,000
2018 to Present	Michael Wirthlin, Jeffrey Goeders , Brad Hutchings, and Brent Nelson, "Phase-I IUCRC Brigham Young University: Center For Space, High-Performance, and Resilient Computing (SHREC)" <i>National Science Foundation (NSF)</i> , \$1,209,256
2021	Jeffrey Goeders and Brad Hutchings, "Empirical Investigations of Field-Programmable Gate Arrays" <i>Northrup Grumman</i> , \$30,000
2021	Jeffrey Goeders and Brent Nelson, "Virtual Xilinx Platform in VTR" <i>Google</i> , \$60,000
2021	Jeffrey Goeders and Brad Hutchings, "Improving Bitstream Verification Tooling" <i>Google</i> , \$40,000
2021	Brent Nelson, Jeffrey Goeders , Mike Wirthlin, and Brad Hutchings, "Boot Camp for the FPGA Community" <i>Google</i> , \$40,000
2017	Brent Nelson and Jeffrey Goeders , "CHREC Industry Memberships" <i>National Instruments</i> , \$40,000