EE120A Logic Design
Department of Electrical Engineering
University of California – Riverside

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LABORATORY # 5
L A B M A N U A L

Timer Design

Objectives

1. Design of counters, synthesis and implementation;
2. Usage of internal "clock" signal to drive CLK inputs of flip-flops;
3. Design of special purpose timers

Equipment

- PC or compatible
- Digilent's Basys Spartan-3E FPGA Evaluation Board

Software

- Xilinx ISE Design Software Suite 10.1
- ModelSim XE III modeling software
- Digilent's Adept ExPort Software

Parts

- N/A

Timer Design

In this FPGA application development experiment, we will implement a special purpose 1 ms timer

Specification

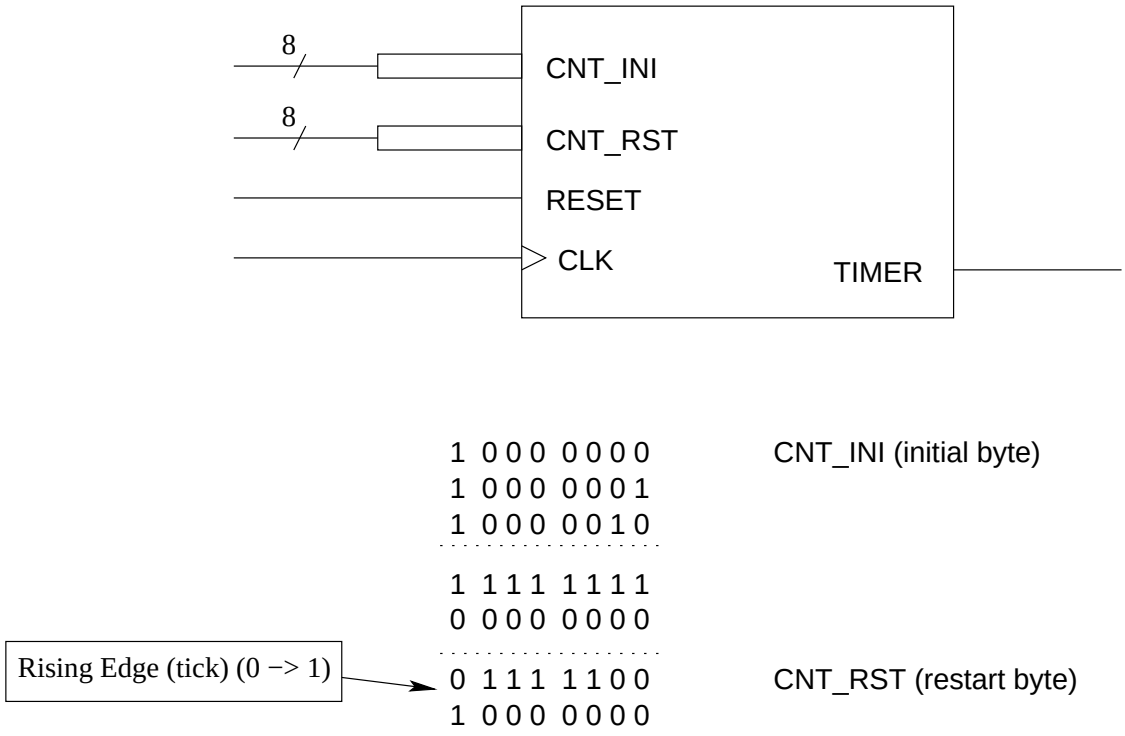

Figure L5-1. Timer Structure and Function

The action of timers is based on system clock's time division. It is built as a counter whose MSB controls the output (a tick). For example, an 8-bit counter will switch its MSB from 0 to 1 only once per 256 internal clock counts (from 0 to 255). But what if we need a timer that creates a tick every 250 counts (from 0 to 249) starting from MSB=1 ? From this description we can infer the required timer block diagram as shown in Figure 1.

The assignment is to create such a timer and implement it on the Basys board which uses 25 MHz internal clock (CLK) and output a timer tick every 1 ms. Use one of Basys board Pmod pins to ooserve the timer operation on an oscilloscope.

Implementation Utilities and Hints

1. Make sure that the jumper is set to 25 MHz clock on the Basys Board (default is 50 MHz).

2. The following CLK configuratio nmust be used in the constraints file:

```
# clock pin for Basys Board
NET "CLK" LOC = "p54"; # Bank = 2, Signal name = CLK1
```

Demonstration

Demostrate that the application performs according to specs: both simulation and oscilloscope periodic signal with 1 ms period (that is 1 kHz frequency).

Procedures

1. Xilinx ISE Design and Synthesis environment;
2. Creation of Configuration files;
3. Usage of Adept ExPort download software;

Presentation and Report

Must be presented according to the general EE120A lab guidelines posted in iLearn.

Prelab

1. Review Lectures 10-11;
2. Try to answer all the questions, prepare logic truth tables, do all necessary computations