Final exam for CMPE 3403 (Electronics for Computer Engineering)

1:15pm-3:00pm 5/5/2020

You have 15 minutes for uploading your answer sheets to Blackboard, so please finish uploading by 3:15pm.

Name: _____, ID#:_____

Note: this exam is an online exam with open-book and open-notes. For your convenience of uploading, you can write your solutions (including reasonable details) on papers and scan/take pictures, upload to Blackboard in the same way as you did for homework assignments. **Please be sure to write you name, and ID# on the first page of your submission**, and to submit your work to Blackboard **by 3:15 pm**.

I. Multiple Choice (30 points)

1. The *i-v* curve of the diode in Fig.1(a) is plotted in Fig.1.(b), then the value of v_o in Fig.1(a) is
   a) 0 V
   b) 0.5 V
   c) 1 V
   d) 10 V

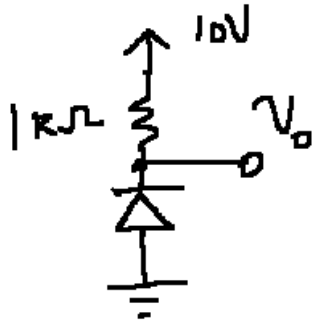

Fig.1 (a)

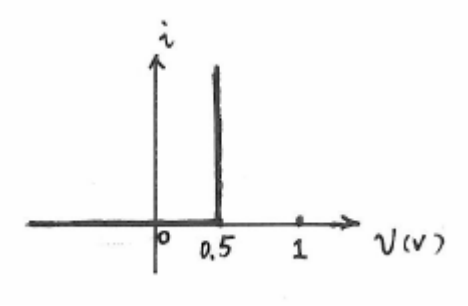

Fig.1 (b)

2. The 3D structure of a MOSFET is shown in Fig.2. The channel width of the transistor is
   a) 1.8 um
   b) 0.18 um
   c) Not shown
   d) Could be any

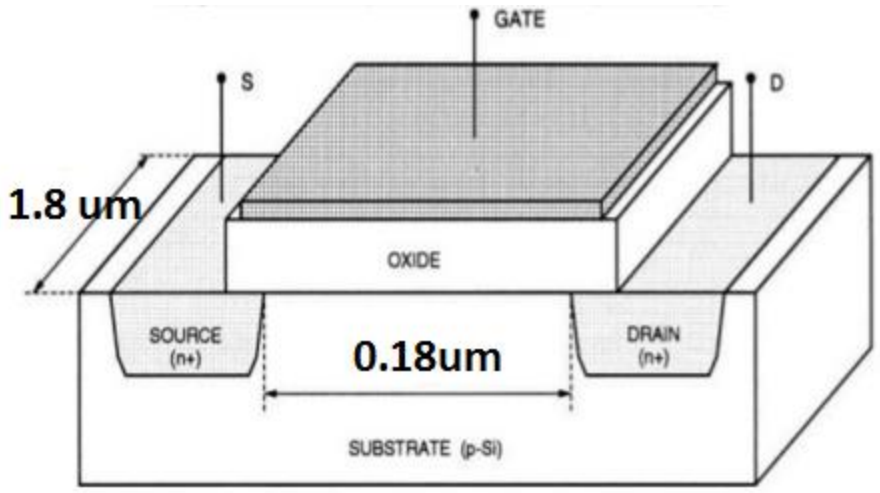

Fig.2 the structure of a transistor

3. The voltage gain of the circuit in Fig.3 is defined as v_o/v_I. What is the voltage gain?
   a) 1
   b) 2
   c) 3
   d) 4

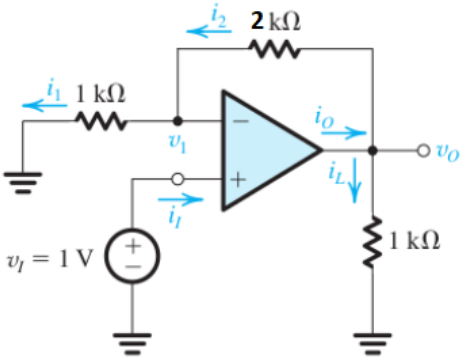

Fig.3

4. In Fig.3, the value of i_o is
   a) 1 mA
   b) 2 mA
   c) 3 mA
   d) 4 mA

5. The PMOS transistor has Vtp=-1 V. If the voltages of three terminals are: Vg=2 V, Vs=5V, Vd=1V, then the transistor is operated in
   a) Cut off region
   b) Triode region
   c) Saturation region
   d) Unknown

6. The voltage transfer characteristic of a CMOS inverter is shown in Fig.4. Threshold voltages $V_{tn} = |V_{tp}| = 0.5V$. If the input v_i=1V, then
   a) Both PMOS and NMOS in triode region
   b) Both PMOS and NMOS in saturation
   c) PMOS in triode region, and NMOS in saturation
   d) PMOS in saturation, and NMOS in triode

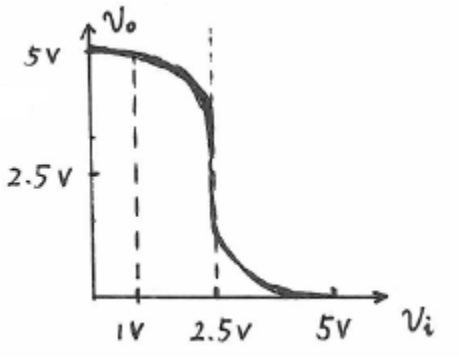

Fig. 4

II. (20 points) For the circuit in Fig.5, find the value of R that results in V_D=1V. The PMOS transistor has V_{tp}=-0.5 V, u_pC_{ox}=100uA/V^2, W/L=7.2um/0.18um, and λ=0.

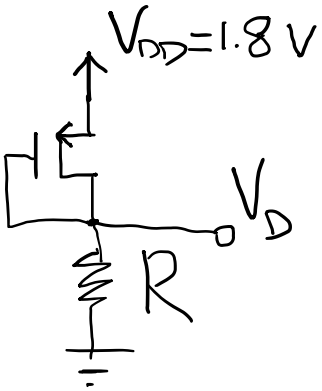

Fig.5

III. (20 points) Logic gate design at transistor level:

1) Find the Pull-up network (PUN) that corresponds to the Pull-down network (PDN) shown in Fig.6.
2) Draw the complete CMOS logic circuit using the PUN and PDN.
3) Find the logic function for the circuit you derived in 2).

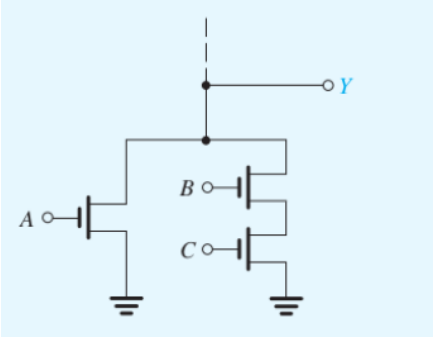

Fig.6

IV. (30 points) The circuit in Fig.7 utilizes an ideal operational amplifier.

a) Find $I_1, I_2, I_3, I_L, and\ V_x$.
b) If V_o is not to be lower than -13 V, find the maximum allowed value for R_L.
c) If R_L is varied in the range 100 Ω to 1 kΩ, what is the corresponding change in I_L and in V_o?

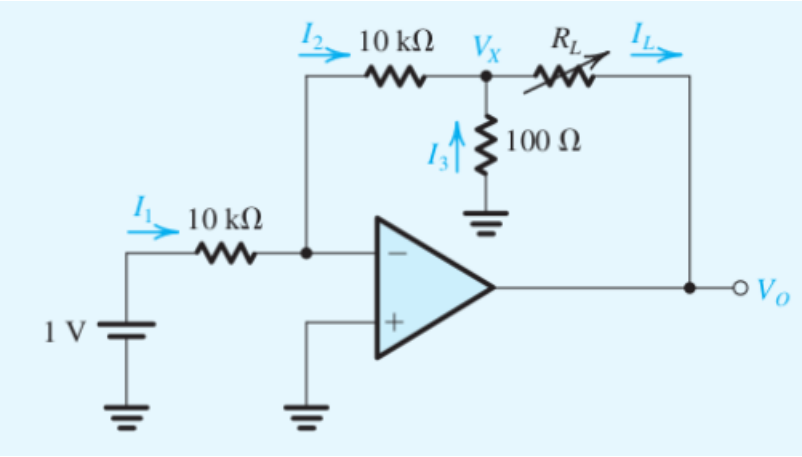

Fig.7