EE 310 – Lab 5

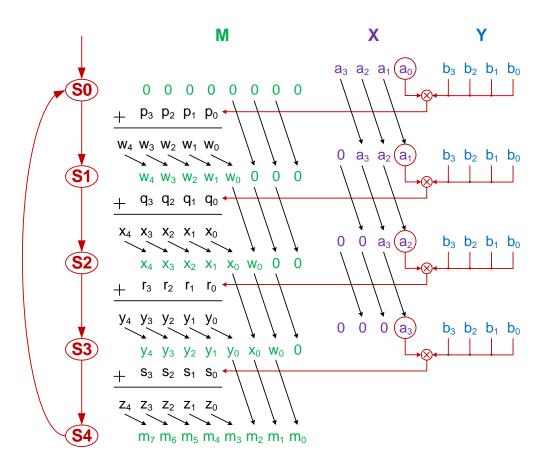
NAU, 5-6 March 2020

In this lab, you are going to design a synchronous 4-bit unsigned multiplier. Unsigned binary multiplication operation is realized using simple schoolbook multiplication as shown below, where how the algorithms works is also illustrated with a numerical example, where $A = 11_{10} = 1011_2$ and $B = 13_{10} = 1101_2$:

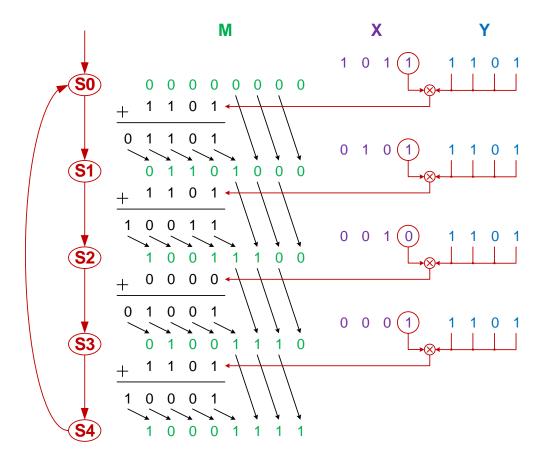
The same multiplication can also be implemented as follows:

As can be seen here, multiplication can be implemented with 4 iterations, where a single 4-bit addition is performed at each iteration. Iterative nature of the operation make it possible to implement it using a state machine.

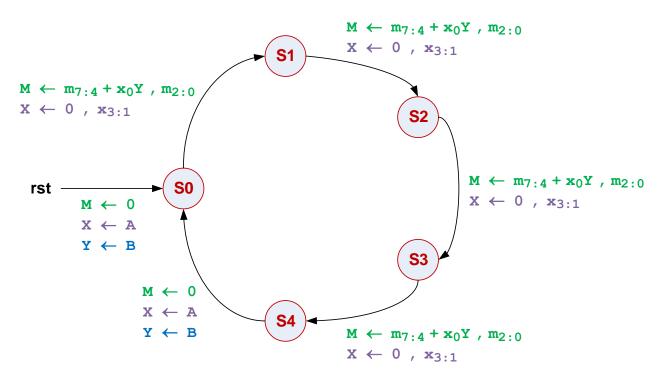
The state machine can be implemented using 3 registers only, where two 4-bit registers, X and Y, are used to store A and B values, and an 8-bit register M is used to store intermediate (iteration) values of multiplication result. Following the final iteration, value inside the M register is equal to $M = A \times B$. This scheme is illustrated as follows:



Let's apply the same numerical example as before to this state machine. Data inside registers will change as follows:



State transition diagram for this state machine will look like:



In the lab:

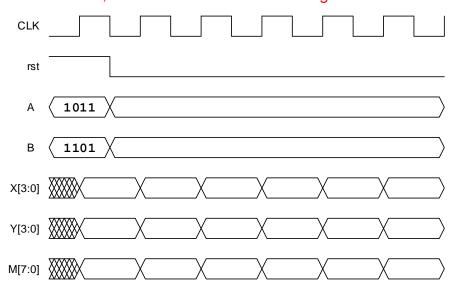
- Connect switch 8 to rst input,
- Connect switches 7 to 4 to A input,
- Connect switches 3 to 0 to B input,
- Connect bits 7 to 4 of M output to 7-segment display 1 (HEX1),
- Connect bits 3 to 0 of M output to 7-segment display 0 (HEX0),
- Connect clock input to push-button key 0 (KEY[0]) as usual,
- You can use the 7-segment decoder module from the previous lab in order to convert 4-bit portions of M to 7-segment display.

You will, as always, implement your circuit via writing Verilog HDL code for it. Your module should be named "lab5" with "rst", "clk", "A" and "B" as inputs, and "SS1" and "SS0" as outputs:

```
// Lab5 module
module lab5 ( rst , clk , A , B , SS1 , SS0 ) ;
...
endmodule
```

As a preliminary for the lab:

1. First, you are going to write the Verilog-HDL code for your module and the testbench to multiply A = 11 and B = 13, simulate it for the waveforms given below.



2. You will **present** your codes (**both** the module and the testbench) and Modelsim waveform outputs (screenshots) to the assistants as your preliminary lab report. Otherwise, you **will not be admitted** to the lab.

You can refer to the "Cyclone V GX Starter Kit User Manual" provided as a supplement, as well as your notes and sample codes on BBlearn.

You will be graded for:

- 1. Preliminary Verilog-HDL code and analysis (simulation results) of the circuit (1 pt.) Remember: Without your preliminary report, you will not be admitted to the lab! You may keep it, use it during the lab and then add it to your lab report. Do not forget to prepare it individually and write your name on it.
- 2. Programming and running your design on the Cyclone V board (1 pt.) and showing it to the assistants, after which you can check out and leave the lab,
- 3. Project report (2 pts.),
 - a. Project reports should be prepared individually.
 - b. Project reports should be turned in on BBLearn by midnight Feb 23rd, 2020. Late submissions will not be accepted.
 - c. You should complete the project report after you demonstrate your solution (above).
 - d. Project reports submitted without a corresponding demonstration grade on record (without proper check-out) will not be accepted.
 - e. Your project report should include the following:
 - Problem Description (0.5 pts.): You should describe the problem in your own words.
 - ii. **Solution Plan (0.5 pts.):** Describe your strategy for finding a solution.
 - iii. **Implementation and Test Plan (1 pt.):** Describe how you implemented the solution and what testing plan you devised. You should include the truth tables for both circuits you obtained developed in lab.