1. Description

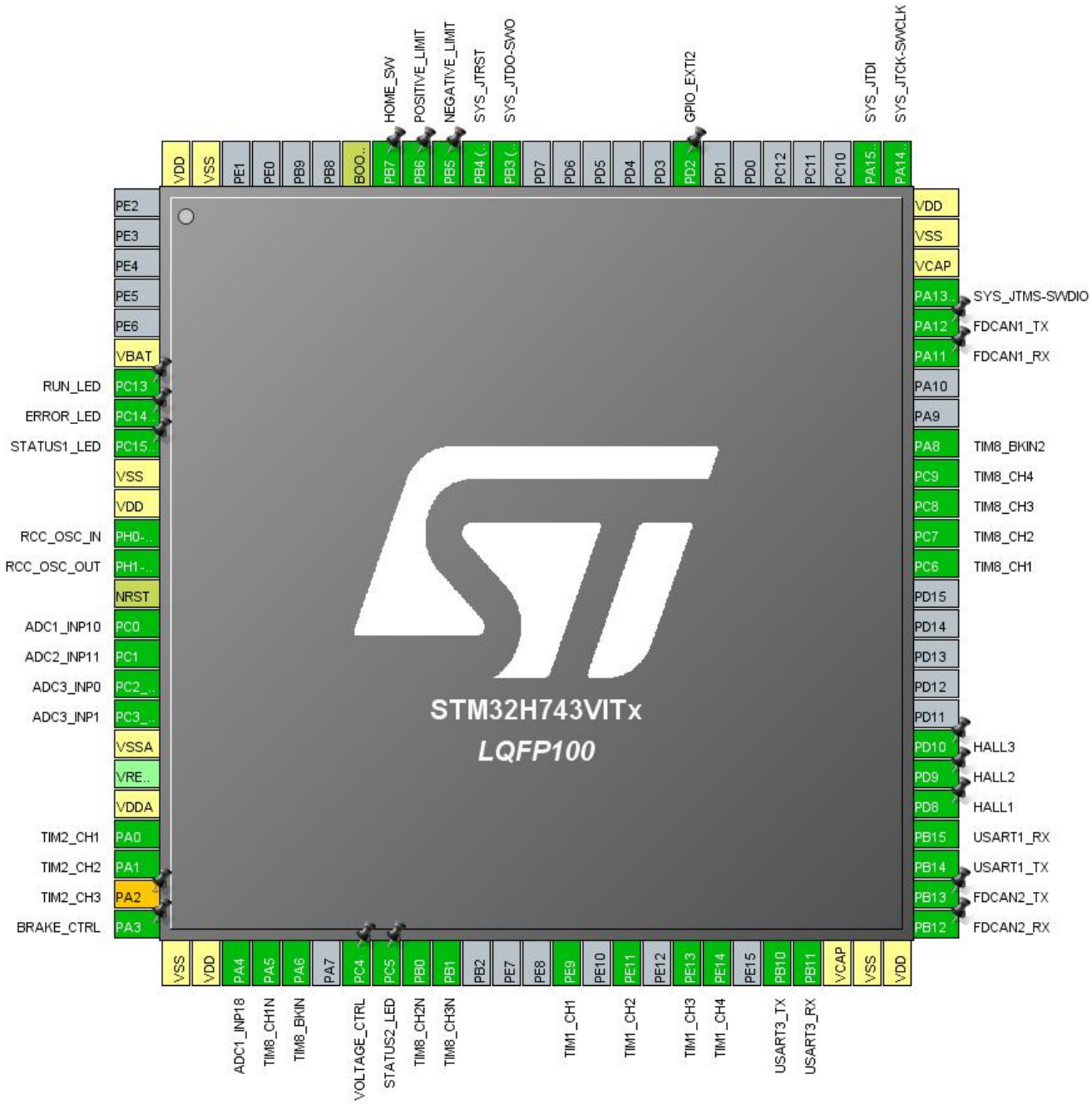
1.1. Project

Project Name	MotorDrv
Board Name	custom
Generated with:	STM32CubeMX 5.0.1
Date	02/12/2019

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743VITx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



3. Pins Configuration

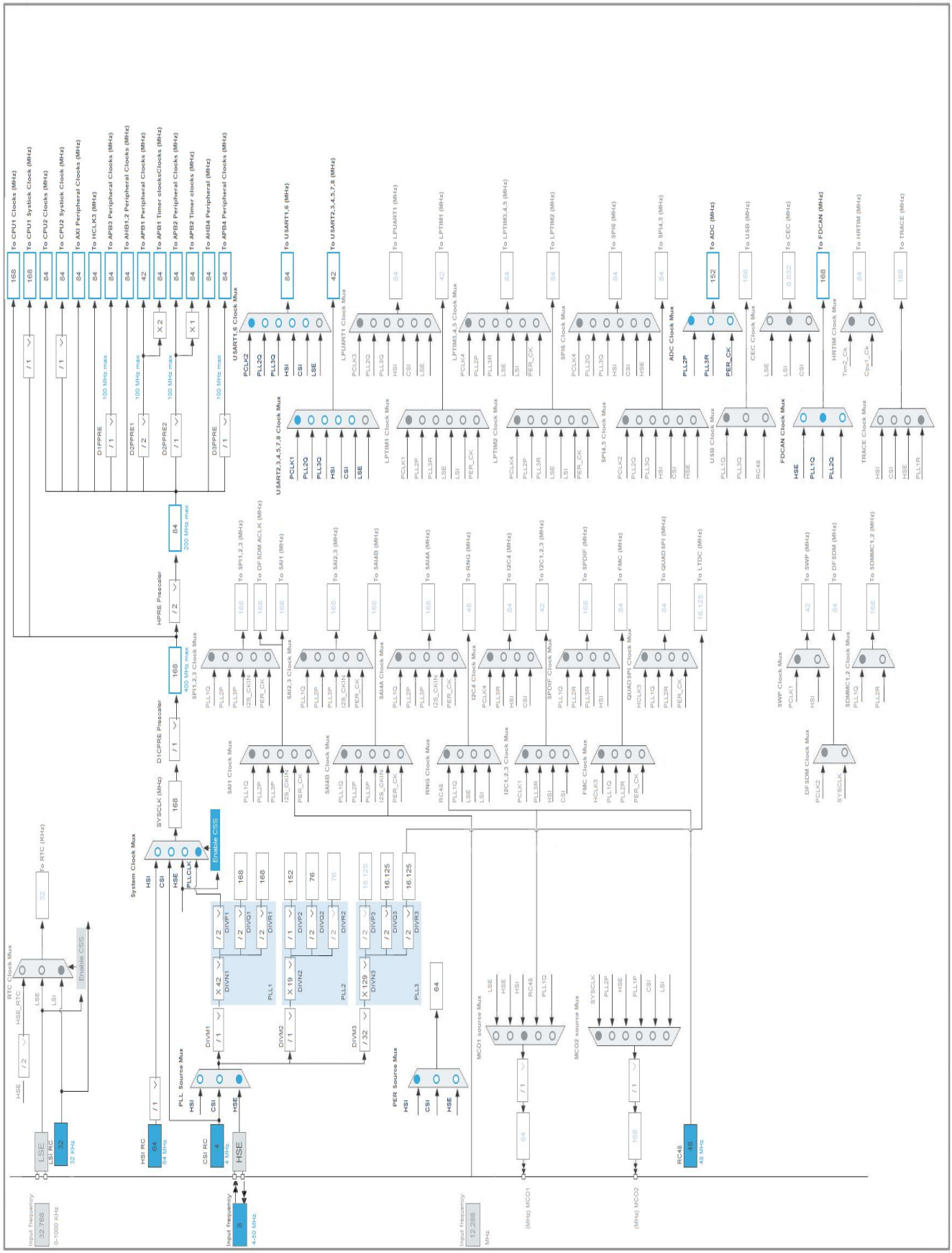
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	RUN_LED
8	PC14-OSC32_IN (OSC32_IN) *	I/O	GPIO_Output	ERROR_LED
9	PC15-OSC32_OUT (OSC32_OUT) *	I/O	GPIO_Output	STATUS1_LED
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC1_INP10	
16	PC1	I/O	ADC2_INP11	
17	PC2_C	I/O	ADC3_INP0	
18	PC3_C	I/O	ADC3_INP1	
19	VSSA	Power		
21	VDDA	Power		
22	PA0	I/O	TIM2_CH1	
23	PA1	I/O	TIM2_CH2	
24	PA2 **	I/O	TIM2_CH3	
25	PA3 *	I/O	GPIO_Output	BRAKE_CTRL
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	ADC1_INP18	
29	PA5	I/O	TIM8_CH1N	
30	PA6	I/O	TIM8_BKIN	
32	PC4 *	I/O	GPIO_Output	VOLTAGE_CTRL
33	PC5 *	I/O	GPIO_Output	STATUS2_LED
34	PB0	I/O	TIM8_CH2N	
35	PB1	I/O	TIM8_CH3N	
39	PE9	I/O	TIM1_CH1	
41	PE11	I/O	TIM1_CH2	
43	PE13	I/O	TIM1_CH3	
44	PE14	I/O	TIM1_CH4	
46	PB10	I/O	USART3_TX	
47	PB11	I/O	USART3_RX	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	FDCAN2_RX	
52	PB13	I/O	FDCAN2_TX	
53	PB14	I/O	USART1_TX	
54	PB15	I/O	USART1_RX	
55	PD8 *	I/O	GPIO_Input	HALL1
56	PD9 *	I/O	GPIO_Input	HALL2
57	PD10 *	I/O	GPIO_Input	HALL3
63	PC6	I/O	TIM8_CH1	
64	PC7	I/O	TIM8_CH2	
65	PC8	I/O	TIM8_CH3	
66	PC9	I/O	TIM8_CH4	
67	PA8	I/O	TIM8_BKIN2	
70	PA11	I/O	FDCAN1_RX	
71	PA12	I/O	FDCAN1_TX	
72	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	
77	PA15 (JTDI)	I/O	SYS_JTDI	
83	PD2	I/O	GPIO_EXTI2	
89	PB3 (JTDO/TRACESWO)	I/O	SYS_JTDO-SWO	
90	PB4 (NJTRST)	I/O	SYS_JTRST	
91	PB5 *	I/O	GPIO_Input	NEGATIVE_LIMIT
92	PB6 *	I/O	GPIO_Input	POSITIVE_LIMIT
93	PB7 *	I/O	GPIO_Input	HOME_SW
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	MotorDrv
Project Folder	D:\project\HEXAR\MotorDrv
Toolchain / IDE	EWARM V8
Firmware Package Name and Version	STM32Cube FW_H7 V1.3.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743VITx
Datasheet	030538_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. ADC1

IN10: IN10 Single-ended

IN18: Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 4 ***
Resolution	**ADC 12-bit resolution ***
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data preserved
Boost Mode	Disabled
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	**2 ***
External Trigger Conversion Source	**Timer 8 Trigger Out event ***
External Trigger Conversion Edge	**Trigger detection on the falling edge ***
Rank	1
Channel	Channel 10
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 18 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

mode: IN11

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 4 ***
Resolution	**ADC 12-bit resolution ***
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data preserved
Boost Mode	Disabled
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 8 Trigger Out event ***
External Trigger Conversion Edge	**Trigger detection on the falling edge ***
Rank	1
Channel	Channel 11
Sampling Time	**32.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. ADC3

mode: IN0

IN1: IN1 Single-ended

mode: Temperature Sensor Channel

7.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 4 ***
Resolution	**ADC 12-bit resolution ***
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data preserved
Boost Mode	Disabled
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	**3 ***
External Trigger Conversion Source	**Timer 8 Trigger Out event ***
External Trigger Conversion Edge	**Trigger detection on the falling edge ***
Rank	1
Channel	Channel 0
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**3 ***

Channel	**Channel Temperature Sensor ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.4. FDCAN1

Mode: Classic

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Tx Delay Compensation	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	1
Nominal Sync Jump Width	1
Nominal Time Seg1	2
Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Message Ram Offset	0
Std Filters Nbr	0
Ext Filters Nbr	0
Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	8 bytes data field
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	8 bytes data field
Rx Buffers Nbr	0

Rx Buffer Size	8 bytes data field
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	8 bytes data field

msgRam:

Standard Filter Sa	0
Extended Filter Sa	0
Rx Fifo0 Sa	0
Rx Fifo1 Sa	0
Rx Buffer Sa	0
Tx Event Fifosa	0
Tx Buffer Sa	0
Tx Fifoqsa	0
Tt Memory Sa	0
End Address	0

Error_Code:

Error Code	0

7.5. FDCAN2

Mode: FD

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	FD mode without BitRate Switshing
Mode	Normal mode
Auto Retransmission	Disable
Tx Delay Compensation	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	1
Nominal Sync Jump Width	1
Nominal Time Seg1	2
Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Message Ram Offset	0

Std Filters Nbr	0
Ext Filters Nbr	0
Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	8 bytes data field
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	8 bytes data field
Rx Buffers Nbr	0
Rx Buffer Size	8 bytes data field
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	8 bytes data field

msgRam:

Standard Filter Sa	0
Extended Filter Sa	0
Rx Fifo0 Sa	0
Rx Fifo1 Sa	0
Rx Buffer Sa	0
Tx Event Fifosa	0
Tx Buffer Sa	0
Tx Fifoqsa	0
Tt Memory Sa	0
End Address	0

Error_Code:

Error Code	0

7.6. IWDG1

mode: Activated

7.6.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	4
IWDG window value	4095
IWDG down-counter reload value	4095

7.7. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.7.1. Parameter Settings:

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	16

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	1 WS (2 CPU cycle)

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 3

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	MEDIUM VCO range
PLL Fractional Part	0
PLL2 Fractional Part	0

7.8. SYS

Debug: JTAG (5 pins)

Timebase Source: SysTick

7.9. TIM1

Channel4: Input Capture direct mode

Combined Channels: XOR ON / Hall Sensor Mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection TRGO	Output Compare (OC2REF)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Hall Sensor:

Prescaler Division Ratio	No division
Polarity	Rising Edge
Input Filter	0
Commutation Delay	0

7.10. TIM2

Combined Channels: Encoder Mode

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**4294967295 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.11. TIM8

Clock Source : Internal Clock

Channel1: PWM Generation CH1 CH1N

Channel2: PWM Generation CH2 CH2N

Channel3: PWM Generation CH3 CH3N

Channel4: Output Compare CH4

Activate-Break-Input: Activate Break Input

Activate-Break-Input-2: Activate Break Input 2

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	**Center Aligned mode1 ***
Counter Period (AutoReload Register - 16 bits value)	**4200 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Output Compare (OC4REF) ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Enable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Enable
Digital Input Polarity	Polarity High
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Enable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Enable

Digital Input Polarity	Polarity High
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Enable
Off State Selection for Idle Mode (OSSI)	Enable
Lock Configuration	Off
Dead Time	**84 ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1 and 1N:

Mode	**PWM mode 2 ***
Pulse (16 bits value)	**4200 ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	**PWM mode 2 ***
Pulse (16 bits value)	**4200 ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 3 and 3N:

Mode	**PWM mode 2 ***
Pulse (16 bits value)	**4200 ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 4:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High

CH Idle State	Reset

7.12. USART1

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.13. USART3

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None

Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_INP10	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_INP18	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC1	ADC2_INP11	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PC2_C	ADC3_INP0	Analog mode	No pull-up and no pull-down	n/a	
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	
FDCAN1	PA11	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FDCAN2	PB12	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA15 (JTDI)	SYS_JTDI	n/a	n/a	n/a	
	PB3 (JTDO/TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	
	PB4 (NJTRST)	SYS_JTRST	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PA5	TIM8_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	TIM8_BKIN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	TIM8_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	TIM8_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA8	TIM8_BKIN2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB14	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PA2	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RUN_LED
	PC14-OSC32_IN (OSC32_IN)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ERROR_LED
	PC15-OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STATUS1_LED
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BRAKE_CTRL
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VOLTAGE_CTRL
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STATUS2_LED
	PD8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	HALL1
	PD9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	HALL2
	PD10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	HALL3
	PD2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NEGATIVE_LIMIT
	PB6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	POSITIVE_LIMIT
	PB7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	HOME_SW

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line2 interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
FDCAN1 interrupt 0	unused		
FDCAN2 interrupt 0	unused		
FDCAN1 interrupt 1	unused		
FDCAN2 interrupt 1	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
USART1 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
FDCAN calibration unit interrupt	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		
ADC3 global interrupt	unused		

*** User modified value**

9. Software Pack Report