1 Introduction

This Artefact Description-Actefact Evaluation Appendix form is related to the paper "Introducing multi-level parallelism, at coarse, fine and instruction level to enhance the performance of iterative solvers for large sparse linear systems on Multi and Many core architecture" submmited to the SC20 HiPar20 workshop.

2 AD-AE Appendix Form

2.1 Summary of experiments

In the paper 1, some experiments have been realized to illustrate and validate the proposed approach to handle multi-level parallelism. The experiments consist in benchmarking iterative linear solvers with various preconditioners on linear systems extracted either from simple Laplacian problems either from the simulation of the realistic reservoir study model SPE10.

The experiments have been run on a single node linux machine with a Knights Landing processor which handles 32 bi-cores processors and on a multi-node Linux cluster of 240 dual-socket Nodes with Intel Skylake G-6140 processors at 2.3 GHz.

2.2 Software Arctifact Availability

The approach presented in 1 has been implemented in the *HTSSolver 2.0* library which depends on following opensource libraries :

- The *Eigen 3.2* library `http://eigen.tuxfamily.org/index.php?title=Main_Page`;
- The *SuperLU 5.2.1* library `https://portal.nersc.gov/project/sparse/superlu/`;
- The *Trilinos 12.18* library `https://trilinos.github.io/`;
- The *SpectraLib 0.8.0* library `https://spectralib.org/`;

All libraries have been compiled for the KNL processor with the Intel 2017 compiler with GCC 5.4 compatibility, for the SkyLake processor with the GCC 7.3 compiler, activating AVX512 vector instructions for the two architectures.

2.3 Hardware Arctifact Availability

The experiments have been run on two standard linux machines:

- The first machine is a single node machine with a Knights Landing processor which handles 32 bi-cores processors, 16GB of MCDRAM high bandwidth memory and 64GB of DRAM standard memory. The KNL processor cores topology was configured with the Quadrant mode. The MCDRAM memory was configured as a cache for DRAM.

- The second machine is a multi-node Linux cluster of 240 dual-socket Nodes with Intel Skylake G-6140 processors at 2.3 GHz.(18 cores per socket), connected with an Infiniband FDR (2 links 56Gb/s per node).

2.4 Data Arctifact Availability

The linear systems used for the experiments were extracted either from simple Laplacian problems on a unit square discretized with grids of size $N_x \times N_x$ leading to systems of size $N_{rows} = N_x * N_x$, or from the simulation of the well known realistic reservoir study case SPE10 leading to systems of size $N_{rows} = 10^6$ or $N_{rows} = 8 * 10^6$ for the version using a 8 times refined 8 times.

The data related to the extracted linear systems, and the tools to import these data or to generate Laplacian problems are available in the GitHub Project HiPar20Arctefact at : `https://github.com/jgratien/HiPar20Arctefact.git`

2.5 Proprietary Arctifact

The approach presented in 1 is implemented in the *HTSSolver 2.0* and the *HARTS* libraries. These libraries are available in the projects :

- HARTS project : `https://gitlab.ifpen.fr/R1140/harts.git`
- HTSSolver project : `https://gitlab.ifpen.fr/R1140/hartssolver.git`

Righ now, these projects are still proprietary and are not freely available.

2.6 List of URLs andor DOIs where actifacts are available

- HiPar20Arctefact : `https://github.com/jgratien/HiPar20Arctefact.git`
- SPE10, 10th SPE Comparative Solution project : `https://www.spe.org/web/csp/datasets/set02.htm`

2.7 Do you wish your paper to be considered for Cluster Competition Reproduccibility Challenge in SC2020

No