OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

# MSM5260

## 80-DOT COMMON/SEGMENT DRIVER

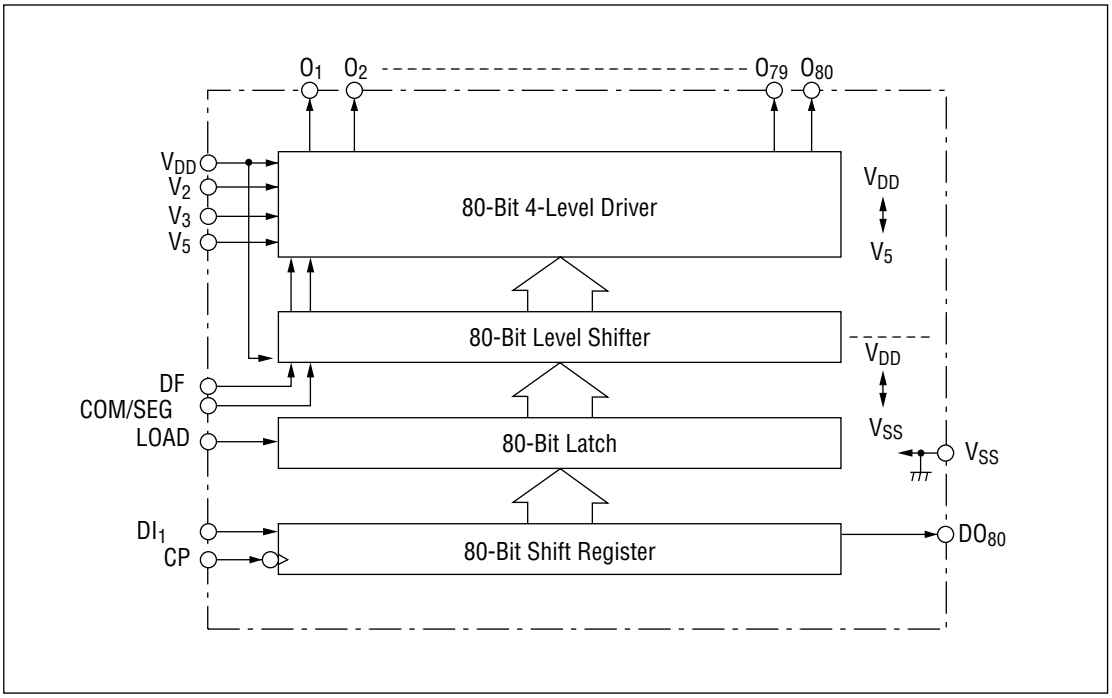
## GENERAL DESCRIPTION

The MSM5260 is a dot matrix common/segment LCD driver LSI which is fabricated using low power CMOS metal gate technology. This LSI consists of 80-bit shift register, 80-bit latch, 80-bit level shifter and 80-bit 4-level driver.
It converts display data, which is serially received from an LCD controller LSI, to parallel data, and outputs LCD driving waveform to LCD.
This LSI can drive a variety of LCD panels since the bias voltage can be optionally supplied from an external source.

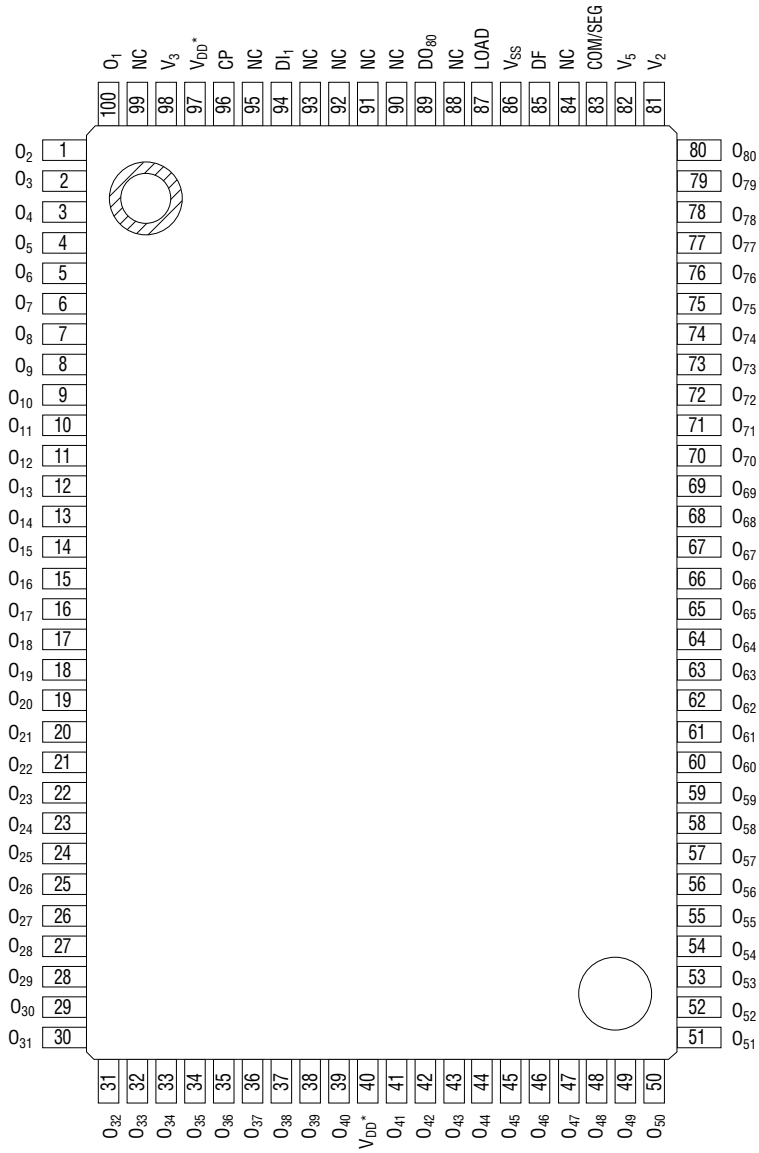
## FEATURES

- Supply voltage : 4.5 to 5.5V
- LCD driving voltage : 8 to 18V
- Applicable LCD duty : static and 1/32 to 1/64
- Bias voltage can be supplied externally
- Can be used either as common or segment driver
- Interface with MSM6255 LCD controller LSI
- Package options :
  100-pin plastic QFP (QFP100-P-1420-0.65-K) (Product name : MSM5260GS-K)
  100-pin plastic QFP (QFP100-P-1420-0.65-L) (Product name : MSM5260GS-L)
  100-pin plastic QFP (QFP100-P-1420-0.65-BK) (Product name : MSM5260GS-BK)

## BLOCK DIAGRAM



## PIN CONFIGURATION (TOP VIEW)

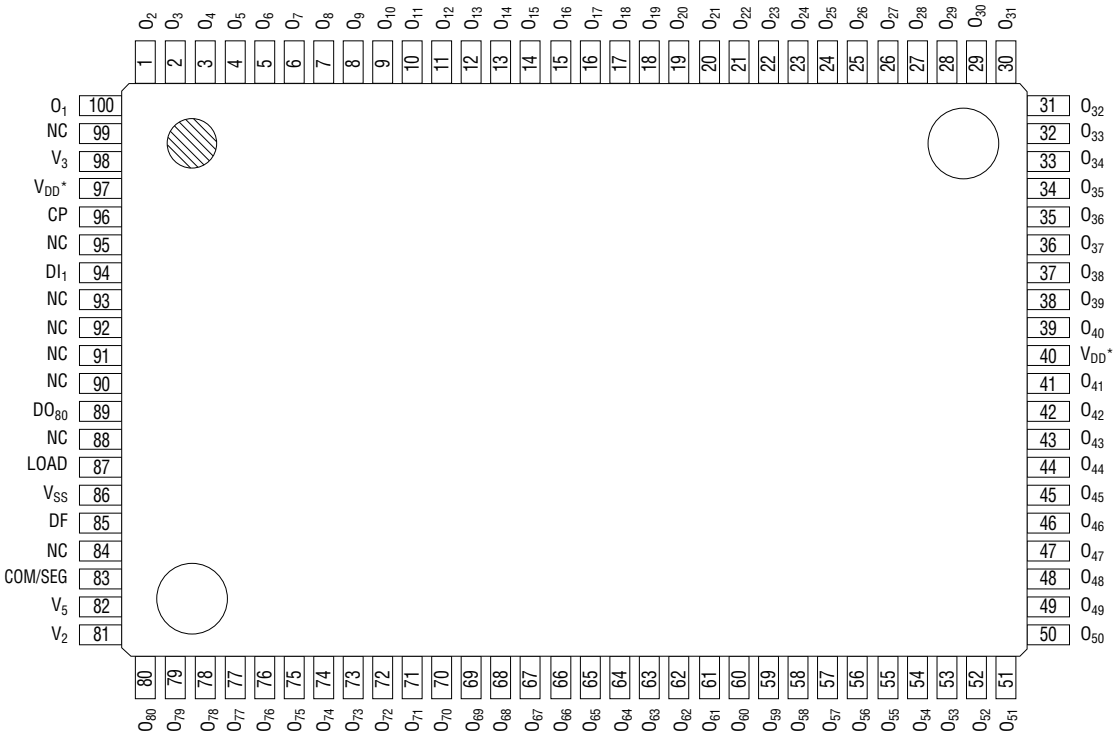



NC : No connection

**100-Pin Plastic QFP (Type K)**

*$V_{DD}$ must be supplied to both pin 40 and pin 97.

## PIN CONFIGURATION




NC : No connection

**100-Pin Plastic QFP (Type L)**

*$V_{DD}$ must be supplied to both pin 40 and pin 97.

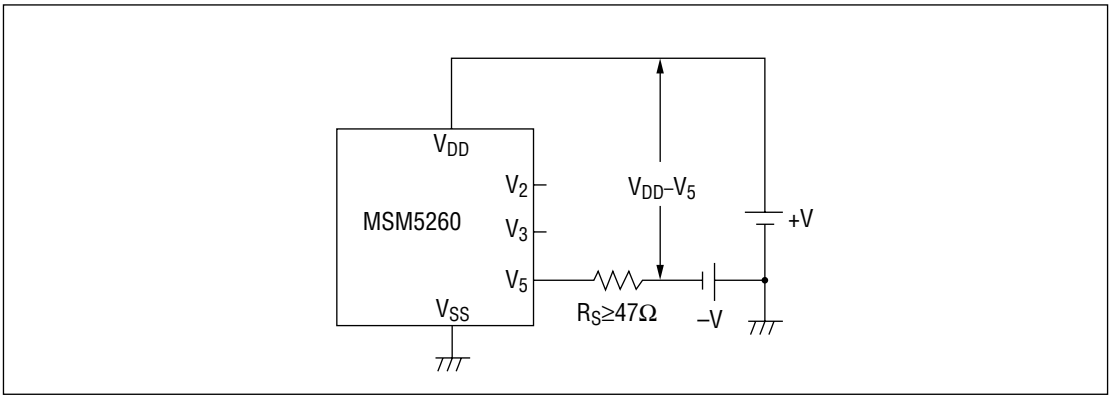
Note: This figure shows the configuration viewed from the reverse side of the package. Pay attention to the difference in pin arrangement.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply Voltage (1) | $V_{DD}$ | $T_a$ = 25°C | –0.3 to +6.0 | V |
| Supply Voltage (2) | $V_{LCD}$ | $T_a$ = 25°C, $V_{DD} - V_5$ *1 | 0 to 18 | V |
| | | $T_a$ = 25°C, $V_{DD} - V_5$ *1*2 | 0 to 20 | V |
| Input Voltage | $V_I$ | $T_a$ = 25°C | –0.3 to $V_{DD}$ +0.3 | V |
| Storage Temperature | $T_{STG}$ | — | –55 to +150 | °C |

*1 $V_{DD} > V_2 > V_3 > V_5$

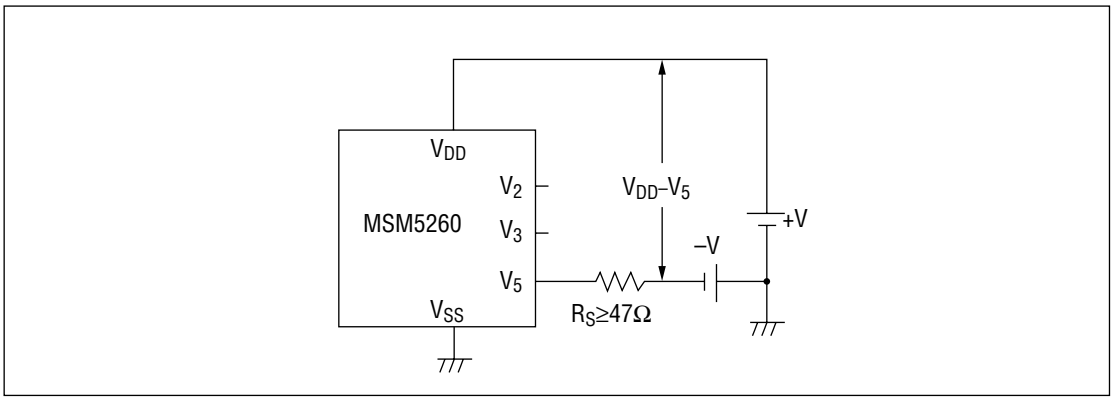
*2 When a series resistance of more than 47Ω is connected as shown below:



## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Supply Voltage (1) | $V_{DD}$ | — | 4.5 to 5.5 | V |
| Supply Voltage (2) | $V_{LCD}$ | $V_{DD} - V_5$ *1 | 8 to 16 | V |
| | | $V_{DD} - V_5$ *1*2 | 8 to 18 | V |
| Operating Temperature | $T_{op}$ | — | –20 to +85 | °C |

*1 $V_{DD} > V_2 > V_3 > V_5$
*2 When a series resistance of more than 47Ω is connected as shown below:




## ELECTRICAL CHARACTERISTICS

### DC Characteristics

($V_{DD}$ = 5V ± 10%, Ta = –20 to +85°C)

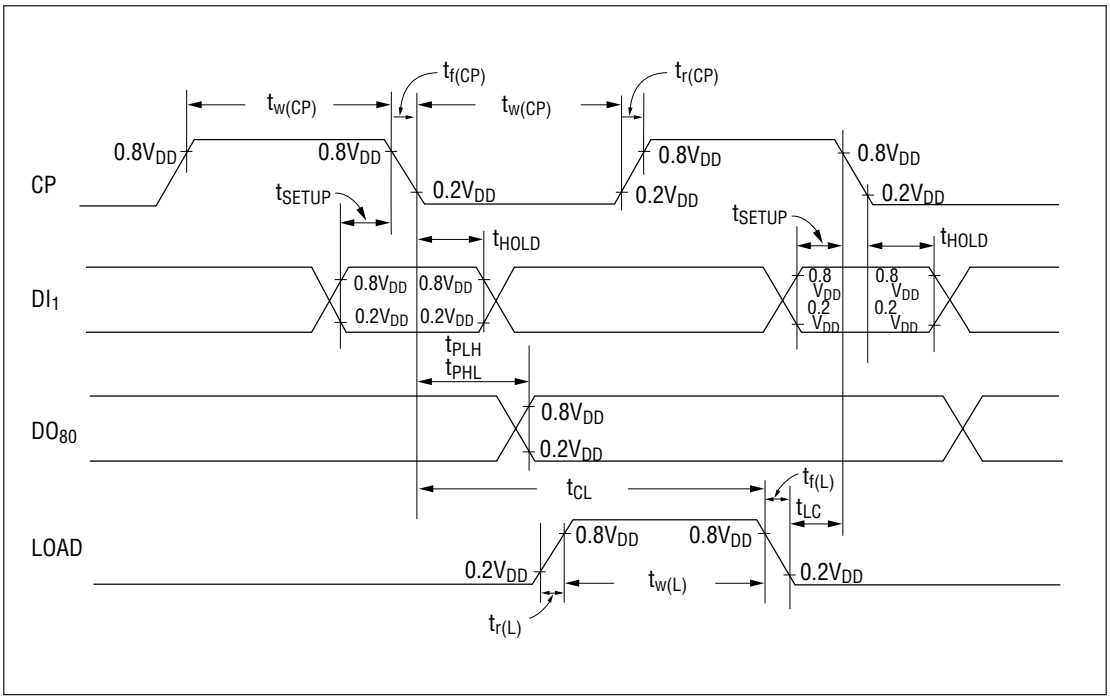
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| "H" Input Voltage | $V_{IH}$ *1 | | 0.8$V_{DD}$ | — | $V_{DD}$ | V |
| "L" Input Voltage | $V_{IL}$ *1 | | $V_{SS}$ | — | 0.2$V_{DD}$ | V |
| "H" Input Current | $I_{IH}$ *1 | $V_{IH} = V_{DD}$ | — | — | 1 | µA |
| "L" Input Current | $I_{IL}$ *1 | $V_{IL}$ = 0V | — | — | –1 | µA |
| "H" Output Voltage | $V_{OH}$ *2 | $I_O$ = –0.4mA | $V_{DD}$ – 0.4 | — | — | V |
| "L" Output Voltage | $V_{OL}$ *2 | $I_O$ = 0.4mA | — | — | 0.4 | V |
| ON Resistance | $R_{ON}$ *4 | $V_{DD}–V_5$ = 10V<br>$\lvert V_N–V_O \rvert$ = 0.25V *3 | — | 1 | 2 | kΩ |
| Supply Current | $I_{DD}$ | CP = DC<br>$V_{DD}–V_5$ = 18V, no load | — | — | 100 | µA |

*1 Applied to LOAD, CP, $DI_1$, DF and COM/SEG
*2 Applied to $DO_{80}$
*3 $V_N = V_{DD}$ to $V_5$, $V_2 = 8/9\ (V_{DD} – V_5)$, $V_3 = 1/9\ (V_{DD} – V_5)$
*4 Applied to $O_1$ to $O_{80}$

## Switching Characteristics

($V_{DD}$ = 5V ± 10%, Ta = –20 to +85°C, $C_L$ = 15pF)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| "H","L" Propagation Delay Time | $t_{pLH}$ $t_{pHL}$ | — | — | — | 250 | ns |
| Clock Frequency | $f_{CP}$ | Duty = 50% | — | — | 3.3 | MHz |
| Clock Pulse Width | $t_{W(CP)}$ | — | 125 | — | — | ns |
| LOAD Pulse Width | $t_{W(L)}$ | — | 125 | — | — | ns |
| Data Setup Time DI→CP | $t_{SETUP}$ | — | 50 | — | — | ns |
| CP→LOAD Time | $t_{CL}$ | — | 250 | — | — | ns |
| LOAD→CP Time | $t_{LC}$ | — | 0 | — | — | ns |
| Data Hold Time DI→CP | $t_{HOLD}$ | — | 50 | — | — | ns |
| CP Rise/Fall Time | $t_{r(CP)}$ $t_{f(CP)}$ | — | — | — | 50 | ns |
| LOAD Rise/Fall Time | $t_{r(L)}$ $t_{f(L)}$ | — | — | — | 1 | µs |



## FUNCTIONAL DESCRIPTION

### Pin Functional Description

- **$DI_1$**
  The data input pin for the 80-bit shift register (between 1st to 80th bit). The display data is clocked in to this pin. (Positive logic)

- **CP**
  Clock pulse input pin for 80-bit shift register. The data is shifted to the 80-bit shift register at the falling edge of the clock pulse. A data setup time ($t_{SETUP}$) and a data hold time ($t_{HOLD}$) are required between a $DI_1$ signal and a clock pulse.
  Clock pulse rise time ($t_r$) and clock pulse fall time ($t_f$) should be a maximum of 50ns respectively.

- **$DO_{80}$**
  The 80th bit output from the 80-bit shift register.
  The data which is input from $DI_1$ is clocked out with the delay in the number of the bits of the shift register.
  When extending the number of characters, this pin is used to connect to the next MSM5260 in cascade.

- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at "H" level, the shift register contents are transferred to the 80-bit 4-level driver through the 80-bit level shifter.
  When LOAD pin is set at "L" level, the last display output data ($O_1$ to $O_{80}$), which was transferred when LOAD pin was at "H" level, is held.

- **DF**
  Synchronous signal input pin for alternate signal for LCD driving.

- **COM/SEG**
  Selection signal input pin. MSM5260 is used either as common driver or segment driver according to input signal level at COM/SEG pin.
  When this pin is set when at "H" level, MSM5260 is used as a common driver, while it is used as a segment driver when at "L" level.
  The display driving data $O_1$ to $O_{80}$ are determined according to the combination of latched data and DF signal, as shown in Table 1 below.

**Table 1**

| COM/SEG | Latched data level | DF | Driver data output level ($O_1$ - $O_{80}$) | Remarks |
|---|---|---|---|---|
| H | High (Select) | H | $V_{DD}$ | Common driver |
| | | L | $V_5$ | |
| | Low (Non-select) | H | $V_3$ | |
| | | L | $V_2$ | |
| L | High (Select) | H | $V_5$ | Segment driver |
| | | L | $V_{DD}$ | |
| | Low (Non-select) | H | $V_3$ | |
| | | L | $V_2$ | |

When MSM5260 is used as a common driver, both LOAD pin and COM/SEG pin are to be connected to $V_{DD}$. In this case, a bias voltage of common side's non-select level is to be supplied to $V_2$ and $V_3$ pins.

- **$V_{DD}$, $V_{SS}$**
  Supply voltage pins. $V_{DD}$ should be 4.5 to 5.5V.
  $V_{SS}$ is a ground pin ($V_{SS}$ = 0V)

- **$V_2$, $V_3$, $V_5$**
  Bias supply voltage pins to drive the LCD. Use an external bias voltage supply for driving the LCD.

- **$O_1$ to $O_{80}$**
  Display data output pins which correspond to each bit of the 80-bit latch.
  One of $V_{DD}$, $V_2$, $V_3$ and $V_5$ is selected as a display driving voltage source according to the combination of latched data level and DF signal.

## NOTES ON USE

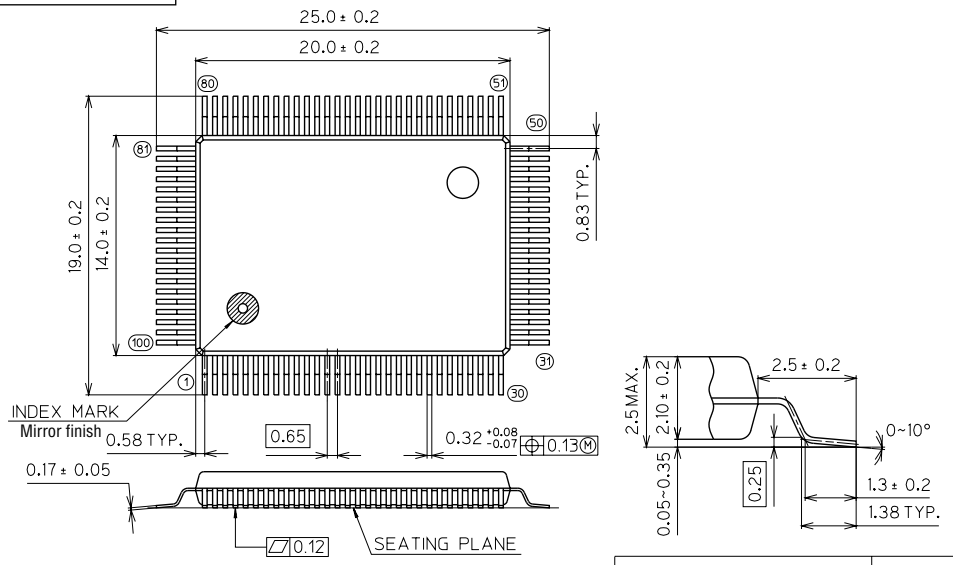
Note the following when turning power on and off :
The LCD drivers of this IC requiers a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC. Be sure to carry out the following power-on and power-off sequences :

When turning power on :
First $V_{DD}$ ON, next $V_5$, $V_3$, $V_2$ ON. Or both ON at the same time.
When turning power off :
First $V_5$, $V_3$, $V_2$ OFF, next $V_{DD}$ OFF. Or both OFF at the same time.

## PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-K



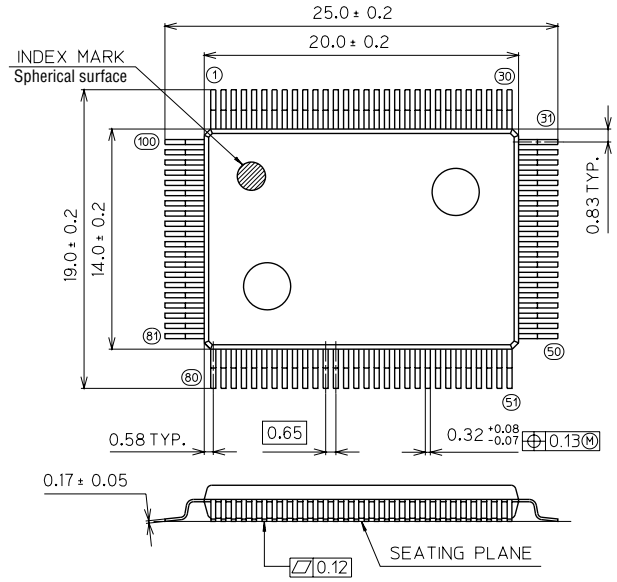

| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 1.29 TYP. |

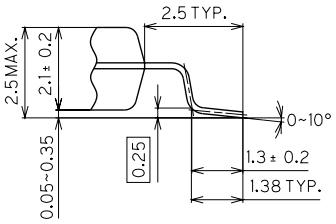
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP100-P-1420-0.65-L




| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 1.29 TYP. |

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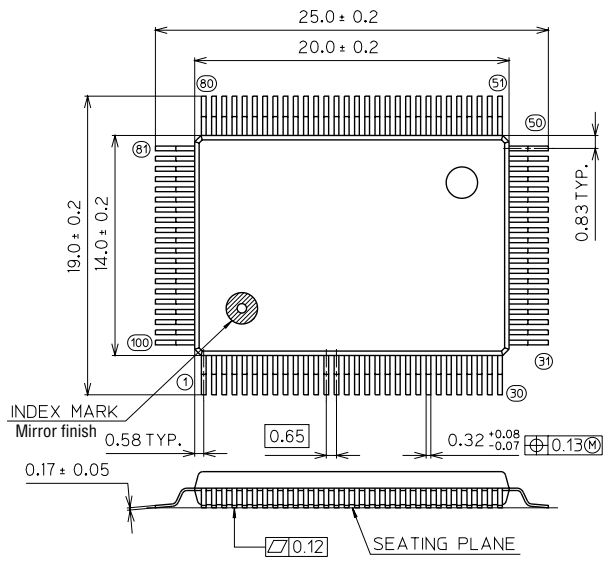
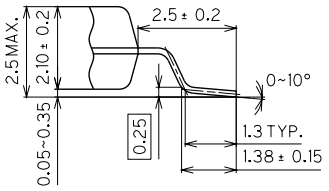
(Unit : mm)

QFP100-P-1420-0.65-BK




| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 1.29 TYP. |

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