

## 1. Description

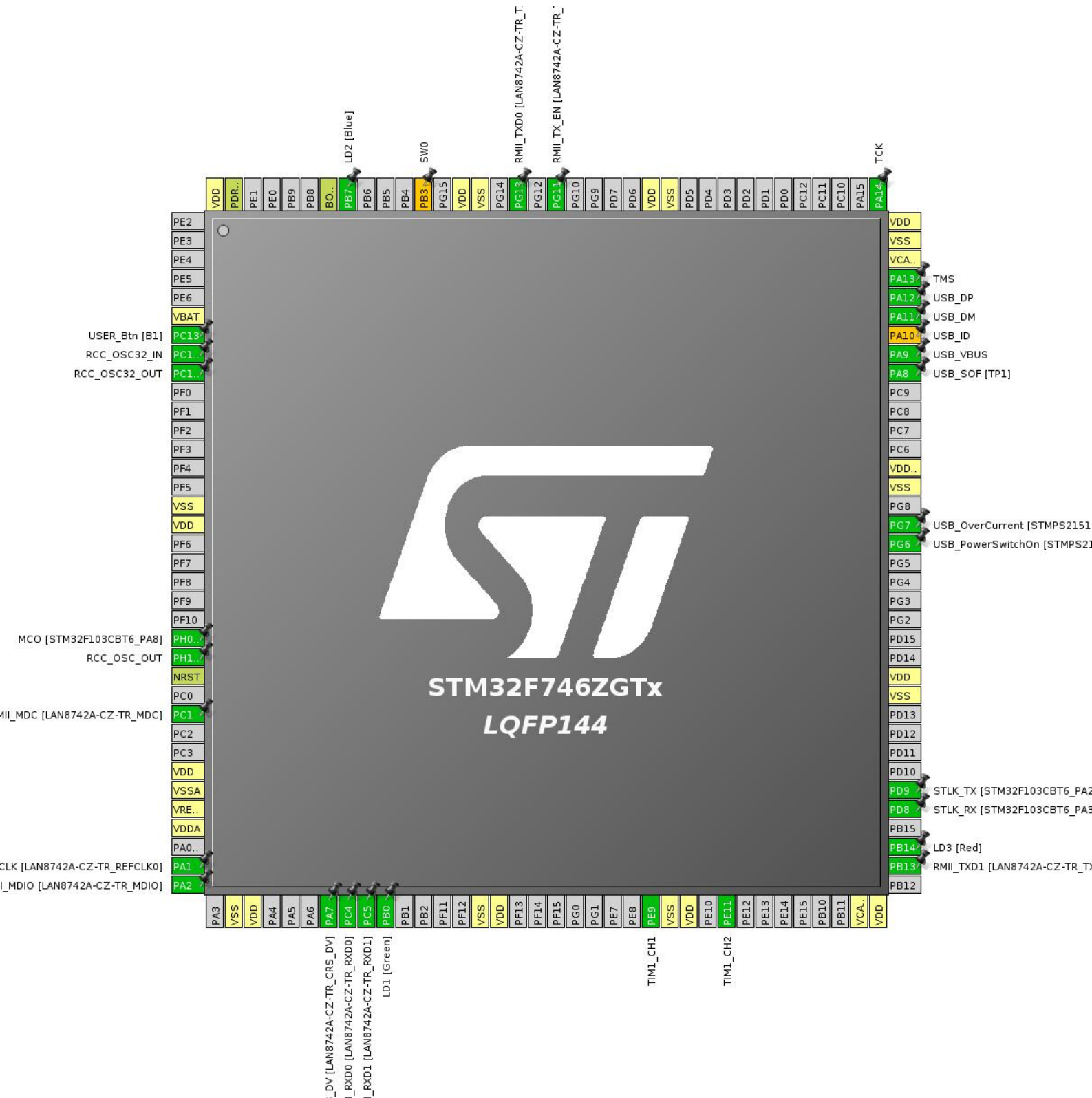
### 1.1. Project

Project Name	test_freeRtOs
Board Name	NUCLEO-F746ZG
Generated with:	STM32CubeMX 4.25.1
Date	05/14/2018

### 1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746ZGTx
MCU Package	LQFP144
MCU Pin number	144

## 2. Pinout Configuration



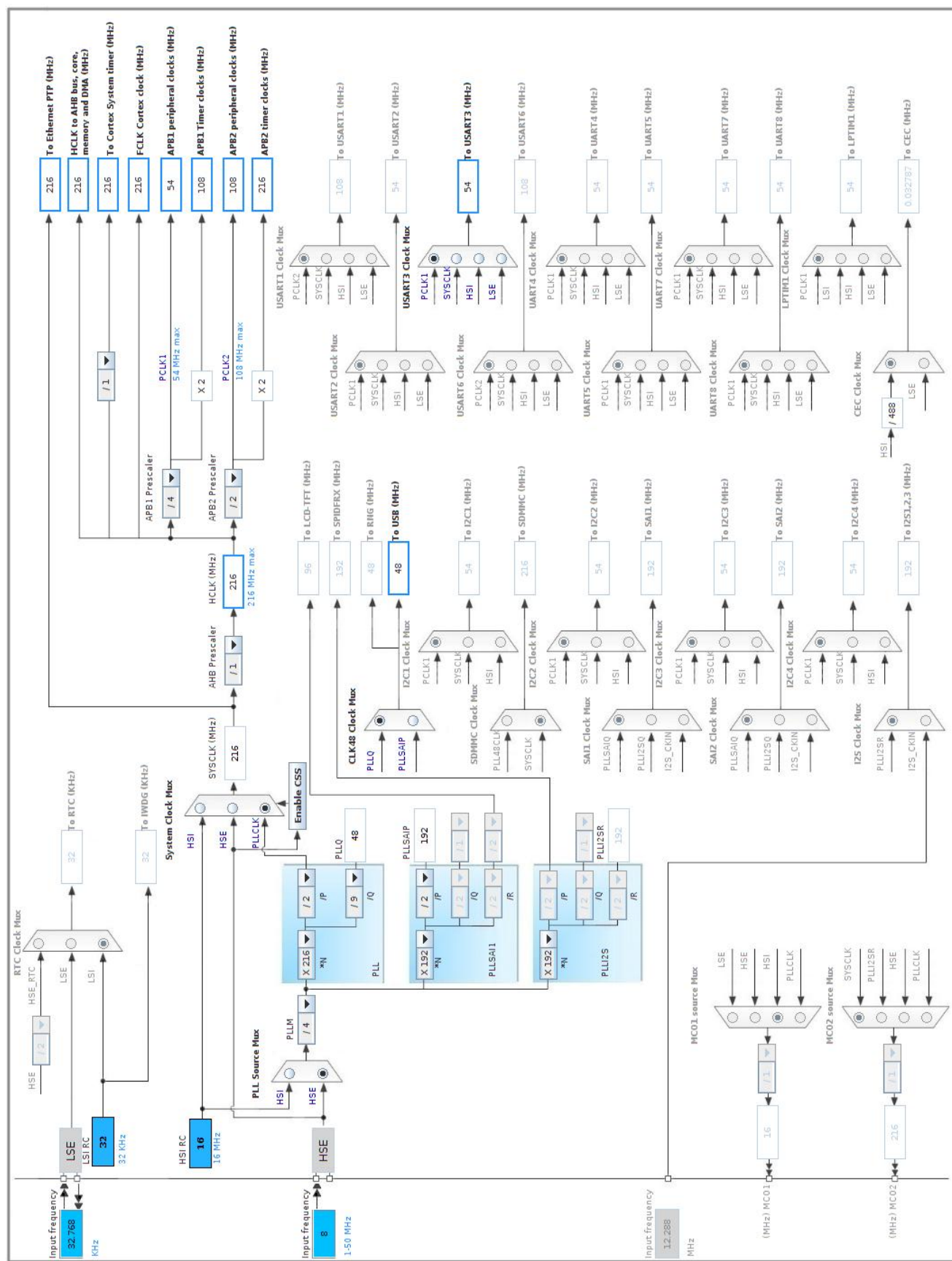
### 3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ- TR_MDC]
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ- TR_REFCLK0]
36	PA2	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ- TR_MDIO]
38	VSS	Power		
39	VDD	Power		
43	PA7	I/O	ETH_CRS_DV	RMII_CRS_DV [LAN8742A- CZ-TR_CRS_DV]
44	PC4	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ- TR_RXD0]
45	PC5	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ- TR_RXD1]
46	PB0 *	I/O	GPIO_Output	LD1 [Green]
51	VSS	Power		
52	VDD	Power		
60	PE9	I/O	TIM1_CH1	
61	VSS	Power		
62	VDD	Power		
64	PE11	I/O	TIM1_CH2	
71	VCAP_1	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ- TR_TXD1]
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
83	VSS	Power		
84	VDD	Power		
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7 *	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
94	VSS	Power		
95	VDDUSB	Power		
100	PA8	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 **	I/O	USB_OTG_FS_ID	USB_ID
103	PA11	I/O	USB_OTG_FS_DM	USB_DM
104	PA12	I/O	USB_OTG_FS_DP	USB_DP
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
120	VSS	Power		
121	VDD	Power		
126	PG11	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A- CZ-TR_TXEN]
128	PG13	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ- TR_TXD0]
130	VSS	Power		
131	VDD	Power		
133	PB3 **	I/O	SYS_JTDO-SWO	SW0
137	PB7 *	I/O	GPIO_Output	LD2 [Blue]
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

- \* The pin is affected with an I/O function
- \*\* The pin is affected with a peripheral function but no peripheral mode is activated

#### 4. Clock Tree Configuration



## 5. IPs and Middleware Configuration

### 5.1. ETH

**Mode: RMII**

#### 5.1.1. Parameter Settings:

##### Advanced : Ethernet Media Configuration:

Auto Negotiation Enabled

##### General : Ethernet Configuration:

Ethernet MAC Address 00:80:E1:00:00:00

PHY Address 0 \*

##### Ethernet Basic Configuration:

Rx Mode Interrupt Mode

TX IP Header Checksum Computation By hardware

#### 5.1.2. Advanced Parameters:

##### External PHY Configuration:

PHY LAN8742A\_PHY\_ADDRESS

PHY Address Value 0

PHY Reset delay these values are based on a 1 ms SysTick interrupt 0x000000FF \*

PHY Configuration delay 0x00000FFF \*

PHY Read TimeOut 0x0000FFFF \*

PHY Write TimeOut 0x0000FFFF \*

##### Common : External PHY Configuration:

Transceiver Basic Control Register 0x00 \*

Transceiver Basic Status Register 0x01 \*

PHY Reset 0x8000 \*

Select loop-back mode 0x4000 \*

Set the full-duplex mode at 100 Mb/s 0x2100 \*

Set the half-duplex mode at 100 Mb/s 0x2000 \*

Set the full-duplex mode at 10 Mb/s 0x0100 \*

Set the half-duplex mode at 10 Mb/s 0x0000 \*

Enable auto-negotiation function 0x1000 \*

Restart auto-negotiation function	0x0200 *
Select the power down mode	0x0800 *
Isolate PHY from MII	0x0400 *
Auto-Negotiation process completed	0x0020 *
Valid link established	0x0004 *
Jabber condition detected	0x0002 *

#### Extended : External PHY Configuration:

PHY special control/status register Offset	0x10 *
PHY Speed mask	0x0002 *
PHY Duplex mask	0x0004 *
PHY Interrupt Source Flag register Offset	0x000B *
PHY Link down interrupt	0x000B *

## 5.2. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

### 5.2.1. Parameter Settings:

#### System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

#### RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

#### Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

## 5.3. SYS

Debug: Serial Wire

Timebase Source: TIM11



## 5.4. TIM1

### Combined Channels: Encoder Mode

#### 5.4.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

##### Encoder:

Encoder Mode	Encoder Mode T11
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\_\_\_\_ Parameters for Channel 1 \_\_\_\_

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

\_\_\_\_ Parameters for Channel 2 \_\_\_\_

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

## 5.5. USART3

### Mode: Asynchronous

#### 5.5.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)

Parity	None
Stop Bits	1
<b>Advanced Parameters:</b>	
Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
<b>Advanced Features:</b>	
Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 5.6. USB\_OTG\_FS

**Mode: Device\_Only**

**mode: Activate\_VBUS**

**mode: Activate\_SOF**

### 5.6.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Enabled

## 5.7. FREERTOS

**mode: Enabled**

### 5.7.1. Config parameters:

**Versions:**

FreeRTOS version 9.0.0  
CMSIS-RTOS version 1.02

**Kernel settings:**

USE\_PREEMPTION Enabled  
CPU\_CLOCK\_HZ SystemCoreClock  
TICK\_RATE\_HZ 1000  
MAX\_PRIORITIES 7  
MINIMAL\_STACK\_SIZE 128  
MAX\_TASK\_NAME\_LEN 16  
USE\_16\_BIT\_TICKS Disabled  
IDLE\_SHOULD\_YIELD Enabled  
USE\_MUTEXES Enabled  
USE\_RECURSIVE\_MUTEXES Disabled  
USE\_COUNTING\_SEMAPHORES Disabled  
QUEUE\_REGISTRY\_SIZE 8  
USE\_APPLICATION\_TASK\_TAG Disabled  
ENABLE\_BACKWARD\_COMPATIBILITY Enabled  
USE\_PORT\_OPTIMISED\_TASK\_SELECTION Enabled  
USE\_TICKLESS\_IDLE Disabled  
USE\_TASK\_NOTIFICATIONS Enabled

**Memory management settings:**

Memory Allocation Dynamic  
TOTAL\_HEAP\_SIZE 15360  
Memory Management scheme heap\_4

**Hook function related definitions:**

USE\_IDLE\_HOOK Disabled  
USE\_TICK\_HOOK Disabled  
USE\_MALLOC\_FAILED\_HOOK Disabled  
USE\_DAEMON\_TASK\_STARTUP\_HOOK Disabled  
CHECK\_FOR\_STACK\_OVERFLOW Disabled

**Run time and task stats gathering related definitions:**

GENERATE\_RUN\_TIME\_STATS Disabled  
USE\_TRACE\_FACILITY Disabled  
USE\_STATS\_FORMATTING\_FUNCTIONS Disabled

**Co-routine related definitions:**

USE\_CO\_ROUTINES Disabled  
MAX\_CO\_ROUTINE\_PRIORITIES 2

**Software timer definitions:**

USE\_TIMERS Disabled

**Interrupt nesting behaviour configuration:**

LIBRARY\_LOWEST\_INTERRUPT\_PRIORITY 15  
LIBRARY\_MAX\_SYSCALL\_INTERRUPT\_PRIORITY 5

### 5.7.2. Include parameters:

#### Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

## 5.8. LWIP

### mode: Enabled

Advanced parameters are not listed except if modified by user.

### 5.8.1. General Settings:

#### LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX \*\* CubeMX specific \*\*) 2.0.3

#### IPv4 - DHCP Options:

LWIP\_DHCP (DHCP Module) Enabled

#### RTOS Dependency:

WITH\_RTOS (Use FREERTOS \*\* CubeMX specific \*\*) Enabled

#### Protocols Options:

LWIP\_ICMP (ICMP Module Activation) Enabled

LWIP\_IGMP (IGMP Module) Disabled

LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

## 5.8.2. Key Options:

### Infrastructure - OS Awareness Option:

NO_SYS (OS Awareness)	OS Used
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### Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled
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### Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled
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### Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	1600
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### Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

### Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

### IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled
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### Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

### Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Disabled

### NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled
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### Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	3
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwip"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

#### Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled
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#### Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0

### 5.8.3. PPP:

#### PPP Options:

PPP_SUPPORT (PPP Module)	Disabled
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### 5.8.4. IPv6:

#### IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled
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### 5.8.5. HTTPD:

#### HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled
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### 5.8.6. SNMP:

#### SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled
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### 5.8.7. SNTP:

#### SNTP Options:

LWIP\_SNTP (LWIP SNTP Support \*\* CubeMX specific \*\*) Disabled

### 5.8.8. MDNS/TFTP:

#### MDNS Options:

LWIP\_MDNS (Multicast DNS Support \*\* CubeMX specific \*\*) Disabled

#### TFTP Options:

LWIP\_TFTP (TFTP Support \*\* CubeMX specific \*\*) Disabled

### 5.8.9. Perf/Checks:

#### Sanity Checks:

LWIP\_DISABLE\_TCP\_SANITY\_CHECKS (TCP Sanity Checks) Disabled

LWIP\_DISABLE\_MEMP\_SANITY\_CHECKS (MEMP Sanity Checks) Disabled

#### Performance Options:

LWIP\_PERF (Performance Testing for LwIP) Disabled

### 5.8.10. Statistics:

#### Debug - Statistics Options:

LWIP\_STATS (Statistics Collection) Disabled

### 5.8.11. Checksum:

#### Infrastructure - Checksum Options:

CHECKSUM\_BY\_HARDWARE (Hardware Checksum \*\* CubeMX specific \*\*) Disabled

LWIP\_CHECKSUM\_CTRL\_PER\_NETIF (Generate/Check Checksum per Netif) Disabled

CHECKSUM\_GEN\_IP (Generate Software Checksum for Outgoing IP Packets) Disabled

CHECKSUM\_GEN\_UDP (Generate Software Checksum for Outgoing UDP Packets) Disabled

CHECKSUM\_GEN\_TCP (Generate Software Checksum for Outgoing TCP Packets) Disabled

CHECKSUM\_GEN\_ICMP (Generate Software Checksum for Outgoing ICMP Packets) Disabled

CHECKSUM\_GEN\_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets) Disabled

CHECKSUM\_CHECK\_IP (Generate Software Checksum for Incoming IP Packets) Disabled

CHECKSUM\_CHECK\_UDP (Generate Software Checksum for Incoming UDP Packets) Disabled

CHECKSUM\_CHECK\_TCP (Generate Software Checksum for Incoming TCP Packets) Disabled

CHECKSUM\_CHECK\_ICMP (Generate Software Checksum for Incoming ICMP Packets) Disabled

CHECKSUM\_CHECK\_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets) Disabled

### 5.8.12. Debug:

#### LwIP Main Debugging Options:

LWIP\_DBG\_MIN\_LEVEL (Minimum Level)

All

\* User modified value



## 6. System Configuration

### 6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_MDC [LAN8742A-CZ-TR_MDC]
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down		STLK_RX

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					<b>Very High</b> *	[STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	STLK_TX [STM32F103CBT6_PA2]
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	USB_SOF [TP1]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	<b>n/a</b>	USB_VBUS
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	USB_DP
Single Mapped Signals	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	USB_ID
	PB3	SYS_JTDO-SWO	n/a	n/a	<b>n/a</b>	SW0
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B1]
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green]
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]

## 6.2. DMA configuration

nothing configured in DMA service

### 6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM1 trigger and commutation interrupts and TIM11 global interrupt	true	0	0
Ethernet global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 capture compare interrupt	unused		
USART3 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
USB On The Go FS global interrupt	unused		
FPU global interrupt	unused		

\* User modified value

## ***7. Power Consumption Calculator report***

### 7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746ZGTx
Datasheet	027590_Rev4

### 7.2. Parameter Selection

Temperature	25
Vdd	3.6

## ***8. Software Pack Report***

## 9. Software Project

### 9.1. Project Settings

Name	Value
Project Name	test_freeRtOs
Project Folder	/home/cheff/robotik/test_freeRtOs
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F7 V1.11.0

### 9.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No