Title:

Physical (Layout) design of Complex Functions for Implementation in Various Target (Implementation) technologies – MPGAs, Full-Custom Chips and CBICs.

Abstraction:

In this experiment we are going to learn how to design Physical layout of complex Function in various technologies like Mask Programmable Gate Arrays, Cell Based Integrated Circuits, Full-Custom chips. We are going to learn how to prepare a transistor level schematic and design complex Boolean Function using complimentary CMOS logic and NAND-NOR network.

Theory and Methodology:

The complimentary CMOS logic implementation of Boolean Function $Y = ((A \cdot B) + (C \cdot D))'$.

Logic Level View :

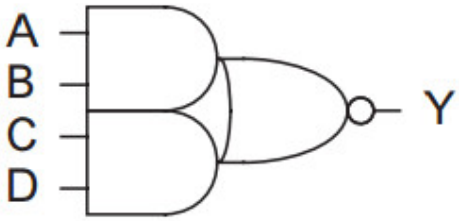
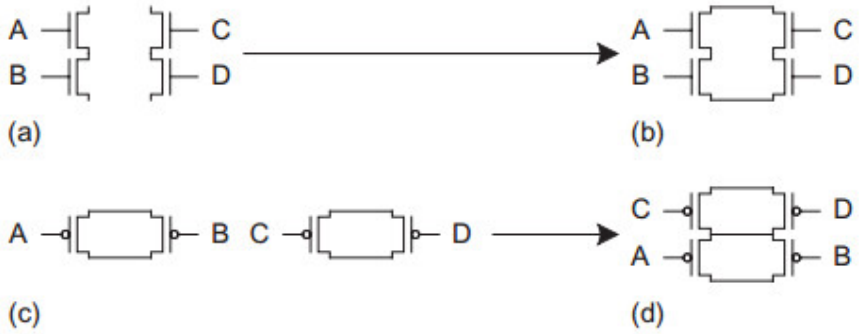
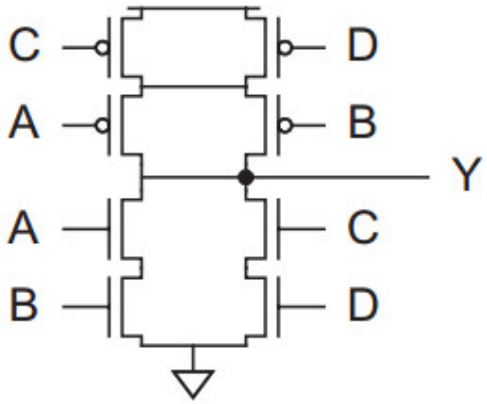


Figure 1: Logic Level Schematic of $Y = ((A \cdot B) + (C \cdot D))'$.

Circuit (Transistor) Level View :

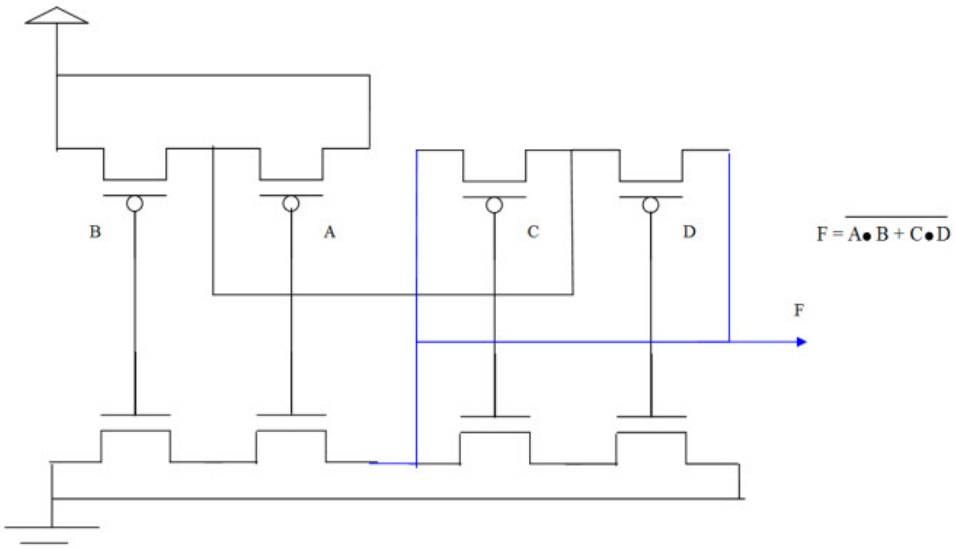




(e)

Y = $((A \cdot B) + (C \cdot D))'$ designed with 8 transistors—4 PMOS devices and 4 NMOS devices in Full-Custom Design Implementation Technology.

Modified Circuit Diagram :



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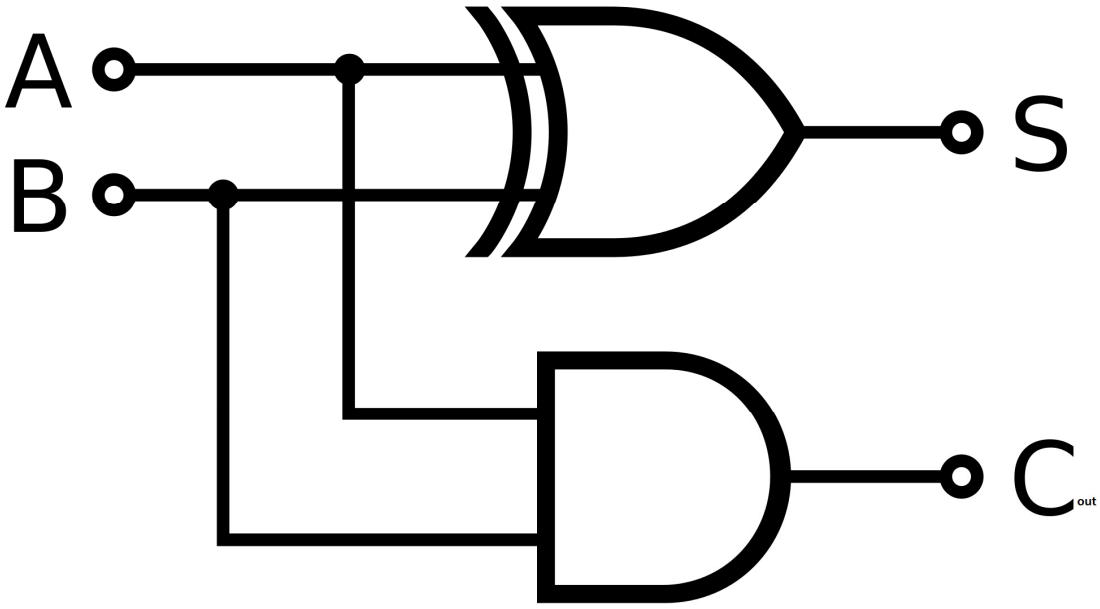
Implementation of Half adder:

Logic Level View :



Half adder sum equation is $S = A \oplus B$.

$$= \overline{\overline{A \oplus B}}$$

$$= \overline{\overline{A} \bullet \overline{B} + A \bullet B} \quad \ldots\ldots\ldots\ldots\ldots (2A1)$$

$$= \overline{\overline{A + B} + A \bullet B}$$

$$= \overline{\overline{A + B} + Cout} \quad \ldots\ldots\ldots\ldots\ldots (2A2)$$

$Cout = A \bullet B$

$$= \overline{\overline{A \bullet B}} \qquad = \overline{\overline{A} + \overline{B}} \quad \ldots\ldots\ldots\ldots\ldots (2B)$$

Circuit (Transistor) Level View :

Apparatus:

- A Windows-based (XP or 7) PC with standard word processors (i.e. Microsoft Office) and PDF readers (i.e. Adobe Acrobat Reader/Writer, Foxit Reader/Phantom) installed.

Simulation And Measurement:

Complimentary CMOS Logic:

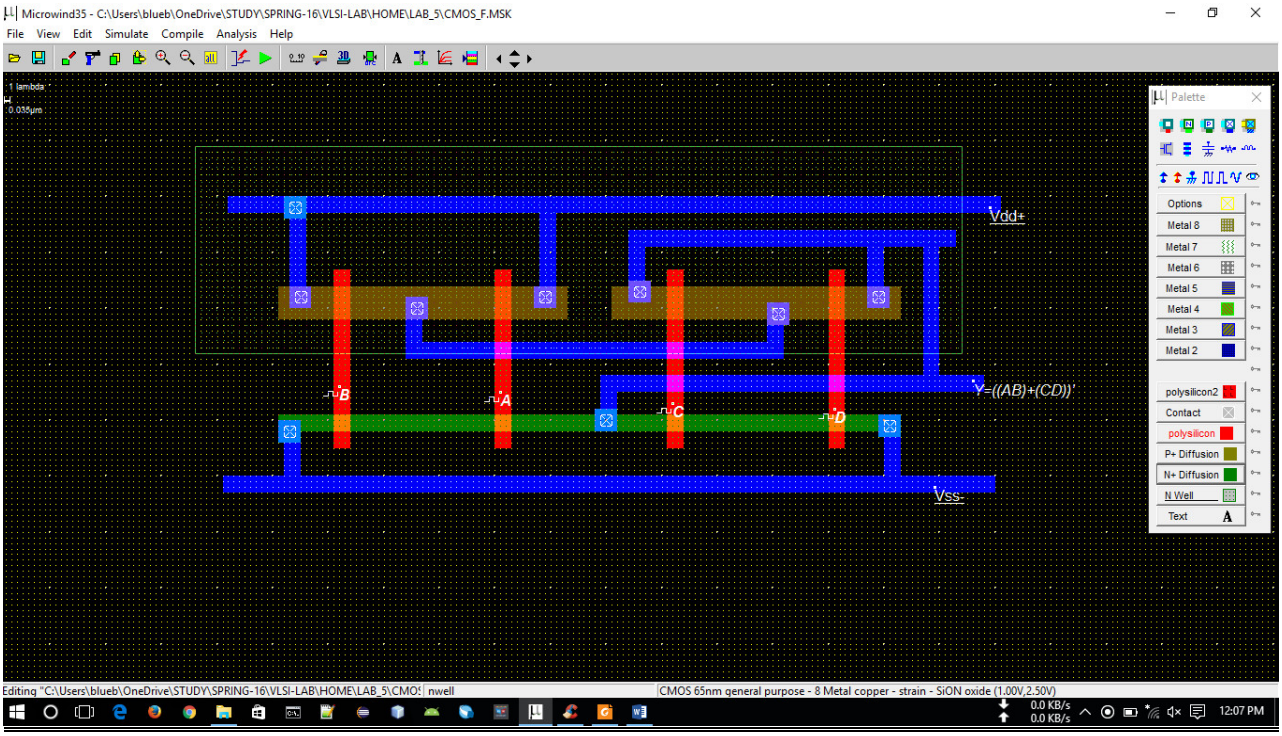


Fig: Complimentary CMOS implementation of $Y = ((A \cdot B) + (C \cdot D))'$

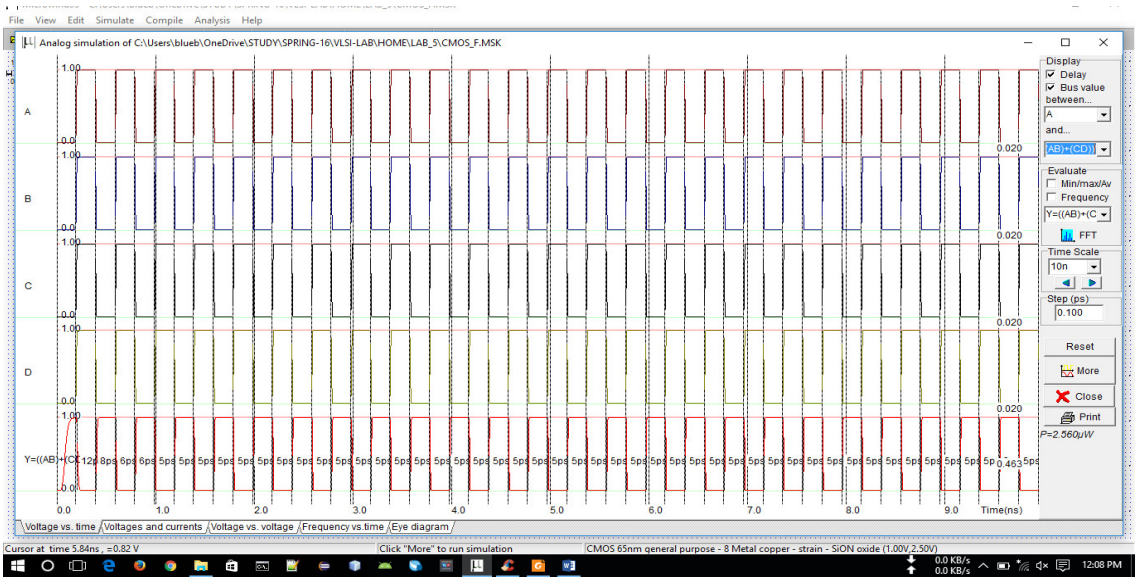


Fig: OUTPUT of $Y = ((A \cdot B) + (C \cdot D))'$

Using NAND-NOR Network:

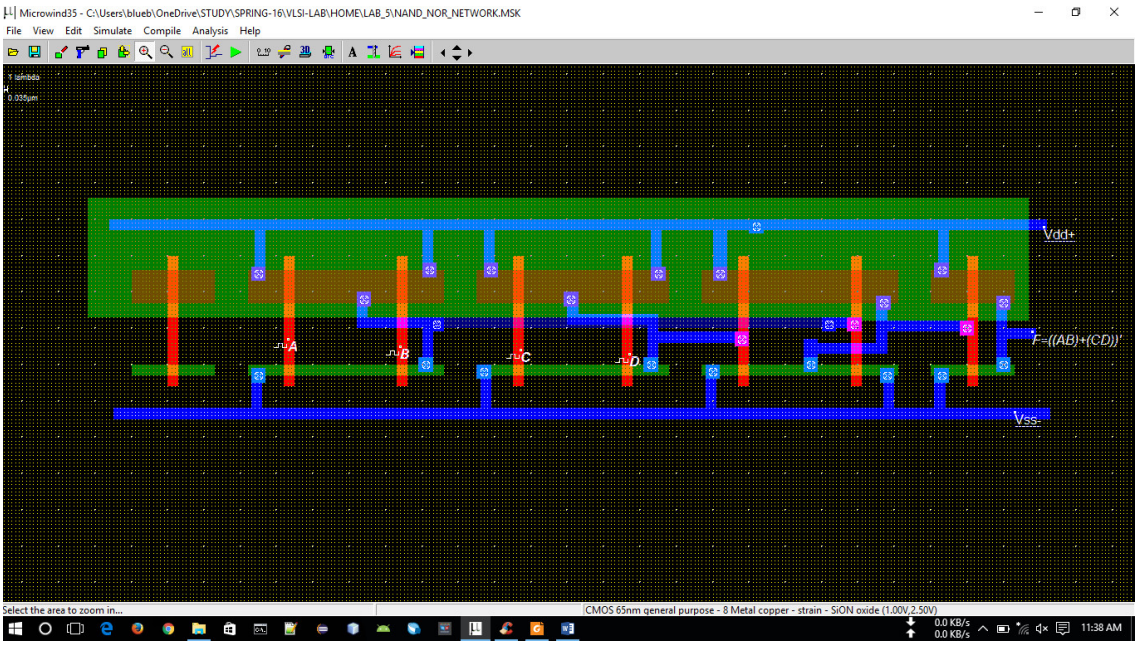


Fig: implementation of $Y = ((A \cdot B) + (C \cdot D))'$ using NAND-NOR Network.

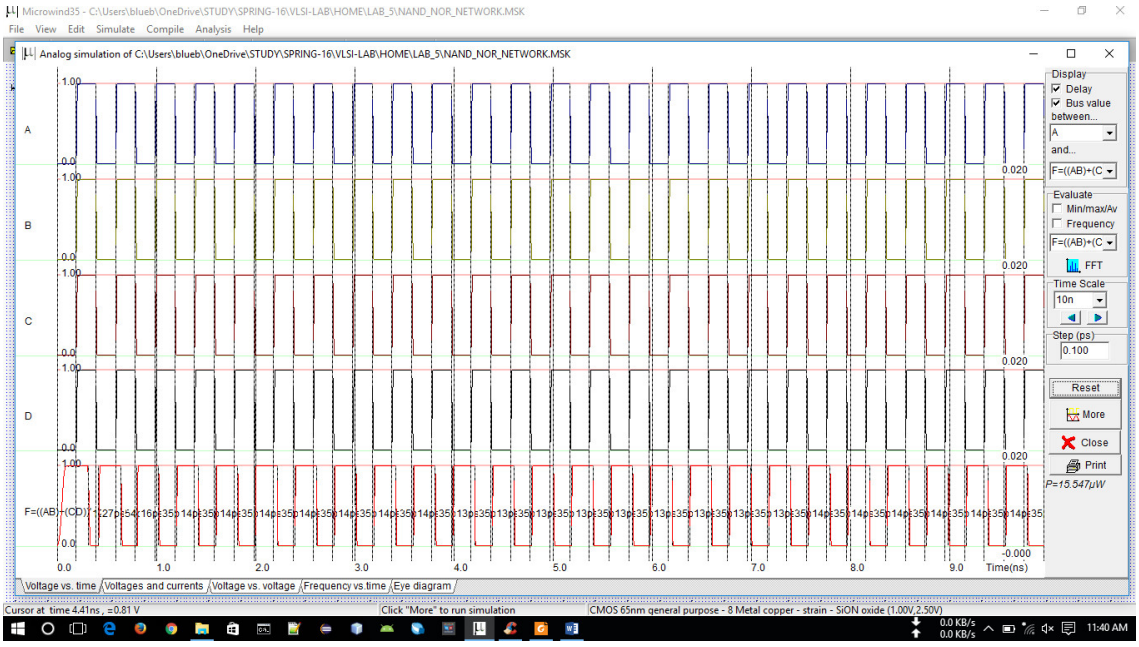


Fig: OUTPUT of $Y = ((A \cdot B) + (C \cdot D))'$

NAND-NOR Network implementation of Boolean Function

$Y = ((A \cdot B) + (C \cdot D))'$.

Implementing Half Adder Using NOR:

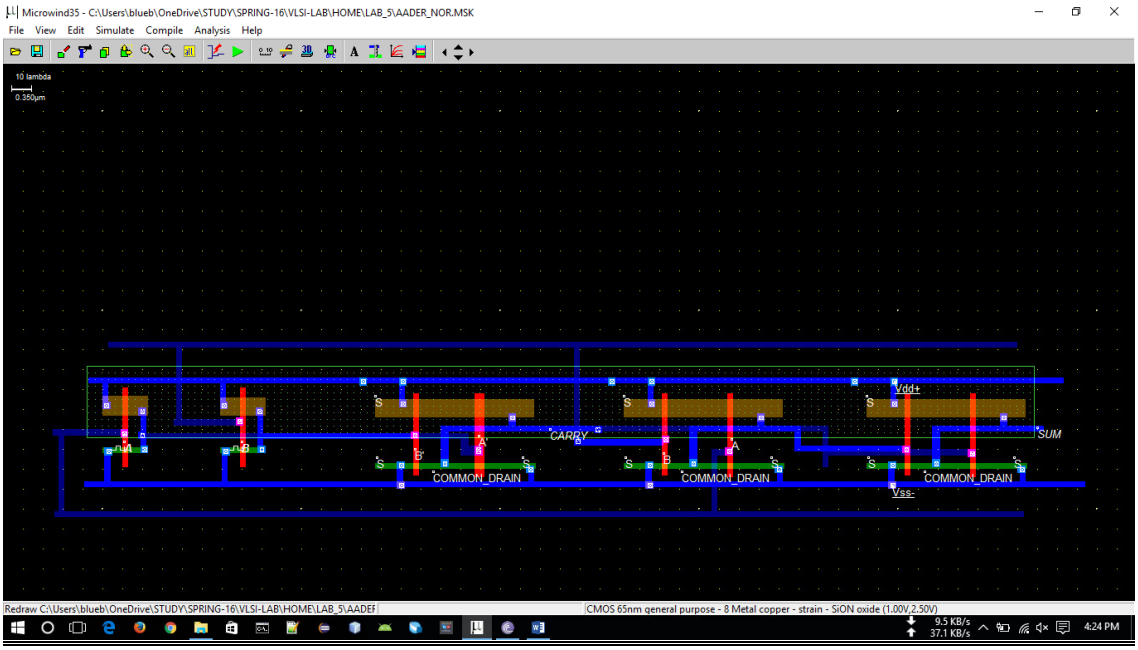


Fig: implementation of Half Adder using NOR.

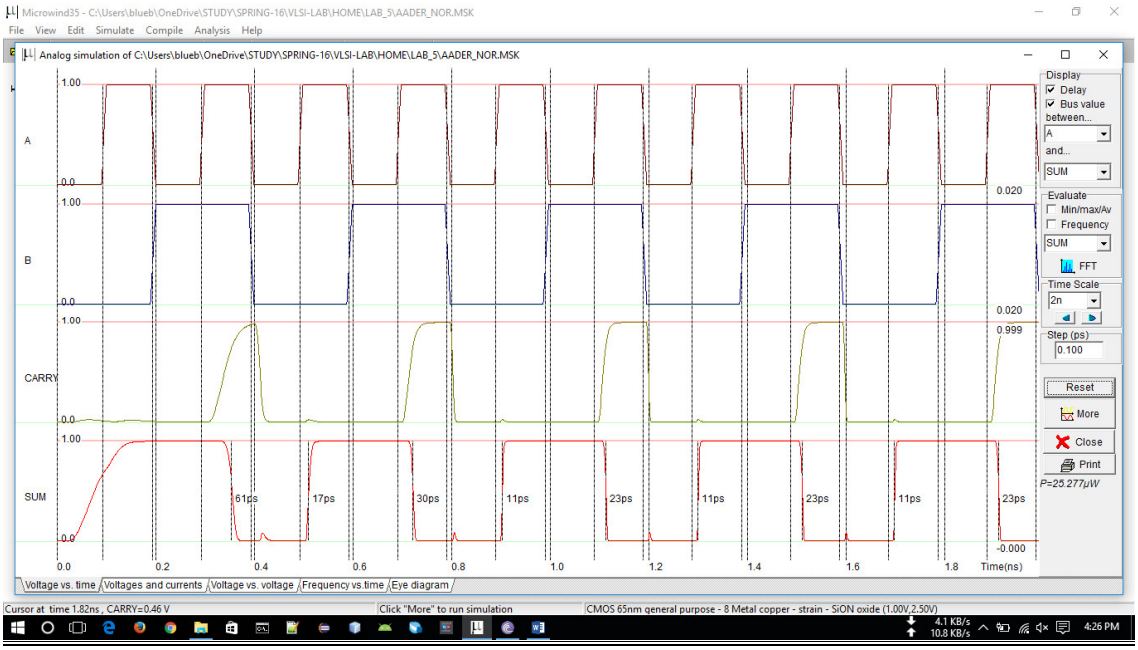


Fig: Output of Half Adder.

Discussion And Conclusion:

In this experiment, we have learnt about how to design Full-custom Chip, implementing Function using complimentary CMOS logic, NAND-NOR network. We also introduced with different type of technologies like- Mask Programmable Gate Array, Cell Based Integrated Circuits.

Reference:

1. *R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation",3rd Edition, John Wiley & Sons, 2010.*
2. *John P. Uyemura, "CMOS Logic Circuit Design", Kluwer Academic Publishers, 2002.*
3. *Etienne Sicard and Sonia Delmas Bendhia, "Advanced CMOS Cell Design", McGraw-Hill, 2007.*