Title:

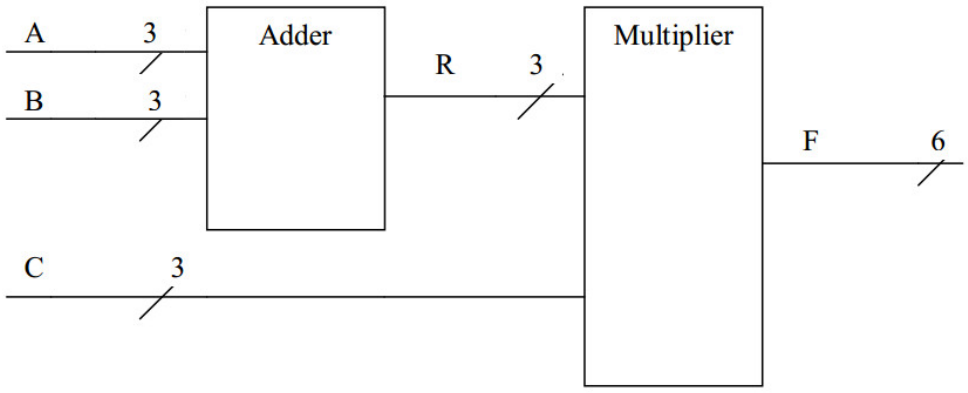
Introduction to HDL Design of Integer and Fixed-point Multiply-Accumulators(MAC) and Introduction to SystemVerilog HDL and VHDL-2008

Introduction:

The main objective of this experiment is to design multiply-accumulators (MAC) using combinational and sequential logic. Most of the arithmetic operation in digital system involves addition, subtraction and multiplication. Multiplier is one of the essential component in DSP circuit.

Theory and Methodology:

Asynchronous or combinational multipliers are generally the fastest possible multiplier available. However, sequential multipliers can also be designed that performance different multiplication steps cycle by cycle. A block diagram of MAC is given below.



Simulation And Measurement:

//package declaration

```
timeunit 1ns;
timeprecision 1ps;
package MAC_PKG;
parameter IN1_WIDTH=3;
parameter IN2_WIDTH=3;
localparam OUT_WIDTH=IN1_WIDTH+IN2_WIDTH;
endpackage: MAC_PKG
```

//design module

```
timeunit 1ns;
timeprecision 1ps;

import MAC_PKG::*;

extern module MAC(
        input logic [IN1_WIDTH-1:0]A,
                logic [IN2_WIDTH-1:0]B,
                logic SYS_CLK,
                logic SCLR,LOAD,
        output logic [OUT_WIDTH-1:0]MAC_OUT);

module MAC(.*);

logic[5:0] SUM, PRODUCT;

always_comb
begin: ADDER_MULT
PRODUCT=A*B;
SUM=PRODUCT+MAC_OUT;
//S=A*B;       // checking the output of A * B
end:ADDER_MULT

always_ff@(posedge SYS_CLK)
begin: REG
```

if(SCLR) MAC_OUT<=0;
else if(LOAD) MAC_OUT<=SUM;
else MAC_OUT<=MAC_OUT;
end: REG

endmodule: MAC

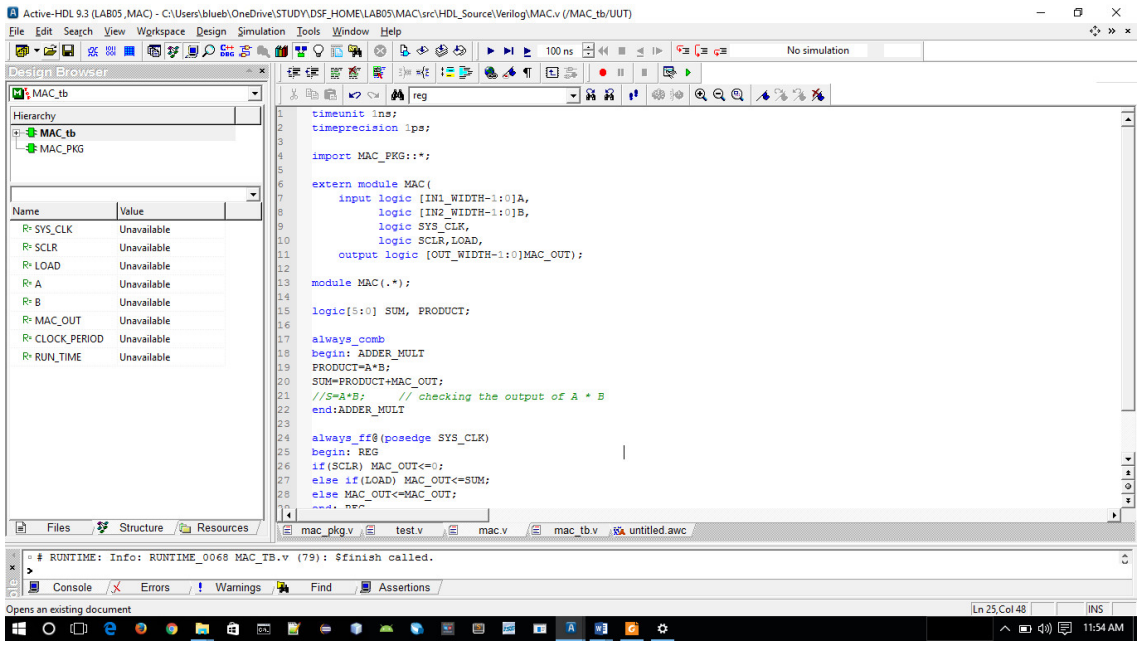


Fig: Source Code

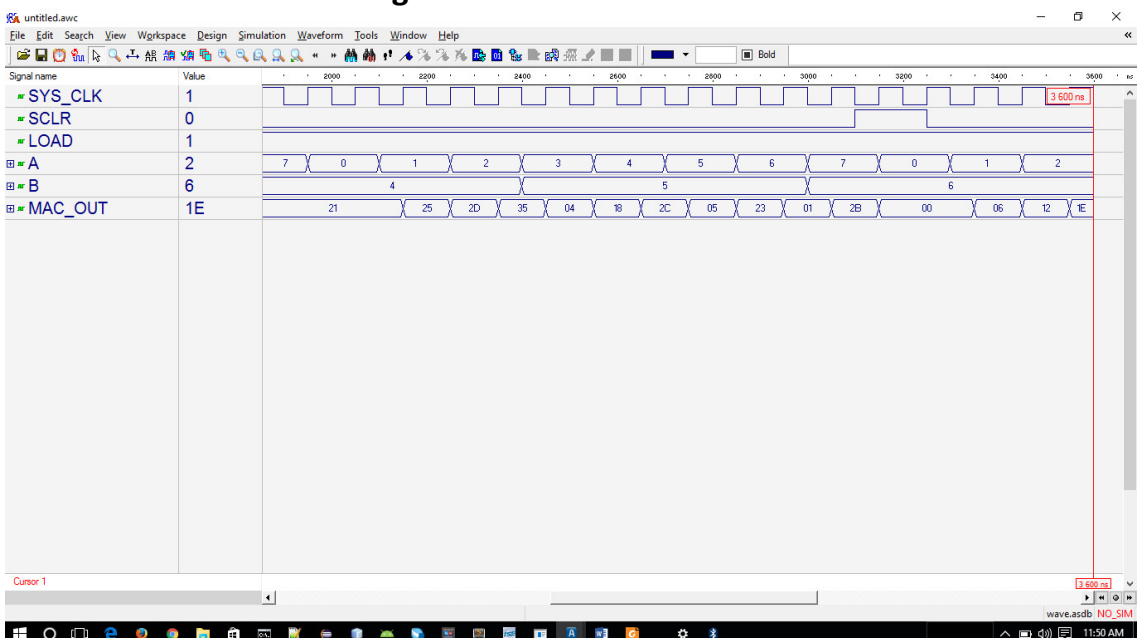


Fig: Functional Verification

Apparatus:

1. A Windows-based (XP or 7 or 10) PC with standard word processors (i.e. Microsoft Office) and PDF readers (i.e. Adobe Acrobat Reader/Writer, Foxit Reader/Phantom) installed.
2. ISE WebPack.

Precautions:

A PC with a standard Anti-Virus program installed was used.

Reference:

1. *D.J. Smith, HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASUC & FPGA using VHDL or Verilog , Madison, AL, USA, Doone Publications. 1996, 6th Printing-1999(minor revisions and code updates for FPGA synthesis)*