Title:

SPICE Simulation of Logic Gates.

Introduction:

For digital designers, it is important to not only know how basic and complex logic gates operate but also to learn how a complex CMOS logic gate can be modeled in a standard circuit simulation language such as PSPICE and how their component transistors can be sized based on a reference inverter. The objective of this experiment is determine the size of the transistors in CMOS logic through PSPICE.

Apparatus:

1. A Windows-based (XP or 7 or 10) PC with standard word processors (i.e. Microsoft Office) and PDF readers (i.e. Adobe Acrobat Reader/Writer, Foxit Reader/Phantom) installed.
2. A PSPICE simulator, preferably ORCAD PSpice Student 9.1 Student from Cadence

Theory and Methodology:

Transistor Sizing:

To size the transistors of the two input NAND gate, consider a reference inverter (any symmetric inverter) with,

$(W/L)_P = 12\mu m/3\mu m$ and $(W/L)_N = 4\mu m/3\mu m$

So that the fall time and rise time of NAND gate are equal (output Resistance of NAND gate is same as the reference inverter)

To ensure,

$t_f = t_r$.

we need,

$I_{inv\_pull\_down} = I_{inv\_pull\_up}$

To do this, we need-

$V_{TN} = |V_{TP}|$ and $\beta_N = \beta_P$

V_T = threshold voltage

β = MOS gain factor
= Device transconductance

Let assume,

$V_{TN} = |V_{TP}|$

So we need,

$\beta_N = \beta_P$

or, $\mu_N Cox(W/L)_N = \mu_P Cox(W/L)_P$

here,

Cox= Oxide capacitance / area

μ = Mobility of charge carrier

W = gate width

L = gate length

μ_n = mobility of electrons

μ_p = mobility of holes

or, , $\mu_N(W/L)_N = \mu_P(W/L)_P$

Mobility of electron = 3* mobility of holes.

$\mu_N = 3\mu_P$

So need,

$(W/L)_P = 3(W/L)_N$

In a specific manufacturing process and for specific design, all gate lengths are kept same.

$L_N = L_P$

So,

$W_p = 3\ W_N$

NAND2:

To ensure ,

$$t_f = t_r$$

we need,

$$I_{NAND2\_PULL\_DOWN} = I_{NAND2\_PULL\_UP}$$

or, $$R_{NAND2\_PULL\_DOWN} = R_{NAND2\_PULL\_UP}$$

To do this, we need-

$$R_{NAND2\_PULL\_DOWN} = R_{INV\_PULL\_DOWN}$$

and, $$R_{NAND2\_PULL\_UP} = R_{INV\_PULL\_UP}$$

So need,

$$R_{NAND2\_PULL\_UP} = R_{INV\_PULL\_UP}$$

or, $$R_{NA} + R_{NB} = R_N$$

$$R_{MOS} \approx 1/\beta_{MOS}$$

or, $$1/\beta_{NA} + 1/\beta_{NB} = 1/\beta_N$$

or, $$1/(\mu_N Cox(W/L)_{NA}) + 1/(\mu_N Cox(W/L)_{NB}) = 1/(\mu_N Cox(W/L)_N)$$

All transistors in a design have same cox and all NMOS in a design have same μ_N.

or, $$1/(W/L)_{NA} + 1/(W/L)_{NB} = 1/(W/L)_N$$

or, $$1/(W/L)_{NA} + 1/(W/L)_{NB} = 1/(4/3)$$

1 equation, 2 unknown.

If we make, $(W/L)_{NA} = (W/L)_{NB} = (W/L)_{N\_NAND2}$

Then we have 1 equation, 1 unknown,

$$2*1/(W/L)_{N\_NAND2} = 1/(4/3)$$

or, $(W/L)_{N\_NAND2} = 8/3$.

To ensure,

$$R_{NAND\_PULL\_UP} = R_{INV\_PULL\_UP}$$

Since in pull up network, MOS devices have parallel configuration, worst case scenario is that only 1 p-MOS is on if 1 p-MOS is on in NAND2 gate, its pull up network is identical to the pull up network of inverter.

$$R_{NAND\_PULL\_UP} = R_{PA} = R_{PB} = R_{INV\_PULL\_UP}$$

or, $1/\beta_{NAND\_PULL\_UP} = 1/\beta_{PA} = 1/\beta_{PB} = 1/R_{INV\_PULL\_UP}$

or, $1/(W/L)_{NAND\_PULL\_UP} = 1/(W/L)_{PA} = 1/(W/L)_{PB} = 1/(W/L)_{INV\_PULL\_UP} = 1/(12/3)$

so,

$$(W/L)_{PA} = (W/L)_{PB} = 12/3$$

Simulation And Measurement:

NAND 2

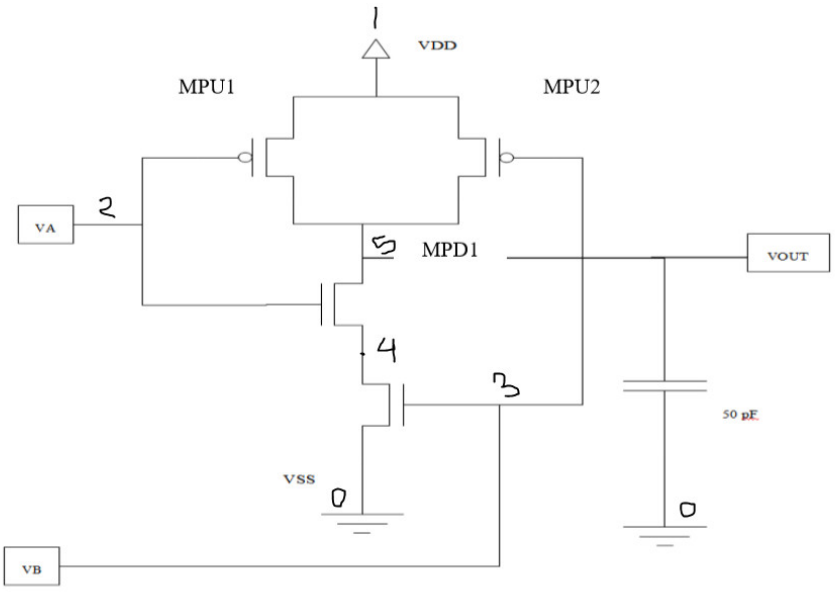

Figure 1: Circuit Diagram of NAND 2

NAND2 SPICE CODE:

CMOS NAND2

*****MOS Description**

***device_name drain_node gate_node source_node body_node device_type gate_width gate_length**

```
mpu1 5 2 1 1 penh w=12u l=3u
mpu2 5 3 1 1 penh w=12u l=3u

mpd1 5 2 4 4 nenh w=8u l=3u
mpd2 4 3 0 0 nenh w=8u l=3u

***Load Capacitor Description
*Device_name node+ node- value

cl 5 0 50f

***Source Description
**********************

**constant voltage source
*source_name node+ node- value

vdd 1 0 5

**pulse voltage_source
*source_name node+ node- pulse ( Vmin Vmax delay/offset/(td) rise_time/(tr) fall_time/(tr) time_width/(pw)  period/(per))

va 2 0 pulse (0 5 3ns 3ns 3ns 20ns 40ns)
vb 3 0 pulse (0 5 3ns 3ns 3ns 30ns 60ns)


***********************************************
*Model Specification
***********************************************
****NMOS Model (MOS type is Enhancement-MODE)

.model nenh nmos level=2 vto=.85 kp=30e-6 tox=470e-10 nsub=38e14
+ld=0.6e-6 uo=624 uexp=0.055 vmax=20e4 neff=9.8 delta=2.0
+ cj=160e-6 cjsw=430e-12 mj=0.5 mjsw=0.33 pb=0.81

***********************************************
****PMOS Model (MOS type is Enhancement-MODE)

.model penh pmos level=2 vto=-.85 kp=12e-6 tox=470e-10 nsub=8.7e14
+ld=0.5e-6 uo=200 uexp=0.18 vmax=12e4 neff=4.0 delta=2.0
+ cj=100e-6 cjsw=180e-12 mj=0.5 mjsw=0.33 pb=0.7

***transient Analysis

.tran 1ns 160ns
.probe
***END of Simulation
.end
```

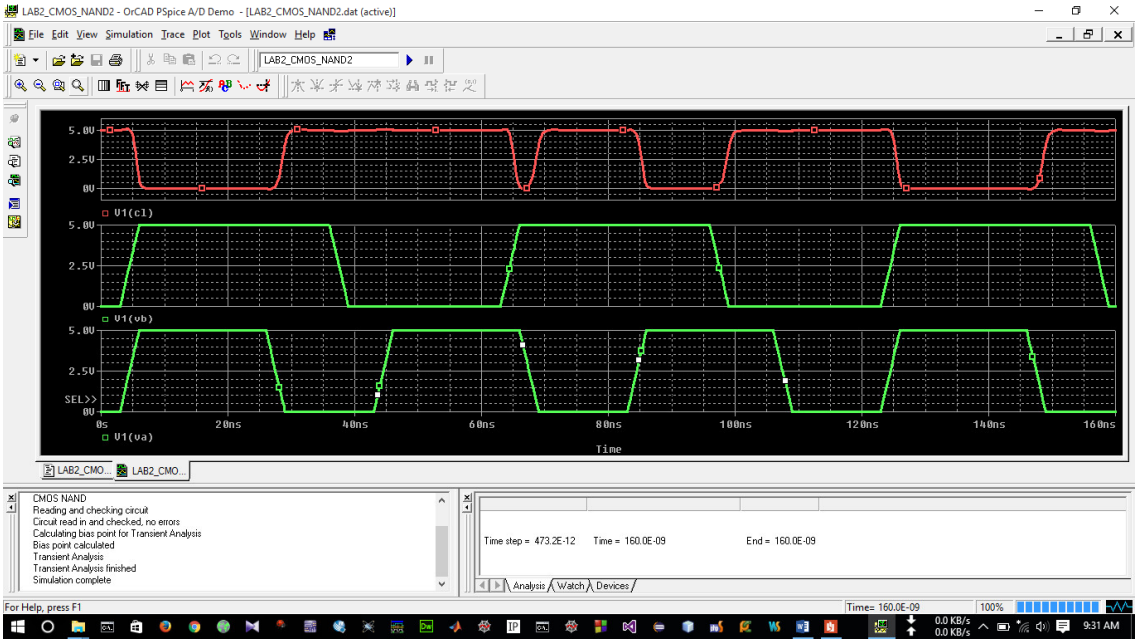

Figure 2: Output of NAND 2

- Fall Time (t_f) = (7-5) ns
  = 2ns
- Rise Time (t_r) = (30-28) ns
  = 2ns

  Time delay ($t_{d)}$ = 5ns

NOR 2:

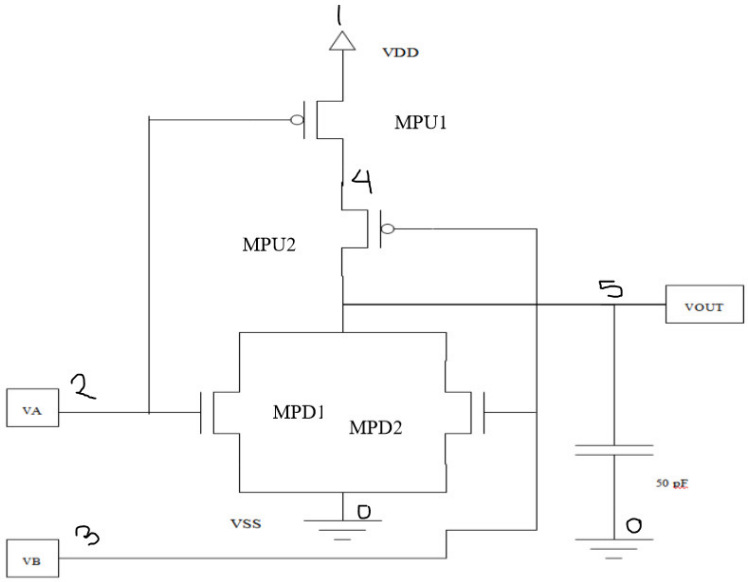

Figure 3: Circuit Diagram Of NOR

NOR2 SPICE CODE:

```
CMOS NOR


***MOS Description
*device_name drain_node gate_node source_node body_node device_type gate_width gate_length

mpu1 4 2 1 1 penh w=24u l=3u
mpu2 5 3 4 4 penh w=24u l=3u

mpd1 5 2 0 0 nenh w=4u l=3u
mpd2 5 3 0 0 nenh w=4u l=3u

***Load Capacitor Description
*Device_name node+ node- value

cl 5 0 50f

***Source Description
**********

**constant voltage source
*source_name node+ node- value

vdd 1 0 5

**pulse voltage_source
*source_name node+ node- pulse ( Vmin Vmax delay/offset/(td) rise_time/(tr) fall_time/(tr) time_width/(pw)  period/(per))

va 2 0 pulse (1 4 1ns 2ns 3ns 10ns 20ns)
vb 3 0 pulse (1 4 1ns 2ns 3ns 20ns 40ns)




**********
*Model Specification
**********

**********
****NMOS Model (MOS type is Enhancement-MODE)

.model nenh nmos level=2 vto=.85 kp=30e-6 tox=470e-10 nsub=38e14
+ld=0.6e-6 uo=624 uexp=0.055 vmax=20e4 neff=9.8 delta=2.0
+ cj=160e-6 cjsw=430e-12 mj=0.5 mjsw=0.33 pb=0.81

**********
****PMOS Model (MOS type is Enhancement-MODE)

.model penh pmos level=2 vto=-.85 kp=12e-6 tox=470e-10 nsub=8.7e14
+ld=0.5e-6 uo=200 uexp=0.18 vmax=12e4 neff=4.0 delta=2.0
+ cj=100e-6 cjsw=180e-12 mj=0.5 mjsw=0.33 pb=0.7


***transient Analysis
```

.tran 1ns 160ns

.probe

*****END of Simulation**

.end

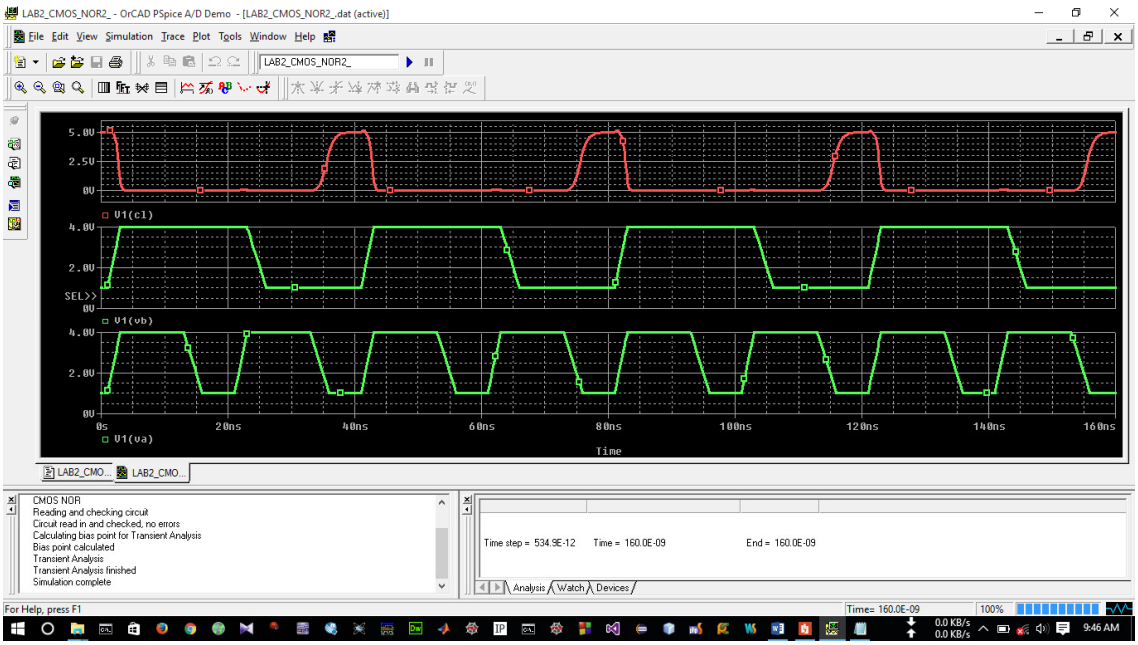

Figure 4: Output Of NOR 2

- Fall Time (t_f) = (4-1) ns
  = 3ns
- Rise Time (t_r) = (38-34) ns
  = 4ns

  Time delay ($t_{d)}$ = 1ns

CMOS Inverter:

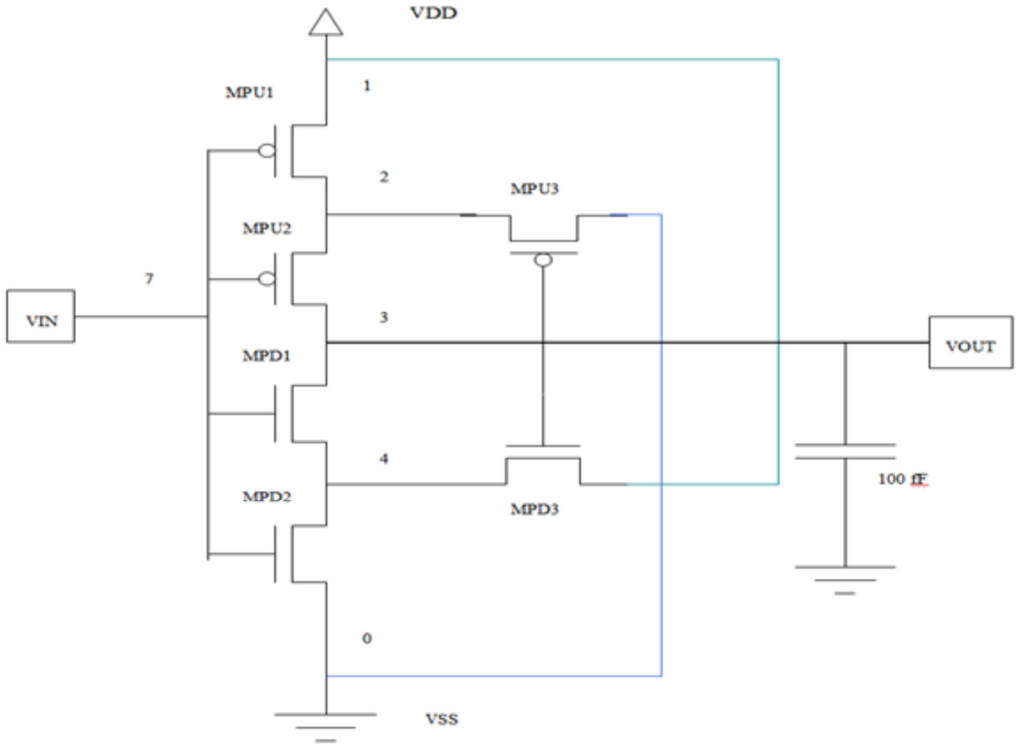

Figure 5: Circuit Diagram Of CMOS Inverter

SPICE Code of CMOS Inverter:

```
SIX TRANSISTORS CMOS INVERTER


***MOS Description
*device_name drain_node gate_node source_node body_node device_type gate_width gate_length

mpu1 2 7 1 1 penh w=20u l=3u
mpu2 3 7 2 2 penh w=20u l=3u
mpu3 0 3 2 2 penh w=8u l=3u

mpd1 3 7 4 4 nenh w=10u l=3u
mpd2 4 7 0 0 nenh w=10u l=3u
mpd3 1 3 4 4 nenh w=4u l=3u

***Load Capacitor Description
*Device_name node+ node- value

cl 3 0 100f

***Source Description
```

****

**constant voltage source
*source_name node+ node- value

vdd 1 0 5

**pulse voltage_source
*source_name node+ node- pulse (Vmin Vmax delay/offset/(td) rise_time/(tr) fall_time/(tr) time_width/(pw) period/(per))

vin 7 0 pulse (0 5 1ns 2ns 3ns 10ns 20ns)

****
*Model Specification
****

****
****NMOS Model (MOS type is Enhancement-MODE)

.model nenh nmos level=2 vto=.85 kp=30e-6 tox=470e-10 nsub=38e14
+ld=0.6e-6 uo=624 uexp=0.055 vmax=20e4 neff=9.8 delta=2.0
+ cj=160e-6 cjsw=430e-12 mj=0.5 mjsw=0.33 pb=0.81

****
****PMOS Model (MOS type is Enhancement-MODE)

.model penh pmos level=2 vto=-.85 kp=12e-6 tox=470e-10 nsub=8.7e14
+ld=0.5e-6 uo=200 uexp=0.18 vmax=12e4 neff=4.0 delta=2.0
+ cj=100e-6 cjsw=180e-12 mj=0.5 mjsw=0.33 pb=0.7

***DC Analysis

.dc vin 0 5 0.1

***transient Analysis

.tran 1ns 120ns

.probe

***END of Simulation
.end

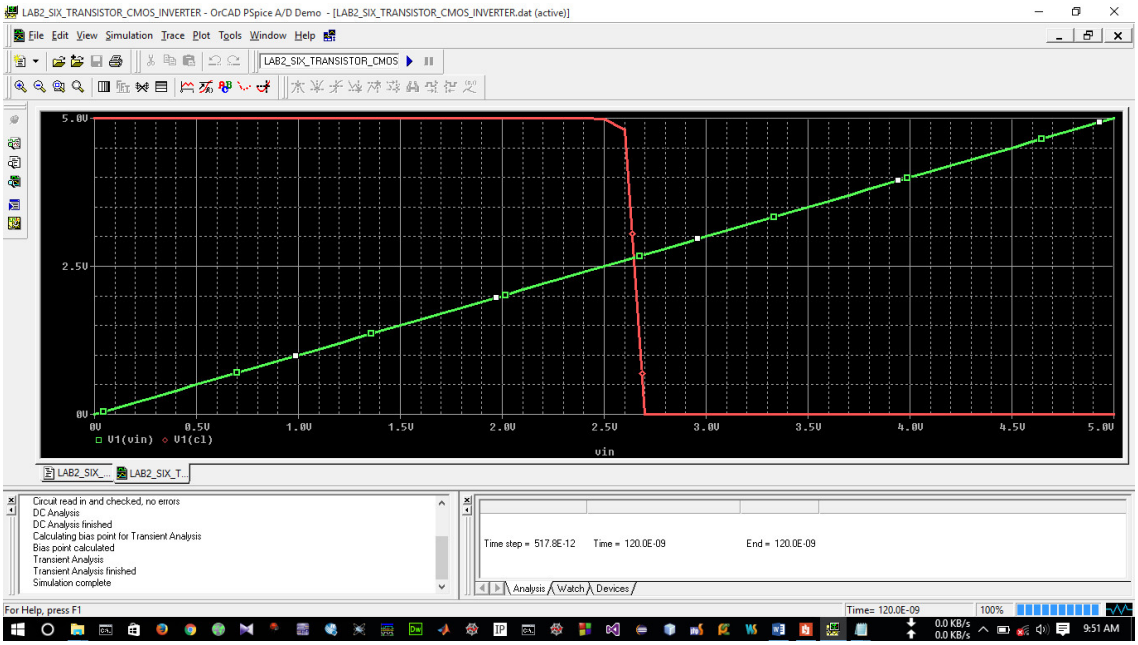

Figure 6: DC Analysis Of CMOS Inverter

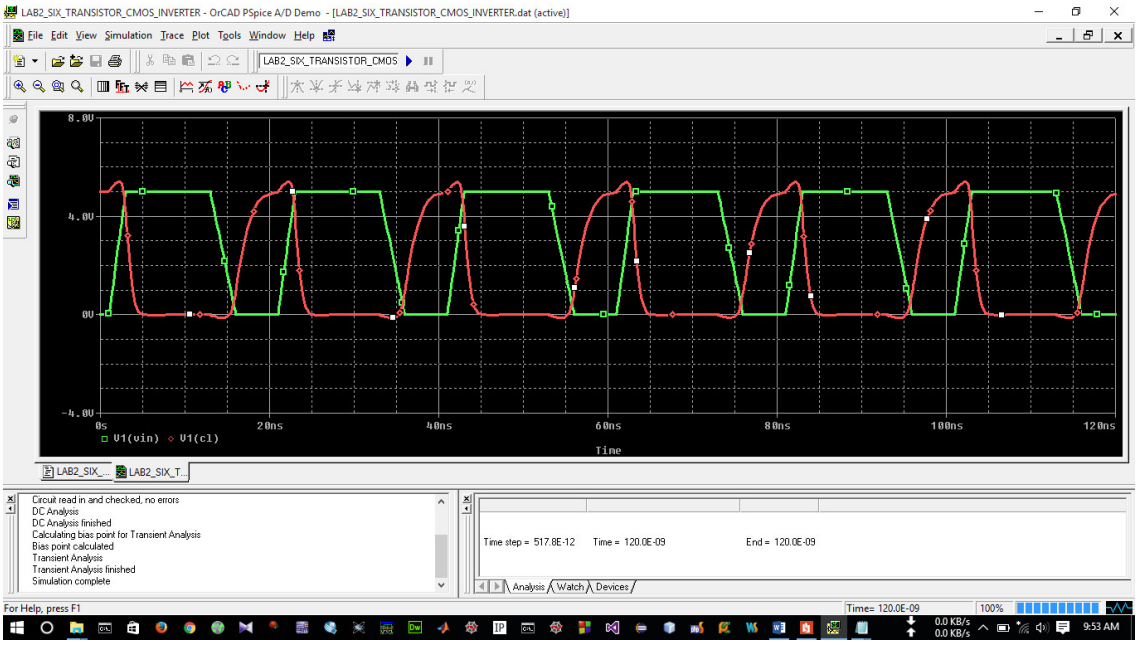

Figure 16: Output (Transient) Of CMOS Inverter

- Fall Time (t_f) = (5-3) ns
  = 2ns
- Rise Time (t_r) = (20-15) ns
  = 5ns

Discussion And Conclusion:

In this experiment, history of PSpice was known. How to use PSpice and coding for CMOS Inverter in PSpice was learned in this experiment. The importance of the size of PMOS and NMOS was examined in this experiment. By combining different type of PMOS and NMOS, the logic gates was examined. By examined the output, input wave shapes, Calculation of the threshold voltage, delay time, rise time, fall time, pulse period, was also learned.

Reference:

1. *http://www.cadence.com/products/orcad/pages/default.aspx*
2. http://www.cadence.com/products/orcad/pages/default.aspx
3. Orcad PSpice A/D User's Guide
4. http://www.eecs.berkeley.edu/Pubs/TechRpts/1973/22871.html