Experiment# 10: HDL Modeling and Synthesis of a Half-Wave, Voltage Controller for AC Loads

ABSTRACT:

The objective of this experiment is the following.

1. To understand the role of digital controllers in AC Voltage Control
2. To understand the role of pseudo-random number generators and zero crossing detection in AC Voltage Control.
3. To simulate, synthesize and fit the designs in Xilinx 5.1i ISE design environment.

INTRODUCTION:

It is possible to control the speed of a motor by supplying appropriate portions of AC half cycles to the load and blocking the rest of the AC signal from "going" to the load. This is called Phase control. This typically generates Radio Frequency Interference (RFI). The frequency spectrum of the AC wave shows lot of power dissipation (frequency components) at frequencies other than the principle frequency (50/60 Hz).

A technique has been developed by Dr. Jerry J. Cupal, Associate Professor Emeritus, University of Wyoming, USA, to reduce RFI, by passing complete half cycles of the AC signal to the load. This type of control is called Cycle Control. What is unique in this design is that while each zero crossing of the input AC wave is detected, an appropriate number of the half cycles is passed according to user demand in the "overall" picture, but in reality they are passed in a pseudo-random sequence. This reduces the RFI.

This laboratory experiment and instruction sheet were developed by
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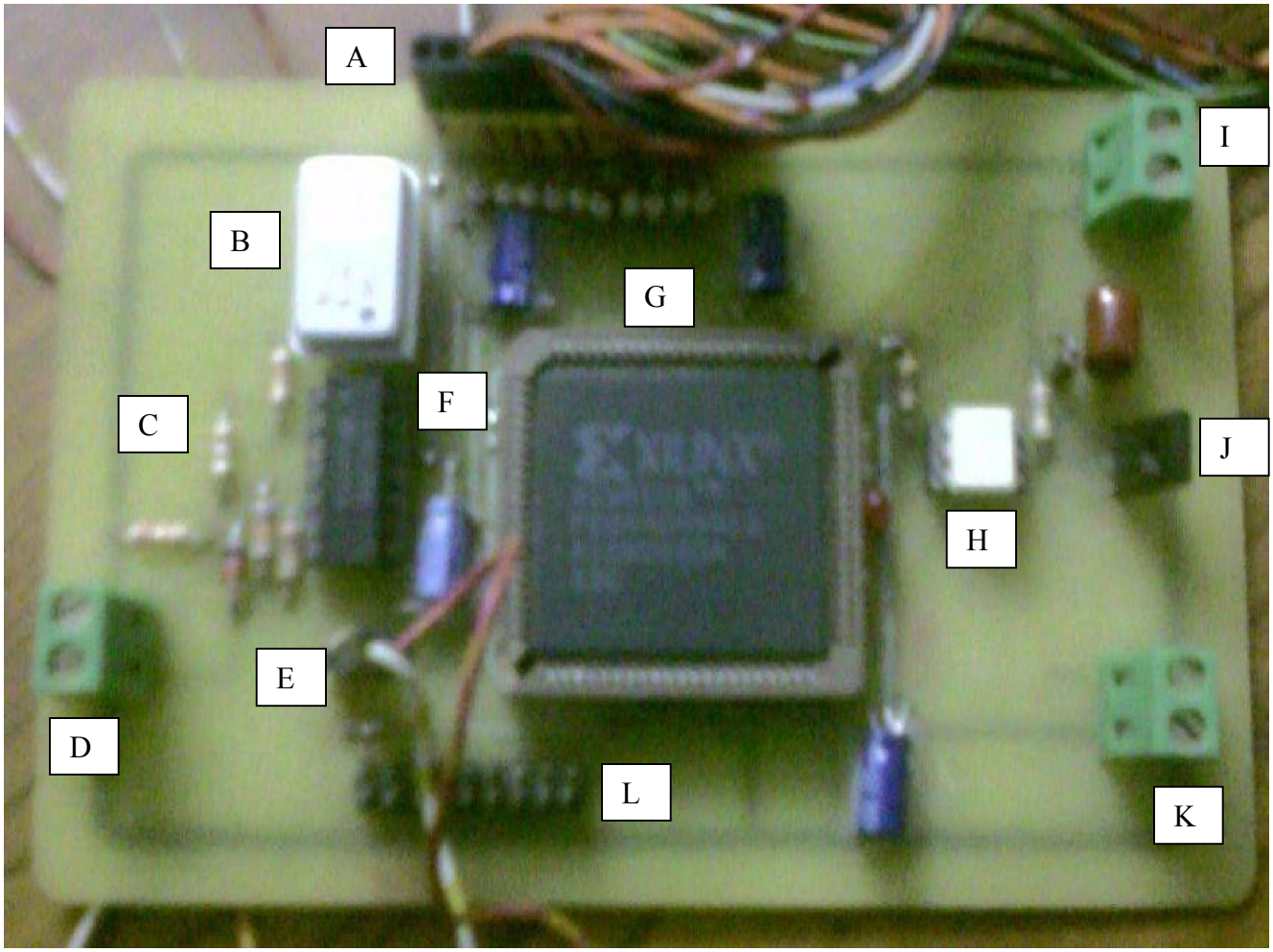
THEORY AND METHODOLOGY:

I implemented this design as part of my senior design project (undergraduate thesis) at University of Wyoming, USA, in 2000. The implemented design included a Xlinx 95108 CPLD, an operational amplifier (used as a zero crossing detector), a Triac (for switching the AC load), a Triac driver, a 4 MHz oscillator (for system clock) and 10 input switches (for supplying the seed) etc. It was implemented on a PCB board and successfully tested on a 60 Hz light bulb (see the figure in page 2). Resulting RFI was indeed much lower. The central digital controller was modeled in Verilog HDL (explicit style, 2 states, 10-bit pseudo-random number generator) and implemented in Xilinx 95108-PC84 CPLD. VeriBest VB99 (VeriBest) was used as the design entry tool, FPGA Express (Synopsys) as the synthesis tool and Xilinx Foundation (Xilinx) was used as the place-and-route and programming (configuration) tool.

One of my students in University of Wyoming (during my Teaching Assistantship years) designed the digital part (FSMD) using 4 states as part of an assignment (you will have to do the same in this lab). An undergraduate thesis group at AIUB under my supervision has improved this design, which included incorporation of efficient digitizedAC sampling, analysis of wide range of pseudo-random number generators and their effects, elimination of DC components and using SCRs instead of TRIACs so that switching is smoother etc.



A = 10-bit user input	G = Xilinx 95108-PC84 CPLD
B = 4 MHz Clock Oscillator	H = Triac Driver
C = Resistor network	I = AC Load Connector
D = 110 V 60 Hz AC power supply	J = Triac (for switching AC Load)
E = Reset Button	K = 5 V DC power supply (for CPLD)
F = Op-Amp (Voltage Comparator)	L = Programming Header for CPLD (for programming/configuration)

APPARATUS:

1. A Windows-based (XP or 7) PC with standard word processors (i.e. Microsoft Office) and PDF readers (i.e. Adobe Acrobat Reader/Writer, Foxit Reader/Phantom) installed.

2. Necessary EDA tools such Active-HDL (Aldec), Precision RTL (Mentor Graphics) and ISE WebPack (Xilinx).

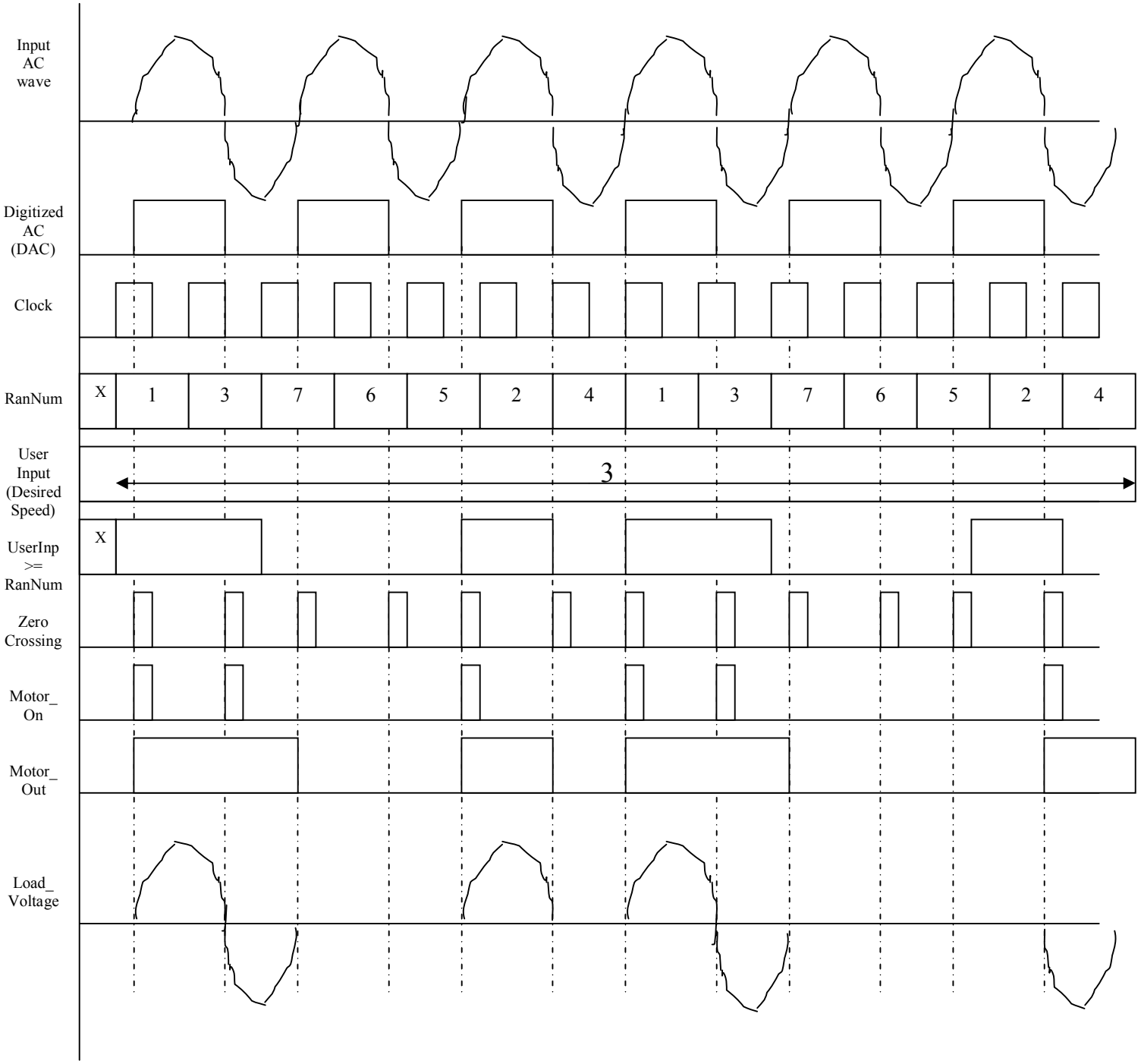
PRECAUTIONS:

1. A PC with a standard Anti-Virus program installed should be used.

EXPERIMENTAL PROCEDURE:

Part-1:

Your teacher will explain to you how half-wave control works utilizing a 3-bit pseudo-random number generator. Analyze the ASM chart, hardware structure, code and simulation.



Part-2:

Develop the ASM chart and relevant hardware structures for the full-wave controller using 3 states and a 10-bit pseudo-random number generator. Use an idle state that outputs Ready and checks the value of Go. If Go is true, activate normal operation (enable pseudo-random number generator, check digitized AC, make decisions about turning on or off the motor), otherwise wait in the idle state. Use a synchronous reset signal that can reset the FSM to the initial state. Write the VHDL code. Simulate, Synthesize and Fit the design into Xilinx XC6SLX16-CSG324 FPGA.

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Extra Credit:

Can you design a half-wave version that does not generate DC component? That is, half cycles are passed in such a way that one will never have a situation where 2 consecutive positive or two consecutive negative half cycles are passed to the load.

SIMULATION AND MEASUREMENT:

Add the simulation, synthesis results, constraints for the circuits discussed above in you simulation segment of the lab report.

RESULT:

To be added later for teachers, if needed.

DISCUSSION AND CONCLUSION:

Attach all the relevant hardware structure diagrams, ASM charts, HDL codes, stimulus, simulations and synthesis reports.

Answer these questions in the conclusion part of your lab report.

How can you increase the accuracy of the pseudo-random sequence without affecting the overall amount of half cycles passed to the load? Which version of the controller is better—half wave or full wave and why?

REFERENCE:

HDL Design Reference:

1. D. J. Smith, HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs using VHDL or Verilog, Madison, AL, USA, Doone Pubications, 1996, 6th Printing-1999 (minor revisions and code updates for FPGA synthesis).

2. Advanced Digital Design/HDL Digital Design Course Notes, Jerry J. Cupal, Associate Professor Emeritus, University of Wyoming, Laramie, WY, USA.

SystemVerilog-2005/2009 Reference:

2. Mark Zwoli´nski, *Digital System Design with SystemVerilog*, 1st Edition, Prentice Hall, 2009.

VHDL-2008 References:

3. P. J. Ashenden and J. Lewis, The Designer's Guide to VHDL, 3rd Edition, Morgan Kaufmann, 2008.

EDA reference:

4. Active-HDL 9.3 Reference Manual—Aldec.

5. Precision Synthesis 2012 Reference Manual—Mentor Graphics.

6. ISE 14.6 Reference Manual—Xilinx

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