PSoC® Creator™
Project Datasheet for chickybot

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Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intl): 408.943.2600
http://www.cypress.com

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1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C54LP family member PSoC 5 device. For details on all the systems listed above, please refer to the PSoC 5 Technical Reference Manual .

Figure 1. CY8C54LP Device Family Block Diagram

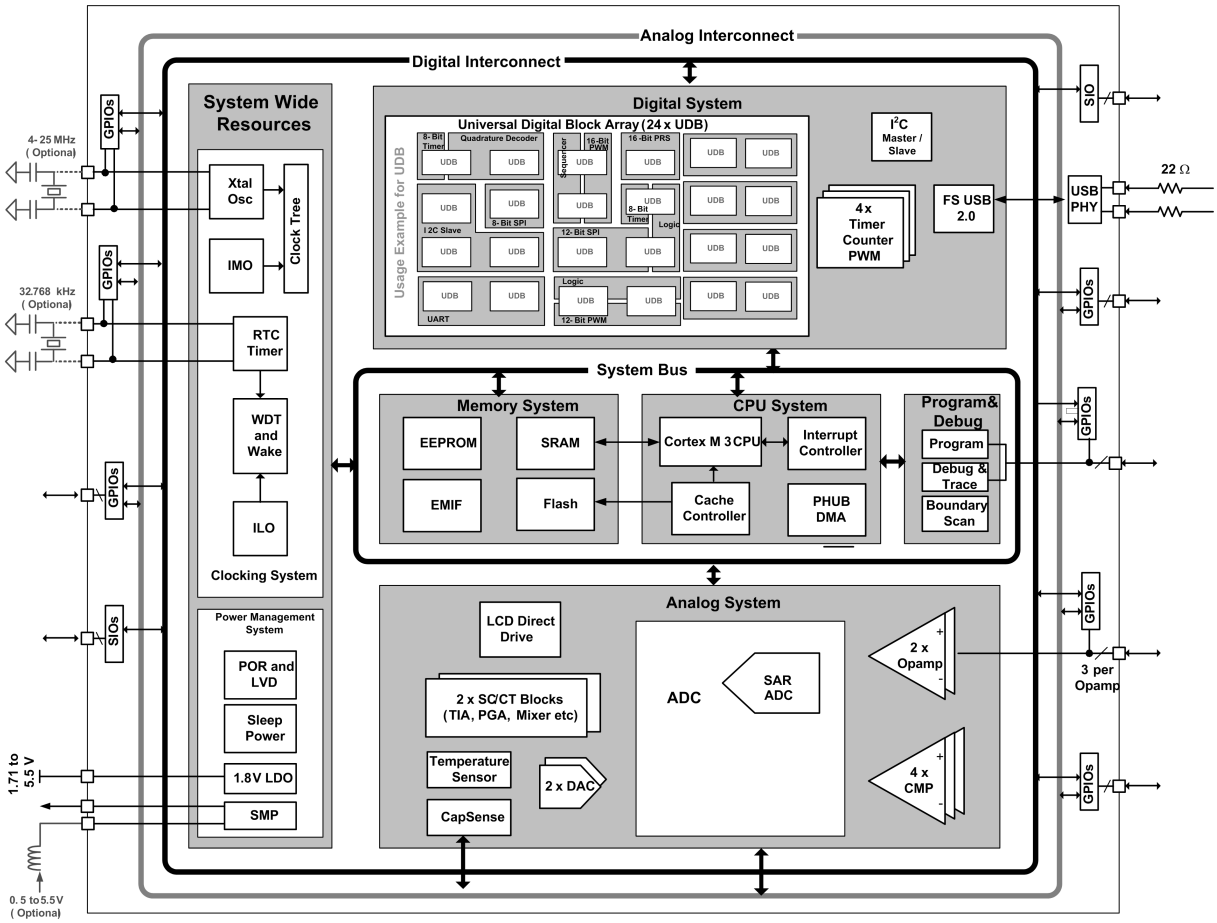


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C5488AXI-LP120
Package Name	100-TQFP
Architecture	PSoC 5
Family	CY8C54LP
CPU speed (MHz)	80
Flash size (kBytes)	256
SRAM size (kBytes)	64
EEPROM size (Bytes)	2048
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x2E178069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

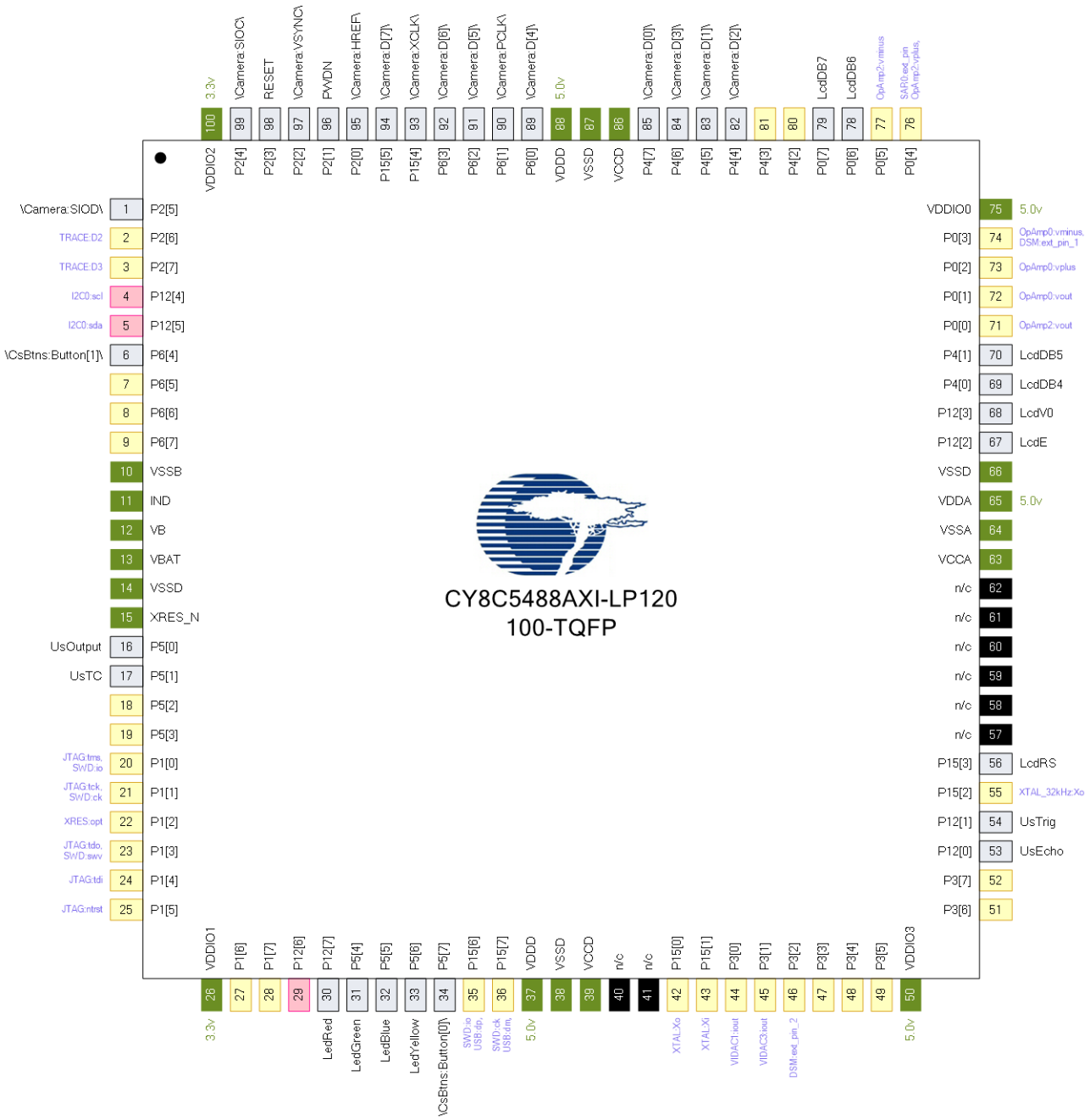
Table 2. Device Resources

Name	In Use	Free	Total Resources Available	% in Use
Digital clock dividers	5	3	8	62.5%
Analog clock dividers	0	4	4	0.0%
Pins	33	39	72	45.8%
UDB Macrocells	19	173	192	9.9%
UDB Unique Pterms	25	359	384	6.5%
UDB Datapath Cells	5	19	24	20.8%
UDB Status Cells	3	21	24	12.5%
UDB Control Cells	3	21	24	12.5%
DMA Channels	1	23	24	4.2%
Interrupts	4	28	32	12.5%
VIDAC Fixed Blocks	0	2	2	0.0%
SC Fixed Blocks	0	2	2	0.0%
Comparator Fixed Blocks	0	4	4	0.0%
Opamp Fixed Blocks	0	2	2	0.0%
CapSense Buffers	0	2	2	0.0%
I2C Fixed Blocks	1	0	1	100.0%
Timer Fixed Blocks	1	3	4	25.0%
USB Fixed Blocks	0	1	1	0.0%
LCD Fixed Blocks	0	1	1	0.0%
EMIF Fixed Blocks	0	1	1	0.0%
LPF Fixed Blocks	0	2	2	0.0%
SAR Fixed Blocks	0	1	1	0.0%

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	\Camera:SIOD\	Dgtl I/O	OD, DL	HiZ Analog Unb
2	P2[6]	GPIO [unused]			HiZ Analog Unb
3	P2[7]	GPIO [unused]			HiZ Analog Unb
4	P12[4]	SIO [unused]			HiZ Analog Unb
5	P12[5]	SIO [unused]			HiZ Analog Unb
6	P6[4]	\CsBtns:Button[1]\	Dgtl I/O	Res pull down	HiZ Analog Unb
7	P6[5]	GPIO [unused]			HiZ Analog Unb
8	P6[6]	GPIO [unused]			HiZ Analog Unb
9	P6[7]	GPIO [unused]			HiZ Analog Unb
10	VSSB	VSSB	Dedicated		
11	IND	IND	Dedicated		
12	VB	VB	Dedicated		
13	VBAT	VBAT	Dedicated		
14	VSSD	VSSD	Power		
15	XRES_N	XRES_N	Dedicated		
16	P5[0]	UsOutput	Dgtl Out	Strong drive	HiZ Analog Unb
17	P5[1]	UsTC	Dgtl Out	Strong drive	HiZ Analog Unb
18	P5[2]	GPIO [unused]			HiZ Analog Unb
19	P5[3]	GPIO [unused]			HiZ Analog Unb
20	P1[0]	GPIO [unused]			HiZ Analog Unb
21	P1[1]	GPIO [unused]			HiZ Analog Unb
22	P1[2]	GPIO [unused]			HiZ Analog Unb
23	P1[3]	GPIO [unused]			HiZ Analog Unb
24	P1[4]	GPIO [unused]			HiZ Analog Unb
25	P1[5]	GPIO [unused]			HiZ Analog Unb
26	VDDIO1	VDDIO1	Power		
27	P1[6]	GPIO [unused]			HiZ Analog Unb
28	P1[7]	GPIO [unused]			HiZ Analog Unb
29	P12[6]	SIO [unused]			HiZ Analog Unb
30	P12[7]	LedRed	Software Output	Strong drive	HiZ Analog Unb
31	P5[4]	LedGreen	Software Output	Strong drive	HiZ Analog Unb
32	P5[5]	LedBlue	Software Output	Strong drive	HiZ Analog Unb
33	P5[6]	LedYellow	Software Output	Strong drive	HiZ Analog Unb
34	P5[7]	\CsBtns:Button[0]\	Dgtl I/O	Res pull down	HiZ Analog Unb
35	P15[6]	USB IO [unused]			HiZ Analog Unb
36	P15[7]	USB IO [unused]			HiZ Analog Unb
37	VDDD	VDDD	Power		
38	VSSD	VSSD	Power		
39	VCCD	VCCD	Power		
42	P15[0]	GPIO [unused]			HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
43	P15[1]	GPIO [unused]			HiZ Analog Unb
44	P3[0]	GPIO [unused]			HiZ Analog Unb
45	P3[1]	GPIO [unused]			HiZ Analog Unb
46	P3[2]	GPIO [unused]			HiZ Analog Unb
47	P3[3]	GPIO [unused]			HiZ Analog Unb
48	P3[4]	GPIO [unused]			HiZ Analog Unb
49	P3[5]	GPIO [unused]			HiZ Analog Unb
50	VDDIO3	VDDIO3	Power		
51	P3[6]	GPIO [unused]			HiZ Analog Unb
52	P3[7]	GPIO [unused]			HiZ Analog Unb
53	P12[0]	UsEcho	Dgtl In	HiZ digital	HiZ Analog Unb
54	P12[1]	UsTrig	Dgtl Out	Strong drive	HiZ Analog Unb
55	P15[2]	GPIO [unused]			HiZ Analog Unb
56	P15[3]	LcdRS	Dgtl Out	Strong drive	HiZ Analog Unb
63	VCCA	VCCA	Power		
64	VSSA	VSSA	Power		
65	VDDA	VDDA	Power		
66	VSSD	VSSD	Power		
67	P12[2]	LcdE	Dgtl Out	Strong drive	HiZ Analog Unb
68	P12[3]	LcdV0	Dgtl Out	Strong drive	HiZ Analog Unb
69	P4[0]	LcdDB4	Dgtl Out	Strong drive	HiZ Analog Unb
70	P4[1]	LcdDB5	Dgtl Out	Strong drive	HiZ Analog Unb
71	P0[0]	GPIO [unused]			HiZ Analog Unb
72	P0[1]	GPIO [unused]			HiZ Analog Unb
73	P0[2]	GPIO [unused]			HiZ Analog Unb
74	P0[3]	GPIO [unused]			HiZ Analog Unb
75	VDDIO0	VDDIO0	Power		
76	P0[4]	GPIO [unused]			HiZ Analog Unb
77	P0[5]	GPIO [unused]			HiZ Analog Unb
78	P0[6]	LcdDB6	Dgtl Out	Strong drive	HiZ Analog Unb
79	P0[7]	LcdDB7	Dgtl Out	Strong drive	HiZ Analog Unb
80	P4[2]	GPIO [unused]			HiZ Analog Unb
81	P4[3]	GPIO [unused]			HiZ Analog Unb
82	P4[4]	\Camera:D[2]\	Dgtl In	HiZ digital	HiZ Analog Unb
83	P4[5]	\Camera:D[1]\	Dgtl In	HiZ digital	HiZ Analog Unb
84	P4[6]	\Camera:D[3]\	Dgtl In	HiZ digital	HiZ Analog Unb
85	P4[7]	\Camera:D[0]\	Dgtl In	HiZ digital	HiZ Analog Unb
86	VCCD	VCCD	Power		
87	VSSD	VSSD	Power		
88	VDDD	VDDD	Power		
89	P6[0]	\Camera:D[4]\	Dgtl In	HiZ digital	HiZ Analog Unb
90	P6[1]	\Camera:PCLK\	Dgtl In	HiZ digital	HiZ Analog Unb
91	P6[2]	\Camera:D[5]\	Dgtl In	HiZ digital	HiZ Analog Unb
92	P6[3]	\Camera:D[6]\	Dgtl In	HiZ digital	HiZ Analog Unb
93	P15[4]	\Camera:XCLK\	Dgtl Out	Strong drive	HiZ Analog Unb
94	P15[5]	\Camera:D[7]\	Dgtl In	HiZ digital	HiZ Analog Unb
95	P2[0]	\Camera:HREF\	Dgtl In	HiZ digital	HiZ Analog Unb
96	P2[1]	PWDN	Software Output	Strong drive	HiZ Analog Unb
97	P2[2]	\Camera:VSYNC\	Software Input	HiZ digital	HiZ Analog Unb
98	P2[3]	RESET	Software Output	Strong drive	HiZ Analog Unb
99	P2[4]	\Camera:SIOC\	Dgtl I/O	OD, DL	HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
100	VDDIO2	VDDIO2	Power		

Abbreviations used in Table 3 have the following meanings:

- Dgtl I/O = Digital In/Out
- OD, DL = Open drain, drives low
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Res pull down = Resistive pull down
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- HiZ digital = High impedance digital

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	71	GPIO [unused]			HiZ Analog Unb
P0[1]	72	GPIO [unused]			HiZ Analog Unb
P0[2]	73	GPIO [unused]			HiZ Analog Unb
P0[3]	74	GPIO [unused]			HiZ Analog Unb
P0[4]	76	GPIO [unused]			HiZ Analog Unb
P0[5]	77	GPIO [unused]			HiZ Analog Unb
P0[6]	78	LcdDB6	Dgtl Out	Strong drive	HiZ Analog Unb
P0[7]	79	LcdDB7	Dgtl Out	Strong drive	HiZ Analog Unb
P1[0]	20	GPIO [unused]			HiZ Analog Unb
P1[1]	21	GPIO [unused]			HiZ Analog Unb
P1[2]	22	GPIO [unused]			HiZ Analog Unb
P1[3]	23	GPIO [unused]			HiZ Analog Unb
P1[4]	24	GPIO [unused]			HiZ Analog Unb
P1[5]	25	GPIO [unused]			HiZ Analog Unb
P1[6]	27	GPIO [unused]			HiZ Analog Unb
P1[7]	28	GPIO [unused]			HiZ Analog Unb
P12[0]	53	UsEcho	Dgtl In	HiZ digital	HiZ Analog Unb
P12[1]	54	UsTrig	Dgtl Out	Strong drive	HiZ Analog Unb
P12[2]	67	LcdE	Dgtl Out	Strong drive	HiZ Analog Unb
P12[3]	68	LcdV0	Dgtl Out	Strong drive	HiZ Analog Unb
P12[4]	4	SIO [unused]			HiZ Analog Unb
P12[5]	5	SIO [unused]			HiZ Analog Unb
P12[6]	29	SIO [unused]			HiZ Analog Unb
P12[7]	30	LedRed	Software Output	Strong drive	HiZ Analog Unb
P15[0]	42	GPIO [unused]			HiZ Analog Unb
P15[1]	43	GPIO [unused]			HiZ Analog Unb
P15[2]	55	GPIO [unused]			HiZ Analog Unb
P15[3]	56	LcdRS	Dgtl Out	Strong drive	HiZ Analog Unb
P15[4]	93	\Camera:XCLK\	Dgtl Out	Strong drive	HiZ Analog Unb
P15[5]	94	\Camera:D[7]\	Dgtl In	HiZ digital	HiZ Analog Unb
P15[6]	35	USB IO [unused]			HiZ Analog Unb
P15[7]	36	USB IO [unused]			HiZ Analog Unb
P2[0]	95	\Camera:HREF\	Dgtl In	HiZ digital	HiZ Analog Unb
P2[1]	96	PWDN	Software Output	Strong drive	HiZ Analog Unb
P2[2]	97	\Camera:VSYNC\	Software Input	HiZ digital	HiZ Analog Unb
P2[3]	98	RESET	Software Output	Strong drive	HiZ Analog Unb
P2[4]	99	\Camera:SIOC\	Dgtl I/O	OD, DL	HiZ Analog Unb
P2[5]	1	\Camera:SIOD\	Dgtl I/O	OD, DL	HiZ Analog Unb
P2[6]	2	GPIO [unused]			HiZ Analog Unb
P2[7]	3	GPIO [unused]			HiZ Analog Unb
P3[0]	44	GPIO [unused]			HiZ Analog Unb
P3[1]	45	GPIO [unused]			HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P3[2]	46	GPIO [unused]			HiZ Analog Unb
P3[3]	47	GPIO [unused]			HiZ Analog Unb
P3[4]	48	GPIO [unused]			HiZ Analog Unb
P3[5]	49	GPIO [unused]			HiZ Analog Unb
P3[6]	51	GPIO [unused]			HiZ Analog Unb
P3[7]	52	GPIO [unused]			HiZ Analog Unb
P4[0]	69	LcdDB4	Dgtl Out	Strong drive	HiZ Analog Unb
P4[1]	70	LcdDB5	Dgtl Out	Strong drive	HiZ Analog Unb
P4[2]	80	GPIO [unused]			HiZ Analog Unb
P4[3]	81	GPIO [unused]			HiZ Analog Unb
P4[4]	82	\Camera:D[2]\	Dgtl In	HiZ digital	HiZ Analog Unb
P4[5]	83	\Camera:D[1]\	Dgtl In	HiZ digital	HiZ Analog Unb
P4[6]	84	\Camera:D[3]\	Dgtl In	HiZ digital	HiZ Analog Unb
P4[7]	85	\Camera:D[0]\	Dgtl In	HiZ digital	HiZ Analog Unb
P5[0]	16	UsOutput	Dgtl Out	Strong drive	HiZ Analog Unb
P5[1]	17	UsTC	Dgtl Out	Strong drive	HiZ Analog Unb
P5[2]	18	GPIO [unused]			HiZ Analog Unb
P5[3]	19	GPIO [unused]			HiZ Analog Unb
P5[4]	31	LedGreen	Software Output	Strong drive	HiZ Analog Unb
P5[5]	32	LedBlue	Software Output	Strong drive	HiZ Analog Unb
P5[6]	33	LedYellow	Software Output	Strong drive	HiZ Analog Unb
P5[7]	34	\CsBtns:Button[0]\	Dgtl I/O	Res pull down	HiZ Analog Unb
P6[0]	89	\Camera:D[4]\	Dgtl In	HiZ digital	HiZ Analog Unb
P6[1]	90	\Camera:PCLK\	Dgtl In	HiZ digital	HiZ Analog Unb
P6[2]	91	\Camera:D[5]\	Dgtl In	HiZ digital	HiZ Analog Unb
P6[3]	92	\Camera:D[6]\	Dgtl In	HiZ digital	HiZ Analog Unb
P6[4]	6	\CsBtns:Button[1]\	Dgtl I/O	Res pull down	HiZ Analog Unb
P6[5]	7	GPIO [unused]			HiZ Analog Unb
P6[6]	8	GPIO [unused]			HiZ Analog Unb
P6[7]	9	GPIO [unused]			HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl I/O = Digital In/Out
- OD, DL = Open drain, drives low
- Res pull down = Resistive pull down

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
\Camera:D[0]\	P4[7]	Dgtl In	HiZ Analog Unb
\Camera:D[1]\	P4[5]	Dgtl In	HiZ Analog Unb
\Camera:D[2]\	P4[4]	Dgtl In	HiZ Analog Unb
\Camera:D[3]\	P4[6]	Dgtl In	HiZ Analog Unb
\Camera:D[4]\	P6[0]	Dgtl In	HiZ Analog Unb
\Camera:D[5]\	P6[2]	Dgtl In	HiZ Analog Unb
\Camera:D[6]\	P6[3]	Dgtl In	HiZ Analog Unb
\Camera:D[7]\	P15[5]	Dgtl In	HiZ Analog Unb
\Camera:HREF\	P2[0]	Dgtl In	HiZ Analog Unb
\Camera:PCLK\	P6[1]	Dgtl In	HiZ Analog Unb
\Camera:SIOC\	P2[4]	Dgtl I/O	HiZ Analog Unb
\Camera:SIOD\	P2[5]	Dgtl I/O	HiZ Analog Unb
\Camera:VSYNC\	P2[2]	Software Input	HiZ Analog Unb
\Camera:XCLK\	P15[4]	Dgtl Out	HiZ Analog Unb
\CsBtns:Button[0]\	P5[7]	Dgtl I/O	HiZ Analog Unb
\CsBtns:Button[1]\	P6[4]	Dgtl I/O	HiZ Analog Unb
LcdDB4	P4[0]	Dgtl Out	HiZ Analog Unb
LcdDB5	P4[1]	Dgtl Out	HiZ Analog Unb
LcdDB6	P0[6]	Dgtl Out	HiZ Analog Unb
LcdDB7	P0[7]	Dgtl Out	HiZ Analog Unb
LcdE	P12[2]	Dgtl Out	HiZ Analog Unb
LcdRS	P15[3]	Dgtl Out	HiZ Analog Unb
LcdV0	P12[3]	Dgtl Out	HiZ Analog Unb
LedBlue	P5[5]	Software Output	HiZ Analog Unb
LedGreen	P5[4]	Software Output	HiZ Analog Unb
LedRed	P12[7]	Software Output	HiZ Analog Unb
LedYellow	P5[6]	Software Output	HiZ Analog Unb
PWDN	P2[1]	Software Output	HiZ Analog Unb
RESET	P2[3]	Software Output	HiZ Analog Unb
UsEcho	P12[0]	Dgtl In	HiZ Analog Unb
UsOutput	P5[0]	Dgtl Out	HiZ Analog Unb
UsTC	P5[1]	Dgtl Out	HiZ Analog Unb
UsTrig	P12[1]	Dgtl Out	HiZ Analog Unb

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl I/O = Digital In/Out
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x80
Stack Size (bytes)	0x0800
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	GPIO
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

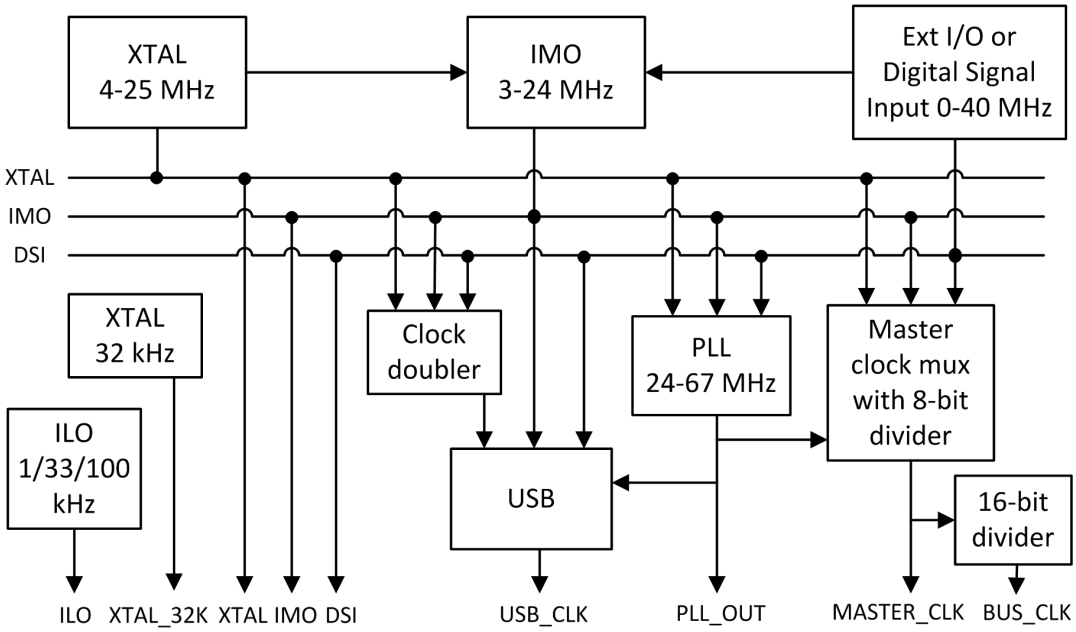
Name	Value
Variable VDDA	False
VDDA (V)	5.0
VDDD (V)	5.0
VDDIO0 (V)	5.0
VDDIO1 (V)	3.3
VDDIO2 (V)	3.3
VDDIO3 (V)	5.0
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 74.7 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	24 MHz	±1	True	True
PLL_OUT	DIGITAL	IMO	24 MHz	24 MHz	±1	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	24 MHz	±1	True	True
IMO	DIGITAL		3 MHz	3 MHz	±1	True	True
ILO	DIGITAL		? MHz	1 kHz	-50,+100	True	True
USB_CLK	DIGITAL	IMO	48 MHz	? MHz	±0	False	False
XTAL	DIGITAL		24 MHz	? MHz	±0	False	False
XTAL 32kHz	DIGITAL		32.768 kHz	? MHz	±0	False	False
Digital Signal	DIGITAL		? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

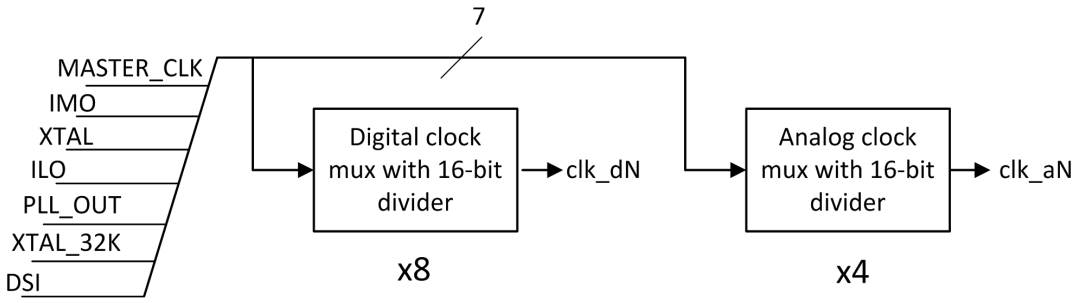


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
ClockCamera	DIGITAL	MASTER_CLK	24 MHz	24 MHz	±1	True	True
Camera_I2C_-BusClock	DIGITAL	BUS_CLK	? MHz	24 MHz	±1	True	True
ClockCsBtns	DIGITAL	MASTER_CLK	12 MHz	12 MHz	±1	True	True
ClockUsPWM	DIGITAL	MASTER_CLK	6 MHz	6 MHz	±1	True	True
Clock_1	DIGITAL	MASTER_CLK	1 MHz	1 MHz	±1	True	True
ClockLcdBac-klight	DIGITAL	MASTER_CLK	10 kHz	10 kHz	±1	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5 Technical Reference Manual

- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines
  - CyMaster API routines
  - CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Priority	Vector
Camera_I2C_I2C_IRQ	7	15
IsrBtn0Pressed	7	0
IsrBtn1Pressed	7	1
IsrUsTimer	7	2

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains the following DMA components: (0 is the highest priority)

Table 12. DMAs

Name	Priority	Channel Number
Camera_DMA	2	0

For more information on DMAs, please refer to:

- PHUB and DMAC chapter in the PSoC 5 Technical Reference Manual
- DMA chapter in the System Reference Guide
  - DMA API routines and related registers
- Datasheet for cy_dma component

6 Flash Memory

PSoC 5 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 13 lists the Flash protection settings for your design.

Table 13. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

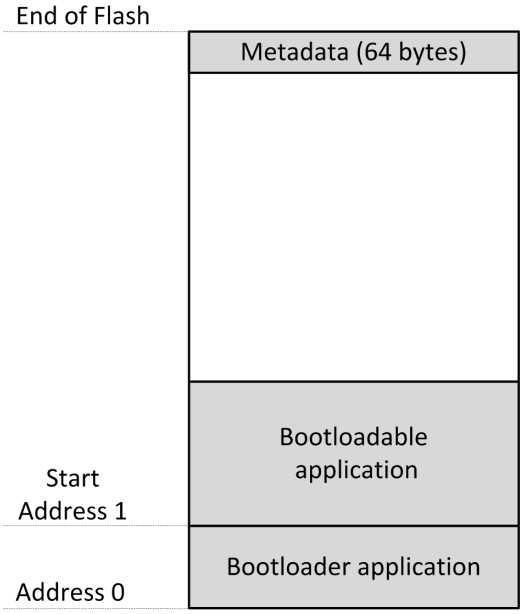
For more information on Flash memory and protection, please refer to:

- Flash Protection chapter in the PSoC 5 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Bootloader and Bootloadable

Figure 5 details the Flash memory map for the bootloader and/or bootloadable application(s) included in this design.

Figure 5. Bootloader Memory Map



7.1 Bootloadable Application

Table 14. Bootloadable Settings

Name	Value
Application Version	0x0000
Application ID	0x0000
Application Custom ID	0x0
Application Image 1 Start Address	0x2800
Application Image 1 End Address	0x3FEFF
Manual Application Image Placement	False

7.2 Bootloader Application

Table 15. Bootloader Settings

Name	Value
Checksum Type	BasicChecksum
Supports Multiple Application Images	False
Application Version	0x0000
Bootloader Start Address	0x0
Bootloader End Address	0x2720

For more information on the bootloader and startup please refer to:

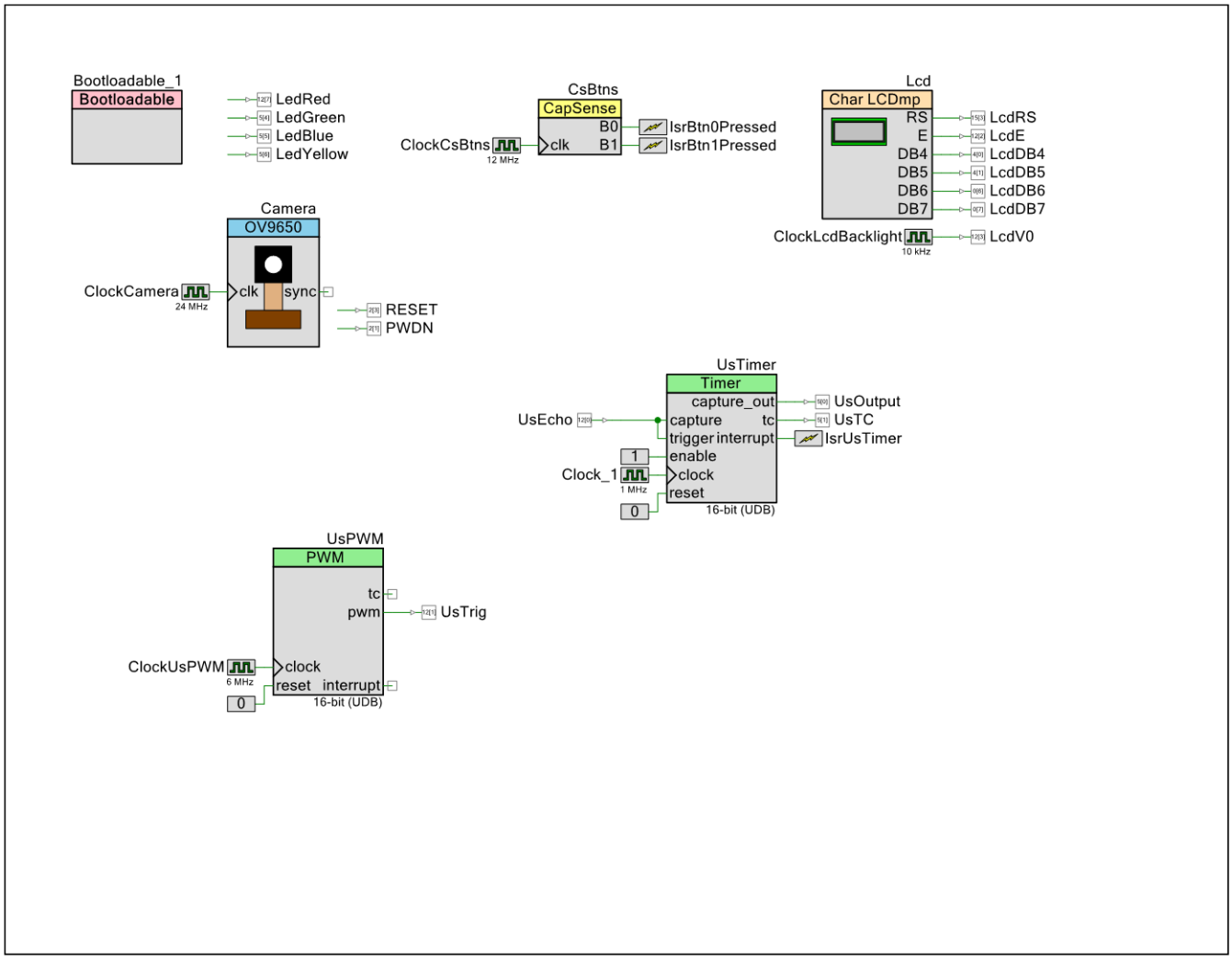
- Startup and Linking chapter in the System Reference Guide
- Datasheet for Bootloader and Bootloadable component

8 Design Contents

This design's schematic content consists of the following schematic sheet:

8.1 Schematic Sheet: Page 1

Figure 6. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance Bootloadable_1 (type: Bootloadable_v1_30)
- Instance Camera (type: OV9650)
- Instance CsBtns (type: CapSense_Simple)
- Instance Lcd (type: CharLCDmp_v1_2)
- Instance UsPWM (type: PWM_v3_30)
- Instance UsTimer (type: Timer_v2_70)

9 Components

9.1 Component type: Bootloadable [v1.30]

9.1.1 Instance Bootloadable_1

Description: Provides bootloadable application functionality.
Instance type: Bootloadable [v1.30]
Datasheet: online component datasheet for Bootloadable

Table 16. Component Parameters for Bootloadable_1

Parameter Name	Value	Description
appCustomID	0	Provides a 4 byte custom ID number to represent anything in the Bootloadable application.
appID	0	Provides a 2 byte number to represent the ID of the bootloadable application.
appVersion	0	Provides a 2 byte number to represent the version of the bootloadable application.
autoPlacement	true	Provides a method for PSoC Creator to place a Bootloadable application image at a specified location. If true, the image will be placed automatically. If false, the image will be placed at an address specified by the Placement Address option.
elfFilePath	..\..\..\..\Glomerida\bootloader.elf	Provides a reference to the Bootloader application (.elf) that is associated with this Bootloadable application.
hexFilePath	..\..\..\..\Glomerid-a\bootloader.hex	Provides a reference to the Bootloader application (.hex) that is associated with this Bootloadable application.
placementAddress	0	Allows specifying an address where the bootloadable application will be placed in the memory. Available only if the Automatic Application Image Placement option is true.

9.2 Component type: CapSense_Simple [v0.0]

9.2.1 Instance CsBtns

Description: (custom component)
Instance type: CapSense_Simple [v0.0]
Datasheet: (not available)

9.3 Component type: CharLCDmp [v1.2]

9.3.1 Instance Lcd

Description: Character LCD (mp) Component
Instance type: CharLCDmp [v1.2]
Datasheet: online component datasheet for CharLCDmp

Table 17. Component Parameters for Lcd

Parameter Name	Value	Description
ConversionRoutines	true	Defines if the conversion routines will be included in the project.
CUSTOM0	0,E,8,8,8,E,0	Defines encoded representation of first custom character of the user-defined font.
CUSTOM1	0,A,A,4,4,4,0	Defines encoded representation of second custom character of the user-defined font.
CUSTOM2	0,E,A,E,8,8,0	Defines encoded representation of third custom character of the user-defined font.
CUSTOM3	0,E,A,C,A,A,0	Defines encoded representation of fourth custom character of the user-defined font.
CUSTOM4	0,E,8,C,8,E,0	Defines encoded representation of fifth custom character of the user-defined font.
CUSTOM5	0,E,8,E,2,E,0	Defines encoded representation of sixth custom character of the user-defined font.
CUSTOM6	0,E,8,E,2,E,0	Defines encoded representation of seventh custom character of the user-defined font.
CUSTOM7	0,4,4,4,0,4,0	Defines encoded representation of eighth custom character of the user-defined font.
CustomCharacterSet	None	Defines the type of custom character set (User defined, Vertical or Horizontal bargraph). Based on the selection a look-up table with proper characters representation will be generated in the source code.

9.4 Component type: OV9650 [v0.0]

9.4.1 Instance Camera

Description: (custom component)
Instance type: OV9650 [v0.0]
Datasheet: (not available)

9.5 Component type: PWM [v3.30]

9.5.1 Instance UsPWM

Description: 8 or 16-bit Pulse Width Modulator
Instance type: PWM [v3.30]
Datasheet: online component datasheet for PWM

Table 18. Component Parameters for UsPWM

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO.
CompareStatusEdgeSense	true	Enables edge sense detection on compare outputs for use in edge sensitive interrupts
CompareType1	Less	Sets the compare value comparison type setting for the compare 1 output
CompareType2	Less	Sets the compare value comparison type setting for the compare 2 output
CompareValue1	60	Compares Output 1 to value
CompareValue2	63	Compares Output 2 to value
DeadBand	Disabled	Defines whether dead band outputs are desired or not.
DeadTime	1	Defines the number of required dead band clock cycles
DitherOffset	0.00	Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM.
EnableMode	Software Only	Specifies the method of enabling the PWM. This can be either hardware or software.
FixedFunction	false	Determines whether the fixed function counter timer is used or the UDB implementation is used.
InterruptOnCMP1	false	Enables the interrupt on compare1 true event
InterruptOnCMP2	false	Enables the interrupt on compare2 true event
InterruptOnKill	false	Enables the interrupt on a kill event
InterruptOnTC	false	Enables the interrupt on terminal count event
KillMode	Disabled	Parameter to select the kill mode for build time.
MinimumKillTime	1	Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode
Period	65535	Defines the PWM period value
PWMMode	One Output	Defines the overall mode of the PWM
Resolution	16	Defines the bit width of the PWM (8 or 16 bits)
RunMode	Continuous	Defines the run mode options to be either continuous or one shot
TriggerMode	None	Determines the mode of starting the PWM, i.e. triggering the PWM counter to start
UseInterrupt	true	Enables the placement and usage of the status register

9.6 Component type: Timer [v2.70]

9.6.1 Instance UsTimer

Description: 8, 16, 24 or 32-bit Timer
Instance type: Timer [v2.70]
Datasheet: online component datasheet for Timer

Table 19. Component Parameters for UsTimer

Parameter Name	Value	Description
CaptureAlternatingFall	false	Enables data capture on either edge but not until a valid falling edge is detected first.
CaptureAlternatingRise	false	Enables data capture on either edge but not until a valid rising edge is detected first.
CaptureCount	2	The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed.
CaptureCounterEnabled	false	Enables the capture counter to count capture events (up to 127) before a capture is triggered.
CaptureMode	Falling Edge	This parameter defines the capture input signal requirements to trigger a valid capture event
EnableMode	Software and Hardware	This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled.
FixedFunction	false	Configures the component to use fixed function HW block instead of the UDB implementation.
InterruptOnCapture	true	Parameter to check whether interrupt on a capture event is enabled or disabled.
InterruptOnFIFOFull	false	Parameter to check whether interrupt on a FIFO Full event is enabled disabled.
InterruptOnTC	false	Parameter to check whether interrupt on a TC is enabled or disabled.
NumberOfCaptures	1	Number of captures allowed until the counter is cleared or disabled.
Period	37999	Defines the timer period (This is also the reload value when terminal count is reached)

Parameter Name	Value	Description
Resolution	16	Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals.
RunMode	Continuous	Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered.
TriggerMode	Rising Edge	Defines the required trigger input signal to cause a valid trigger enable of the timer

10 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5 register map is covered in the PSoC 5 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5 Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine