CMPE 110 Homework #3

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1. **Question #1 - Basic Cache**

Consider a 512-KByte cache with 32 word cache lines.This cache uses write-back scheme, and the address is 32 bits wide. (The three tables for parts A, B, and C have been condensed into a single table found below part C).

Note - Since it is not stated, I am assuming that the lower 2 bits are hard-coded as `00`, which means all accesses are word-aligned. I am also including both the word offset and byte offset in my calculation of cacheline offset, as we are supposed to do as stated in question 436 on Piazza.

(a) **Question 1.A Direct-Mapped, Cache fields** Assume the cache is direct mapped. Fill in the table below to specify the size of each address field.

Explanation - For a direct-mapped cache, we need to have a 5-bit word offset because each cache-line is 32 words wide, we then need the 2 hard-coded bits to account for byte offset within each word, for a total of 7 bits for cacheline offset. Since our cache is 52-KByte large, and each line is 32 words, we have 4,096 cache lines. The amount of bits needed to address this amount of cache-lines is 12 ($2^{12} = 4,096$). This leaves 13 bits for the tag.

(b) **Question 1.B Fully Associative Cache Fields**
Assume the cache is fully associative, fill in the table below to specify the size of each address field.

Explanation - For a fully-associative cache, we still need 7 bits for the offset, which determines which of the 32 words in a cache-line our data is stored at. Since fully-associative caches do not use an index, this leaves 25 bits left for the tag.

(c) **Question 1.C 8-Way Set-Associative, Cache Fields**
Assume the cache is 8-way associative, fill in the table below to specify the size of each address field.

Explanation - Once again, we need 7 bits for the offset because each cache-line is 32-words wide. With 512Kbyte of memory and an 8-way set-associative cache, we will need 11 bits to state which set we are looking for ($2^9 = 4,096/8$). Finally we have 16 bits left to form the tag.

Table 1: Q 1A, 1B, and 1C Calculations

Field	Size (1A)	Size (1B)	Size (1C)
Cache line offset	7	7	7
Cache line index	12	0	9
Tag	13	25	16

(d) **Question 1.D Direct Mapped Cache Transactions**

Assume the cache is direct-mapped. Fill in the table on the next page to identify the content of the cache after each of the following memory accesses. Assume the cache is initially empty (aka cold). Specify if an entry causes another line to be replaced from the cache, and if an entry has to write its data back to memory. For the data column, specify the data in the block by referring to its address like M[address]

Table 2: Q1D Calculations

Address	Request	Cacheline Ind	Valid	Modified	Tag	Data	Caused Replace	Write-back?
0x128	read	2	0	0	0	M[0x100]	0	0
0xF40	write	30	0	0	0	D[0xF00]	0	0
0xC00024	read	0	0	0	24	M[0xC00000]	0	0
0x014	write	0	1	0	0	D[0x000]	1	0
0x100F44	read	30	1	0	2	D[0x100F00]	1	1

Explanation -

(e) **Question 1.E 8-Way Set Associative, Cache Transactions**
Assume the cache is 8-way set-associative. Fill the table below to identify the content of the cache after each of the following memory accesses. Assume the cache is empty in the beginning (also known as cold cache). Specify if an entry causes another line to be replaced from the cache, and if an entry has to write its data back to memory. For the data column, specify the data in the block by referring to its address like M[address]. Write accesses will modify the data, so lets indicate the data after a write access with D[address].

Table 3: Q1D Calculations

Address	Request	Cacheline Ind	Valid	Modified	Tag	Data	Caused Replace	Write-back?
0x128	read	2	0	0	0	M[0x100]	0	0
0xF40	write	30	0	0	0	D[0xF00]	0	0
0xC00024	read	0	0	0	96	M[0xC00000]	0	0
0x014	write	0	1	0	0	D[0x000]	0	0
0x100F44	read	30	1	0	16	D[0x100F00]	0	0

2. **Question #2 -**

   (a) **Question 2.A**
   (b) **Question 2.B**

3. **Question #3 : CPI Changes**

   (a)

4. **Question #4 :**

   (a) nothing

5. **Question #5 : Multipliers**

   (a) nothing

6. **Question #6 : Hazards**

   (a) nothing