

CMPE 110 Homework #1

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1. Question #1 - Power

- (a) Question #1A : ‘...However, we discussed that nowadays power density and heat has become an issue preventing scaling of frequency. Discuss why power and temperature are becoming an issue’.

Answer :

- (b) Question #1B : Given the rough formulations governing power and frequency for each voltage region, discuss which region (consider Near and Super-threshold only) is more energy efficient.

Answer : To start, we will make the following assumptions :

Near-threshold voltage = $V_{nth} = k$, Super-threshold voltage = $V_{sth} = 2k : k \in \mathbb{R}^+$

Power $\propto V^3$, Delay $\propto \frac{1}{V}$, Energy \propto Power \times Delay

Energy Efficiency \propto Energy \times Delay = Power \times Delay²

The energy efficiency can then be calculated for both the near and super threshold voltage levels, as shown below.

Table 1: Efficiency Calculations

Near-Threshold	Super-Threshold
$P_{nth} = V_{nth}^3 = k^3$	$P_{sth} = V_{sth}^3 = (2k)^3 = 8k$
$D_{nth} = \frac{1}{V_{nth}} = \frac{1}{k}$	$D_{sth} = \frac{1}{2k}$
$E_{nth} = P_{nth} * D_{nth} = \frac{k^3}{k} = k^2$	$E_{sth} = P_{sth} * D_{sth} = \frac{8k^3}{2k} = 4k^2$
$EE_{nth} = E_{nth} * D_{nth} = \frac{k^2}{k} = k$	$EE_{sth} = E_{sth} * D_{sth} = \frac{4k^2}{2k} = 2k$

Thus voltage levels that are near the threshold are more energy efficient.

2. Question #2 Computing ISA's

Table 2: Question #2 Answers

Architecture	Bytes in Program	Bytes Fetched	Bytes Loaded	Bytes Stored
x86	13	89	40	40
MIPS	32	248	40	40
Stack ISA	24	195	20	20

- (a) Question #2A x86 CISC ISA

Fill out the first row of the above table (from the handout), but assume 32-bit data values.

Answer : (See Table #2, row #1)

Exaplanation - There are 13 bytes in the program, we know this by summing the 6 instructions by there byte count. 89 bytes fetches is determined by tracing the routine through 10 iterations plus the initializing instructions. Bytes loaded and Bytes stored all come from the `inc(ra, rb, imm)` instruction, which loads and stores 4 bytes for each of the 10 calls.

- (b) Question #2B MIPS RISC ISA

Write the assembly code that would generate if the C code were compiled on a machine that uses the MIPS ISA. Fill out the second row of the above table.

Answer :

r1 is the counter variable. r2 contains the size variable (10). r3 contains the address of the first item in the array.

```
        subu r1, r1, r1    # initialize counter to zero
        j CMPR             # jump to comparison
LOOP:   lw r4, r3           # load current array value
        addiu r4, r4, #1   # increment current array value
        sw r4, r3          # store the incremented value
        addiu r3, r3, #4   # move to the next index in the array
        addiu r1, r1, #1   # increment the counter
CMPR:   bne r1, r2, #-6    # compare counter with size, loop again if !=
```

Explanation - The second row table values were calculated as follows. There are 8 instructions in the program, consisting of a constant 4 bytes each, giving 32 total bytes. There are 6 instructions inside of the loop, which iterates 10 times, giving $6 \times 4 \times 10$ bytes fetched for the loop, plus the 2 instructions before the loop. This totals 248 bytes fetched. 40 bytes are loaded and stored as is the same with the x86 code, 4 bytes for each iteration of the loop.

(c) Question #2C STACK ISA

Write the assembly code that would generate if the C code were compiled on a machine that uses this stack-based architecture. Assume that going into the code, that the top of stack contains size and the second entry in the stack contains aptr. Fill out the third row in the above table

Answer :

```
        goto CMPR         # Compare counter at stack top
LOOP:   swap              # put address at top of stack
        dup               # dup the address so popm doesn't destroy it
        pushm             # get array value at address on stack top
        pushi #1          # put 1 on stack
        add               # increment array value
        popm              # put inc'd value back at memory address
        pushi #2          # put 2 on stack
        add               # increment the address by 2 bytes
        swap              # put counter at the top, address at 2nd spot
        pushi #-1         # put -1 on stack
        add               # decrement the counter by 1
CMPR:   bgtz LOOP         # if counter not zero, loop again
```

Explanation - The third row table values were calculated as follows. There are 13 instructions in the program, summing up over their respective instruction lengths yields 24 bytes. Of these 24 bytes, 19 are inside of the loop, which iterates 10 times, which gives 190 bytes. Add in the 5 bytes to do this initial goto and you end up with 195 bytes fetched. The program performs 10 loads and 10 stores, each with 2 bytes, giving 20 bytes total load/stored.

(d) Question #2D COMPARISON

Compare the three ISAs studied with respect to static code size, number of instruction bytes fetched during execution, and memory traffic. Don't simply summarize the table but analyze what the numbers mean.

Answer :

For static code size, it makes sense that the x86 RISC ISA had a smaller code size than MIPS, because they are both 32-bit but the x86 ISA has variable length instructions, meaning it doesn't need to waste 4 bytes for instructions that need less. It also had the fewest lines of code because each line could accomplish so much. Compare this to the STACK ISA, which was much longer because each instruction only does a little bit of work. The static code size between MIPS ISA and the STACK ISA seems like it could go either way, MIPS instructions do more work, but each instruction is twice as large as the STACK ISA instructions, so depending on the complexity of the code it seems like either one could be bigger than the other.

For the bytes fetched, this parallels the static code size in a way. Because each of these functions has to do 10 iterations plus some outside work, each of the bytes fetched will be roughly proportional to ten times the static code size. The `x86` ISA fetched less than 10 times its static code size, because over $\frac{1}{3}$ of the bytes in the static code are outside of the loop, and thus are only executed once. The `MIPS` ISA and `STACK` ISA are a little closer to 10 times their static code size, because a larger proportion of the instructions are inside of the loop

For memory traffic, all of these different ISAs needed to do the same number of loads and stores, 10 each (one for each iteration). This means that the `MIPS` ISA and the `x86` ISA loaded and stored the same number of bytes, because they both work on 32-bit data values. The `STACK` ISA only works on 16 bit values, so it only had half as much traffic from the data memory.

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