PIC32CM JH00/JH01 Family Silicon Errata and Data Sheet Clarifications

PIC32CM JH00/JH01

PIC32CM JH00/JH01 Family Errata

The PIC32CM JH00/JH01 family of devices that you have received conforms functionally to the current Device Data Sheet (DS60001632), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in the Silicon Issues Summary.

The errata described in this document will be addressed in future revisions of the PIC32CM JH00/JH01 family of devices.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in 5. Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. PIC32CM JH00 Family Silicon Device Identification

Devices	Device ID (DID[31:0])	Silicon Revision ID (DID.REVISION[3:0])	
		B0	C0
PIC32CM5164JH00100	0x11060X0E	0x1	0x2
PIC32CM5164JH00064	0x11060X0F	0x1	0x2
PIC32CM5164JH00048	0x11060X14	0x1	0x2
PIC32CM5164JH00032	0x11060X15	0x1	0x2
PIC32CM2532JH00100	0x11060X0D	0x1	0x2
PIC32CM2532JH00064	0x11060X10	0x1	0x2
PIC32CM2532JH00048	0x11060X13	0x1	0x2
PIC32CM2532JH00032	0x11060X16	0x1	0x2

Table 2. PIC32CM JH01 Family Silicon Device Identification

Devices	Device ID (DID[31:0])	Silicon Revision ID (DID.REVISION[3:0])	
		B0	C0
PIC32CM5164JH01100	0x11060X00	0x1	0x2
PIC32CM5164JH01064	0x11060X01	0x1	0x2
PIC32CM5164JH01048	0x11060X02	0x1	0x2
PIC32CM5164JH01032	0x11060X03	0x1	0x2
PIC32CM2532JH01100	0x11060X04	0x1	0x2
PIC32CM2532JH01064	0x11060X05	0x1	0x2
PIC32CM2532JH01048	0x11060X06	0x1	0x2
PIC32CM2532JH01032	0x11060X07	0x1	0x2

Note:

1. Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS60001632) for a detailed information on Device Identification and Revision IDs for your specific device.

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1. Silicon Errata Summary

Table 1-1. Silicon Errata Summary

Module	Feature	Item #	Issue Summary	Affected Revisions	
				B0	C0
AC	Analog Pins	2.1.1	Analog pins are shared between PTC and AC module.	X	X
ADC	Offset Correction	2.2.1	Offset correction is not supported in the 8-bit and 10-bit conversion resolution.	X	X
ADC	Reference Buffer Offset	2.2.2	First ADC conversions are incorrect when using Reference Buffer Offset Compensation.	X	X
ADC	Sequence State	2.2.3	The SEQSTATUS register is not updated properly when exiting Standby mode by an ADC conversions sequence event.	X	X
CAN	On-demand Clock Source	2.3.1	The CAN is not compatible with an on-demand clock source.	X	X
CAN	Debug Message State Machine	2.3.2	Debug message handling state machine is not reset to Idle state when CCCR.INIT is set.	X	X
CAN	Transmit Message Order Inversion	2.3.3	Message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID.	X	X
CAN	User Manual update	2.3.4	Incomplete description in Section 3.5.2 Dedicated Tx Buffers and 3.5.4 Tx Queue of the M_CAN User's Manual related to transmission from multiple buffers configured with the same Message ID.	X	X
Device	Standby entry	2.4.1	Potential hard fault upon standby entry when systick interrupt is enabled.	X	X
Device	Overconsumption in Standby	2.4.2	An overconsumption can happen when entering in Standby Sleep mode when The TC is enabled with run in standby disabled.	X	X
Device	Performance Mode	2.4.3	In Standby mode, the regulator configured in performance mode is not behaving as expected.	X	X
Device	Chip Erase	2.4.4	Chip Erase is not functional at ambient temperatures higher than 85°C.	X	X
EVSYS	Generic Clock	2.5.1	Using synchronous, spurious overrun can appear with generic clock for the channel always on.	X	X
EVSYS	Event Channel Configuration	2.5.2	Right after an Event channel configuration is done and enabled, the channel is busy for 1 generic clock (GCLK_EVSYS_Channelx) tick; however the EVSYS.CHSTATUS.CHBUSYn corresponding bit is not set during that time.	X	X
EVSYS	CHBUSY Flag Stuck	2.5.3	CHBUSY flag never reset upon software events in synchronous/resynchronized path modes with event detection on falling edges.	X	X
EVSYS	Spurious Overrun	2.5.4	Overrun interrupt flag may be incorrectly set upon software events in synchronous/resynchronized path modes with event detection on both rising and falling edges.	X	X
FREQM	PAC protection	2.6.1	FREQM reads on the Control B register generate a PAC protection error.	X	X
FREQM	Lost Interrupt	2.6.2	DONE interrupt may be lost.	X	X
FREQM	STATUS.BUSY	2.6.3	No time-out period for a FREQM measurement cycle.	X	X
MCRAMC	PAC Write Protection	2.7.1	INTSTA register is PAC write protected.	X	X
OSCCTRL	FDPLL Unlock	2.8.1	Spurious DPLL unlocks may be detected during operation.	X	X
OSCCTRL	FDPLL96M On-Demand in Standby	2.8.2	The FDPLL96M On Demand mode is not functional in Standby Sleep mode.	X	X
PDEC	Counter mode	2.9.1	Counting starts before the first retrigger event or command.	X	X
PDEC	Counter mode	2.9.2	Count of events is not functional.	X	X
PDEC	Angular and Revolution Counters	2.9.3	With index input enabled i.e., EVCTRL.EVEI[2] and operating in X4/X2 mode, angular and revolution counters are incremented/decremented by two separate and unsynchronized sources.	X	X
PDEC	Error Flags	2.9.4	An error detection (INTFLAG.ERR = 1) updates the STATUS Error flags (HERR, WINERR, MPERR, IDXERR, QERR) with a variable delay.	X	X
PDEC	Direction Change	2.9.5	A direction change detection (INTFLAG.DIR = 1) updates the STATUS.DIR bit with a variable delay.	X	X

.....continued

Module	Feature	Item #	Issue Summary	Affected Revisions	
				B0	C0
PDEC	Hall Mode	2.9.6	A windows error (WINERR) can be reported after a START command execution, or when leaving standby (with RUNSTDBY = 0).	X	X
PDEC	Hall Mode	2.9.7	In HALL mode, WINERR Error interrupt (INTFLAG.WINERR = 1) can rise several times on a low-speed window error detection.	X	X
SERCOM	Software Reset	2.10.1	When CTRLA.ENABLE = 0 and CTRLA.SWRST is asserted, software reset sequence is not initiated.	X	X
SERCOM I²C	Status Flag	2.11.1	The BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR Status register bits are not automatically cleared.	X	X
SERCOM I²C	CLKHOLD Bit Status	2.11.2	The CLKHOLD Status bit is not read only.	X	X
SERCOM I²C	Repeated Start / Host mode 10-bit	2.11.3	Repeated Start in 10-bit addressing mode for Host Write operations does not work.	X	X
SERCOM I²C	Repeated start	2.11.4	Bus error is generated during a Repeated Start (when QCEN = 1 and SCLSM = 1).	X	X
SERCOM I²C	NACK and Repeated Start	2.11.5	Repeated Start is not supported for High-Speed mode Host Read operations.	X	X
SERCOM I²C	Repeated Start / High-Speed mode	2.11.6	Repeated Start is not supported for High-Speed mode Host Write operations.	X	X
SERCOM I²C	Client Mode with DMA	2.11.7	Character lost in I²C Client mode with DMA when a NACK occurs.	X	X
SERCOM I²C	Client mode 10-bit	2.11.8	I²C Client 10-bit addressing mode is not functional.	X	X
SERCOM I²C	Wakeup	2.11.9	When an unexpected STOP occurs on the I²C bus the STATUS.BUSERR and INTFLAG.ERROR bits are set, but may not wake the system from Sleep mode. An unexpected START will not produce this issue.	X	X
SERCOM I²C	Automatic Acknowledge	2.11.10	The I²C Client Automatic Acknowledge feature (CTRLB.AACKEN = 1) is not supported when doing a repeated start.	X	X
SERCOM I²C	RXNACK	2.11.11	The RXNACK status bit is invalid during the first DRDY interrupt.	X	X
SERCOM SPI	Data Preload	2.12.1	Data lost in SPI Client mode with Data Preload Enabled.	X	X
SERCOM SPI	Power Consumption	2.12.2	Extra power consumption in Standby Sleep mode after preloading a data.	X	X
SERCOM SPI	Reserved	2.12.3	Reserved		
SERCOM USART	Wakeup	2.13.1	The USART does not wake up the device on Error Interrupt (INTFLAG.ERROR=1).	X	X
SERCOM USART	Collision Detection	2.13.2	Collision Detection does not stop Data Transfer.	X	X
SERCOM USART	Over Consumption in Standby	2.13.3	Unexpected over consumption in Standby mode.	X	X
SERCOM USART	LIN Host Delays	2.13.4	In SERCOM USART LIN Host mode, in the case where break, sync and identifier fields are automatically transmitted when DATA is written with the identifier, the LIN Host Header Delay between the sync and the ID transmission fields is not correct.	X	X
SERCOM USART	Two stop bits mode in LIN Host	2.13.5	Two stop bits mode is not supported in SERCOM USART LIN Host mode in the case where break, sync and identifier fields are automatically transmitted when DATA is written with the identifier.	X	X
TC	SYNCBUSY Flag	2.14.1	When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.	X	X
TC	Event Retrigger	2.14.2	If a Retrigger event occurs exactly at the Channel Compare Match [n] time, the next Waveform Output [n] is missing or disturbed.	X	X
TCC	Re-trigger in RAMP2 Operations	2.15.1	Re-trigger in RAMP2 operations is not supported if a prescaler is used and the re-trig of the counter is done on the next GCLK.	X	X
TCC	DMA Request	2.15.2	On a TCC compare match, a DMA request is set whatever the CTRLA.DMAOS value.	X	X
OSC48M	Start-Up	2.16.1	In some very rare cases, the OSC48M internal oscillator may not start at power-up or may not re-start during runtime after having been turned off manually or automatically by the system.	X	X

Notes:

- Cells with 'X' indicate the issue is present in this revision of the silicon
- Cells with '-' indicate this silicon revision does not exist for this issue
- The blank cell indicates the issue has been corrected or does not exist in this revision of the silicon

2. PIC32CM JH00/JH01 Silicon Errata Issues

The following issues apply to the PIC32CM JH00/JH01 family of devices.

Notes:

- Cells with 'X' indicate the issue is present in this revision of the silicon
- Cells with '-' indicate this silicon revision does not exist for this issue
- The blank cell indicates the issue has been corrected or does not exist in this revision of the silicon

2.1 Analog Comparator (AC)

2.1.1 Analog Pins

Reference:UANA138-4

Analog pins are shared between PTC and AC module. This may result in PTC accuracy issues.

Workaround

To guarantee the accuracy of the PTC measurement when using these shared pins, configure the AC input to anything different from default configuration, that is, VDD scaler, DAC, or Bandgap.

Affected Silicon Revisions

B0	C0			
X	X			

2.2 Analog-to-Digital Converter (ADC)

2.2.1 Offset Correction Reference

Reference: ADC101-16

Offset correction using the OFFSETCORR register is not supported in the 8-bit and 10-bit conversion resolution.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.2.2 Reference Buffer Offset

Reference:CHIP003-247, ADC101-11, ADC102-8

Total Unadjusted Error (TUE) of the ADC conversion result is out of specification when,

- Using the reference source as REFCTRL.REFSEL ≠ AVDD
- Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1)

Workaround

The first five conversions after enabling ADC must be ignored. All further ADC conversions are within the specification.

Affected Silicon Revisions

B0	C0			
X	X			

2.2.3 Sequence State

Reference:ADC101-31

The SEQSTATUS register is not updated properly when exiting Standby mode by an ADC conversions sequence event.

The first conversion source is done (available in the RESULT register), but is not identified and reported in the SEQSTATUS register.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.3 Controller Area Network (CAN)

2.3.1 On-Demand Clock Source

Reference: 14406, CAN100-9

The CAN is not compatible with an on-demand clock source.

Workaround

Clear the ONDEMAND bit to zero for the oscillator source that provides the GCLK to the CAN.

Affected Silicon Revisions

B0	C0			
X	X			

2.3.2 Debug Message State Machine

Reference: CAN100-40

If the CCCR.INIT bit is set by the Host by writing to the CCCR register or when the M_CAN enters BusOff state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Setting the CCCR.CCE does not change RXF1S.DMS.

Scope:

The erratum is limited to the case when the Debug on CAN Support feature is active. Regular operation is not affected, in regular operation the debug message handling state machine always remains in Idle state.

Effects:

In the described case the debug message handling state machine is stopped and remains in the current state signaled by RXF1S.DMS. If RXF1S.DMS = "11", output `m_can_dma_req` remains active.

Workaround

If the debug message handling state machine has stopped while RXF1S.DMS = "01" or RXF1S.DMS = "10", it can be reset to Idle state by hardware reset or by reception of debug messages after CCCR.INIT is reset to zero.

If the debug message handling state machine has stopped while RXF1S.DMS = "11" with `m_can_dma_req` active, it can be reset to Idle state by hardware reset or by activating input `m_can_dma_ack`.

Affected Silicon Revisions

B0	C0			
X	X			

2.3.3 Transmit Message Order Inversion

Reference: CAN100-50

It may happen, depending on the delay between the individual Tx requests, that in the case where multiple Tx Buffers are configured with the same message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).

Scope:

The erratum is limited to the case when multiple Tx Buffers are configured with the same message ID.

Effects:

In the case described it may happen, that Tx Buffers configured with the same message ID and pending Tx request are not transmitted with lowest Tx Buffer number first (message order inversion).

Workaround

First write the group of Tx messages with same message ID to the message RAM and then afterwards request transmission of all these messages concurrently by a single write access to TXBAR. Before requesting a group of Tx messages with this message ID ensure that no message with this message ID has a pending Tx request.

Use the Tx FIFO instead of dedicated Tx Buffers for the transmission of several messages with the same message ID in a specific order, as described in Section 3.5.3 of the “M_CAN User’s Manual”.

Affected Silicon Revisions

B0	C0			
X	X			

2.3.4 User Manual Update

Reference: CAN100-52

Incomplete description in Section 3.5.2 “Dedicated Tx Buffers” and 3.5.4 “Tx Queue of the M_CAN User’s Manual” related to transmission from multiple buffers configured with the same message ID.

Description:

3.5.2 Dedicated Tx Buffers

Wording User’s Manual:

In case that multiple dedicated Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.

Enhancement:

These Tx buffers will be requested in ascending order with lowest buffer number first. Alternatively, all Tx buffers configured with the same message ID can be requested simultaneously by a single write access to TXBAR.

3.5.4 Tx Queue

Wording User's Manual:

In case that multiple Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

Replacement:

If multiple Tx Queue buffers are configured with the same message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT index, a prediction of the transmission order is not possible.

Wording User's Manual:

An Add Request cyclically increments the Put Index to the next free Tx Buffer.

Replacement:

The Put Index always points to that free buffer of the Tx Queue with the lowest buffer number.

Scope:

Use of multiple dedicated Tx Buffers or Tx Queue buffers configured with same message ID.

Effects:

If the dedicated Tx buffers with the same message ID are not requested in ascending order or at the same time or in case of multiple Tx Queue buffers with the same message ID, it cannot be guaranteed, that these messages are transmitted in ascending order with lowest buffer number first.

Workaround

If a defined order of transmission is required, the Tx FIFO will be used for transmission of messages with the same message ID. Alternatively dedicated Tx buffers with same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to TXBAR. Alternatively, a single Tx Buffer can be used to transmit those messages one after the other.

Affected Silicon Revisions

B0	C0			
X	X			

2.4 Device

2.4.1 Standby Entry

Reference:CHIP003-325

When the Systick interrupt is enabled and the standby back-bias option is set (STDBYCFG.BBIAS = 1), an hard fault can occur when the Systick interrupt coincides with the standby entry.

Workaround

Disable the Systick interrupt before entering standby and re-enable it after wake up.

Affected Silicon Revisions

B0	C0			
X	X			

2.4.2 Overconsumption in Standby

Reference:CHIP003-3

An overconsumption can happen when entering in Standby Sleep mode when the TC is enabled (CTRLA.ENABLE = 1) with run in Standby disabled (CTRLA.RUNSTDBY = 0).

Workaround

Disable the TC when entering in Standby Sleep mode.

Affected Silicon Revisions

B0	C0			
X	X			

2.4.3 Performance Mode

Reference:CHIP003-609

When entering Standby mode with the regulator configured in Performance mode (STDBYCFG.VREGSMOD = 0x1), the system will wrongly switch to the low-power regulator and keep requesting GCLK0.

Workaround

Set SUPC VREG.RUNSTDBY = 0x1, which will force the system to use the main regulator.

Another possible option is to configure the regulator in Auto mode (STDBYCFG.VREGSMOD = 0x0) and let the hardware automatically switch between main and low-power regulator.

Affected Silicon Revisions

B0	C0			
X	X			

2.4.4 Chip Erase

Reference:M32PRV-1093

Chip Erase is not functional at ambient temperatures higher than 85°C.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.5 Event System (EVSYS)

2.5.1 Generic Clock

Reference:14532, PTG102-1

In synchronous mode, spurious overrun interrupts can be generated when the generic clock for a channel is always on (CHANNEL.ONDEMAND = 0).

Workaround

Set Generic Clock on Demand feature by setting CHANNEL.ONDEMAND = 1.

Affected Silicon Revisions

B0	C0			
X	X			

2.5.2 Event Channel Configuration

Reference: PTG102-3

Right after an event channel configuration is done and enabled, the channel is busy for one generic clock (GCLK_EVSYS_Channelx) tick; however, the EVSYS.CHSTATUS.CHBUSYn corresponding bit is not set during that time. This is noticeable when the EVSYS input GCLK frequency is less than the CPU frequency.

Workaround

Wait for at least one generic clock(GCLK_EVSYS_Channelx) tick before triggering the channel for the first time after it has been configured and enabled.

Affected Silicon Revisions

B0	C0			
X	X			

2.5.3 CHBUSY Flag Stuck

Reference:PTG102-10

If a software event occurs when the EVSYS is set in synchronous or resynchronized path modes (CHANNELn.PATH = 0x0/0x1) with event detection set on falling edges (CHANNELn.EDGESEL = 0x2), the CHSTATUS.CHBUSYn flag will be set but will never come back to 0. It is then impossible to know if the event user for this channel is ready or not to accept new events.

Workaround

Generate software events for this user through a dedicated channel configured with event detection set on rising edges (CHANNELn.EDGESEL = 0x1).

Affected Silicon Revisions

B0	C0			
X	X			

2.5.4 Spurious Overrun Interrupts

Reference:PTG102-11

If a software event occurs when the EVSYS is set in synchronous or resynchronized path modes (CHANNELn.PATH = 0x0/0x1) with event detection set on both rising and falling edges (CHANNELn.EDGESEL = 0x3), spurious overrun interrupts may occur (INTFLAG.OVRn).

Workaround

Generate software events for the event user through a dedicated channel configured with event detection set on rising edges (CHANNELn.EDGESEL = 0x1).

Affected Silicon Revisions

B0	C0			
X	X			

2.6 Frequency Meter (FREQM)

2.6.1 PAC Protection Error

Reference: CLK101-9

FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.6.2 Lost Interrupt

Reference: CLK101-104

The DONE interrupt may be lost when the measurement period (CFGA.REFNUM * the reference clock period) is less than 4 APB clock periods.

Workaround

The measurement reference period must be longer than 4 APB clock periods.

Affected Silicon Revisions

B0	C0			
X	X			

2.6.3 STATUS.BUSY

Reference: CLK101-115

There is no timeout period for a FREQM measurement cycle. If the cycle count does not reach CFGA.REFNUM, the measurement cycle will not end and STATUS.BUSY will never deassert.

Workaround

If the measure signal may be very slow, may stop during the measurement, or have a frequency of 0 Hz, the application code must monitor the measurement cycle and terminate it in an appropriate period of time.

Affected Silicon Revisions

B0	C0			
X	X			

2.7 MCRAMC

2.7.1 INTSTA Register is PAC Write Protected.

Reference:DRM036-30

When the MCRAMC is protected against register writes by the PAC, the INTSTA register becomes unexpectedly protected too.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.8 Oscillator Controller (OSCCTRL)

2.8.1 FDPLL Unlock

Reference:CHIP003-553

When using FDPLL at temperature below 25°C, spurious DPLL unlocks (OSCCTRL.DPLLSTATUS.LOCK = 0) may be detected while the FDPLL still adheres to the electrical characteristics metrics defined in the data sheet. During these unlock periods, the DPLL output clock is halted and then restarts.

Workaround

When using FDPLL at temperature below 25°C, enable the lock bypass (OSCCTRL.DPLLCTRLB.LBYPASS = 1) to avoid losing FDPLL clock output during a false unlock status. The workaround does not avoid false unlock indications, but it disables the gating of the FDPLL clock output by the lock status, therefore, the clock is issued even if the FDPLL status shows unlocked.

Pseudo Code:

Set OSCCTRL.DPLLCTRLB.LBYPASS = 1

Set DPLLCTRLA.ENABLE = 1

Wait (OSCCTRL.DPLLSTATUS.CLKRDY = 1)

Set Source for GCLK with DPLL

Affected Silicon Revisions

B0	C0			
X	X			

2.8.2 FDPLL96M On Demand Standby

Reference:PLL100-19, PLL100-20

The FDPLL96M On Demand mode (DPLLCTRLA.ONDEMAND = 1) is not functional in Standby Sleep mode.

Workaround

Set DPLLCTRLA.ONDEMAND = 0 which makes the FDPLL96M always running in Standby Sleep mode.

Affected Silicon Revisions

B0	C0			
X	X			

2.9 Position Decoder (PDEC)

2.9.1 Counter Mode Reference: QEI100-51

Start, restart, or retrigger on event (EVCTRL.EVACT = 0x1) is not functional in COUNTER operating mode (CTRLA.MODE = 0x2).

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.9.2 Counter Mode Reference: QEI100-50

Counting Events (EVCTRL.EVACT = 0x2) is not functional in COUNTER operating mode (CTRLA.MODE = 0x2).

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.9.3 Angular and Revolution Counters Reference: QEI100-55

With index input enabled, that is, EVCTRL.EVEI[2] and operating in X4/X2 mode, angular and revolution counters are incremented or decremented by two separate and unsynchronized sources (phases and index). This can lead to generating erroneous MC0 and MC1 events.

Workaround

If the application use case permits, operate PDEC in X4S/X2S mode by setting CTRLA.CONF[2:0] = 0b001/ 0b011. In this mode, the revolution counter is incremented or decremented by a single source, that is angular counter overflow or underflow.

If the application use case restricts operation in X4S/X2S mode, then disable index input event, that is EVCTRL.EVEI[2] = 0. This ensures that revolution counter is incremented or decremented by a single source, that is, angular counter overflow or underflow. First occurrence of the index pulse can be detected using an external interrupt input and angular counter value can be reset in the corresponding interrupt service routine.

Affected Silicon Revisions

B0	C0			
X	X			

2.9.4 Error Flags Reference: QEI100-61

An Error Detection (INTFLAG.ERR = 1) updates the STATUS Error flags (HERR, WINERR, MPERR, IDXERR, QERR) with a variable delay.

Workaround

Poll the STATUS Error flags until one of these bits is set.

Affected Silicon Revisions

B0	C0			
X	X			

2.9.5 Direction Change Reference: QEI100-62

A direction change detection (INTFLAG.DIR = 1) updates the STATUS.DIR bit with a variable delay.

Workaround

Do not consider the STATUS.DIR bit status when using the INTFLAG.DIR bit.

Affected Silicon Revisions

B0	C0			
X	X			

2.9.6 Hall Mode Reference: QEI100-65

A Windows Error (WINERR) flag can be reported after a START command execution, or when leaving standby (with RUNSTDBY = 0).

Workaround

Ignore the Windows Error (WINERR) flag in Hall mode after a START command execution, or when leaving standby.

Affected Silicon Revisions

B0	C0			
X	X			

2.9.7 Hall Mode Reference: QEI100-67

In HALL mode, the WINERR Error interrupt (INTFLAG.WINERR = 1) can rise several times on a low-speed window error detection.

Workaround

Disable the WINERR (INTCLR.WINERR = 1) at first error detection, then re-enable it once the error root cause at the application level is solved.

Affected Silicon Revisions

B0	C0			
X	X			

2.10 SERCOM

2.10.1 Software Reset

Reference:COM100-71

Software Reset (CTRLA.SWRST=1) is not functional when the SERCOM is not enabled (CTRAL.ENABLE = 0).

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.11 SERCOM I^2C

2.11.1 Status Flags

Reference:COM100-102

In Client mode, the SEXTOUT, LOWTOUT, COLL, and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.

Workaround

Manually clear the status bits, SEXTOUT, LOWTOUT, COLL, and BUSERR, by writing these bits to '1' when INTFLAG.AMATCH is cleared.

Affected Silicon Revisions

B0	C0			
X	X			

2.11.2 Status Flags

Reference:COM100-114

The STATUS.CLKHOLD bit in Host and Client modes can be written, whereas it is a read-only status bit.

Workaround

Do not clear the STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

B0	C0			
X	X			

2.11.3 Repeated Start

Reference:COM100-128

For Host Write operations (excluding High-Speed mode) in 10-bit Addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.

Workaround

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate a Repeated Start.

Affected Silicon Revisions

B0	C0			
X	X			

2.11.4 Repeated Start

Reference:COM100-84

When the Quick command is enabled (CTRLB.QCEN = 1), the software can issue a Repeated Start by either writing the CTRLB.CMD or ADDR.ADDR bit fields. If in these conditions, SCL Stretch mode is CTRLA.SCLSM = 1, a bus error will be generated.

Workaround

Use Quick Command mode (CTRLB.QCEN = 1) only if SCL Stretch mode is CTRLA.SCLSM = 0.

Affected Silicon Revisions

B0	C0			
X	X			

2.11.5 Repeated Start or Host Mode 10-bit

Reference:COM100-123

For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.11.6 Repeated Start

Reference:COM100-122

For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.11.7 Client Mode with DMA

Reference:COM100-94

In I^2C Client Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Since a NACK was received, the transfer on the I^2C bus will not occur causing the loss of this data.

Workaround

Configure the DMA transfer size to the number of data to be received by the I^2C Host. DMA cannot be used if the number of data to be received by the Host is not known.

Affected Silicon Revisions

B0	C0			
X	X			

2.11.8 10-bit Addressing Mode

Reference:COM100-101

I^2C Client 10-bit addressing mode is not functional.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.11.9 No Wakeup Upon Unexpected STOP

Reference:COM100-157

When an unexpected STOP occurs on the I^2C bus, the STATUS.BUSERR and INTFLAG.ERROR bits are set but may not wake the system from Sleep mode. An unexpected START will not produce this issue.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.11.10 Automatic Acknowledge

Reference:COM100-216

The I^2C Client Automatic Acknowledge feature (CTRLB.AACKEN = 1) is not supported when doing a repeated start.

Workaround

Do not use the AACKEN feature, implement a AMATCH handler instead.

Affected Silicon Revisions

B0	C0			
X	X			

2.11.11 RXNACK

Reference:COM100-98

The RXNACK status bit is invalid during the first DRDY interrupt.

Workaround

Use a software flag to track when to ignore RXNACK and reset this flag in the I2CS_AMATCH interrupt handler (workaround is not applicable when AACKEN = 1).

Affected Silicon Revisions

B0	C0			
X	X			

2.12 SERCOM SPI

2.12.1 SPI-Client Data Lost with Data Preload Enabled

Reference:COM100-83

In SPI Client mode with Client Data Preload Enabled (CTRLB.PLOADEN = 1), the client transmitter may discard some data if the Host cannot keep the SPI Select pin low until the end of transmission.

Workaround

In SPI Client mode, the Client Select ($\overline{SS}$) pin must be kept low by the Host until the end of the transmission if the Client Data Preload feature is used (CTRLB.PLOADEN = 1).

Affected Silicon Revisions

B0	C0			
X	X			

2.12.2 SPI-Client Extra Power Consumption in Standby Sleep Mode

Reference:COM100-202

Preloading a new SPI data (CTRLB.PLOADEN = 1) before going into Standby Sleep mode, may lead to extra power consumption.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.12.3 Reserved

2.13 SERCOM USART

2.13.1 Wakeup

Reference:COM100-41

The USART does not wake-up the device on Error Interrupt (INTFLAG.ERROR = 1).

Workaround

Configure the USART to wake-up the device on the RX Complete Interrupt (INTENSET.RXC = 1) in order to check the PERR/FERR status (STATUS.PERR = 1 or STATUS.FERR = 1).

Affected Silicon Revisions

B0	C0			
X	X			

2.13.2 Collision Detection

Reference:COM100-75

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.

Workaround

The SERCOM APB clock must always be higher than the SERCOM Generic Clock to support collision detection.

Affected Silicon Revisions

B0	C0			
X	X			

2.13.3 Over Consumption in Standby

Reference:COM100-185

When SERCOM USART CTRLA.RUNSTDBY = 0 and the receiver is disabled (CTRLB.RXEN = 0), the clock request to the GCLK generator feeding the SERCOM will stay asserted during Standby mode, leading to unexpected over consumption.

Workaround

Configure CTRLA.RXPO and CTRLA.TXPO to use the same SERCOM PAD for RX and TX, or add an external pull up on the RX pin.

Affected Silicon Revisions

B0	C0			
X	X			

2.13.4 LIN Host Delays

Reference:COM100-235

In SERCOM USART LIN Host Mode (CTRLA.FORM = 0x2), in the case where break, sync, and identifier fields are automatically transmitted when DATA is written with the identifier (CTRLB.LINCMD = 0x2), the LIN Host Header Delay between the sync and the ID transmission fields is not correct for the following cases:

- CTRLC.HDRDLY = 0x2: Where the delay between sync and ID transmission fields is 8-bit time instead of 4-bit time.
- CTRLC.HDRDLY = 0x3: Where the delay between sync and ID transmission fields is 14-bit time instead of 4-bit time.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.13.5 Two stop bits mode in LIN Host

Reference:COM100-237

Two Stop Bits Mode (CTRLB.SBMODE = 0x1) is not supported in SERCOM USART LIN Host Mode (CTRLA.FORM = 0x2) in the case where break, sync, and identifier fields are automatically transmitted when DATA is written with the identifier (CTRLB.LINCMD = 0x2). One Stop bit is only supported.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.14 Timer/Counter (TC)

2.14.1 SYNCBUSY Flag

Reference:15056, TMR100-12

When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.

Workaround

Clear successively twice the STATUS.PERBUFV/STATUS.CCBUFx flag to ensure that the PERBUF/CCBUFx register value is restored before updating it.

Affected Silicon Revisions

B0	C0			
X	X			

2.14.2 Event Retrigger

Reference:TMR100-51

If a re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

Workaround

Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

Affected Silicon Revisions

B0	C0			
X	X			

2.15 Timer/Counter for Control (TCC)

2.15.1 Re-Trigger in RAMP2 Operations

Reference:TMR101-140

Re-trigger in RAMP2 operations (RAMP2, RAMP2A, RAMP2C, RAMP2CS) is not supported if a prescaler is used (CTRLA.PRESCALER ! = 0) and the re-trig of the counter is done on the next GCLK (CTRLA.PRESCSYNC = GCLK or CTRLA.PRESCSYNC = RESYNC).

Workaround

Configure the re-trig of the counter on the next prescaler clock (CTRLA.PRESCSYNC = PRESC).

Affected Silicon Revisions

B0	C0			
X	X			

2.15.2 DMA Request on Compare Match

Reference:TMR101-143

On a TCC compare match, a DMA request is set whatever the CTRLA.DMAOS value.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

2.16 OSC48M

2.16.1 Start-Up

Reference:UANA141-6

In some very rare cases, the OSC48M internal oscillator may not start at power-up, or may not re-start during runtime after having been turned off manually or automatically by the system.

Workaround

Failures at power-up can be solved by power cycling the unit.

Failures at run-time can be addressed by keeping the OSC48M always enabled (OSC48MCTRL.ENABLE = 1, OSC48MCTRL.ONDEMAND = 0, OSC48MCTRL.RUNSTDBY = 1).

Affected Silicon Revisions

B0	C0			
X	X			

3. Silicon Debug Related Errata Summary

Table 3-1. Silicon Debug Related Errata Summary

Module	Feature	Item #	Issue Summary	Affected Revisions	
				B0	C0
AC	The DBGCTRL Register Reset	4.1.1	The DBGCTRL register is unexpectedly reset by CTRLA.SWRST.	X	X
CAN	Bits corruption	4.2.1	ECR.CEL, PSR.PXE, PSR.RFDF, PSR.RBRS, PSR.RESI, PSR.DLEC and PSR.LEC bits can be corrupted by a debug access.	X	X
CAN	Bits corruption	4.2.2	An expected clear on read of ECR.CEL, PSR.PXE, PSR.RFDF, PSR.RBRS, PSR.RESI, PSR.DLEC and PSR.LEC bits can be unexpectedly filtered-out when the CPU is halted.	X	X
NVMCTRL	Single ECC Errors	4.3.1	When DBGECC = 0x1 or 0x3, single ECC error are unexpectedly corrected upon debugger reads.	X	X
NVMCTRL	DBGCTRL Register Write	4.3.2	The DBGCTRL Register is only writable through debugger access.	X	X
SERCOM	DBGCTRL Register Reset	4.4.1	The DBGCTRL register is unexpectedly reset by CTRLA.SWRST	X	X
SERCOM USART	Debug Mode	4.5.1	Debug mode is not functional.	X	X

Notes:

- Cells with 'X' indicate the issue is present in this revision of the silicon
- Cells with '-' indicate this silicon revision does not exist for this issue
- The blank cell indicates the issue has been corrected or does not exist in this revision of the silicon

4. PIC32CM JH00/JH01 Silicon Debug Related Errata Issues

The following debug related errata issues apply to the PIC32CM JH00/JH01 family of devices.

Notes:

- Cells with 'X' indicate the issue is present in this revision of the silicon
- Cells with '-' indicate this silicon revision does not exist for this issue
- The blank cell indicates the issue has been corrected or does not exist in this revision of the silicon

4.1 Analog Comparator (AC)

4.1.1 DBGCTRL Register Reset

Reference:CMP102-2

The AC DBGCTRL register is unexpectedly reset by CTRLA.SWRST.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

4.2 Controller Area Network (CAN)

4.2.1 Bits corruption

Reference: CAN100-49

The ECR.CEL, PSR.PXE, PSR.RFDF, PSR.RBRS, PSR.RESI, PSR.DLEC, and PSR.LEC bits can be corrupted by a debug access.

Workaround

Do not read the ECR, PSR registers with a debugger when the CPU is not halted in debug, otherwise debug access will clear those bits.

Affected Silicon Revisions

B0	C0			
X	X			

4.2.2 Bits corruption

Reference: CAN100-49

An expected clear on read of the ECR.CEL, PSR.PXE, PSR.RFDF, PSR.RBRS, PSR.RESI, PSR.DLEC, and PSR.LEC bits can be unexpectedly filtered-out when the CPU is halted.

Workaround

Do not halt the CPU if other hosts in the application are accessing the ECR or PSR registers.

Affected Silicon Revisions

B0	C0			
X	X			

4.3 Non-Volatile Memory Controller (NVMCTRL)

4.3.1 Single ECC Errors Unexpectedly Corrected Upon Debugger Reads

Reference:PFM038-94

When DBGCTRL.DBGECC = 0x1 or 0x3, single ECC error are unexpectedly corrected upon debugger reads.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

4.3.2 DBGCTRL Register is Only Writable Through Debugger Access

Reference:PFM038-137

CPU writes to the NVMCTRL.DBGCTRL register will be discarded and generate an error.

Workaround

Use debugger accesses to write the register, which anyway is only meaningful while in Debug mode.

Affected Silicon Revisions

B0	C0			
X	X			

4.4 SERCOM

4.4.1 DBGCTRL Register Reset

Reference:COM100-46

The DBGCTRL register is unexpectedly reset by CTRLA.SWRST.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

4.5 SERCOM USART

4.5.1 Debug Mode

Reference:COM100-80

In USART Operating mode, if DBGCTRL.DBGSTOP = 1, data transmission is not halted after entering Debug mode.

Workaround

None.

Affected Silicon Revisions

B0	C0			
X	X			

5. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the device data sheet (DS60001632**C**):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are no Data Sheet Clarifications to report at this time.

6. Revision History

Revision F - 11/2023

The following updates were performed for this revision:

- Removed obsolete Data Sheet Clarifications

Revision E - 03/2023

This revision contains numerous typographical updates throughout the document along with the updates listed here.

- The following Errata were added in this revision:
  - FREQM: 2.6.2 Lost Interrupt
  - FREQM: 2.6.3 STATUS.BUSY
  - SERCOM USART: 2.13.4 LIN Host Delays
  - SERCOM USART: 2.13.5 Two stop bits mode in LIN Host
  - OSC48M: 2.16.1 Start-Up

The following Data Sheet Clarifications were added in this revision:

- Peripheral Touch Controller (PTC) Electrical Specifications
- NVM User Row BOOTPROT Production Sectting
- SERCOM4-5 Pins are not Available in PIC32CMJH00/JH01 32-PIN Variants

Revision D - December 2022

The silicon revision was updated throughout the document to C0.

The following Data Sheet Clarifications were added in this revision:

- OSC48M Active Current Electrical Specifications

Revision C - September 2022

The following errata were added in this revision:

- DEVICE: 2.4.4 Chip Erase

Revision B - July 2022

The following errata were added in this revision:

- DEVICE: 2.4.3 Performance Mode

The following two new chapters were added:

- 3. Silicon Debug Related Errata Summary
- 4. PIC32CM JH00/JH01 Silicon Debug Related Errata Issues

Revision A - February 2022

This is the initial release of this document.

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